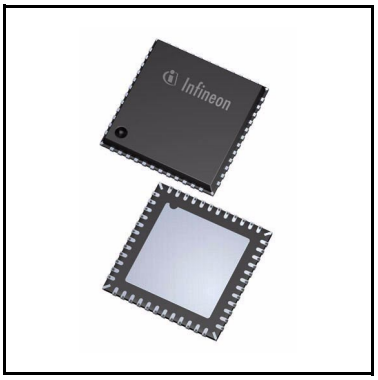
TLE9261-3BQX
System Basis Chip

Mid-Range+ System Basis Chip Family



Features

- Two integrated Low-Drop Voltage Regulators: Main regulator (5 V or 3.3 V up to 250 mA) and auxiliary regulator (5 V up to 100 mA) with off-board usage protection
- Voltage regulator (5 V, 3.3 V or 1.8 V) with external PNP transistor configurable for off-board usage or for load sharing
- 1 high-speed CAN transceiver supporting FD communication up to 5 Mbit/s featuring CAN Partial Networking & CAN FD tolerant mode according to ISO 11898-2:2016 & SAE J2284
- 4 high-side outputs 7 Ω typ., 2 HV GPIOs, 3 HV wake inputs
- Integrated fail-safe and supervision functions, e.g. fail-safe, watchdog, interrupt- and reset outputs
- 16-bit SPI for configuration and diagnostics

Potential applications

- Body Control Modules (BMC), Passive keyless entry and start modules, Gateway applications
- Heating, ventilation and air conditioning (HVAC)
- Seat, roof, tailgate, trailer, door and other closure modules
- Light control modules
- Gear shifters and selectors

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

Body System IC with Integrated Voltage Regulators, Power Management Functions, HS-CAN Transceiver supporting CAN FD featuring Partial Networking (incl. FD Tolerant Mode).
Featuring Multiple High-Side Switches and High-Voltage Wake Inputs.

Type	Package	Marking
TLE9261-3BQX	PG-VQFN-48-31	TLE9261-3BQX

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1 Overview

Scalable System Basis Chip Family

- Product family with various products for complete scalable application coverage.
- Dedicated Data Sheets are available for the different product variants
- Complete compatibility (hardware and software) across the family
- TLE9263 with 2 LIN transceivers, 3 voltage regulators
- TLE9262 with 1 LIN transceiver, 3 voltage regulators
- TLE9261 without LIN transceivers, 3 voltage regulators
- Product variants for 5V (TLE926xQX) and 3.3V (TLE926xQXV33) output voltage for main voltage regulator
- CAN Partial Networking variants for 5V (TLE926x-3QX) and 3.3V (TLE926x-3QXV33) output voltage

Device Description

The TLE9261-3BQX is a monolithic integrated circuit in an exposed pad VQFN-48 (7mm x 7mm) power package with Lead Tip Inspection (LTI) feature to support Automatic Optical Inspection (AOI).
The device is designed for various CAN automotive applications as main supply for the microcontroller and as interface for a CAN bus network including the CAN Partial Networking feature.

To support these applications, the System Basis Chip (SBC) provides the main functions, such as a 5V low-dropout voltage regulator (LDO) for e.g. a microcontroller supply, another 5V low-dropout voltage regulator with off-board protection for e.g. sensor supply, another 5V/3.3V regulator to drive an external PNP transistor, which can be used as an independent supply for off-board usage or in load sharing configuration with the main regulator VCC1, a HS-CAN transceiver supporting CAN FD and CAN Partial Networking (incl. FD tolerant mode) for data transmission, high-side switches with embedded protective functions and a 16-bit Serial Peripheral Interface (SPI) to control and monitor the device. Also implemented are a configurable timeout / window watchdog circuit with a reset feature, three Fail Outputs and an undervoltage reset feature.

The device offers low-power modes in order to minimize current consumption on applications that are connected permanently to the battery. A wake-up from the low-power mode is possible via a message on the buses, via the bi-level sensitive monitoring/wake-up inputs as well as via cyclic wake.

The device is designed to withstand the severe conditions of automotive applications.

Overview

Product Features

- Very low quiescent current consumption in Stop- and Sleep Mode
- Periodic Cyclic Wake in SBC Normal- and Stop Mode
- Periodic Cyclic Sense in SBC Normal-, Stop- and Sleep Mode
- Low-Drop Voltage Regulator 5V, 250mA
- Low-Drop Voltage Regulator 5V, 100mA, protected features for off-board usage
- Low-Drop Voltage Regulator, driving an external PNP transistor - 5V in load sharing configuration or 5V/3.3V in stand-alone configuration, protected features for off-board usage. Current limitation by shunt resistor (up to 350mA with 470mΩ external shunt resistor) in stand-alone configuration
- High-Speed CAN Transceiver:
  - fully compliant to HS-CAN standard ISO 11898-2:2016
  - fully compliant to CAN Partial Networking including CAN FD tolerant feature (acc. ISO 11898-2:2016)
  - supporting CAN FD communication up to 5 Mbps
- Fully compliant to “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications” Revision 1.3, 2012-05-04
- Four High-Side Outputs 7Ω typ.
- Dedicated supply pin for High-Side Outputs
- Two General Purpose High-Voltage In- and Outputs (GPIOs) configurable as add. Fail Outputs, Wake Inputs, Low-Side switches or High-Side switches
- Three universal High-Voltage Wake Inputs for voltage level monitoring
- Alternate High-Voltage Measurement Function, e.g. for battery voltage sensing
- Configurable wake-up sources
- Reset Output
- Configurable timeout and window watchdog
- Up to three Fail Outputs (depending on configuration)
- Overtemperature and short circuit protection feature
- Wide supply input voltage and temperature range
- Software compatible to all SBC families TLE926x and TLE927x
- Green Product (RoHS compliant) & AEC Qualified
- PG-VQFN-48 leadless exposed-pad power package with Lead Tip Inspection (LTI) feature to support Automatic Optical Inspection (AOI)

2 Block Diagram

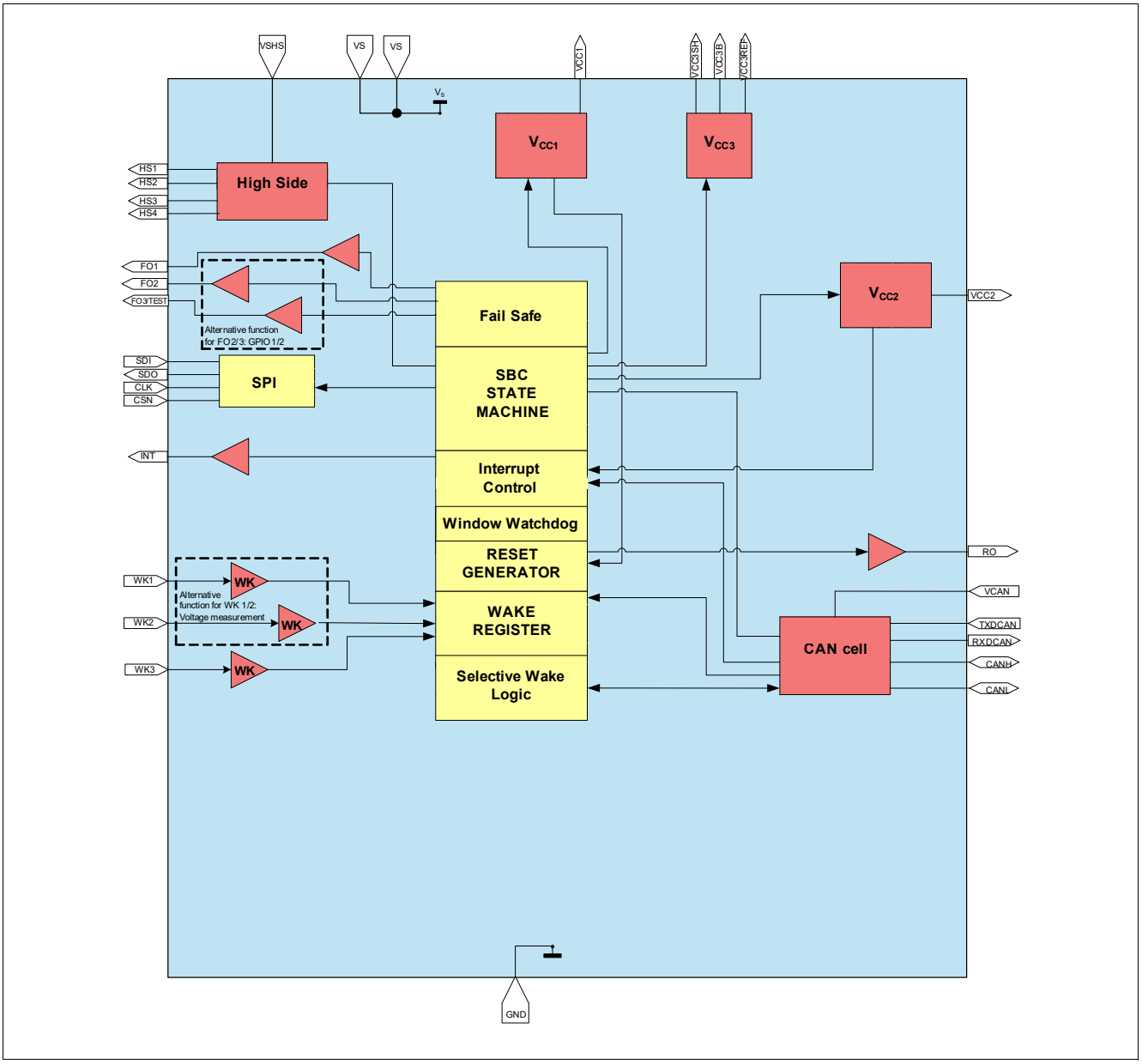

Figure 1 Block Diagram with CAN Partial Networking

3 Pin Configuration

3.1 Pin Assignment

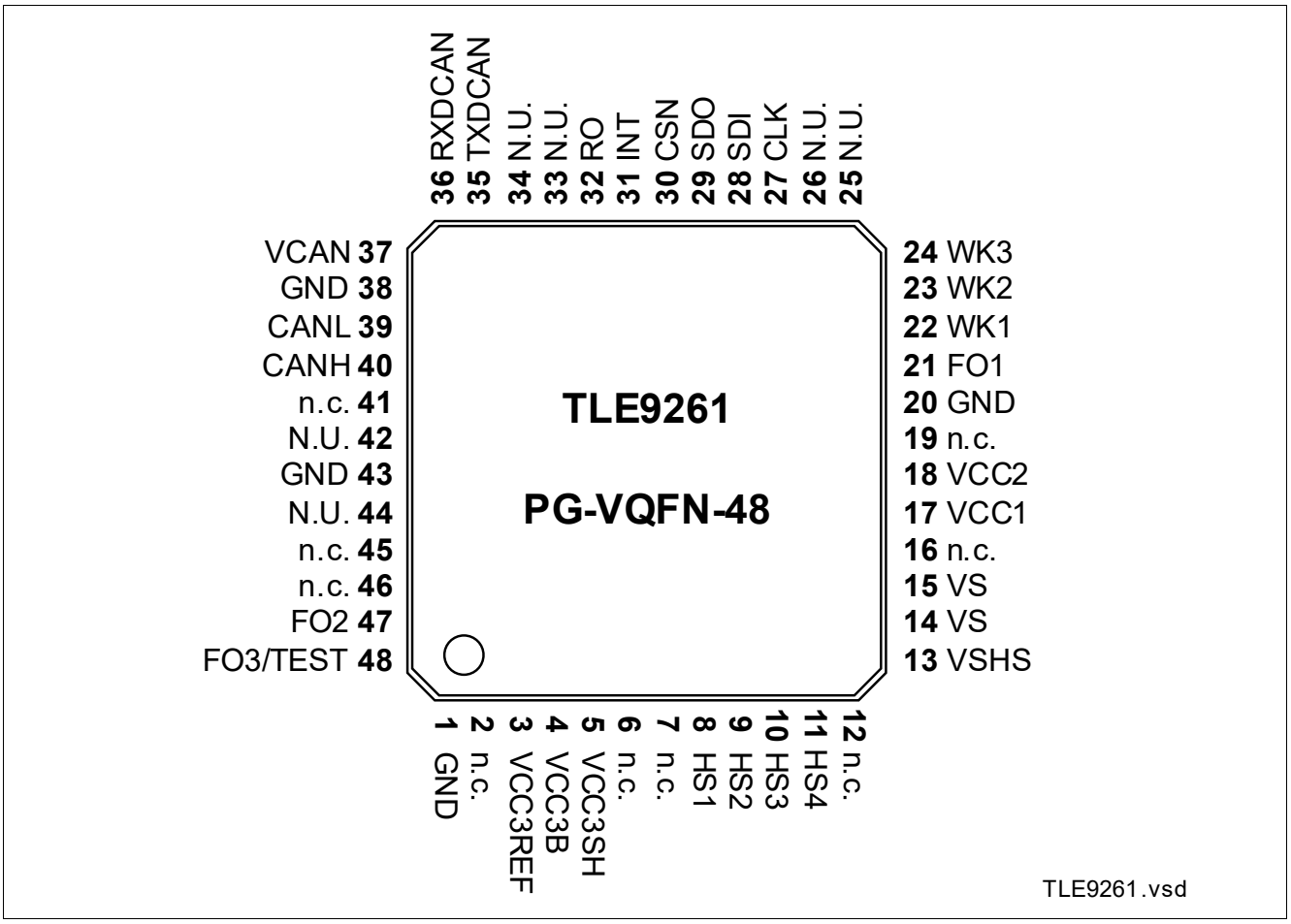

Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**Ground**
2	n.c.	**not connected;** internally not bonded.
3	VCC3REF	**VCC3REF;** Collector connection for external PNP, reference input
4	VCC3B	**VCC3B;** Base connection for external PNP
5	VCC3SH	**VCC3SH;** Emitter connection for external PNP, shunt connection
6	n.c.	**not connected;** internally not bonded.
7	n.c.	**not connected;** internally not bonded.
8	HS1	**High Side Output 1;** typ. 7Ω
9	HS2	**High Side Output 2;** typ. 7Ω
10	HS3	**High Side Output 3;** typ. 7Ω
11	HS4	**High Side Output 4;** typ. 7Ω
12	n.c	**not connected;** internally not bonded.
13	VSHS	**Supply Voltage HS and GPIO1/2 in HS configuration; Supply voltage for High-Side Switches modules and respective UV-/OV supervision; Connected to battery voltage with reverse protection diode and filter against EMC**; connect to VS if separate supply is not needed
14	VS	**Supply Voltage; Supply voltage for chip internal supply and voltage regulators; Connected to Battery Voltage with external reverse protection Diode and Filter against EMC**
15	VS	**Supply Voltage; Supply voltage for chip internal supply and voltage regulators; Connected to Battery Voltage with external reverse protection Diode and Filter against EMC**
16	n.c.	**not connected;** internally not bonded.
17	VCC1	**Voltage Regulator Output 1**
18	VCC2	**Voltage Regulator Output 2**
19	n.c.	**not connected;** internally not bonded.
20	GND	**GND**
21	FO1	**Fail Output 1**
22	WK1	**Wake Input 1;** Alternative function: HV-measurement function input pin (only in combination with WK2, see **Chapter 11.2.2**)
23	WK2	**Wake Input 2;** Alternative function: HV-measurement function output pin (only in combination with WK1, see **Chapter 11.2.2**)
24	WK3	**Wake Input 3**
25	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
26	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
27	CLK	**SPI Clock Input**
28	SDI	**SPI Data Input; into SBC (=MOSI)**
29	SDO	**SPI Data Output;** out of SBC (=MISO)

Pin Configuration

Pin	Symbol	Function
30	CSN	**SPI Chip Select Not Input**
31	INT	**Interrupt Output**; used as wake-up flag for microcontroller in SBC Stop or Normal Mode and for indicating failures. Active low. During start-up used to set the SBC configuration. External pull-up sets config 1/3, no external pull-up sets config 2/4.
32	RO	**Reset Output**
33	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
34	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
35	TXDCAN	**Transmit CAN**; alternate function: calibration of high-precision oscillator
36	RXDCAN	**Receive CAN**
37	VCAN	**Supply Input; for internal HS-CAN cell**
38	GND	**GND**
39	CANL	**CAN Low Bus Pin**
40	CANH	**CAN High Bus Pin**
41	n.c.	**not connected;** internally not bonded.
42	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
43	GND	**Ground**
44	N.U.	**Not Used;** Used for internal testing purpose. Do not connect, leave open
45	n.c.	**not connected;** internally not bonded.
46	n.c.	**not connected;** internally not bonded.
47	FO2	**Fail Output 2** - Side Indicator; Side indicators 1.25Hz 50% duty cycle output; Open drain. Active LOW. **Alternative Function: GPIO1**; configurable pin as WK, or LS, or HS supplied by VSHS (default is FO2, see also **Chapter 13.1.1**)
48	FO3/TEST	**Fail Output 3** - Pulsed Light Output; Break/rear light 100Hz 20% duty cycle output; Open drain. Active LOW **TEST**; Connect to GND to activate SBC Development Mode; Integrated pull-up resistor. Connect to VS with pull-up resistor or leave open for normal operation. **Alternative Function: GPIO2**; configurable pin as WK, or LS, or HS supplied by VSHS (default is FO3, see also **Chapter 13.1.1**)
Cooling Tab	GND	Cooling Tab - Exposed Die Pad; For cooling purposes only, do not use as an electrical ground.[1)]

1) The exposed die pad at the bottom of the package allows better power dissipation of heat from the SBC via the PCB. The exposed die pad is not connected to any active part of the IC an can be left floating or it can be connected to GND (recommended) for the best EMC performance.

*Note: all VS Pins must be connected to battery potential or insert a reverse polarity diodes where required; all GND pins as well as the Cooling Tab must be connected to one common GND potential; note that the tie bars at each package corner are connected to the cooling tab (see also **Chapter 17**)*

3.3 Hints for Unused Pins

It must be ensured that the correct configurations are also selected, i.e. in case functions are not used that they are disabled via SPI:

- WK1/2/3: connect to GND and disable WK inputs via SPI
- HSx: leave open
- CANH/L, RXDCAN, TXDCAN: leave all pins open
- RO / FOx: leave open
- INT: leave open
- TEST: connect to GND during power-up to activate SBC Development Mode;
  connect to VS or leave open for normal user mode operation
- VCC2: leave open and keep disabled
- VCC3: See **Chapter 8.5**
- VCAN: connect to VCC1
- n.c.: not connected; internally not bonded; connect to GND
- **N.U.**: Not Used; Used for internal testing purposes only. Do not connect, leave open, i.e. not connected to any potential on the board. In case N.U. pins are connected on the board an open bridge has to be foreseen to avoid external disturbances. The bridge can be shorted by a 0 Ω resistance if signal is needed.

3.4 Hints for Alternate Pin Functions

In case of alternate pin functions, selectable via SPI, it must be ensured that the correct configurations are also selected via SPI, in case it is not done automatically. Please consult the respective chapter. In addition, following topics shall be considered:

- WK1..2: The pins can be either used as HV wake / voltage monitoring inputs or for a voltage measurement function (via bit **WK_MEAS**). In the second case, the WK1..2 pins shall not be used / assigned for any wake detection nor cyclic sense functionality, i.e. WK1 and WK2 must be disabled in the register **WK_CTRL_2** and the level information is to be ignored in the register **WK_LVL_STAT**.
- FO2..3: The pins can also be configured as GPIOs in the **GPIO_CTRL** register. In this case, the pins shall not be used for any fail output functionality. The default function after Power on Reset (POR) is FOx.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage (VS, VSHS)	$VS_{x,\,max}$	-0.3	–	28	V	–	P_4.1.1
Supply Voltage (VS, VSHS)	$VS_{x,\,max}$	-0.3	–	40	V	Load Dump, max. 400 ms	P_4.1.2
Voltage Regulator 1	$V_{CC1,\,max}$	-0.3	–	5.5	V	–	P_4.1.3
Voltage Regulator 2	$V_{CC2,\,max}$	-0.3	–	28	V	V_{CC2} = 40V for Load Dump, max. 400 ms;	P_4.1.4
Voltage Regulator 3 (VCC3REF)	$V_{CC3REF,max}$	-0.3	–	28	V	V_{CC3REF} = 40V for Load Dump, max. 400 ms;	P_4.1.5
Voltage Regulator 3 (VCC3B)	$V_{CC3B,max}$	-0.3	–	V_S + 10	V	V_{CC3B} = 40V for Load Dump, max. 400 ms;	P_4.1.25
Voltage Regulator 3 (VCC3SH)	$V_{CC3SH,max}$	V_S - 0.30	–	V_S + 0.30	V	–	P_4.1.26
Wake Inputs WK1..3	$V_{WK,\,max}$	-0.3	–	40	V	–	P_4.1.6
Fail Pin FO1	$V_{FO1,\,max}$	-0.3	–	40	V	–	P_4.1.7
Fail Pins FO2, FO3/TEST	$V_{FO2_3,\,max}$	-0.3	–	V_S + 0.3	V	–	P_4.1.23
CANH, CANL	$V_{BUS,\,max}$	-27	–	40	V	–	P_4.1.8
Maximum Differential CAN Bus Voltage	$V_{CAN_Diff,\,max}$	-5	–	10	V	–	P_4.1.27
Logic Input Pins (CSN, CLK, SDI, TXDCAN)	$V_{I,\,max}$	-0.3	–	V_{CC1} + 0.3	V	–	P_4.1.9
Logic Output Pins (SDO, RO, INT, RXDCAN)	$V_{O,\,max}$	-0.3	–	V_{CC1} + 0.3	V	–	P_4.1.10
VCAN Input Voltage	$V_{VCAN,\,max}$	-0.3	–	5.5	V	–	P_4.1.11
High Side 1...4	$V_{HS,\,max}$	-0.3	–	V_{SHS} + 0.3	V	–	P_4.1.12
Currents							
Wake input WK1	$I_{WK1,max}$	0	–	500	µA	2)	P_4.1.13
Wake input WK2	$I_{WK2,max}$	-500	–	0	µA	2)	P_4.1.14

Table 1 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.15
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.16
ESD Susceptibility							
ESD Resistivity	$V_{ESD,11}$	-2	–	2	kV	HBM[3)]	P_4.1.17
ESD Resistivity to GND, HSx	$V_{ESD,12}$	-2	–	2	kV	HBM[3)]	P_4.1.18
ESD Resistivity to GND, CANH, CANL	$V_{ESD,13}$	-8	–	8	kV	HBM[4)3)]	P_4.1.19
ESD Resistivity to GND	$V_{ESD,21}$	-500	–	500	V	CDM[5)]	P_4.1.20
ESD Resistivity Pin 1, 12,13,24,25,36,37,48 (corner pins) to GND	$V_{ESD,22}$	-750	–	750	V	CDM[5)]	P_4.1.21

1) Not subject to production test, specified by design.
2) Applies only if WK1 and WK2 are configured as alternative HV-measurement function
3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)
4) For ESD "GUN" Resistivity 6KV (according to IEC61000-4-2 "gun test" (150pF, 330Ω)), will be shown in Application Information and test report will be provided from IBEE
5) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage	$V_{S,func}$	V_{POR}	–	28	V	[1] V_{POR} see **Chapter 14.10**	P_4.2.1
CAN Supply Voltage	$V_{CAN,func}$	4.75	–	5.25	V	–	P_4.2.3
SPI frequency	f_{SPI}	–	–	4	MHz	see **Chapter 15.7** for $f_{SPI,max}$	P_4.2.4
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.5

1) Including Power-On Reset, Over- and Undervoltage Protection

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Device Behavior Outside of Specified Functional Range:

- 28V < $V_{S,func}$ < 40V: Device will still be functional including the state machine; the specified electrical characteristics might not be ensured anymore. The regulators VCC1/2/3 are working properly, however, a thermal shutdown might occur due to high power dissipation. HSx switches might be turned OFF depending on VSHS_OV configurations. The specified SPI communication speed is ensured; the absolute maximum ratings are not violated, however the device is not intended for continuous operation of VS >28V. The device operation at high junction temperatures for long periods might reduce the operating life time;
- V_{CAN} < 4.75V: The undervoltage bit **VCAN_UV** will be set in the SPI register **BUS_STAT_1** and the transmitter will be disabled as long as the UV condition is present;
- 5.25V < V_{CAN} < 5.50V: CAN transceiver still functional. However, the communication might fail due to out-of-spec operation;
- $V_{POR,f}$ < VS < 5.5V: Device will still be functional; the specified electrical characteristics might not be ensured anymore.
  - The voltage regulators will enter the low-drop operation mode (applies for VCC3 only if bit **VCC3_VS_ UV_OFF** is set),
  - A VCC1_UV reset could be triggered depending on the Vrtx settings,
  - HSx switch behavior will depend on the respective configuration:
    - **HS_UV_SD_EN** = '0' (default): HSx will be turned OFF for VSHS < VSHS_UV and will stay OFF;
    - **HS_UV_SD_EN** = '1': HSx stays on as long as possible. An unwanted overcurrent shut down may occur. OC shut down bit set and the respective HSx switch will stay OFF;
  - FOx outputs will remain ON if they were enabled before VS > 5.5V,
  - The specified SPI communication speed is ensured.

4.3 Thermal Resistance

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	6	–	K/W	Exposed Pad	P_4.3.1
Junction to Ambient	R_{thJA}	–	33	–	K/W	2)	P_4.3.2

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board for 1.5W. Board: 76.2x114.3x1.5mm^3 with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm2 cooling area on the bottom layer (70µm).

4.4 Current Consumption

Table 4 Current Consumption

Current consumption values are specified at Tj = 25°C, VS = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SBC Normal Mode							
Normal Mode current consumption	I_{Normal}	–	3.5	6.5	mA	V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; VCC2, CAN, VCC3, HSx = OFF	P_4.4.1
SBC Stop Mode							
Stop Mode current consumption	$I_{Stop_1,25}$	–	44	60	µA	1)VCC2/3, HSx = OFF; CAN2), WKx not wake capable; Watchdog = OFF; no load on VCC1; **I_PEAK_TH** = '0'	P_4.4.2
Stop Mode current consumption	$I_{Stop_1,85}$	–	50	70	µA	1)3)T_j = 85°C; VCC2/3, HSx = OFF; CAN2), WKx not wake capable; Watchdog = OFF; no load on VCC1; **I_PEAK_TH** = '0'	P_4.4.3
Stop Mode current consumption (high active peak threshold)	$I_{Stop_2,25}$	–	64	90	µA	1)VCC2/3, HSx = OFF; CAN2), WKx not wake capable; Watchdog = OFF; no load on VCC1; **I_PEAK_TH** = '1'	P_4.4.35
Stop Mode current consumption (high active peak threshold)	$I_{Stop_2,85}$	–	70	100	µA	1)3)T_j = 85°C; VCC2/3, HSx = OFF; CAN2), WKx not wake capable; Watchdog = OFF; no load on VCC1; **I_PEAK_TH** = '1'	P_4.4.36
SBC Sleep Mode							
Sleep Mode current consumption	$I_{Sleep,25}$	–	15	25	µA	VCC2/3, HSx = OFF; CAN2), WKx not wake capable	P_4.4.5
Sleep Mode current consumption	$I_{Sleep,85}$	–	25	35	µA	3)T_j = 85°C; VCC2/3, HSx = OFF; CAN2), WKx not wake capable	P_4.4.6

Table 4 Current Consumption (cont'd)

Current consumption values are specified at Tj = 25°C, VS = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Feature Incremental Current Consumption							
Current consumption for CAN module, recessive state	$I_{CAN,rec}$	–	2	3	mA	SBC Normal/Stop Mode; CAN Normal Mode; VCC1 connected to VCAN; VTXDCAN = VCC1; no RL on CAN	P_4.4.7
Current consumption for CAN module, dominant state	$I_{CAN,dom}$	–	3	4.5	mA	3)SBC Normal/Stop Mode; CAN Normal Mode; VCC1 connected to VCAN; VTXDCAN = GND; no RL on CAN	P_4.4.8
Current consumption for CAN module, Receive Only Mode	$I_{CAN,RcvOnly}$	–	0.9	1.2	mA	3)4)SBC Normal/Stop Mode; CAN Receive Only Mode; VCC1 connected to VCAN; VTXDCAN = VCC1; no RL on CAN	P_4.4.9
Current consumption during CAN Partial Networking frame detect mode (**RX_WK_ SEL** = '1')	$I_{CAN,SWK,25}$	–	560	690	µA	3)T_j = 25°C; SBC Stop Mode; VCC2, HSx = OFF; WKx not wake capable; CAN SWK wake capable, SWK Receiver enabled, WUF detect; no RL on CAN	P_4.4.4
Current consumption during CAN Partial Networking frame detect mode (**RX_WK_ SEL** = '1')	$I_{CAN,SWK,85}$	–	600	720	µA	3)T_j = 85°C; SBC Stop Mode; VCC2, HSx = OFF; WKx not wake capable; CAN SWK wake capable, SWK Receiver enabled, WUF detect; no RL on CAN	P_4.4.29
Current consumption for WK1..3 wake capability (all wake inputs)	$I_{Wake,WKx,25}$	–	0.2	2	µA	5)6)7) SBC Sleep Mode; WK1..3 wake capable (all WKx enabled); CAN = OFF	P_4.4.13

Table 4 Current Consumption (cont'd)

Current consumption values are specified at Tj = 25°C, VS = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption for WK1..3 wake capability (all wake inputs)	$I_{Wake,WKx,85}$	–	0.5	3	µA	3)5)6)7)SBC Sleep Mode; T_j = 85°C; WK1..3 wake capable; (all WKx enabled); CAN = OFF	P_4.4.14
Current consumption for CAN wake capability (tsilence expired)	$I_{Wake,CAN,25}$	–	4.5	6	µA	2)5)SBC Sleep Mode; CAN wake capable; WK1..3	P_4.4.17
Current consumption for CAN wake capability (tsilence expired)	$I_{Wake,CAN,85}$	–	5.5	7	µA	2)3)5)SBC Sleep Mode; T_j = 85°C; CAN wake capable; WK1..3	P_4.4.18
VCC2 Normal Mode current consumption	$I_{Normal,VCC2}$	–	2.5	3.5	mA	V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; VCC2 = ON (no load)	P_4.4.32
Current consumption for VCC2 in SBC Sleep Mode	$I_{Sleep,VCC2,25}$	–	25	35	µA	1)5)SBC Sleep Mode; VCC2 = ON (no load); CAN, WK1..3 = OFF	P_4.4.19
Current consumption for VCC2 in SBC Sleep Mode	$I_{Sleep,VCC2,85}$	–	30	40	µA	1)3)5)SBC Sleep Mode; T_j = 85°C; VCC2 = ON (no load); CAN, WK1..3 = OFF	P_4.4.20
Current consumption for VCC3 in SBC Sleep Mode in stand-alone configuration	$I_{Sleep,VCC3,25}$	–	40	60	µA	1)5)SBC Sleep Mode; VCC3 = ON (no load, stand-along config.); CAN, WK1..3 = OFF	P_4.4.21
Current consumption for VCC3 in SBC Sleep Mode in stand-alone configuration	$I_{Sleep,VCC3,85}$	–	50	70	µA	1)3)5)SBC Sleep Mode; T_j = 85°C; VCC3 = ON (no load, stand-along config.); CAN, WK1..3 = OFF	P_4.4.22
Current consumption for HSx in SBC Stop Mode	$I_{Stop,HSx,25}$	–	550	675	µA	5)8)SBC Stop Mode; Cyclic Sense & HSx= ON (no load); CAN, WK1..3 = OFF	P_4.4.33

Table 4 Current Consumption (cont'd)

Current consumption values are specified at Tj = 25°C, VS = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption for HSx in SBC Stop Mode	$I_{Stop,HSx,85}$	–	575	700	µA	3)5)8)SBC Stop Mode; T_j = 85°C; Cyclic Sense & HSx = ON (no load); CAN, WK1..3 = OFF	P_4.4.34
Current consumption for cyclic sense function	$I_{Stop,CS25}$	–	20	28	µA	5)9)10)SBC Stop Mode; WD = OFF	P_4.4.23
Current consumption for cyclic sense function	$I_{Stop,CS85}$	–	24	35	µA	3)5)9)10)SBC Stop Mode; T_j = 85°C; WD = OFF	P_4.4.27
Current consumption for watchdog active in Stop Mode	$I_{Stop,WD25}$	–	20	28	µA	3)SBC Stop Mode; Watchdog running	P_4.4.30
Current consumption for watchdog active in Stop Mode	$I_{Stop,WD85}$	–	24	35	µA	3)SBC Stop Mode; T_j = 85°C; Watchdog running	P_4.4.31
Current consumption for active fail outputs (FO1..3)	$I_{Stop,FOx}$	–	1.0	2.0	mA	3)all SBC Modes; T_j = 25°C; FOx = ON (no load);	P_4.4.24

1) If the load current on VCC1 will exceed the configured VCC1 active peak threshold $I_{VCC1,Ipeak1,r}$ or $I_{VCC1,Ipeak2,r}$, the current consumption will increase by typ. 2.9mA to ensure optimum dynamic load behavior. Same applies to VCC2. For VCC3 the current consumption will increase by typ. 1.4mA. See also **Chapter 6**, **Chapter 7**, **Chapter 8**.
2) CAN not configured in selective wake mode.
3) Not subject to production test, specified by design.
4) Current consumption adder also applies for during WUF detection (frame detect mode) when CAN Partial Networking is activated.
5) Current consumption adders of features defined for SBC Sleep Mode also apply for SBC Stop Mode and vice versa (unless otherwise specified).
6) No pull-up or pull-down configuration selected.
7) The specified WKx current consumption adder for wake capability applies regardless how many WK inputs are activated.
8) A typ. 75µA / max 125µA (T_j = 85°C) adder applies for every additionally activated HSx switch in SBC Stop Mode; In SBC Normal Mode every HSx switch consumes the typ. 75µA / max 125µA (T_j = 85°C) without the initial adder because the biasing is already enabled.
9) HS1 used for cyclic sense, Timer 2, 20ms period, 0.1ms on-time, no load on HS1.

   In general the current consumption adder for cyclic sense in SBC Stop Mode can be calculated with below equation: IStop,CS = 18µA + (550µA *tON/TPer)

10) Also applies to Cyclic Wake

Note: There is no additional current consumption contribution due to PWM generators.

5 System Features

This chapter describes the system features and behavior of the TLE9261-3BQX:

- State machine
- SBC mode control
- Device configuration
- State of supply and peripherals
- System functions such as cyclic sense or cyclic wake
- Supervision and diagnosis functions

The System Basis Chip (SBC) offers six operating modes:

- SBC Init Mode: Power-up of the device and after a soft reset,
- SBC Normal Mode: The main operating mode of the device,
- SBC Stop Mode: The first-level power saving mode with the main voltage regulator VCC1 enabled,
- SBC Sleep Mode: The second-level power saving mode with VCC1 disabled,
- SBC Restart Mode: An intermediate mode after a wake event from SBC Sleep or Fail-Safe Mode or after a failure (e.g. WD failure, VCC1 undervoltage reset) to bring the microcontroller into a defined state via a reset. Once the failure condition is not present anymore the device will automatically change to SBC Normal Mode after a delay time (t_{RD1}).
- SBC Fail-Safe Mode: A safe-state mode after critical failures (e.g. WD failure, VCC1 undervoltage reset) to bring the system into a safe state and to ensure a proper restart of the system. VCC1 is disabled. It is a permanent state until either a wake event (via CAN or WKx) occurs or the overtemperature condition is not present anymore.

A special mode, called SBC Development Mode, is available during software development or debugging of the system. All above mentioned operating modes can be accessed in this mode. However, the watchdog counter is stopped and does not need to be triggered. This mode can be accessed by setting the TEST pin to GND during SBC Init Mode.

The device can be configured via hardware (external component) to determine the device behavior after a watchdog trigger failure. See **Chapter 5.1.1** for further information.

The System Basis Chip is controlled via a 16-bit SPI interface. A detailed description can be found in **Chapter 15**.The configuration as well as the diagnosis is handled via the SPI. The SPI mapping of the TLE9261-3BQX is compatible to other devices of the TLE926x and TLE927x families.

5.1 Block Description of State Machine

The different SBC Modes are selected via SPI by setting the respective SBC **MODE** bits in the register **M_S_CTRL**. The SBC **MODE** bits are cleared when going through SBC Restart Mode and thus always show the current SBC mode.

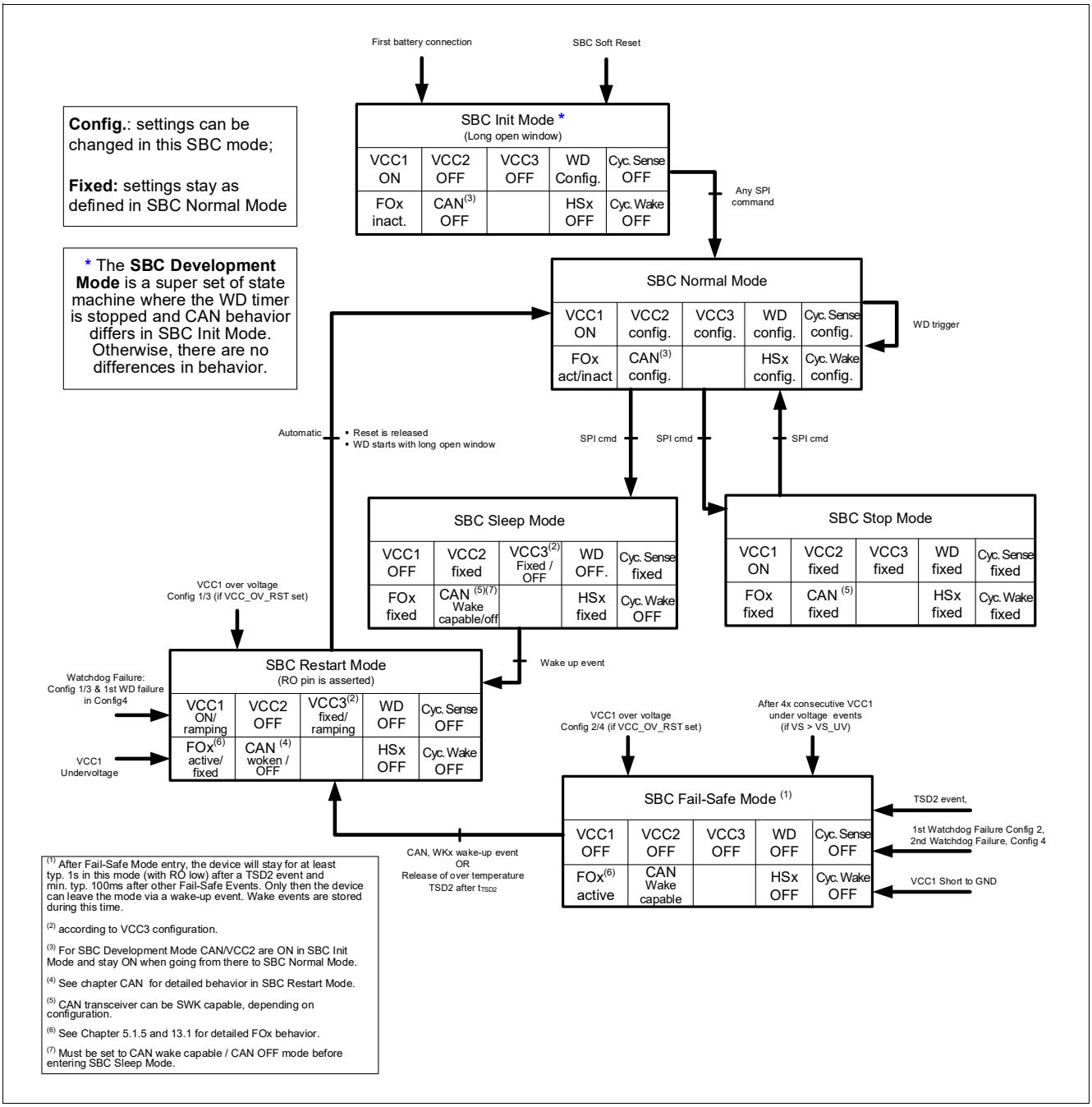

Figure 3 State Diagram showing the SBC Operating Modes including CAN Partial Networking

5.1.1 Device Configuration and SBC Init Mode

The SBC starts up in SBC Init Mode after crossing the power-on reset $V_{POR,r}$ threshold (see also **Chapter 14.3**) and the watchdog will start with a long open window (t_{LW}).
During this power-on phase following configurations are stored in the device:

- The device behavior regarding a watchdog trigger failure and a VCC1 overvoltage condition is determined by the external circuitry on the INT pin (see below)
- The selection of the normal device operation or the SBC Development Mode (watchdog disabled for debugging purposes) will be set depending on the voltage level of the FO3/TEST pin (see also **Chapter 5.1.7**).

5.1.1.1 Device Configuration

The configuration selection is intended to select the SBC behavior regarding a watchdog trigger failure. Depending on the requirements of the application, the VCC1 output shall be switched OFF and the device shall go to SBC Fail-Safe Mode in case of a watchdog failure (1 or 2 fails). To set this configuration (Config 2/4), the INT pin does not need an external pull-up resistor. In case VCC1 should not be switched OFF (Config 1/3), the INT pin needs to have an external pull-up resistor connected to VCC1 (see application diagram in **Chapter 16.1**).
Figure 5 shows the timing diagram of the hardware configuration selection. The hardware configuration is defined during SBC Init Mode. The INT pin is internally pulled LOW with a weak pull-down resistor during the reset delay time t_{RD1}, i.e.after VCC1 crosses the reset threshold VRT1 and before the RO pin goes HIGH. The INT pin is monitored during this time (with a continuos filter time of t_{CFG_F}) and the configuration (depending on the voltage level at INT) is stored at the rising edge of RO.

*Note: If the **POR** bit is not cleared then the internal pull-down resistor will be reactivated every time RO is pulled LOW the configuration will be updated at the rising edge of RO. Therefore it is recommended to clear the **POR** bit right after initialization. In case there is no stable signal at INT, then the default value '0' will taken as the config select value = SBC Fail-Safe Mode.*

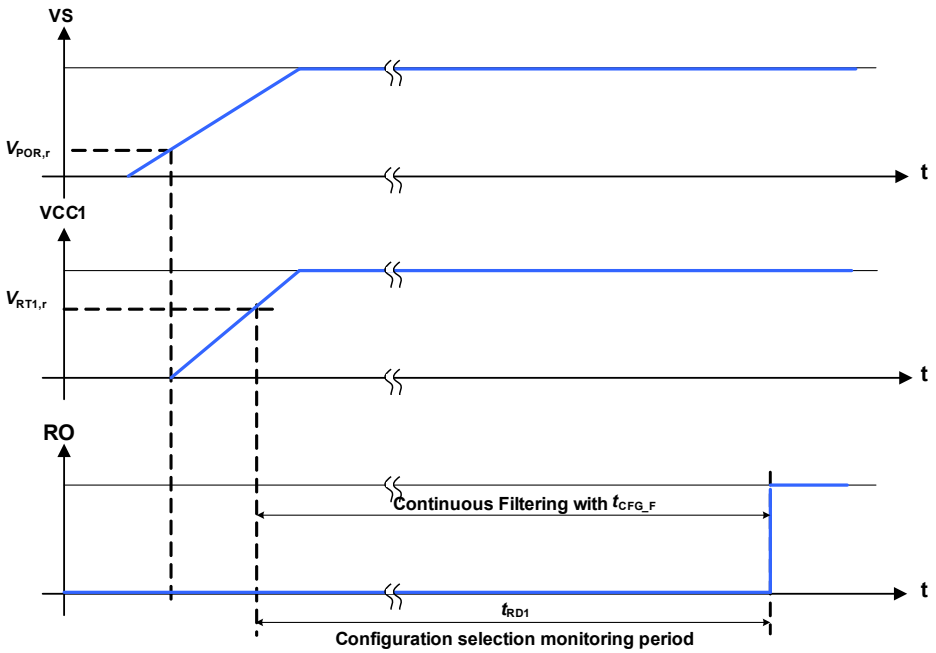

Figure 4 Hardware Configuration Selection Timing Diagram

There are four different device configurations (**Table 5**) available defining the watchdog failure and the VCC1 overvoltage behavior. The configurations can be selected via the external connection on the INT pin and the SPI bit **CFG** in the **HW_CTRL** register (see also **Chapter 15.4**):

- **CFGP** = '1': Config 1 and Config 3:
  - A watchdog trigger failure leads to SBC Restart Mode and depending on **CFG** the Fail Outputs (FOx) are activated after the 1st (Config 1) or 2nd (Config 3) watchdog trigger failure;
  - A VCC1 overvoltage detection will lead to SBC Restart Mode if **VCC1_OV_RST** is set. **VCC1_ OV** will be set and the Fail Outputs are activated;
- **CFGP** = '0': Config 2 and Config 4:
  - A watchdog trigger failure leads to SBC Fail-Safe Mode and depending on **CFG** the Fail Outputs (FOx) are activated after the 1st (Config 2) or 2nd (Config 4) watchdog trigger failure. The first watchdog trigger failure in Config 4 will lead to SBC Restart Mode;
  - A VCC1 overvoltage detection will lead to SBC Fail-Safe Mode if **VCC1_OV_RST** is set. **VCC1_ OV** will be set and the Fail Outputs are activated;

The respective device configuration can be identified by reading the SPI bit **CFG** in the **HW_CTRL** register and the **CFGP** bit in the **WK_LVL_STAT** register.

Table 5 shows the configurations and the device behavior in case of a watchdog trigger failure:

Table 5 Watchdog Trigger Failure Configuration

Config	INT Pin (CFGP)	SPI Bit CFG	Event	FOx Activation	SBC Mode Entry
1	External pull-up	1	1 x Watchdog Failure	after 1st WD Failure	SBC Restart Mode
2	No ext. pull-up	1	1 x Watchdog Failure	after 1st WD Failure	SBC Fail-Safe Mode
3	External pull-up	0	2 x Watchdog Failure	after 2nd WD Failure	SBC Restart Mode
4	No ext. pull-up	0	2 x Watchdog Failure	after 2nd WD Failure	SBC Fail-Safe Mode

Table 6 shows the configurations and the device behavior in case of a VCC1 overvoltage detection when VCC1_OV_RST is set:

Table 6 Device Behavior in Case of VCC1 Overvoltage Detection

Config	INT Pin (CFGP)	CFG Bit	VCC1_OV_RST	Event	VCC1_OV	FOx Activation	SBC Mode Entry
1-4	any value	x	0	1 x VCC1 OV	1	no FOx activation	unchanged
1	External pull-up	1	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Restart Mode
2	No ext. pull-up	1	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Fail-Safe Mode
3	External pull-up	0	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Restart Mode
4	No ext. pull-up	0	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Fail-Safe Mode

The respective configuration will be stored for all conditions and can only be changed by powering down the device (VS < $V_{POR,f}$).

5.1.1.2 SBC Init Mode

In SBC Init Mode, the device waits for the microcontroller to finish its startup and initialization sequence. In the SBC Init Mode any valid SPI command will bring the SBC to SBC Normal Mode. During the long open window the watchdog has to be triggered. Thereby the watchdog will be automatically configured.

A missing watchdog trigger during the long open window will cause a watchdog failure and the device will enter SBC Restart Mode.

Wake events are ignored during SBC Init Mode and will therefore be lost.

*Note: Any SPI command will bring the SBC to SBC Normal Mode even if it is a illegal SPI command (see **Chapter 15.2**).*

*Note: For a safe start-up, it is recommended to use the first SPI command to trigger and to configure the watchdog (see **Chapter 14.2**).*

*Note: At power up no **VCC1_UV** will be issued nor will FOx be triggered as long as VCC1 is below the $V_{RT,x}$ threshold and if VS is below the VCC1 short circuit detection threshold **$V_{S,UV}$**. The RO pin will be kept low as long as VCC1 is below the selected $V_{RT,x}$ threshold.*

5.1.2 SBC Normal Mode

The SBC Normal Mode is the standard operating mode for the SBC. All configurations have to be done in SBC Normal Mode before entering a low-power mode (see also **Chapter 5.1.6** for the device configuration defining the Fail-Safe Mode behavior). A wake-up event on CAN and WKx will create an interrupt on pin INT - however, no change of the SBC mode will occur. The configuration options are listed below:

- VCC1 is active
- VCC2 can be switched ON or OFF (default = OFF)
- VCC3 is configurable (OFF coming from SBC Init Mode; as previously programmed coming from SBC Restart Mode)
- CAN is configurable (OFF coming from SBC Init Mode; OFF or wake capable coming from SBC Restart Mode, see also **Chapter 5.1.5**)
- HS Outputs can be switched ON or OFF (default = OFF) or can be controlled by PWM; HS Outputs are OFF coming from SBC Restart Mode
- Wake pins show the input level and can be selected to be wake capable (interrupt)
- Cyclic sense can be configured with HS1...4 and Timer1 or Timer 2
- Cyclic wake can be configured with Timer1 or Timer2
- Watchdog is configurable
- All FOx outputs are OFF by default. Coming from SBC Restart Mode FOx can be active (due to a failure event, e.g. watchdog trigger failure, VCC1 short circuit, etc.) or inactive (no failure occurred)

In SBC Normal Mode, there is the possibility of testing the FO outputs, i.e. to verify if setting the FO pin to low will create the intended behavior within the system. The FO output can be enabled and then disabled again by the microcontroller by setting the **FO_ON** SPI bit. This feature is only intended for testing purposes.

5.1.3 SBC Stop Mode

The SBC Stop Mode is the first level technique to reduce the overall current consumption by setting the voltage regulators VCC1, VCC2 and VCC3 into a low-power mode. In this mode VCC1 is still active and supplying the microcontroller, which can enter a power down mode. The VCC2 supply, CAN mode as well as the HSx outputs can be configured to stay enabled. All kind of settings have to be done before entering SBC Stop Mode. In SBC Stop Mode any kind of SPI WRITE commands are ignored and the **SPI_FAIL** bit is set, except for changing to SBC Normal Mode, triggering a SBC Soft Reset, refreshing the watchdog as well as for reading and clearing the SPI status registers. A wake-up event on CAN and WKx will create an interrupt on pin INT - however, no change of the SBC mode will occur. The configuration options are listed below:

- VCC1 is ON
- VCC2 is fixed as configured in SBC Normal Mode
- VCC3 is fixed as configured in SBC Normal Mode
- CAN mode is fixed as configured in SBC Normal Mode
- WK pins are fixed as configured in SBC Normal Mode
- HS Outputs are fixed as configured in SBC Normal Mode
- Cyclic sense is fixed as configured in SBC Normal Mode
- Cyclic wake is fixed as configured in SBC Normal Mode
- Watchdog is fixed as configured in SBC Normal Mode
- SBC Soft Reset can be triggered
- FOx outputs are fixed, i.e. the state from SBC Normal Mode is maintained

An interrupt is triggered on the pin INT when SBC Stop Mode is entered and not all wake source signalization flags from **WK_STAT_1** and **WK_STAT_2** were cleared.

*Note: If switches are enabled during SBC Stop Mode, e.g. HSx on with or without PWM, then the SBC current consumption will increase (see **Chapter 4.4**).*

*Note: It is not possible to switch directly from SBC Stop Mode to SBC Sleep Mode. Doing so will also set the **SPI_FAIL** flag and will bring the SBC into Restart Mode.*

*Note: When WK1 and WK2 are configured for the alternate measurement function (**WK_MEAS** = 1) then the wake inputs cannot be selected as wake input sources.*

5.1.4 SBC Sleep Mode

The SBC Sleep Mode is the second level technique to reduce the overall current consumption to a minimum needed to react on wake-up events or for the SBC to perform autonomous actions (e.g. cyclic sense). In this mode, VCC1 is OFF and not supplying the microcontroller anymore.The VCC2 supply as well as the HSx outputs can be configured to stay enabled. The settings have to be done before entering SBC Sleep Mode. A wake-up event on CAN or WKx will bring the device via SBC Restart Mode into SBC Normal Mode again and signal the wake source. The configuration options are listed below:

- VCC1 is OFF
- VCC2 is fixed as configured in SBC Normal Mode
- VCC3 is fixed or OFF as configured in SBC Normal Mode
- CAN mode changes automatically from ON or Receive Only Mode to wake capable mode or can be selected to be OFF
- CAN must be set to CAN wake capable / CAN off mode before entering SBC Sleep Mode
- WK pins are fixed as configured in SBC Normal Mode
- HS Outputs are fixed as configured in SBC Normal Mode
- Cyclic sense is fixed as configured in SBC Normal Mode
- Cyclic wake is not available
- Watchdog is OFF
- FOx outputs are fixed, i.e. the state from SBC Normal Mode is maintained
- As VCC1 is OFF during SBC Sleep Mode, no SPI communication is possible;
- The Sleep Mode entry is signalled in the SPI register **DEV_STAT** with the bit **DEV_STAT**

It is not possible to switch all wake sources off in SBC Sleep Mode. Doing so will set the **SPI_FAIL** flag and will bring the SBC into SBC Restart Mode.

In order to enter SBC Sleep Mode successfully, all wake source signalization flags from **WK_STAT_1** and **WK_STAT_2** need to be cleared. A failure to do so will result in an immediate wake-up from SBC Sleep Mode by going via SBC Restart to Normal Mode.

All settings must be done before entering SBC Sleep Mode.

*Note: If switches are enabled during SBC Sleep mode, e.g. HSx on with or without PWM, then the SBC current consumption will increase (see **Chapter 4.4**).*

Note: Cyclic Sense function will not work properly anymore in case of an overcurrent, overtemperature, under- or overvoltage (in case function is selected) event because the respective HS switch will be disabled.

*Note: When WK1 and WK2 are configured for the alternate measurement function (**WK_MEAS** = 1) then the wake inputs cannot be selected as wake input sources.*

5.1.5 SBC Restart Mode

There are multiple reasons to enter the SBC Restart Mode. The purpose of the SBC Restart Mode is to reset the microcontroller:

- in case of undervoltage on VCC1 in SBC Normal and in SBC Stop Mode,
- in case of overvoltage on VCC1 if the bit **VCC1_OV_RST** is set and if **CFGP** = '1',
- due to 1st incorrect Watchdog triggering (only if Config1, Config3 or Config 4 is selected, otherwise SBC Fail-Safe Mode is immediately entered),
- In case of a wake event from SBC Sleep or SBC Fail-Safe Mode or a release of overtemperature shutdown (TSD2) out of SBC Fail-Safe Mode this transition is used to ramp up VCC1 after a wake in a defined way.

From SBC Restart Mode, the SBC goes automatically to SBC Normal Mode, i.e the mode is left automatically by the SBC without any microcontroller influence. The SBC **MODE** bits are cleared. As shown in **Figure 46** the Reset Output (RO) is pulled low when entering Restart Mode and is released at the transition to Normal Mode after the reset delay time (t_{RD1}). The watchdog timer will start with a long open window starting from the moment of the rising edge of RO and the watchdog period setting in the register **WD_CTRL** will be changed to the respective default value '100'.

Leaving the SBC Restart Mode will not result in changing / deactivating the Fail outputs.

The behavior of the blocks is listed below:

- All FOx outputs are activated in case of a 1st watchdog trigger failure (if Config1 or Config2 is selected) or in case of VCC1 overvoltage detection (if **VCC1_OV_RST** is set)
- VCC1 is ON or ramping up
- VCC2 will be disabled if it was activated before
- VCC3 is fixed or ramping as configured in SBC Normal Mode
- CAN is "woken" due to a wake event or OFF depending on previous SBC and transceiver mode (see also **Chapter 10**). It is wake capable when it was in CAN Normal-, Receive Only or wake capable mode before SBC Restart Mode
- HS Outputs will be disabled if they were activated before
- RO is pulled low during SBC Restart Mode
- SPI communication is ignored by the SBC, i.e. it is not interpreted
- The Restart Mode entry is signalled in the SPI register **DEV_STAT** with the bits **DEV_STAT**

Table 7 Reasons for Restart - State of SPI Status Bits after Return to Normal Mode

Prev. SBC Mode	Event	DEV_STAT	WD_FAIL	VCC1_UV	VCC1_OV	VCC1_SC
Normal	1x Watchdog Failure	01	01	x	x	x
Normal	2x Watchdog Failure	01	10	x	x	x
Normal	VCC1 undervoltage reset	01	xx	1	x	x
Normal	VCC1 overvoltage reset	01	xx	x	1	x
Stop	1x Watchdog Failure	01	01	x	x	x
Stop	2x Watchdog Failure	01	10	x	x	x
Stop	VCC1 undervoltage reset	01	xx	1	x	x
Stop	VCC1 overvoltage reset	01	xx	x	1	x
Sleep	Wake-up event	10	xx	x	x	x
Fail-Safe	Wake-up event	01	see "Reasons for Fail Safe, **Table 8**"			

*Note: An overvoltage event on VCC1 will only lead to SBC Restart Mode if the bit VCC1_OV_RST is set and if **CFGP** = '1' (Config 1/3).*

Note: The content of the WD_FAIL bits will depend on the device configuration, e.g. 1 or 2 watchdog failures.

5.1.6 SBC Fail-Safe Mode

The purpose of this mode is to bring the system in a safe status after a failure condition by turning off the VCC1 supply and powering off the microcontroller. After a wake event the system is then able to restart again.

The Fail-Safe Mode is automatically reached for following events:

- after an SBC thermal shutdown (TSD2) (see also **Chapter 14.9.3**),
- in case of overvoltage on VCC1 if the bit **VCC1_OV_RST** is set and if **CFGP** = '0',
- after a 1st incorrect watchdog trigger in Config2 (**CFG** = 1) and after a 2nd incorrect watchdog trigger in Config4 (**CFG** = 0) (see also **Chapter 5.1.1**),
- if VCC1 is shorted to GND (see also **Chapter 14.7**),
- After 4 consecutive VCC1 undervoltage events (only if VS > $V_{S,UV}$, see **Chapter 14.6**).

In this case, the default wake sources (CAN, WK1...3, see also registers **WK_CTRL_2**, **BUS_CTRL_1**) are activated, the wake events are cleared in the register **WK_STAT_1**, and all output drivers and all voltage regulators are switched off. When WK1 and WK2 are configured for the alternate measurement function (**WK_MEAS** = 1) then WK1 and WK2 will stay configured for the measurement function when SBC Fail-Safe Mode is entered, i.e. they will not be activated as wake sources.

The SBC Fail-Safe Mode will be maintained until a wake event on the default wake sources occurs. To avoid any fast toggling behavior a filter time of typ. 100ms ($t_{FS,min}$) is implemented. Wake events during this time will be stored and will automatically lead to entering SBC Restart Mode after the filter time.
In case of an VCC1 overtemperature shutdown (TSD2) the SBC Restart Mode will be reached automatically after a filter time of typ. 1s (t_{TSD2}) without the need of a wake event.
Leaving the SBC Fail-Safe Mode will not result in deactivation of the Fail Output pins.
The following functions are influenced during SBC Fail-Safe Mode:

- All FOx outputs are activated (see also **Chapter 13**)
- VCC1 is OFF
- VCC2 is OFF
- VCC3 is OFF
- CAN is wake capable
- HS Outputs are OFF
- WK pins are wake capable through static sense (with default 16µs filter time)
- Cyclic sense and Cyclic wake is disabled
- SPI communication is disabled because VCC1 is OFF
- The Fail-Safe Mode activation is signalled in the SPI register **DEV_STAT** with the bits **FAILURE** and **DEV_STAT**

Table 8 Reasons for Fail-Safe - State of SPI Status Bits after Return to Normal Mode

Prev. SBC Mode	Failure Event	DEV_ STAT	TSD2	WD_ FAIL	VCC1_ UV	VCC1_ UV_FS	VCC1_ OV	VCC1_ SC
Normal	1 x Watchdog Failure	01	x	01	x	x	x	x
Normal	2 x Watchdog Failure	01	x	10	x	x	x	x
Normal	TSD2	01	1	xx	x	x	x	x
Normal	VCC1 short to GND	01	x	xx	1	x	x	1
Normal	4x VCC1 UV	01	x	xx	1	1	x	x
Normal	VCC1 overvoltage	01	x	xx	x	x	1	x
Stop	1 x Watchdog Failure	01	x	01	x	x	x	x
Stop	2 x Watchdog Failure	01	x	10	x	x	x	x
Stop	TSD2	01	1	xx	x	x	x	x
Stop	VCC1 short to GND	01	x	xx	1	x	x	1
Stop	4x VCC1 UV	01	x	xx	1	1	x	x
Stop	VCC1 overvoltage	01	x	xx	x	x	1	x

*Note: An overvoltage event on VCC1 will only lead to SBC Fail-Safe Mode if the bit VCC1_OV_RST is set and if **CFGP** = '0' (Config 2/4).*

Note: The content of the WD_FAIL bits will depend on the device configuration, e.g. 1 or 2 watchdog failures.

*Note: See **Chapter 14.6.1** for detailed description of the 4x VCC1 undervoltage behavior.*

5.1.7 SBC Development Mode

The SBC Development Mode is used during the development phase of the module. It is especially useful for software development.

Compared to the default SBC user mode operation, this mode is a super set of the state machine. The device will start also in SBC Init Mode and it is possible to use all the SBC Modes and functions with following differences:

- Watchdog is stopped and does not need to be triggered. Therefore no reset is triggered due to watchdog failure
- SBC Fail-Safe and SBC Restart Mode are not reached due to watchdog failure but the other reasons to enter these modes are still valid
- CAN and VCC2 default value in SBC INIT MODE and entering SBC Normal Mode from SBC Init Mode is ON instead of OFF

The SBC Development Mode is reached automatically if the FO3/TEST pin is set and kept LOW during SBC Init Mode. The voltage level monitoring is started as soon as VS > $V_{POR,f}$. The Development Mode is configured and maintained if SBC Init Mode is left by sending any SPI command while FO3/TEST is LOW. In case the FO3/TEST level will be HIGH for longer than t_{TEST} during the monitoring period then the SBC Development Mode is not reached .

The SBC will remain in this mode for all conditions and can only be left by powering down the device (VS < **$V_{POR,f}$**).

*Note: The absolute maximum ratings of the pin FO3/TEST must be observed. To increase the robustness of this pin during debugging or programming a series resistor between FO3/TEST and the connector can be added (see **Figure 60**).*

5.2 Wake Features

Following wake sources are implemented in the device:

- Static Sense: WK inputs are permanently active (see **Chapter 11**)
- Cyclic Sense: WK inputs only active during on-time of cyclic sense period (see below)
- Cyclic Wake: internal wake source controlled via internal timer (see below)
- CAN wake: Wake-up via CAN message (see **Chapter 10**)

5.2.1 Cyclic Sense

The cyclic sense feature is intended to reduce the quiescent current of the device and the application.
In the cyclic sense configuration, one or more high-side drivers are switched on periodically controlled by **TIMER1_CTRL** and **TIMER2_CTRL**. The respective high-side drivers supply external circuitries e.g. switches and/or resistor arrays, which are connected to one or more wake inputs (see **Figure 5**). Any edge change of the WKx input signal during the on-time of the cyclic sense period causes a wake. Depending on the SBC mode, either the INT is pulled low (SBC Normal Mode and Stop Mode) or the SBC is woken enabling the VCC1 (after SBC Sleep and SBC Fail-Safe Mode).

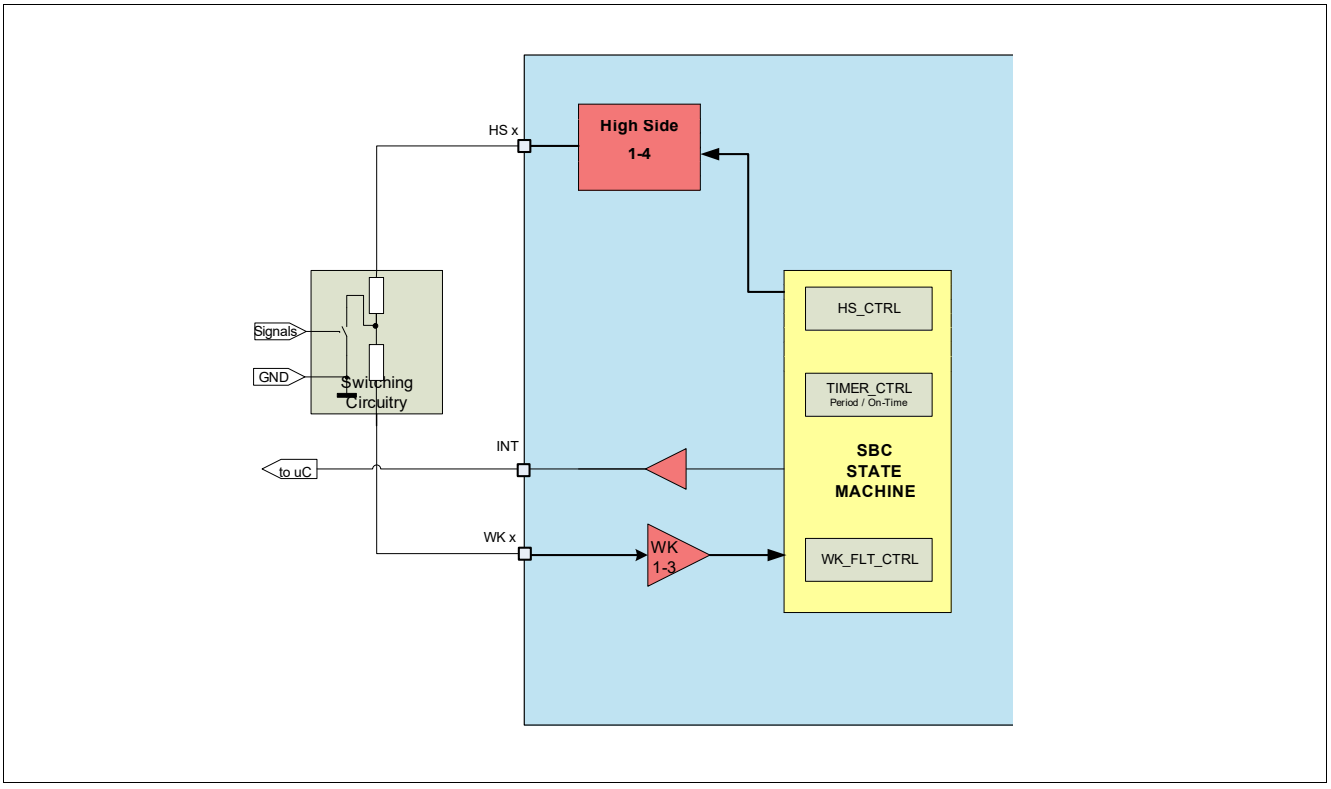

Figure 5 Cyclic Sense Working Principle

5.2.1.1 Configuration and Operation of Cyclic Sense

The correct sequence to configure the cyclic sense is shown in **Figure 6**. All the configurations have to be performed before the on-time is set in the TIMERx_CTRL registers. The settings “OFF / LOW” and “OFF / HIGH” define the voltage level of the respective HS driver before the start of the cyclic sense. The intention of this selection is to avoid an unintentional wake due to a voltage level change at the start of the cyclic sense.

Cyclic Sense (=TimerX) will start as soon as the respective on-time has been selected independently from the assignment of the HS and filter configuration. The selection of the respective timer (Config C/D see **Chapter 11.2.1**) must therefore be done before starting the timer. The correct configuration sequence is as follows:

- Configure the initial level
- Mapping of a Timer to the respective HSx outputs
- Configuring the respective filter timing and WK pins
- Configuring the timer period and on-time

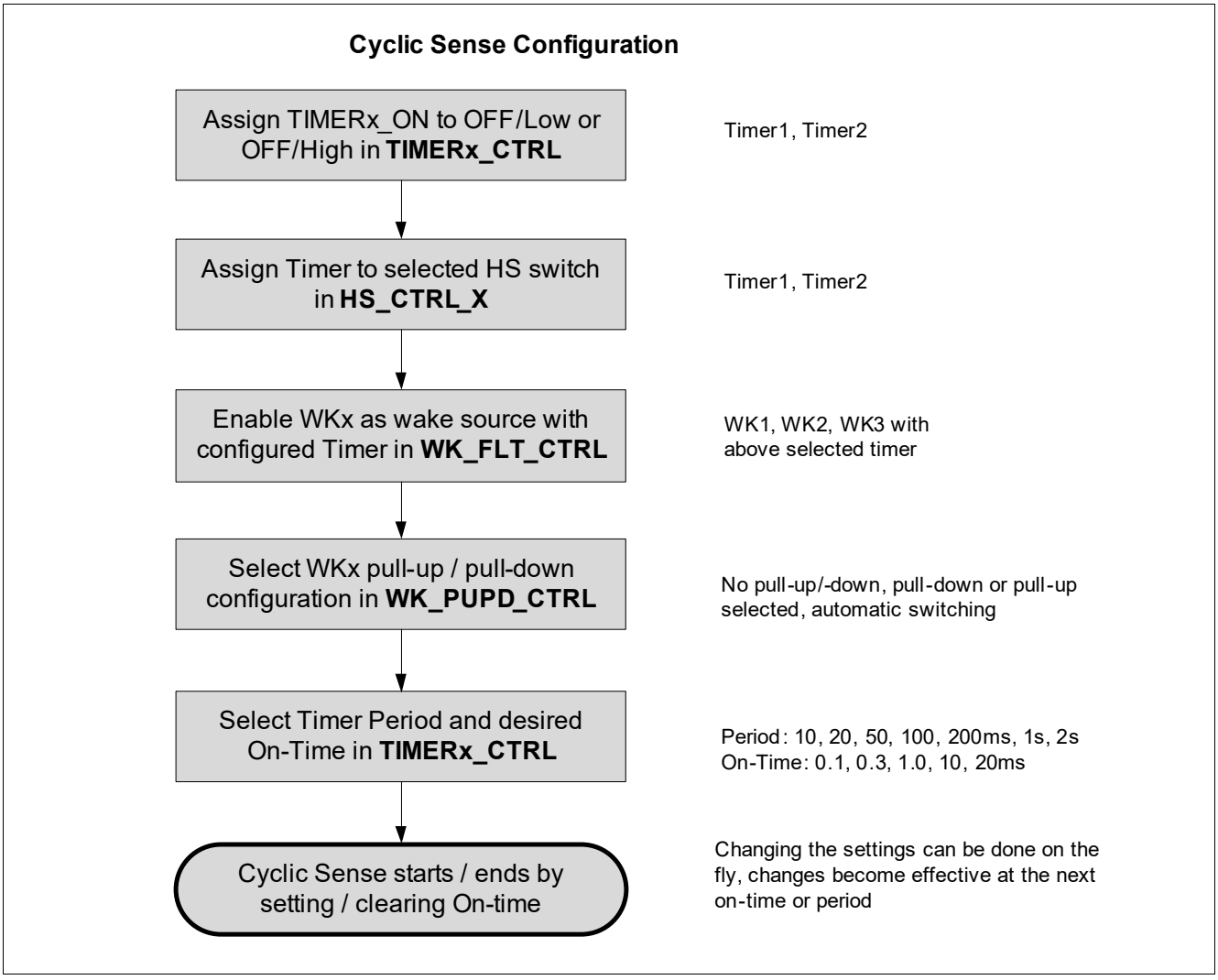

Figure 6 Cyclic Sense: Configuration and Sequence

Note: All configurations of period and on-time can be selected. However, recommended on-times for cyclic sense are 0.1ms, 0.3ms and 1ms. The SPI_FAIL will be set if the on-time is longer than the period.

The first sample of the WK input value (HIGH or LOW) is taken as the reference for the next cycle. A change of the WK input value between the first and second cycle recognized during the on-time of the second cycle will cause a wake from SBC Sleep Mode or an interrupt during SBC Normal or SBC Stop Mode.

A filter time of 16µs is implemented to avoid a parasitic wake-up due to transients or EMC disturbances. The filter time t_{FWK1} is triggered right at the end of the selected on-time and a wake signal is recognized if:

- the input level will not cross the switching threshold level of typ. 3V during the selected filter time (i.e. if the signal will keep the HIGH or LOW level) and
- there was an input level change between the current and previous cycle

A wake event due to cyclic sense will set the respective bit WK1_WU, WK2_WU, or WK3_WU.

During Cyclic Sense, **WK_LVL_STAT** is updated only with the sampled voltage levels of the WKx pins in SBC Normal or SBC Stop Mode.

The functionality of the sampling and different scenarios are depicted in **Figure 7** to **Figure 9**. The behavior in SBC Stop and SBC Sleep Mode is identical except that in Stop Mode INT will be triggered to signal a change of WK input levels and in SBC Sleep Mode, VCC1 will power-up instead.

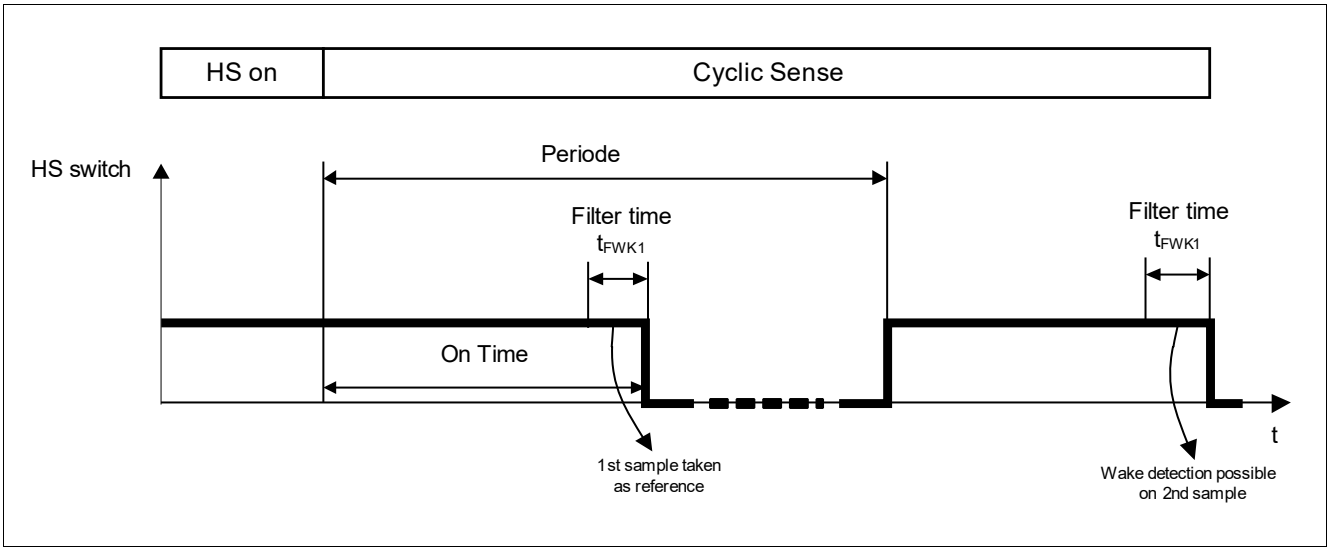

Figure 7 Wake Input Timing

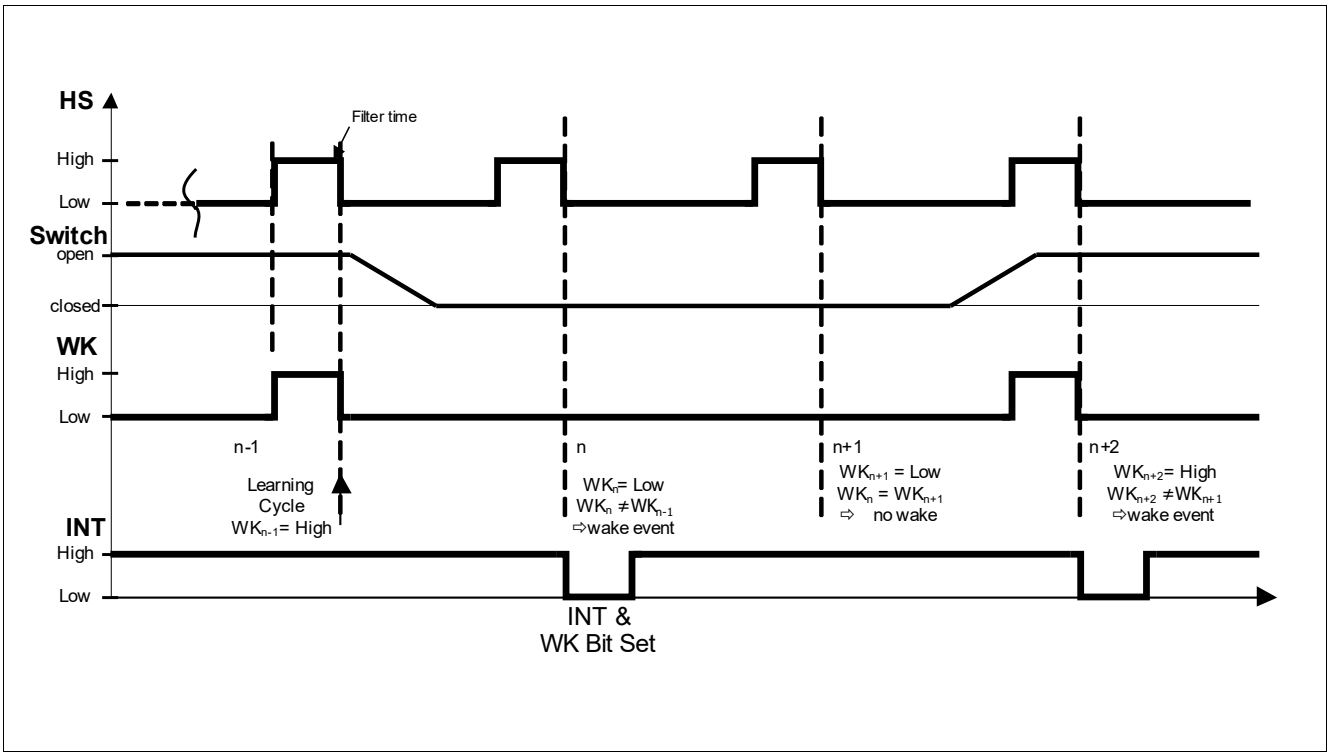

Figure 8 Cyclic Sense Example in SBC Stop Mode, HSx starts “OFF”/LOW, GND based WKx input

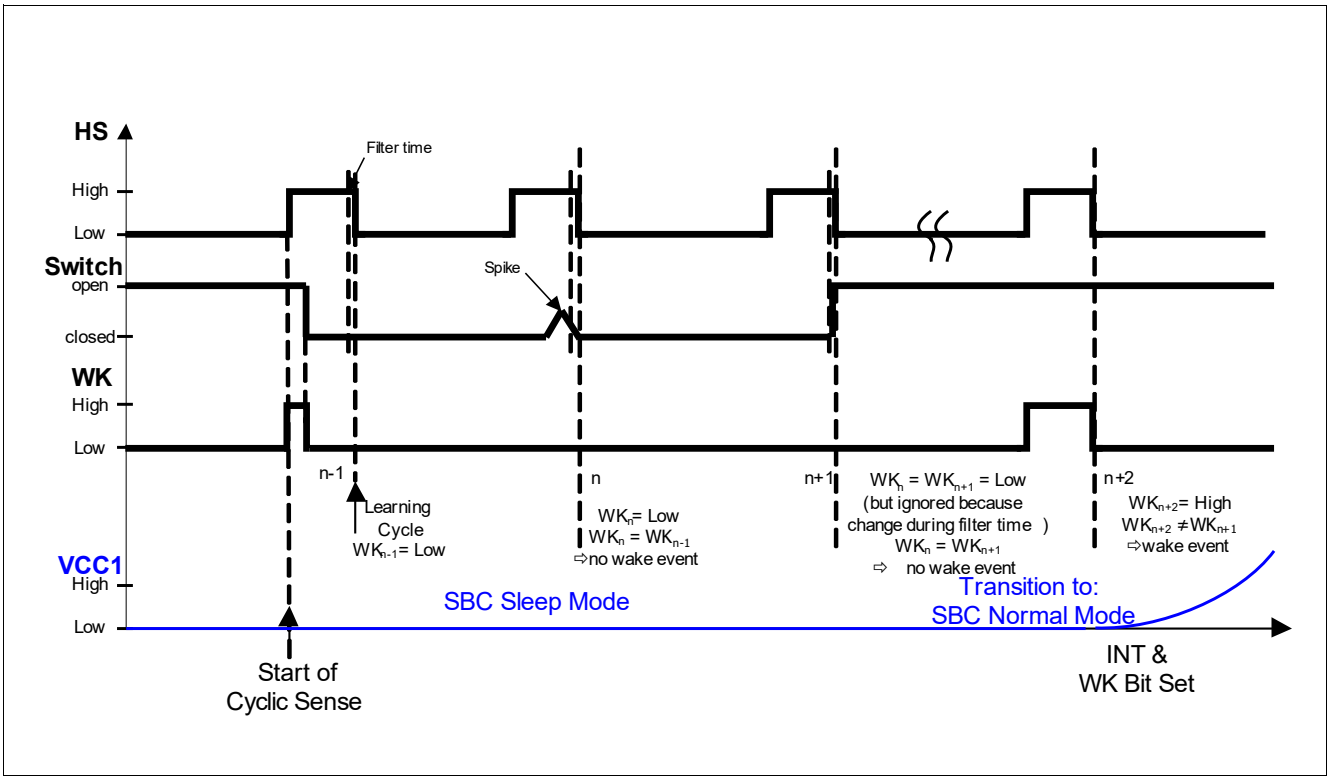

Figure 9 Cyclic Sense Example in SBC Sleep Mode, HSx starts "OFF"/HIGH, GND based WKx input

The cyclic sense function will not work properly anymore in case of following conditions:

- in case SBC Fail-Safe Mode is entered: The respective HS Switch will be disabled and the respective wake pin will be changed to static sensing
- In SBC Normal, Stop, or Sleep Mode in case of an overcurrent, overtemperature, under- or overvoltage (in case function is selected) event: the respective HS switch will be disabled

Note: The internal timers for cyclic sense are not disabled automatically in case the HS switch is turned off due to above mentioned failures.This must be considered to avoid loss of wake events.

5.2.1.2 Cyclic Sense in Low Power Mode

If cyclic sense is intended for SBC Stop or SBC Sleep Mode mode, it is necessary to activate the cyclic sense in SBC Normal Mode before going to the low power mode. A wake event due to cyclic sense will set the respective bit WK1_WU, WK2_WU or WK3_WU. In Stop Mode the wake event will trigger an interrupt, in Sleep Mode the wake event will send the device via Restart Mode to Normal Mode. Before returning to SBC Sleep Mode, the wake status register **WK_STAT_1** and **WK_STAT_2** needs to be cleared. Trying to go to SBC Sleep mode with uncleared wake flags, such as WKx_WU the SBC will directly wake-up from Sleep Mode by going via Restart Mode to Normal Mode, a reset is issued. The WKx_WU bit is seen as source for the wake. This is implemented in order not to loose an wake event during the transition.

5.2.2 Cyclic Wake

The cyclic wake feature is intended to reduce the quiescent current of the device and application.

For the cyclic wake feature one or both timers are configured as internal wake-up source and will periodically trigger an interrupt in SBC Normal and SBC Stop Mode.

The correct sequence to configure the cyclic wake is shown in **Figure 10**. The sequence is as follows:

- First, disable the timers to ensure that there is not unintentional interrupt when activating cyclic wake,
- Enable Timer1 and/or Timer2 as a wake-up source in the register **WK_CTRL_1**,
- Configure the respective period Timer1 and/or Timer2. Also an on-time (any value) must be selected to start the cyclic wake even if the value is ignored.

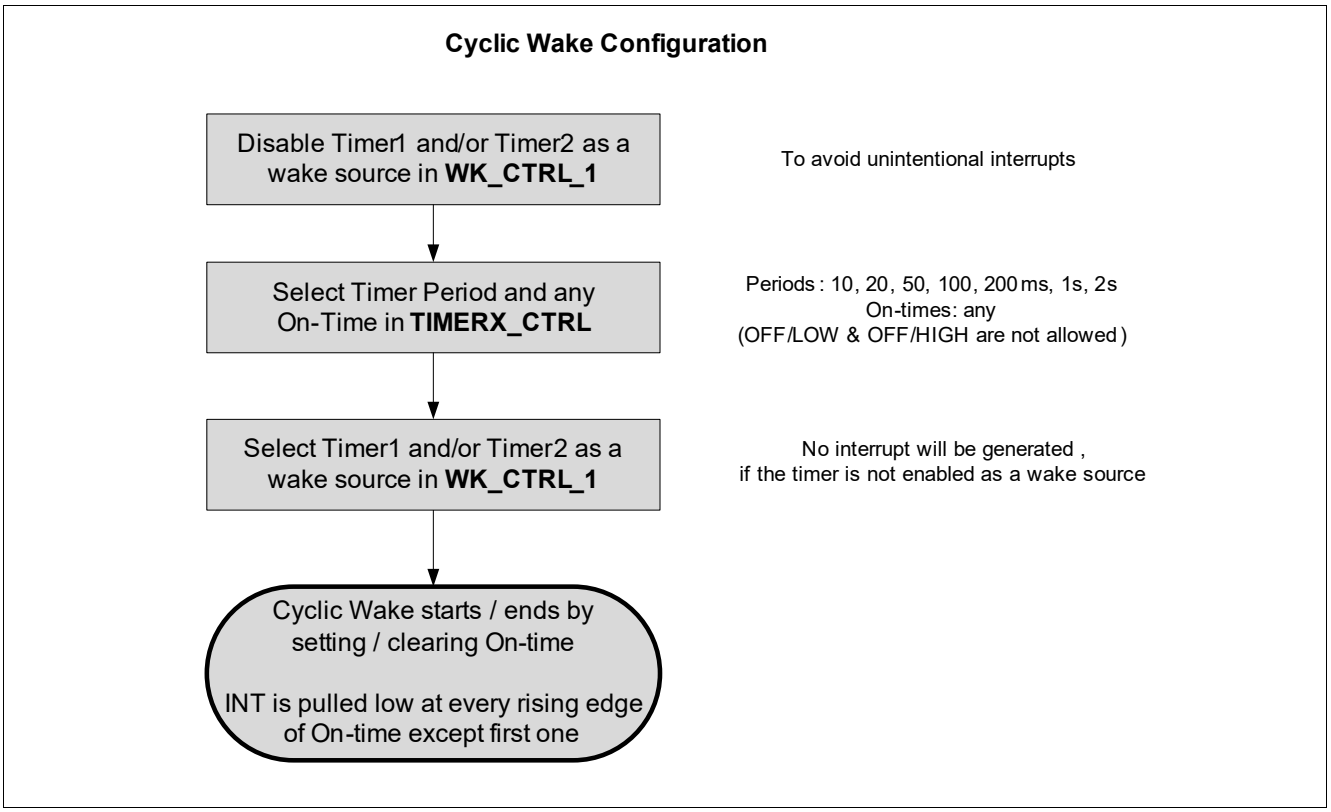

Figure 10 Cyclic Wake: Configuration and Sequence

As in cyclic sense, the cyclic wake function will start as soon as the on-time is configured. An interrupt is generated for every start of the on time except for the very first time when the timer is started

5.2.3 Internal Timer

The integrated Timer1 and Timer2 are typically used to wake up the microcontroller periodically (cyclic wake) or to perform cyclic sense on the wake inputs. Therefore, the timers can be mapped to the dedicated HS switches by SPI (via **HS_CTRL1**...2).

Following periods and on-times can be selected via the register **TIMER1_CTRL** and **TIMER2_CTRL** respectively:

- Period: 10ms / 20ms / 50ms / 100ms / 200ms / 1s / 2s
- On time: 0.1ms / 0.3ms / 1.0ms / 10ms / 20ms / OFF at HIGH or LOW

5.3 Supervision Features

The device offers various supervision features to support functional safety requirements. Please see **Chapter 14** for more information.

5.4 Partial Networking on CAN

5.4.1 CAN Partial Networking - Selective Wake Feature

The CAN Partial Networking feature can be activated for SBC Normal Mode, in SBC Sleep Mode and in SBC Stop Mode. For SBC Sleep Mode the Partial Networking has to be activated before sending the SBC to Sleep Mode. For SBC Stop Mode the Partial Networking has to be activated before going to SBC Stop Mode.

There are 2 detection mechanism available

- WUP (Wake-Up Pattern) this is a CAN wake, that reacts on the CAN dominant time, with 2 dominant signals as defined in ISO 11898-2:2016.
- WUF (Wake-Up frame) this is the wake-up on a CAN frame that matches the programmed message filter configured in the SBC via SPI.

The default baudrate is set to 500kBaud. Besides the commonly used baudrates of 125kBaud and 250kBaud, other baudrates up to 1MBaud can be selected (see **Chapter 15.5.2** and **Chapter 15.5.3** for more details).

5.4.2 SBC Partial Networking Function

The CAN Partial Networking Modes are shown in this figure.

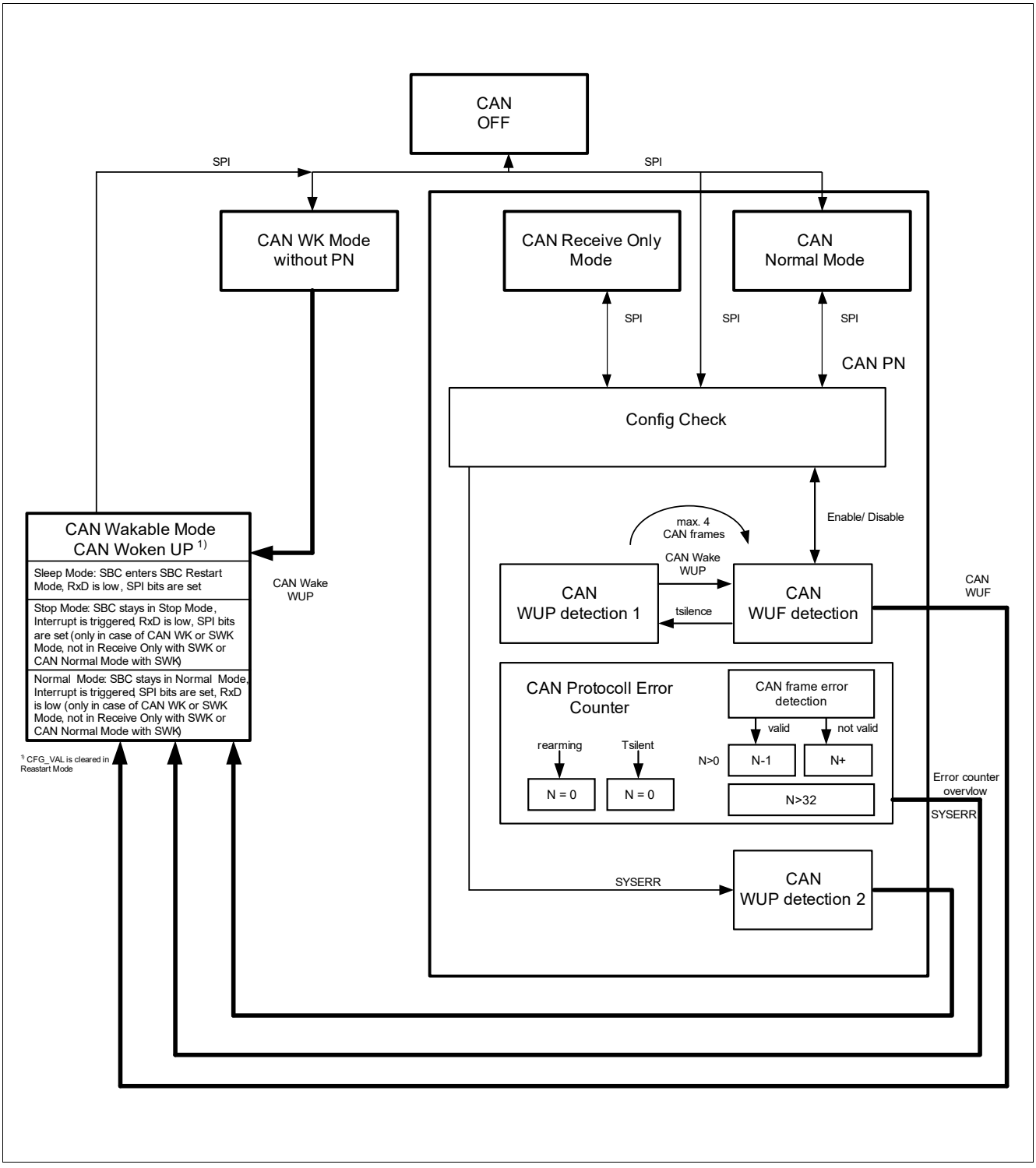

Figure 11 CAN Selective Wake State Diagram

5.4.2.1 Activation of SWK

Below figure shows the principal of the SWK activation.

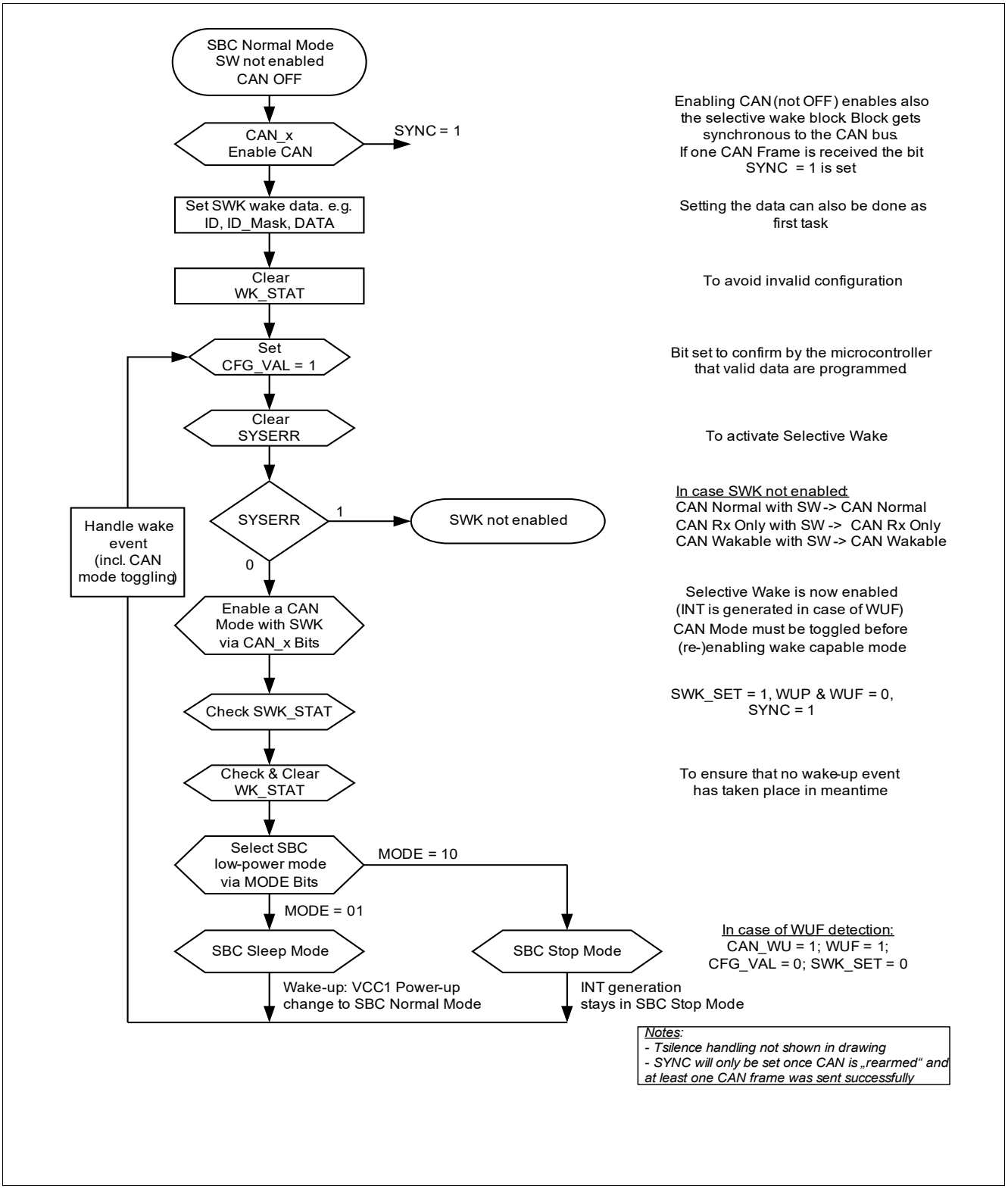

Figure 12 Flow for activation of SWK

5.4.2.2 Wake-up Pattern (WUP)

A WUP is signaled on the bus by two consecutive dominant bus levels for at least t_{Wake1}, each separated by a recessive bus level.

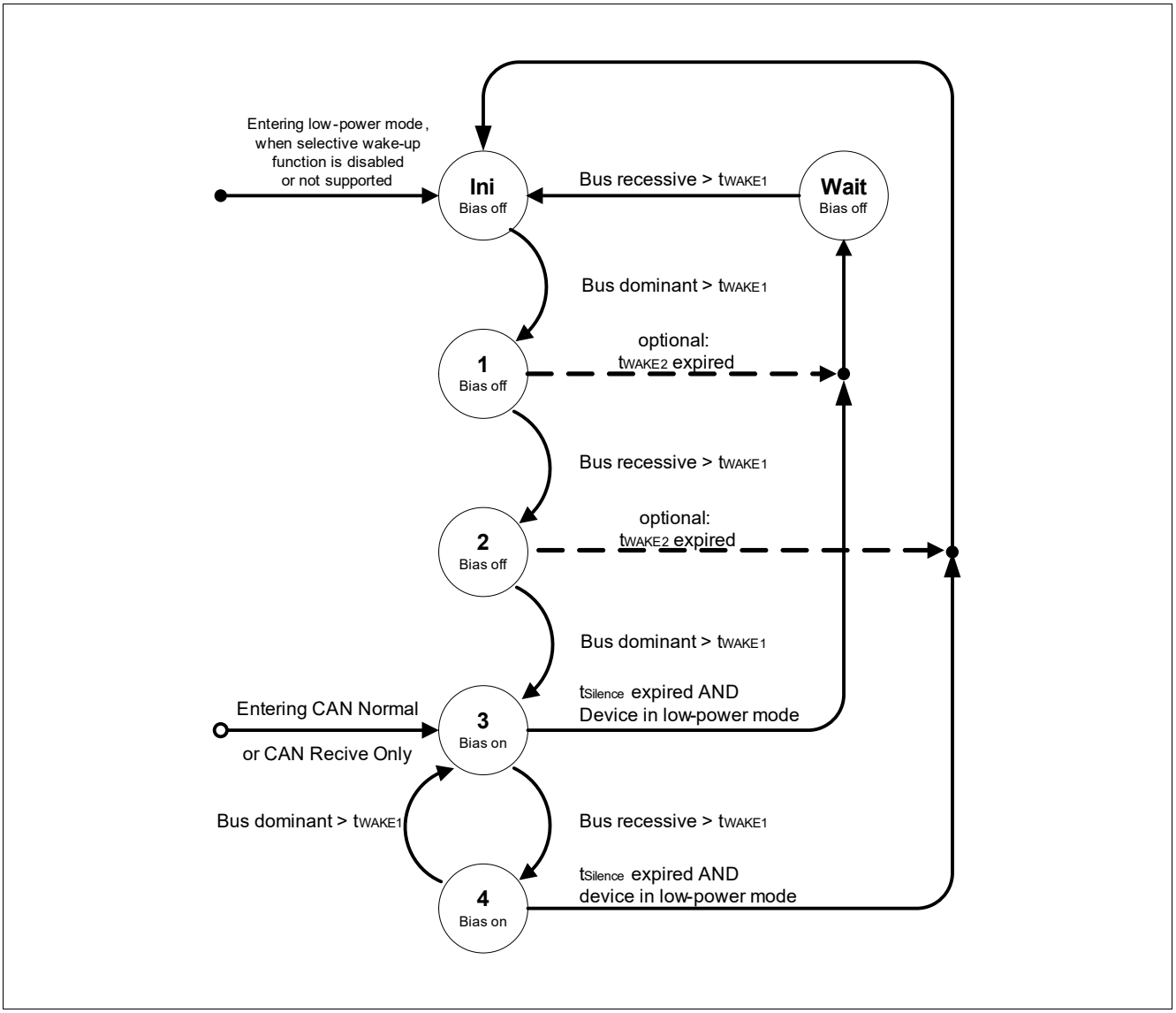

Figure 13 WUP detection following the definition in ISO 11898-2:2016

5.4.2.3 Wake-up Frame (WUF)

The wake-up frame is detection is implemented as defined in ISO 11898-2:2016.

Only CAN frames according ISO11989-1 are considered as potential wake-up frames.

A bus wake-up shall be performed, if selective wake-up function is enabled and a "valid WUF" has been received. The transceiver may ignore up to four consecutive CAN data frames that start after switching on the bias.

A received frame is a “valid WUF” in case all of the following conditions are met:

- The ID of the received frame is exactly matching a configured ID in the relevant bit positions. The relevant bit positions are given by an ID mask. The ID and the ID mask might have either 11 bits or 29 bits.
- The DLC of the received frame is exactly matching the configured DLC.

- In case DLC is greater than 0, the data field of the received frame has at least one bit set in a bit position, where also in the configured data mask in the corresponding bit position the bit is set.
- No error exists according to ISO 11898-1 excepting errors which are signalled in the ACK field and EOF field.

5.4.2.4 CAN Protocol Error Counter

The counter is incremented, when a bit stuffing, CRC or form error according to ISO11898-1 is detected. If a frame has been received that is valid up to the end of the CRC field and the counter is not zero, the counter is decremented.
If the counter has reached a value of 31, the following actions is performed on the next increment of this counter:

- The selective wake function is disabled,
- the CAN transceiver is woken,
- SYSERR is set and the error counter value = 32 can be read.

On each increment or decrement of the counter the decoder unit waits for at least 6 and most 10 recessive bits before considering a dominant bit as new start of frame.

The error counter is enabled:

- whenever the CAN is in Normal Mode, Receive Only Mode or in WUF detection state.

The error counter is cleared under the following conditions:

- at the transition from WUF detection to WUP detection 1 (after $t_{SILENCE}$ expiration, while SWK is correctly enabled)
- When WUF detection state is entered (in this way the counter will start from 0 when SWK is enabled)
- At SBC or CAN rearming (when exiting the woken state)
- When the CAN Mode bits are selected ‘000’, ‘100’ (CAN OFF) or 0’01’ (Wake capable without SWK function enabled)
- While CAN_FD_EN = ‘1’ and DIS_ERR_CNT = ‘1’
  (the counter is cleared and stays cleared when these two bits are set in the SPI registers)

The Error Counter is frozen:

- after a wake-up being in woken state

The counter value can be read out of the bits **ECNT**.

5.4.3 Diagnoses Flags

5.4.3.1 PWRON/RESET-FLAG

The power-on reset can be detected and read by the **POR** bit in the SBC Status register.

The VS power on resets all register in the SBC to reset value. SWK is not configured.

5.4.3.2 BUSERR-Flag

Bus Dominant Time-out detection is implemented and signaled by CAN_Fail_x in register **BUS_STAT_1**.

5.4.3.3 TXD Dominant Time-out flag

TXD Dominant timeout is shown in the SPI bit CAN_FAIL_x in register **BUS_STAT_1**.

5.4.3.4 WUP Flag

The WUP bit in the **SWK_STAT** register shows that a Wake-Up Pattern (WUP) has caused a wake of the CAN transceiver. It can also indicate an internal mode change from WUP detection 1 state to WUF detection after a valid WUP.

In the following case the bit is set:

- SWK is activated: due to $t_{SILENCE}$, the CAN changes into the state WUP detection 1. If a WUP is detected in this state, then the **WUP** bit is set
- SWK is deactivated: the **WUP** bit is set if a WUP wakes up the CAN. In addition, the **CAN_WU** bit is set.
- in case WUP is detected during WUP detection 2 state (after a SYSERR) the bits **WUP** and **CAN_WU** are set

The **WUP** bit is cleared automatically by the SBC at the next rearming of the CAN transceiver.

*Note: It is possible that WUF and WUP bit are set at the same time if a WUF causes a wake out of SWK, by setting the interrupt or by restart out of SBC Sleep Mode. The reason is because the CAN has been in WUP detection 1 state during the time of SWK mode (because of $t_{SILENCE}$). See also **Figure 11**.*

5.4.3.5 WUF Flag (WUF)

The WUF bit in the **SWK_STAT** register shows that a Wake-Up frame (WUF) has caused a wake of the CAN block. In SBC Sleep Mode this wake causes a transition to SBC Restart Mode, in SBC Normal Mode and in SBC Stop Mode it causes an interrupt. Also in case of this wake the bit **CAN_WU** in the register **WK_STAT_1** is set.

The **WUF** bit is cleared automatically by the SBC at the next rearming of the CAN SWK function.

5.4.3.6 SYSERR Flag (SYSERR)

The bit SYSERR is set in case of an configuration error and in case of an error counter overflow. The bit is only updated (set to ‘1’) if a CAN mode with SWK is enabled via CAN_x. If **INT_ GLOBAL** is set, then an interrupt is triggered on INTN every time **SYSERR** is set.

When programming selective wake via CAN_x, SYSERR = ‘0’ signals that the SWK function has been enabled. The bit can be cleared via SPI. The bit is ‘0’ after Power on Reset of the SBC.

5.4.3.7 Configuration Error

A configuration error sets the SYSERR bit to ‘1’. When enabling SWK via the bits CAN_x a config check is done. If the check is successful SWK is enabled, the bit SYSERR is set to ‘0’. In SBC Normal Mode it is also possible to

detect a Configuration Error while SWK is enabled. This will occur if the **CFG_VAL** bit is cleared, e.g. by changing the SWK registers (from address 010 0001 to address 011 0011). In SBC Stop Mode and SBC Sleep Mode this is not possible as the SWK registers can not be changed.

Configuration Check:
in SBC Restart Mode, the **CFG_VAL** bit is cleared by the SBC. If the SBC Restart Mode was not triggered by a WUF wake up from SBC Sleep Mode and the CAN was with SWK enabled, than the **SYSERR** bit will be set.
The SYSERR bit has to be cleared by the microcontroller.
The SYSERR bit cannot be cleared when CAN_2 is '1' and below conditions occur:

- Data valid bit not set by microcontroller, i.e. **CFG_VAL** is not set to '1'. The **CFG_VAL** bit is reset after SWK wake and needs to be set by the microcontroller before activation SWK again.
- **CFG_VAL** bit reset by the SBC when data are changed via SPI programming. (Only possible in SBC Normal Mode)

*Note: The SWK configuration is still valid if only the **SWK_CTRL** register is modified.*

5.4.3.8 CAN Bus Timeout-Flag (CANTO)

In CAN WUF detection and CAN WUP detection 2 state the bit CANTO is set to '1' if the time tSILENCE expires. The bit can be cleared by the microcontroller. If the interrupt function for CANTO is enabled then an interrupt is generated in SBC Stop or SBC Normal Mode when the CANTO set to '1'. The interrupt is enabled by setting the bit **CANTO_ MASK** to '1'. Each CANTO event will trigger a interrupt even if the CANTO bit is not cleared.

There is no wake out of SBC Sleep Mode because of CAN time-out.

5.4.3.9 CAN Bus Silence-Flag (CANSIL)

In CAN WUF detection and CAN WUP detection 2 state the bit CANSIL is set to '1' if the time $t_{SILENCE}$ expires. The CANSIL bit is set back to '0' with a WUP. With this bit the microcontroller can monitor if there is activity on the CAN bus while being in SWK Mode. The bit can be read in SBC Stop and SBC Normal Mode.

5.4.3.10 SYNC-FLAG (SYNC)

The bit SYNC shows that SWK is working and synchronous to the CAN bus. To get a SYNC bit set it is required to enable the CAN to CAN Normal or in Receive Only Mode or in WUF detection. It is not required to enable the CAN SWK Mode.

The bit is set to '1' if a valid CAN frame has been received (no CRC error and no stuffing error). It is set back to '0' if a CAN protocol error is detected. When switching into SWK mode the SYNC bit indicates to the microcontroller that the frame detection is running and the next CAN frame can be detected as a WUF, CAN wake-up can now be handled by the SBC. It is possible to enter a SBC low-power mode with SWK even if the bit is not set to '1', as this is necessary in case of a silent bus.

5.4.3.11 SWK_SET FLAG (SWK_SET)

The SWK_SET bit is set to signalize the following states (see also **Figure 11**):

- when SWK was correctly enabled in WUF Detection state,
- when SWK was correctly enabled when in WUP Detection 1 state,
- after a SYSERR before a wake event in WUP Detection 2 state,

The bit is cleared under following conditions:

- after a wake-up (ECNT overflow, WUP in WUP detection 2, WUF in WUF detection)
- if CAN_2 is cleared

5.4.4 SBC Modes for Selective Wake (SWK)

The SBC mode is selected via the **MODE** bits as described in **Chapter 5.1**.

The mode of the CAN transceiver needs to be selected in SBC Normal Mode. The CAN mode is programed the bits CAN_0, CAN_1 and CAN_2. In the low-power modes (SBC Stop, SBC Sleep) the CAN mode can not be changed via SPI.

The detailed SBC state machine diagram including the CAN selective wake feature is shown in **Figure 6**.

The application must now distinguish between the normal CAN operation an the selective wake function:

- WK Mode: This is the normal CAN wake capable mode without the selective wake function
- SWK Mode: This is the CAN wake capable mode with the selective wake function enabled

Figure 14 shows the possible CAN transceiver modes.

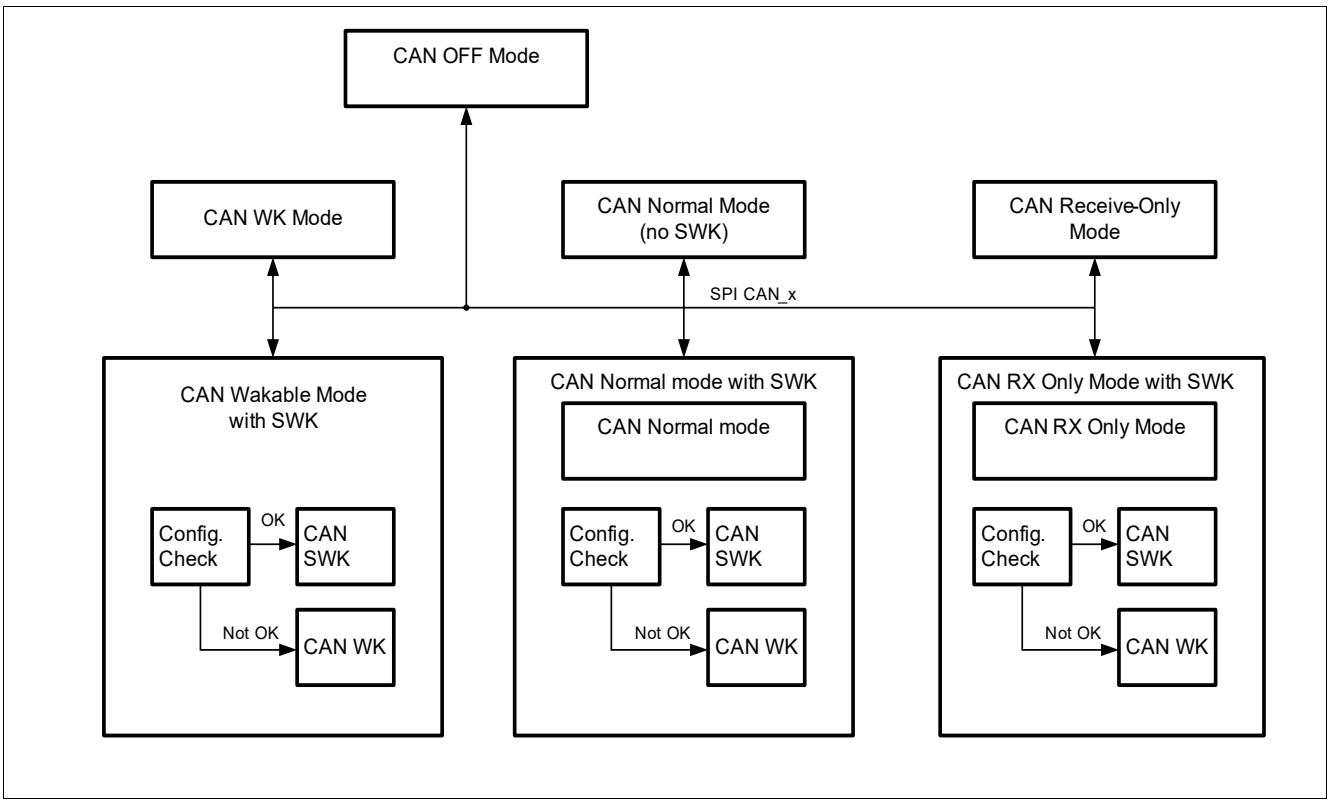

Figure 14 CAN SWK State Diagram

5.4.4.1 SBC Normal Mode with SWK

In SBC Normal Mode the CAN Transceiver can be switched into the following CAN Modes

- CAN OFF
- CAN WK Mode (without SWK)
- CAN SWK Mode
- CAN Receive Only (No SWK activated)
- CAN Receive Only Mode with SWK
- CAN Normal Mode (No SWK activated)
- CAN Normal Mode with SWK

In the CAN Normal Mode with SWK the CAN Transceiver works as in SBC Normal Mode, so bus data is received through RXD, data is transmitted through TXD and sent to the bus. In addition the SWK block is active. It

monitors the data on the CAN bus, updates the error counter and sets the **CANSIL** flag if there is no communication on the bus.
It will generate an CAN Wake interrupt in case a WUF is detected (RXD is not pulled to LOW in this configuration).

In CAN Receive Only Mode with SWK, CAN data can be received on RXD and SWK is active, no data can be sent to the bus.

The bit **SYSERR** = '0' indicates that the SWK function is enabled, and no frame error counter overflow is detected.

Table 9 CAN Modes selected via SPI in SBC Normal Mode

CAN Mode	CAN_2	CAN_1	CAN_0
CAN OFF	0	0	0
CAN WK Mode (no SWK)	0	0	1
CAN Receive Only (no SWK)	0	1	0
CAN Normal Mode (no SWK)	0	1	1
CAN OFF	1	0	0
CAN SWK Mode	1	0	1
CAN Receive Only with SWK	1	1	0
CAN Normal Mode with SWK	1	1	1

When reading back CAN_x the programmed mode is shown in SBC Normal Mode. To read the real CAN mode the bits **SYSERR**, **SWK_SET** and **CAN** have to be evaluated. A change out of SBC Normal Mode can change the CAN_0 and CAN_1 bits.

5.4.4.2 SBC Stop Mode with SWK

In SBC Stop Mode the CAN Transceiver can be operated with the following CAN Modes

- CAN OFF
- CAN WK Mode (no SWK)
- CAN SWK Mode
- CAN Receive Only (no SWK)
- CAN Receive Only with SWK
- CAN Normal Mode (no SWK)
- CAN Normal Mode with SWK

To enable CAN SWK Mode the CAN has to be switched to "CAN Normal Mode with SWK", "CAN Receive Only Mode with SWK" or to "CAN SWK Mode" in SBC Normal Mode before sending the SBC to SBC Stop Mode. The bit SYSERR = '0' indicates that the SWK function is enabled. The table shows the change of CAN Mode when switching from SBC Normal Mode to SBC Stop Mode.

Note: CAN Receive Only Mode in SBC Stop Mode is implemented to also enable pretended networking (Partial networking done in the microcontroller).

Table 10 CAN Modes change when switching from SBC Normal Mode to SBC Stop Mode

Programmed CAN Mode in SBC Normal Mode	CAN_x bits	SYSERR bit	CAN Mode in SBC Stop Mode	CAN_x bits
CAN OFF	000	0	CAN OFF	000
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001
CAN Receive Only (no SWK)	010	0	CAN Receive Only (no SWK)	010
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	011
CAN OFF	100	0	CAN OFF	100
CAN SWK Mode	101	0	CAN SWK Mode	101
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101
CAN Receive Only with SWK	110	0	CAN Receive Only with SWK	110
CAN Receive Only with SWK	110	1	CAN Receive Only (no SWK)	110
CAN Normal Mode with SWK	111	0	CAN Normal Mode with SWK	111
CAN Normal Mode with SWK	111	1	CAN Normal Mode (no SWK)	111

Note: When SYSERR is set then WUF frames will not be detected, i.e. the selective wake function is not activated (no SWK), but the MSB of CAN mode is not changed in the register.

5.4.4.3 SBC Sleep Mode with SWK

In SBC Sleep Mode the CAN Transceiver can be switched into the following CAN Modes

- CAN OFF
- CAN WK Mode (without SWK)
- CAN SWK Mode

To enable “CAN SWK Mode” the CAN has to be switched to “CAN Normal Mode with SWK”, “CAN Receive Only Mode with SWK” or to “CAN SWK Mode” in SBC Normal Mode before sending the device to SBC Sleep Mode. The table shows the change of CAN mode when switching from SBC Normal Mode to Sleep Mode.

A wake from Sleep Mode with Selective Wake (Valid WUF) leads to Restart Mode. In Restart Mode the CFG_VAL bit will be cleared by the SBC, the SYSERR bit is not set. In the register CAN_x the programmed CAN SWK Mode (101) can be read.

To enable the CAN SWK Mode again and to enter SBC Sleep Mode the following sequence can be used; Program a CAN Mode different from CAN SWK Mode (101, 110, 111), set the CFG_VAL, CLEAR SYSERR bit, Set CAN_x bits to CAN SWK Mode (101), switch SBC to Sleep Mode.

To enable the CAN WK Mode or CAN SWK Mode again after a wake on CAN a rearming is required for the CAN transceiver to be wake capable again. The rearming is done by programming the CAN into a different mode with the CAN_x bit and back into the CAN WK Mode or CAN SWK Mode. To avoid lock-up when switching the SBC into Sleep Mode with an already woken CAN transceiver, the SBC does an automatic rearming of the CAN transceiver when switching into Sleep Mode. So after switching into Sleep Mode the CAN transceiver is either in CAN SWK Mode or CAN WK Mode depending on CAN_x setting and SYSERR bit (If CAN is switched to OFF Mode it is also OFF in Sleep Mode)

Table 11 CAN Modes change when switching to SBC Sleep Mode

Programmed CAN Mode in SBC Normal Mode	CAN_x bits	SYSERR bit	CAN Mode in SBC Sleep Mode	CAN_x bits
CAN OFF	000	0	CAN OFF	000
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001
CAN Receive Only (no SWK)	010	0	CAN WK Mode (no SWK)	001
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	001
CAN OFF	100	0	CAN OFF	100
CAN SWK Mode	101	0	CAN SWK Mode	101
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101
CAN Receive Only with SWK	110	0	CAN SWK Mode	101
CAN Receive Only with SWK	110	1	CAN WK Mode (no SWK)	101
CAN Normal Mode with SWK	111	0	CAN SWK Mode	101
CAN Normal Mode with SWK	111	1	CAN WK Mode (no SWK)	101

5.4.4.4 SBC Restart Mode with SWK

If SBC Restart Mode is entered the transceiver can change the CAN mode. During Restart or after Restart the following modes are possible

- CAN OFF
- CAN WK Mode (either still wake cable or already woken up)
- CAN SWK Mode (WUF Wake from Sleep)

Table 12 CAN Modes change in case of Restart out of SBC Normal Mode

Programmed CAN Mode in SBC Normal Mode	CAN_x bits	SYSERR bit	CAN Mode in and after SBC Restart Mode	CAN_x bits	SYSERR bit
CAN OFF	000	0	CAN OFF	000	0
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001	0
CAN Receive Only (no SWK)	010	0	CAN WK Mode (no SWK)	001	0
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	001	0
CAN OFF	100	0	CAN OFF	100	0
CAN SWK Mode	101	0	CAN WK Mode (no SWK)	101	1
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101	1
CAN Receive Only with SWK	110	0	CAN WK Mode (no SWK)	101	1
CAN Receive Only with SWK	110	1	CAN WK Mode (no SWK)	101	1
CAN Normal Mode with SWK	111	0	CAN WK Mode (no SWK)	101	1
CAN Normal Mode with SWK	111	1	CAN WK Mode (no SWK)	101	1

The various reasons for entering SBC Restart Mode and the respective status flag settings are shown in **Table 13**.

Table 13 CAN Modes change in case of Restart out of SBC Sleep Mode

CAN Mode in SBC Sleep Mode	CAN Mode in and after SBC Restart Mode	CAN_x	SYS ERR	CAN_WU	WUP	WUF	ECNT_x	Reason for Restart
CAN OFF	CAN OFF	000	0	0	0	0	0	Wake on other wake source
CAN WK Mode	CAN woken up	001	0	1	1	0	0	Wake (WUP) on CAN
CAN WK Mode	CAN WK Mode	001	0	0	0	0	0	Wake on other wake source
CAN SWK Mode	CAN woken up	101	0	1	0/1[1)]	1	x	Wake (WUF) on CAN
CAN SWK Mode,	CAN woken up	101	1	1	0/1[2)]	0	100000	Wake due to error counter overflow
CAN SWK selected, CAN WK active	CAN woken up.	101	1	1	1	0	0	Wake (WUP) on CAN, config check was not pass
CAN SWK Mode	CAN WK Mode	101	1	0	0/1	0	x	Wake on other wake source

1) In case there is a WUF detection within $t_{SILENCE}$ then the WUP bit will not be set. Otherwise it will always be set together with the WUF bit.

2) In some cases the WUP bit might stay cleared even after $t_{SILENCE}$, e.g. when the error counter expires without detecting a wake up pattern

5.4.4.5 SBC Fail-Safe Mode with SWK

When SBC Fail-Safe Mode is entered the CAN transceiver is automatically set into WK Mode (wake capable) without the selective wake function.

5.4.5 Wake-up

A wake-up via CAN leads to a restart out of SBC Sleep Mode and to an interrupt in SBC Normal Mode, and in SBC Stop Mode. After the wake event the bit CAN_WU is set, and the details about the wake can be read out of the bits WUP, WUF, SYSERR, and ECNT.

5.4.6 Configuration for SWK

The CAN protocol handler settings can be configured in following registers:

- **SWK_BTL1_CTRL** defines the number of time quanta in a bit time. This number depends also on the internal clock settings performed in the register **SWK_CDR_CTRL2**;
- **SWK_BTL2_CTRL** defines the sampling point position;
- The respective receiver during frame detection mode can be selected via the bit **RX_WK_ SEL**;
- The clock and data recovery (see also **Chapter 5.4.8**) can be configured in the registers **SWK_CDR_CTRL1**, **SWK_CDR_CTRL2**, **SWK_CDR_LIMIT_HIGH_CTRL** and **SWK_CDR_LIMIT_LOW_CTRL**;

The actual configuration for selective wake is done via the Selective Wake Control Registers SWK_IDx_CTRL, SWK_MASK_IDx_CTRL, SWK_DLC_CTRL, SWK_DATAx_CTRL.

The oscillator has the option to be trimmed by the microcontroller. To measure the oscillator, the SPI bit OSC_CAL needs to be set to 1 and a defined pulse needs to be given to the TXDCAN pin by the microcontroller (e.g. 1µs pulse, CAN needs to be switched off before). The SBC measures the length of the pulse by counting the time with the integrated oscillator. The counter value can be read out of the register SWK_OSC_CAL_H_STATE and SWK_OSC_CAL_L_STATE. To change the oscillator the trimming function needs to be enabled by setting the bits TRIM_EN_x = 11 (and OSC_CAL = 1). The oscillator can then be adjusted by writing into the registers **SWK_OSC_TRIM_CTRL** and **SWK_OPT_CTRL**. To finish the trimming, the bits TRIM_EN_x need to be set back to “00”.

5.4.7 CAN Flexible Data Rate (CAN FD) Tolerant Mode

The CAN FD tolerant mode can be activated by setting the bit **CAN_FD_ EN** = '1' in the register **SWK_CAN_FD_CTRL**. With this mode the internal CAN frame decoding will be stopped for CAN FD frame formats:

- The high baudrate part of a CAN FD frame will be ignored,
- No Error Handling (Bit Stuffing, CRC checking, Form Errors) will be applied to remaining CAN frame fields (Data Field, CRC Field, …),
- No wake up is done on CAN FD frames.

The internal CAN frame decoder will be ready for new CAN frame reception when the End of frame (EOF) of a CAN FD frame is detected.The identification for a CAN FD frame is based on the EDL Bit, which is sent in the Control Field of a CAN FD frame:

- EDL Bit = 1 identifies the current frame as an CAN FD frame and will stop further decoding on it.
- EDL Bit = 0 identifies the current frame as CAN 2.0 frame and processing of the frame will be continued

.

In this way it is possible to send mixed CAN frame formats without affecting the selective wake functionality by error counter increment and subsequent misleading wake up.In addition to the **CAN_FD_ EN** bit also a filter setting must be provided for the CAN FD tolerant mode. This filter setting defines the minimum dominant time for a CAN FD dominant bit which will be considered as a dominant bit from the CAN FD frame decoder. This value must be aligned with the selected high baudrate of the data field in the CAN network.

To support programming via CAN during CAN FD mode a dedicated SPI bit **DIS_ERR_ CNT** is available to avoid an overflow of the implemented error counter (see also **Chapter 5.4.2.4**).

The behavior of the error counter depends on the setting of the bits **DIS_ERR_ CNT** and **CAN_FD_ EN** and is show in below table:

Table 14 Error Counter Behavior

DIS_ERR_ CNT setting	**CAN_FD_ EN setting**	**Error Counter Behavior**
0	0	Error Counter counts up when a CAN FD frame or an incorrect/corrupted CAN frame is received; counts down when a CAN frame is received properly (as specified in ISO 11898-2:2016)
1	0	Error Counter counts up when a CAN FD frame or an incorrect/corrupted CAN frame is received; counts down when a CAN frame is received properly (as specified in ISO 11898-2:2016)
0	1	Error Counter counts down when correct CAN (incl. CAN FD) frame is received
1	1	Error Counter is and stays cleared to avoid an overflow during programming via CAN

The **DIS_ERR_ CNT** bit is automatically cleared at Tsilence ($t_{SILENCE}$) expiration.

5.4.8 Clock and Data Recovery

In order to compensate possible deviations on the CAN oscillator frequency caused by assembly and lifetime effects, the device features an integrated clock and data recovery (CDR).

It is recommended to always enable the CDR feature during SWK operation.

5.4.8.1 Configuring the Clock Data Recovery for SWK

The Clock and Data Recovery can be optionally enabled or disabled with the **CDR_EN** bit in the **SWK_CDR_CTRL1** SPI register. In case the feature is enabled, the CAN bit stream will be measured and the internal clock used for the CAN frame decoding will be updated accordingly.
Before the Clock and Data Recovery can be used it must be configured properly related to the used baud rate and filtering characteristics (see **Chapter 5.4.8.2**).

It is strongly recommended not to enable/disable the Clock Recovery during a active CAN Communication.

To ensure this, it is recommended to enable/disable it during CAN OFF (**BUS_CTRL_1**; CAN[2:0] = 000).

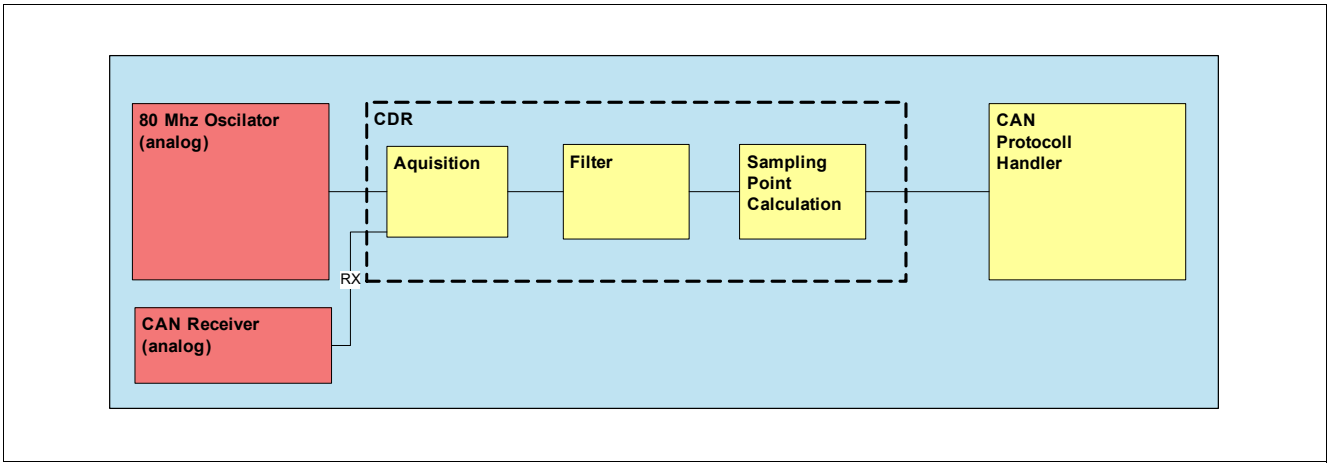

Figure 15 Clock and Data Recovery Block Diagram

5.4.8.2 Setup of Clock and Data Recovery

It is strongly recommended to enable the clock and data recovery feature only when the setup of the clock and data recovery is finished.

The following sequence should be followed for enabling the clock and data recovery feature:

- Step 1: Switch CAN to OFF and **CDR_EN** to OFF
  Write SPI Register **BUS_CTRL_1** (CAN[2:0] = 000).
- Step 2: Configure CDR Input clock frequency
  Write SPI Register **SWK_CDR_CTRL2** (SEL_OSC_CLK[1:0]).
- Step 3: Configure Bit timing Logic
  Write SPI Register **SWK_BTL1_CTRL** and adjust **SWK_CDR_LIMIT_HIGH_CTRL** and **SWK_CDR_LIMIT_LOW_CTRL** according to **Table 36**.
- Step 4: Enable Clock and Data Recovery
  Choose filter settings for Clock and Data recovery. Write SPI Register **SWK_CDR_CTRL1** with **CDR_EN** = 1

Additional hints for the CDR configuration and operation:

- Even if the CDR is disabled, when the baud rate is changed, the settings of **SEL_OSC_CLK** in the register **SWK_CDR_CTRL1** and **SWK_BTL1_CTRL** have to be updated accordingly,
- The **SWK_CDR_LIMIT_HIGH_CTRL** and **SWK_CDR_LIMIT_LOW_CTRL** registers have to be also updated when the baud rate or clock frequency is changed (the CDR is discarding all the acquisitions and looses all acquired information, if the limits are reached - the **SWK_BTL1_CTRL** value is reloaded as starting point for the next acquisitions)
- When updating the CDR registers, it is recommended to disable the CDR and to enable it again only after the new settings are updated,
- The **SWK_BTL2_CTRL** register represents the sampling point position. It is recommended to be used at default value: 11 0011 (~80%)

5.4.9 Electrical Characteristics

Table 15 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < VCAN < 5.25 V; RL = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN Partial Network Timing							
Timeout for bus inactivity	$t_{SILENCE}$	0.6	–	1.2	s	1)	P_5.4.1
Bias reaction time	t_{bias}	–	–	200	µs	1)Load R_L = 60 Ω, C_L = 100 pF, C_{GND} = 100 p	P_5.4.2
Wake-up reaction time (WUP or WUF)	$t_{WU_WUP/WUF}$	–	–	100	µs	1)2)3) Wake-up reaction time after a valid WUP or WUF;	P_5.4.3
Min. Bit Time	t_{Bit_min}	1	–	–	µs	1)4)	P_5.4.4
CAN FD Tolerance[5)]							
SOF acceptance	n_{Bits_idle}	6	–	10	bits	6)Number of recessive bits before a new SOF shall be accepted	P_5.4.5
Dominant signals which are ignored (up to 2MBit/s)	$t_{FD_Glitch_4}$	0	–	5	%	6)7)of arbitration bit time; to be configured via **FD_FILTER**;	P_5.4.6
Dominant signals which are ignored (up to 5MBit/s)	$t_{FD_Glitch_10}$	0	–	2.5	%	6)8)of arbitration bit time; to be configured via **FD_FILTER**;	P_5.4.7
Signals which are detected as a dominant data bit after the FDF bit and before EOF bit (up to 2MBit/s)	$t_{FD_DOM_4}$	17.5	–	–	%	6)7)of arbitration bit time; to be configured via **FD_FILTER**;	P_5.4.8
Signals which are detected as a dominant data bit after the FDF bit and before EOF bit (up to 5MBit/s)	$t_{FD_DOM_10}$	8.75	–	–	%	6)8)of arbitration bit time; to be configured via **FD_FILTER**;	P_5.4.9

1) Not subject to production test, tolerance defined by internal oscillator tolerance
2) Wake-up signalized via INT pin activation in SBC Stop Mode and via VCC1 ramping up with wake from SBC Sleep Mode.
3) WUP: time starts with end of last dominant phase of WUP; WUF: time starts with end of CRC delimiter of the WUF.
4) The minimum bit time corresponds to a maximum bit rate of 1 Mbit/s. The lower end of the bit rate depends on the protocol IC or the permanent dominant detection circuitry preventing a permanently dominant clamped bus.
5) Applies for an arbitration rate of up to 500kbps until the FDF bit is detected.
6) Not subject to production test; specified by design.
7) A data phase bit rate less or equal to four times of the arbitration bit rate or 2 Mbit/s, whichever is lower.
8) A data phase bit rate less or equal to ten times of the arbitration bit rate or 5 Mbit/s, whichever is lower.

6 Voltage Regulator 1

6.1 Block Description

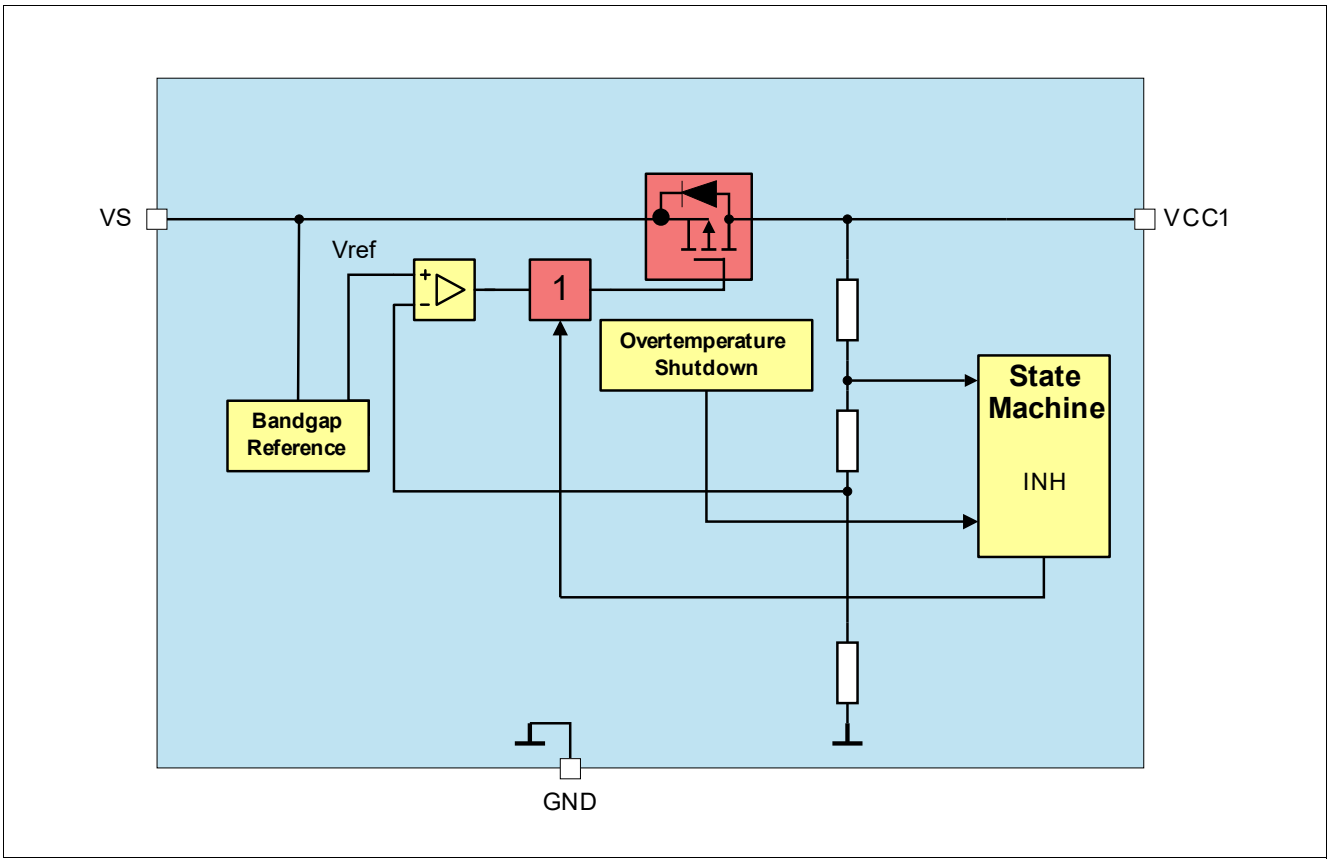

Figure 16 Module Block Diagram

Functional Features

- 5V low-drop voltage regulator
- Undervoltage monitoring with adjustable reset level, VCC1 prewarning and VCC1 short circuit detection ($V_{RT1/2/3/4}$, $V_{PW,f}$). Please refer to **Chapter 14.6** and **Chapter 14.7** for more information.
- Short circuit detection and switch off with undervoltage fail threshold, device enters SBC Fail-Safe Mode
- ≥470nF ceramic capacitor at voltage output for stability, with ESR < 1Ω @ f = 10 kHz, to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram).
- Output current capability up to $I_{VCC1,lim}$.

6.2 Functional Description

The Voltage Regulator 1 (=VCC1) is “ON” in SBC Normal and SBC Stop Mode and is disabled in SBC Sleep and in SBC Fail-Safe Mode. The regulator can provide an output current up to $I_{VCC1,lim}$.
For low-quiescent current reasons, the output voltage tolerance is decreased in SBC Stop Mode because only a low-power mode regulator with a lower accuracy ($V_{CC1,out41}$) will be active for small loads. If the load current on VCC1 exceeds the selected threshold ($I_{VCC1,Ipeak1,r}$ or $I_{VCC1,Ipeak2,r}$) then the high-power mode regulator will be also activated to support an optimum dynamic load behavior. The current consumption will then increase by typ. 2.9mA.
If the load current on VCC1 falls below the selected threshold ($I_{VCC1,Ipeak1,f}$ or $I_{VCC1,Ipeak2,f}$), then the low-quiescent current mode is resumed again by disabling the high-power mode regulator.
Both regulators (low-power mode and high-power mode) are active in SBC Normal Mode.

Two different active peak thresholds can be selected via SPI:

- **I_PEAK_TH** = ‘0’(default): the lower VCC1 active peak threshold 1 is selected with lowest quiescent current consumption in SBC Stop Mode (**$I_{Stop_1,25}$**, **$I_{Stop_1,85}$**);
- **I_PEAK_TH** = ‘1’: the higher VCC1 active peak threshold 2 is selected with an increased quiescent current consumption in SBC Stop Mode (**$I_{Stop_2,25}$**, **$I_{Stop_2,85}$**);

6.3 Electrical Characteristics

Table 16 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage including line and Load regulation	$V_{CC1,out1}$	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC1} < 250mA 6V < V_S < 28V	P_6.3.1
Output Voltage including line and Load regulation	$V_{CC1,out2}$	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC1} < 150mA	P_6.3.7
Output Voltage including line and Load regulation	$V_{CC1,out3}$	4.97	–	5.07	V	1)2)SBC Normal Mode; 20mA < I_{VCC1} < 90mA 8V < V_S < 18V 25°C < T_j < 125°C	P_6.3.12
Output Voltage including line and Load regulation	$V_{CC1,out41}$	4.9	5.05	5.2	V	SBC Stop Mode; 1mA < I_{VCC1} < $I_{VCC1,Ipeak}$	P_6.3.2
Output Voltage including line and Load regulation	$V_{CC1,out42}$	4.9	5.05	5.25	V	SBC Stop Mode; 10µA < I_{VCC1} < 1mA	P_6.3.20
Output Drop	$V_{CC1,d1}$	–	–	500	mV	I_{VCC1} = 50mA V_S=3V	P_6.3.3
Output Drop	$V_{CC1,d2}$	–	–	500	mV	I_{VCC1} = 150mA V_S=5V	P_6.3.4
VCC1 Active Peak Threshold 1 (Transition threshold between low-power and high-power mode regulator)	$I_{VCC1,Ipeak1,r}$	–	1.9	3.5	mA	2) I_{CC1} rising; V_S = 13.5V -40°C < T_j < 150°C; **I_PEAK_TH** = '0'	P_6.3.13
VCC1 Active Peak Threshold 1 (Transition threshold between high-power and low-power mode regulator)	$I_{VCC1,Ipeak1,f}$	0.5	1.3	–	mA	2) I_{CC1} falling; V_S = 13.5V -40°C < T_j < 150°C; **I_PEAK_TH** = '0'	P_6.3.17
VCC1 Active Peak Threshold 2 (Transition threshold between low-power and high-power mode regulator)	$I_{VCC1,Ipeak2,r}$	–	4.3	7.0	mA	2) I_{CC1} rising; V_S = 13.5V -40°C < T_j < 150°C; **I_PEAK_TH** = '1'	P_6.3.18
VCC1 Active Peak Threshold 2 (Transition threshold between high-power and low-power mode regulator)	$I_{VCC1,Ipeak2,f}$	1.7	3.4	–	mA	2) I_{CC1} falling; V_S = 13.5V -40°C < T_j < 150°C; **I_PEAK_TH** = '1'	P_6.3.19
Overcurrent Limitation	$I_{VCC1,lim}$	250	–	1200[2)]	mA	current flowing out of pin, V_{CC1} = 0V	P_6.3.6

1) In SBC Stop Mode, the specified output voltage tolerance applies when I_{VCC1} has exceeded the selected active peak threshold ($I_{VCC1,Ipeak1,r}$ or $I_{VCC1,Ipeak2,r}$) but with increased current consumption.

2) Not subject to production test, specified by design.

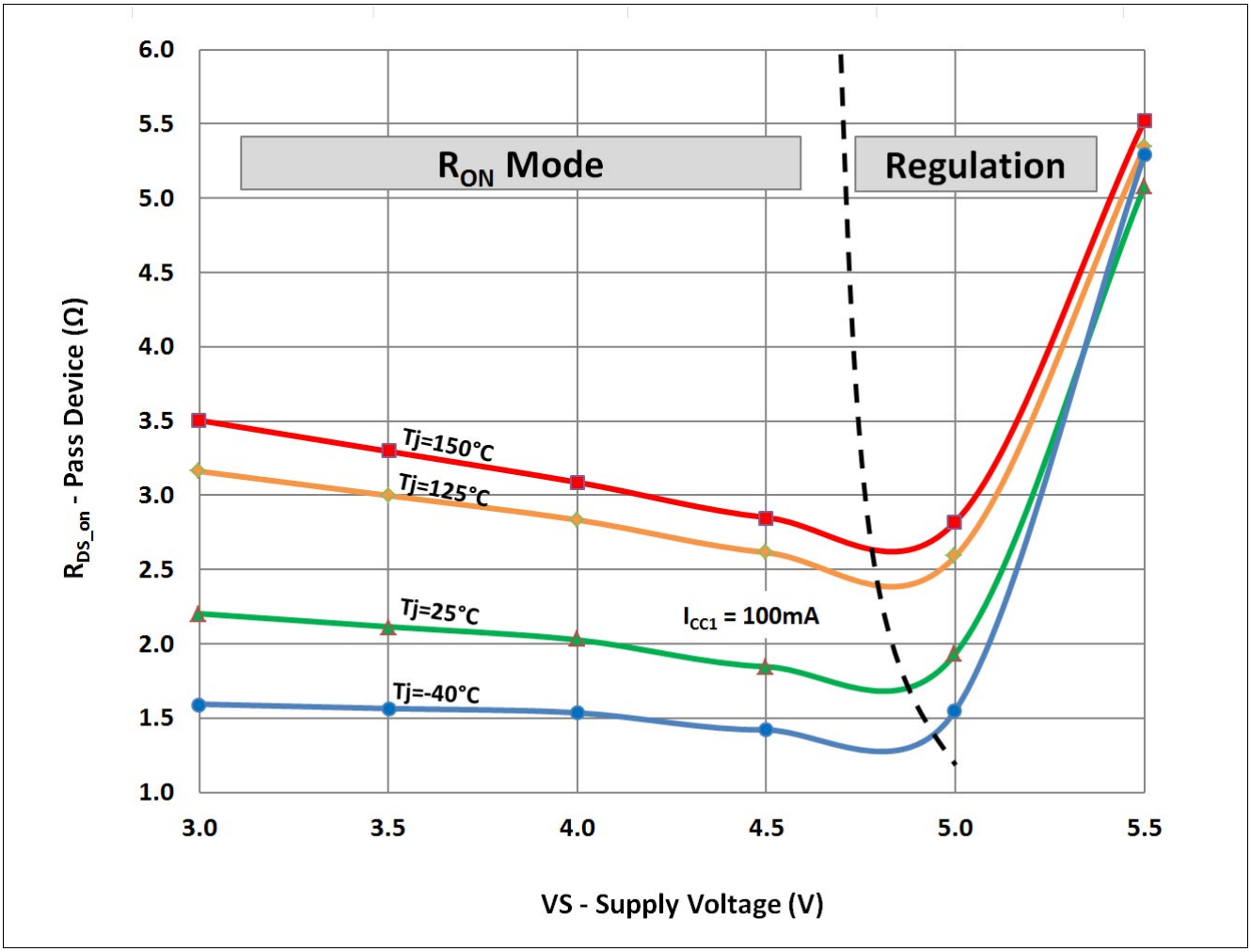

Figure 17 Typical on-resistance of VCC1 pass device during low drop operation for I_{CC1} = 100mA

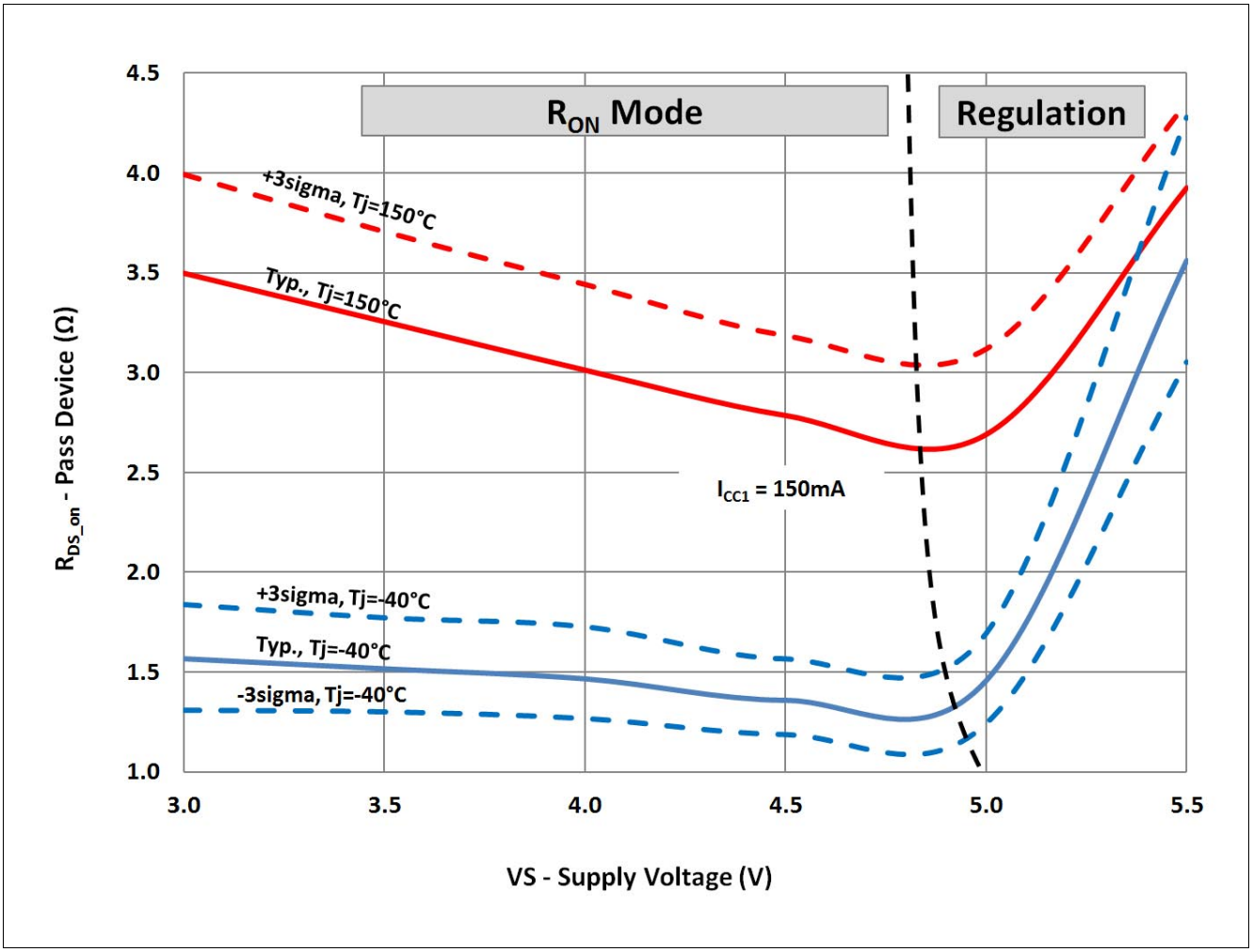

Figure 18 On-resistance range of VCC1 pass device during low drop operation for I_{CC1} = 150mA

7 Voltage Regulator 2

7.1 Block Description

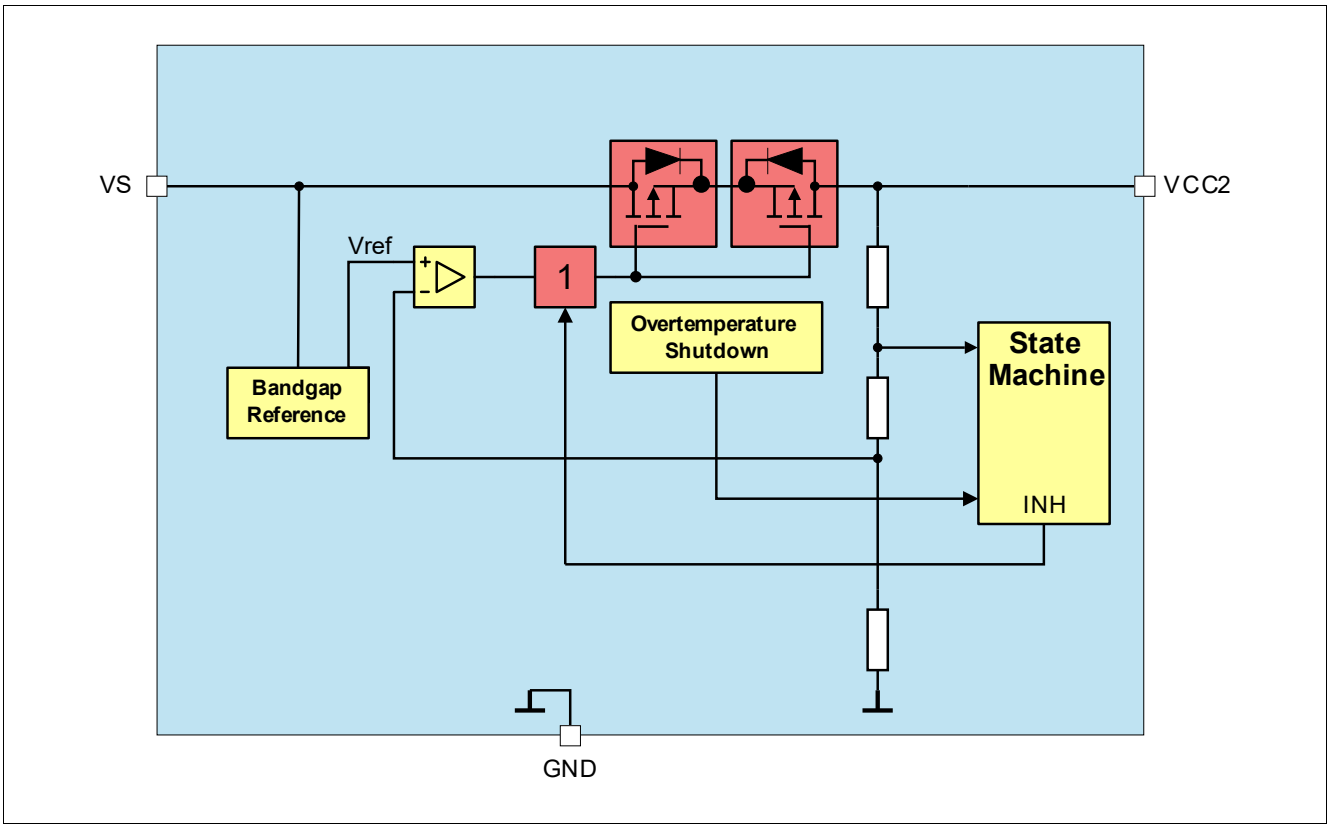

Figure 19 Module Block Diagram

Functional Features

- 5 V low-drop voltage regulator
- Protected against short to battery voltage, e.g. for off-board sensor supply
- Can also be used for CAN supply
- VCC2 undervoltage monitoring. Please refer to **Chapter 14.8** for more information
- Can be active in SBC Normal, SBC Stop, and SBC Sleep Mode (not SBC Fail-Safe Mode)
- VCC2 switch off after entering SBC Restart Mode. Switch off is latched, LDO must be enabled via SPI after shutdown.
- Overtemperature protection
- ≥ 470nF ceramic capacitor at output voltage for stability, with ESR < 1Ω @ f = 10 kHz, to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram).
- Output current capability up to $I_{VCC2,lim}$.

7.2 Functional Description

In SBC Normal Mode VCC2 can be switched on or off via SPI.

For SBC Stop- or Sleep Mode, the VCC2 has to be switched on or off before entering the respective SBC mode.

The regulator can provide an output current up to $I_{VCC2,lim}$.

For low-quiescent current reasons, the output voltage tolerance is decreased in SBC Stop Mode because only a low-power mode regulator with a lower accuracy ($V_{CC2,out5}$) will be active for small loads. If the load current on VCC2 exceeds $I_{VCC2} > I_{VCC2,Ipeak,r}$ then the high-power mode regulator will also be enabled to support an optimum dynamic load behavior. The current consumption will then increase by typ. 2.9mA.
If the load current on VCC2 falls below the threshold ($I_{VCC2} < I_{VCC2,Ipeak,f}$), then the low-quiescent current mode is resumed again by disabling the high-power mode regulator.
Both regulators are active in SBC Normal Mode.

Note: If the VCC2 output voltage is supplying external off-board loads, the application must consider the series resonance circuit built by cable inductance and decoupling capacitor at the load. Sufficient damping must be provided.

7.2.1 Short to Battery Protection

The output stage is protected for short to VBAT.

7.3 Electrical Characteristics

Table 17 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage including line and Load regulation (SBC Normal Mode)	$V_{CC2,out1}$	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC2} < 100mA 6.5V < V_S < 28V	P_7.3.1
Output Voltage including line and Load regulation (SBC Normal Mode)	$V_{CC2,out2}$	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC2} < 80mA 6V < V_S < 28V	P_7.3.16
Output Voltage including line and Load regulation (SBC Normal Mode)	$V_{CC2,out3}$	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC2} < 40mA	P_7.3.2
Output Voltage including line and Load regulation (SBC Normal Mode)	$V_{CC2,out4}$	4.97	–	5.07	V	2)SBC Normal Mode; 10µA < I_{VCC2} < 5mA 8V < V_S < 18V 25°C < T_j < 125°C	P_7.3.14
Output Voltage including line and Load regulation (SBC Stop/Sleep Mode)	$V_{CC2,out5}$	4.9	5.05	5.2	V	Stop, Sleep Mode; 1mA < I_{VCC2} < $I_{VCC2,Ipeak}$	P_7.3.3
Output Voltage including line and Load regulation (SBC Stop/Sleep Mode)	$V_{CC2,out6}$	4.9	5.05	5.25	V	Stop, Sleep Mode; 10µA < I_{VCC2} < 1mA	P_7.3.18
Output Drop	$V_{CC2,d1}$	–	–	500	mV	I_{VCC2} = 30mA V_S = 5V	P_7.3.4
VCC2 Active Peak Threshold (Transition threshold between low-power and high-power mode regulator)	$I_{VCC2,Ipeak,r}$	–	1.9	3.5	mA	2)I_{CC2} rising; V_S = 13.5V -40°C < T_j < 150°C	P_7.3.15
VCC2 Active Peak Threshold (Transition threshold between high-power and low-power mode regulator)	$I_{VCC2,Ipeak,f}$	0.5	1.3	–	mA	2)I_{CC2} falling; V_S = 13.5V -40°C < T_j < 150°C	P_7.3.17
Overcurrent limitation	$I_{VCC2,lim}$	100	–	750 2)	mA	current flowing out of pin, V_{CC2} = 0V	P_7.3.5

1) In SBC Stop Mode, the specified output voltage tolerance applies when I_{VCC2} has exceeded the selected active peak threshold ($I_{VCC2,Ipeak,r}$) but with increased current consumption.

2) Not subject to production test, specified by design.

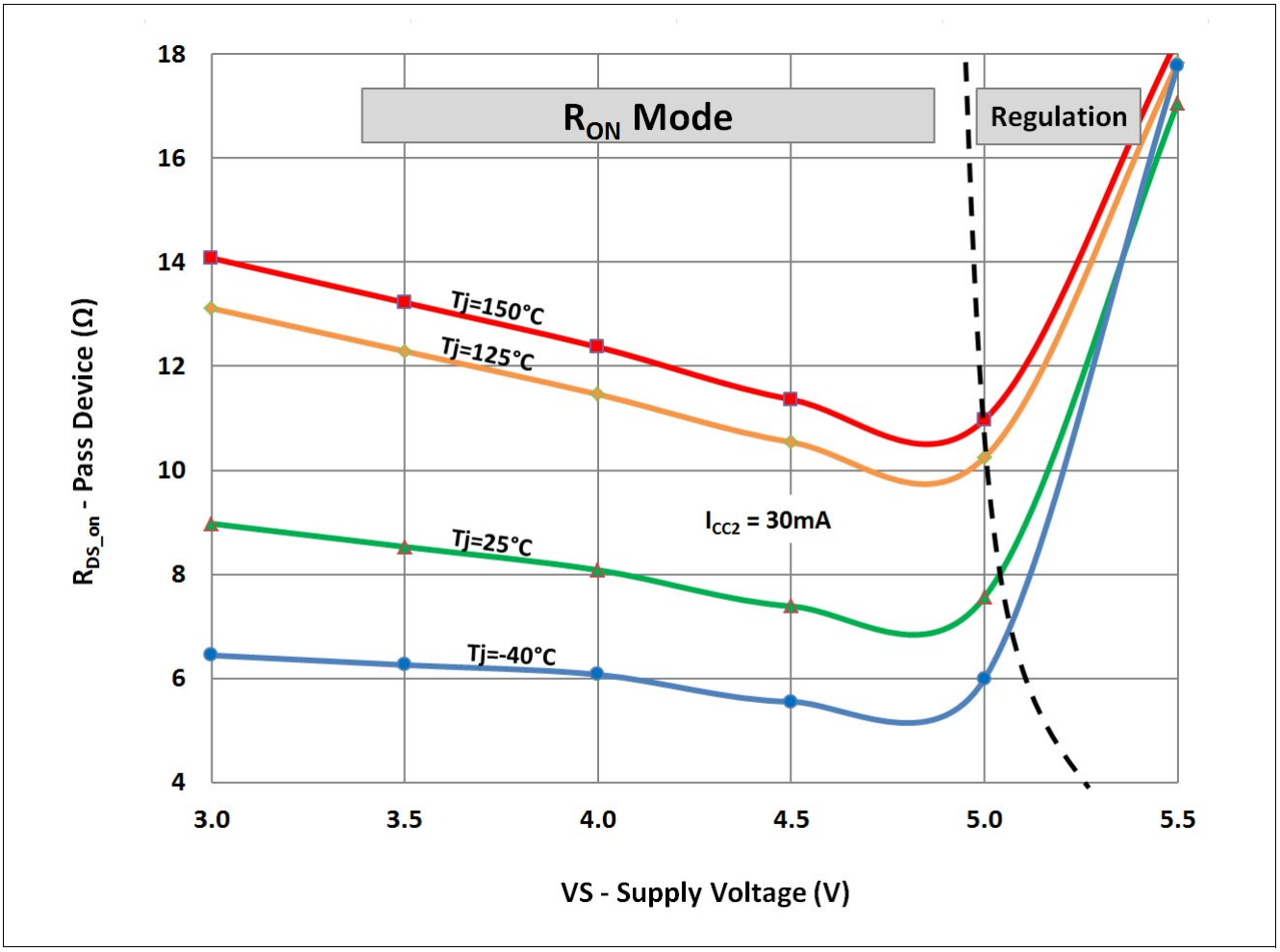

Figure 20 Typical on-resistance of VCC2 pass device during low drop operation for I_{CC2} = 30mA

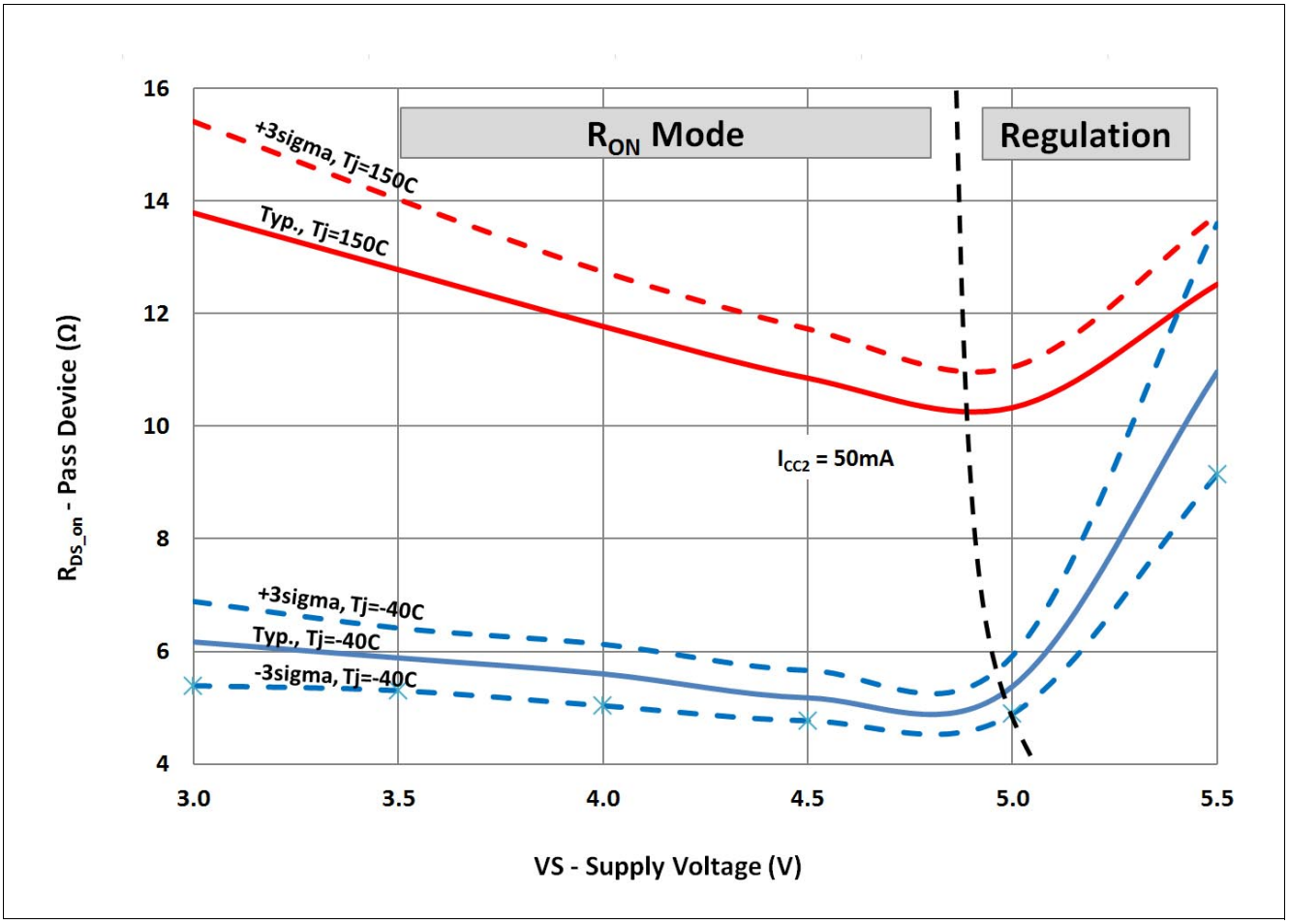

Figure 21 On-resistance range of VCC2 pass device during low drop operation for I_{CC2} = 50mA

8 External Voltage Regulator 3

8.1 Block Description

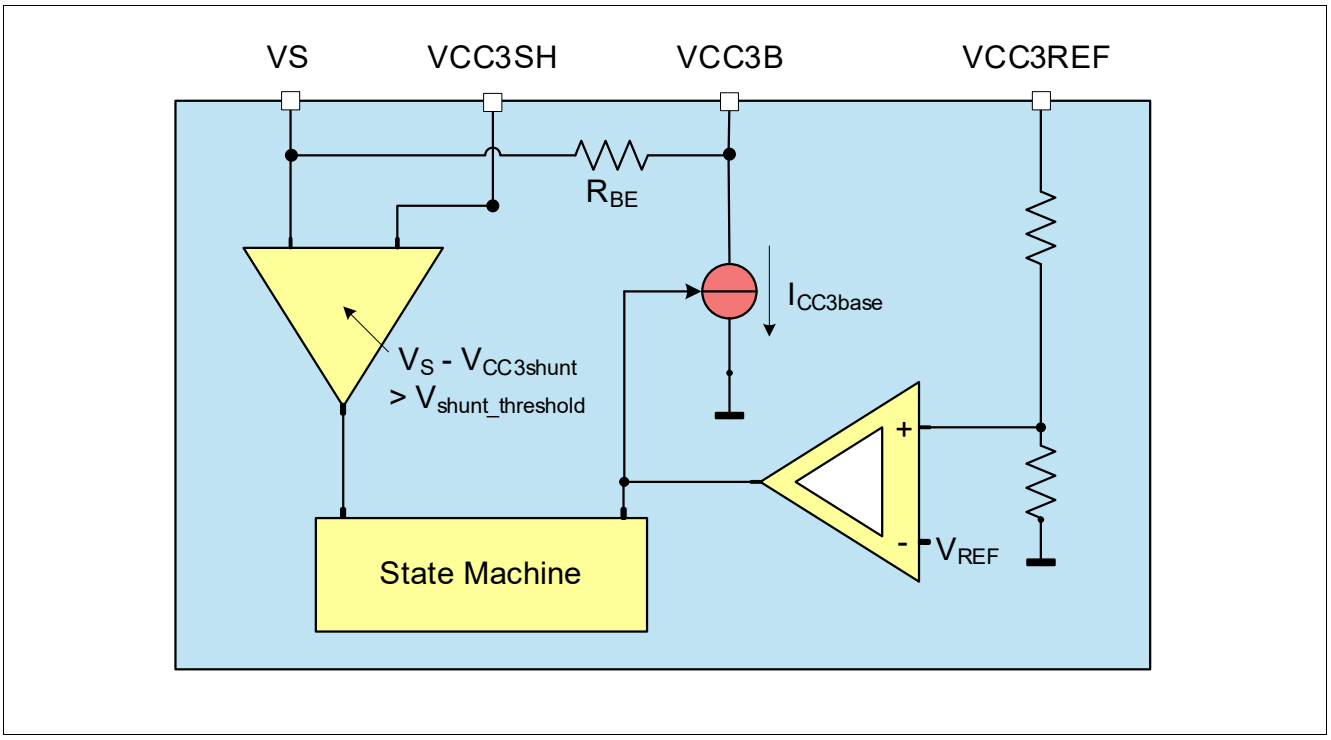

Figure 22 Functional Block Diagram

Functional Features

- Low-drop voltage regulator with external PNP transistor (up to 350mA with 470mΩ shunt resistor)
- Four high-voltage pins are used: VS, VCC3B, VCC3SH, VCC3REF
- Configurable as stand-alone regulator (5V or 3.3V output voltage selectable via SPI) or in load-sharing mode with VCC1 (5V output voltage)
- ≥ 4.7µF ceramic capacitor at output voltage for stability, with ESR < 150mΩ @ f = 10 kHz to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram).
- Overcurrent limitation with external shunt in stand-alone configuration
- Adjustable load current sharing ratio between VCC1 and VCC3 for load-sharing configuration
- Undervoltage shutdown in stand-alone configuration only

Table 18 [1)]External Voltage Regulator Configurations depending on VCC1 output voltage

VCC1 configuration	VCC3 voltage for VCC3_ V_CFG = 0	VCC3 voltage for VCC3_ V_CFG = 1
VCC1 = 5.0V	VCC3 = 5.0V	VCC3 = 3.3V

1) This settings are valid only for the VCC3 stand-alone configuration. The bit VCC3_ V_CFG is ignored for VCC3 load sharing configuration

8.2 Functional Description

The external voltage regulator can be used as an independent voltage regulator or in load-sharing mode with VCC1. Setting **VCC3_ON** in the **M_S_CTRL** register in SBC Normal Mode sets the stand-alone configuration of VCC3 as an independent voltage regulator. The load sharing configuration is set via the SPI bit **VCC3_LS** in the **HW_CTRL** register.

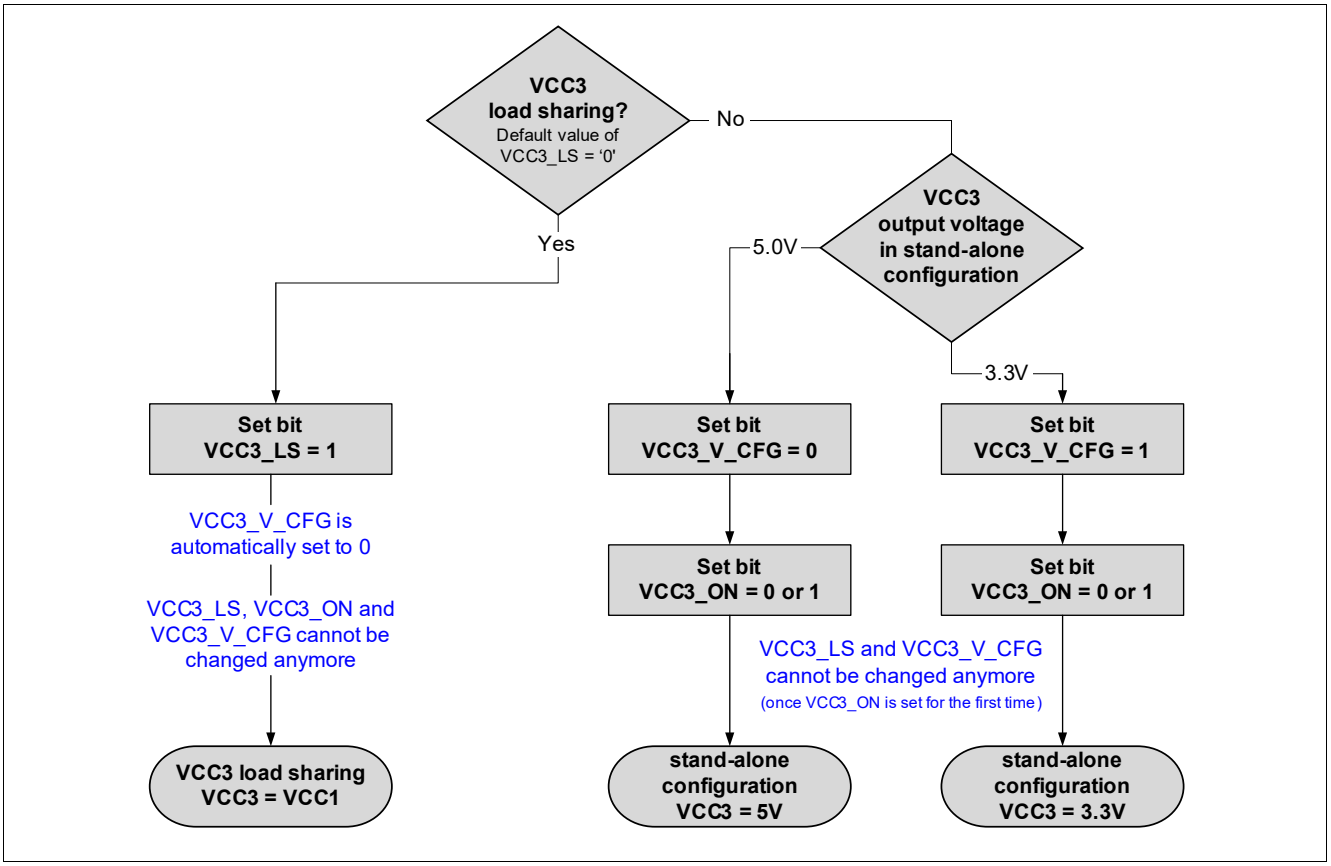

Figure 23 Selecting the Configuration of the VCC3 Regulator

Depending on the configuration the regulator will act in the respective SBC Mode as described in **Table 19**. After the VCC3 configuration has been selected, it cannot be changed anymore.

In stand-alone configuration the maximum current I_{CC3max} is defined by the current limitation determined by the used shunt. In load sharing configuration, the shunt is used to determine the current ratio between VCC1 and VCC3. Since the junction temperature of the external PNP transistor cannot be sensed by the SBC, it cannot be protected against overtemperature by the SBC. Therefore the thermal behavior has to be analyzed by the application.

For low-quiescent current reasons, the output voltage tolerance is decreased in SBC Stop Mode because a low-power mode regulator with a lower accuracy will be active for small loads. If the base current on VCC3 exceeds $I_{VCC3base} > I_{VCC3base,Ipeak,r}$ then the high-power mode regulator is enabled additionally to support an optimum dynamic load behavior. If the base current on VCC3 falls below the threshold ($I_{VCC3base} < I_{VCC3base,Ipeak,f}$), then the low-quiescent current consumption is resumed again by disabling the high-power mode regulator.
Only the high-power mode regulator is active in SBC Normal Mode.

The status of VCC3 is reported in the **SUP_STAT_2** SPI register. The regulator will switch OFF in case of VS dropping below **VS_UV** regardless of the VCC3 configuration and will be automatically enabled again when exceeding this threshold voltage unless the control bit **VCC3_VS_ UV_OFF** is set, i.e. in order to keep VCC3 enabled below **VS_UV** the bit **VCC3_VS_ UV_OFF** must be set. VCC3 will also stay active in SBC Stop Mode

when the bit **VCC3_LS_ STP_ON** is set and when load sharing is configured (for detailed protection features see **Chapter 14.7** and **Chapter 15.3**).

Table 19 External Voltage Regulator State by SBC Mode

SBC Mode	Load Sharing Mode[1)]	Independent Voltage Regulator
INIT Mode	OFF	OFF
Normal Mode	Configurable	Configurable
Stop Mode	OFF/Fixed[2)]	Fixed
Sleep Mode	OFF	Fixed
Restart Mode	ON or ramping	Fixed
Fail-Safe Mode	OFF	OFF

1) Behaves as VCC1 and has to be configured in SBC Normal Mode

2) Load Sharing operation in SBC Stop Mode is by default disabled for power saving reasons but **VCC3_LS** bit will stay set. However, it can be also configured via the SPI bit **VCC3_LS_ STP_ON** to stay enabled in SBC Stop Mode.

Note: The configuration of the VCC3 voltage regulator behavior must be done immediately after power-up of the device and cannot be changed afterwards as long as the device is supplied.

*Note: As soon as the bit **VCC3_ON** or **VCC3_LS** is set for the first time, the configuration for VCC3 cannot be changed anymore. This configuration is valid - also after a SBC Soft Reset - as long as the SBC is powered.*

*Note: If the VCC3 output voltage is supplying external off-board loads, the application must consider the series resonance circuit built by cable inductance and decoupling capacitor at the load. Sufficient damping must be provided (e.g. a 100Ohm resistor between the PNP collector and VCC3REF with 10uF capacitor on collector - see also **Figure 24**).*

8.2.1 External Voltage Regulator as Independent Voltage Regulator

Configured as an independent voltage regulator the SBC offers with VCC3 a third supply which could be used as off-board supply e.g. for sensors due to the integrated HV pins VCC3B, VCC3SH, VCC3REF.

This configuration is set and locked by enabling **VCC3_ON** while keeping **VCC3_LS** = 0. VCC3 can be switched ON or OFF but the configuration cannot be changed anymore. However, the **SPI_FAIL** is not set while trying to change the configuration.

An overcurrent limitation function is realized with the external shunt (see **Chapter 8.4** for calculating the desired shunt value) and the output current shunt voltage threshold ($V_{shunt_threshold}$). If this threshold is reached, then ICC3 is limited and only the current limitation bit **VCC3_OC** is set (no other reaction) and can be cleared via SPI once the overcurrent condition is not present anymore. If the overcurrent limitation feature is not needed, then connect the pins VCC3SH and VS together.
In this configuration VCC3 has the undervoltage signalization enabled and an undervoltage event is signaled with the bit **VCC3_UV** in the **SUP_STAT_2** SPI register.

Note: To avoid undesired current consumption increase of the device it must be ensured that VCC3 is not connected to VCC1 in this configuration.

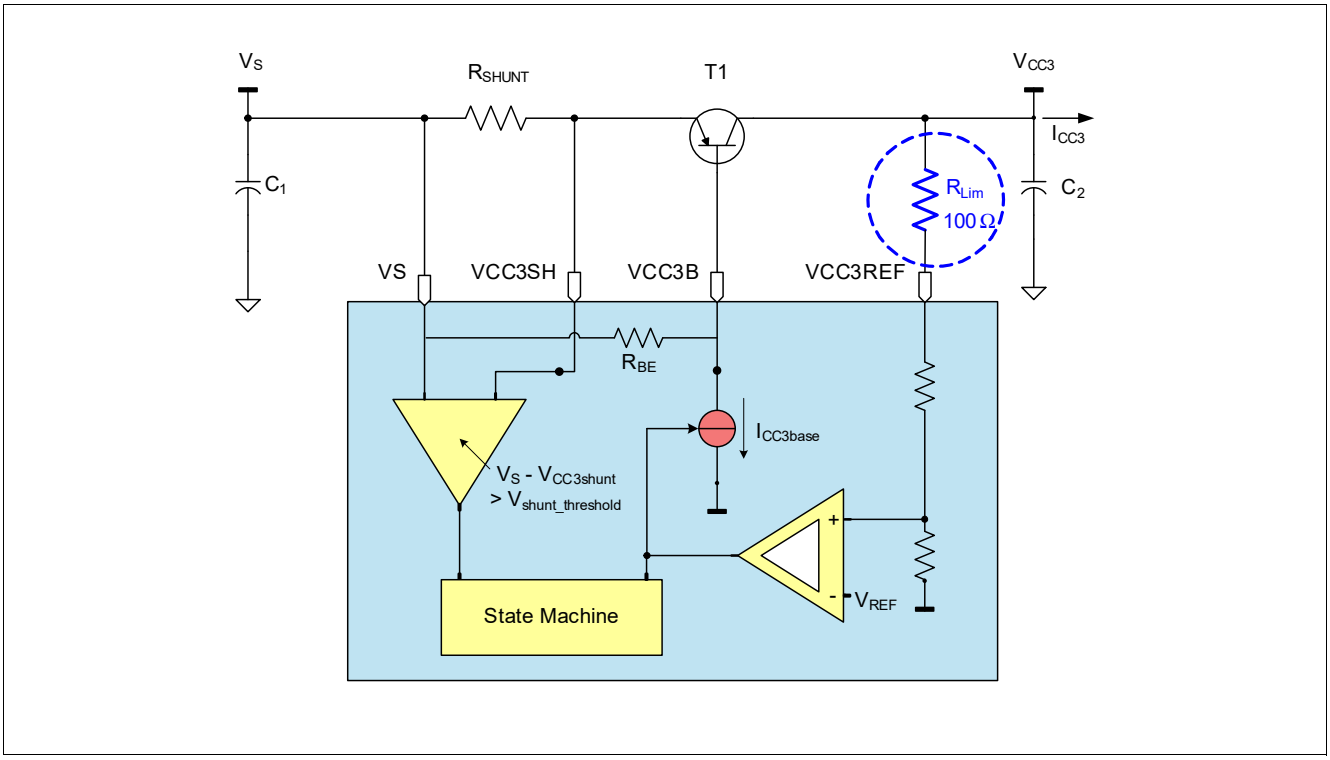

Figure 24 Protecting the VCC3 against inductive short circuits when configured as an independent voltage regulator for off-board supply

8.2.2 External Voltage Regulator in Load Sharing Mode

The purpose of the load sharing mode is to increase the total current capability of VCC1 without increase of the power dissipation within the SBC. The load current is shared between the VCC1 internal regulator and the external PNP transistor of VCC3. **Figure 25** shows the setup for Load Sharing. Load Sharing is active in SBC Normal Mode. It can also be configured via SPI to stay active in SBC Stop Mode.

An input voltage up to $V_{Sx,MAX}$ is regulated to $V_{CC3,nom}$ = 5.0 V with a precision of ±2% when used in the load sharing configuration in SBC Normal Mode.

This configuration is set and locked by enabling **VCC3_LS** for the first time while **VCC3_ON** has no function, i.e. keep **VCC3_ON** = 0. Trying to change the VCC3 configuration after **VCC3_LS** has been set will result in the **SPI_FAIL** bit being set and keeping the VCC3 configurations unchanged. Load sharing will be automatically disabled (only if **VCC3_LS_ STP_ON** = 0) during SBC Stop Mode due to power saving reasons but the bit will remain set to automatically switch back on after returning to SBC Normal Mode. It must be ensured that the same VCC3 output voltage level is selected as for VCC1.

In this configuration VCC3 has no undervoltage signalization. VCC3 shuts down if Fail-Safe Mode is reached, e.g. due to undervoltage shutdown ($V_{S,UV}$ monitoring).

VCC3 has no overcurrent limitation in this configuration and the shunt resistor is defining the load sharing ratio between the VCC1 and VCC3 load currents (see **Equation (8.2)** in **Chapter 8.4**). Thus, no overcurrent condition **VCC3_OC** will be signaled in this configuration.

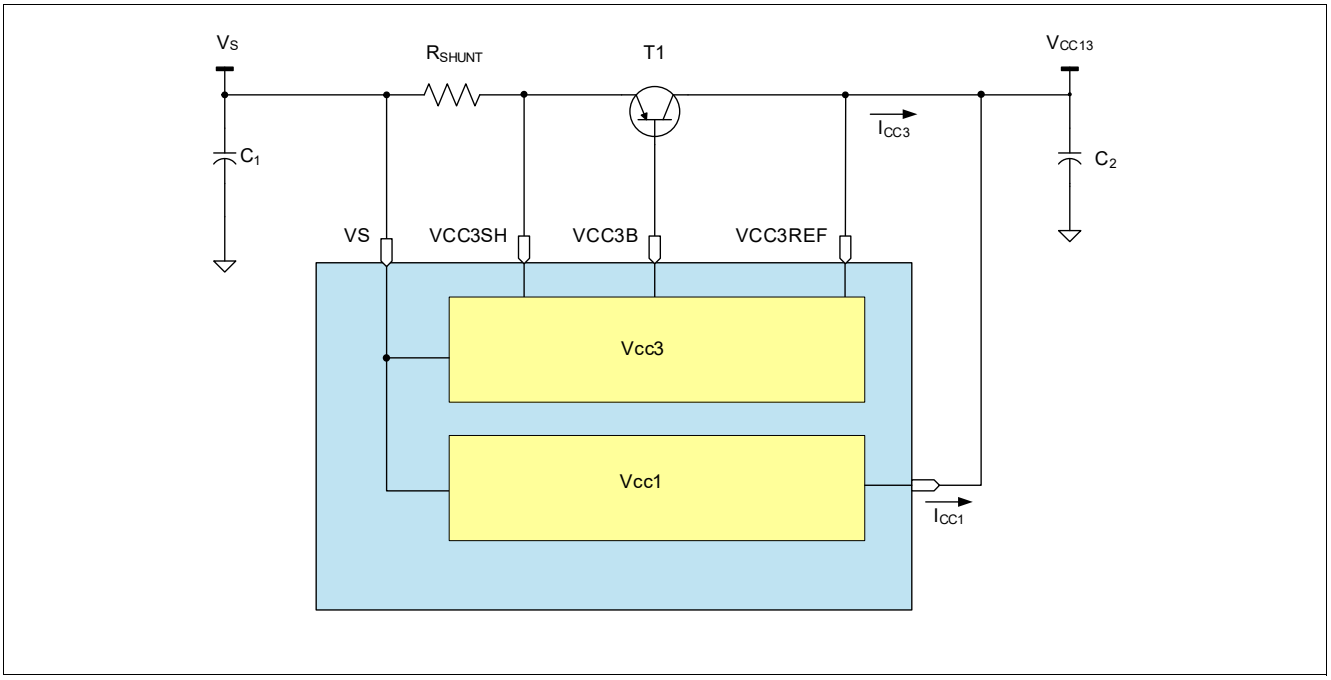

Figure 25 VCC3 in Load Sharing Configuration

8.3 External Components

Characterization is performed with the BCP52-16 from Infineon (I_{CC3} < 200 mA) and with MJD253. Other PNP transistors can be used. However, the functionality must be checked in the application.

Figure 25 shows one hardware set up used.

Table 20 Bill of Materials for the V_{CC3} Function with and without load sharing configuration

Device	Vendor	Reference / Value
C2	Murata	10 µF/10 V GCM31CR71A106K64L
RSHUNT	-	1 Ω (with / without LS)
T1	Infineon	BCP52-16

Note: The SBC is not able to ensure a thermal protection of the external PNP transistor. The power handling capabilities for the application must therefore be chosen according to the selected PNP device, the PCB layout and properties of the application to prevent thermal damage, e.g. via the shunt current limitation in stand alone configuration or by selecting the proper ICC1/ICC3 ratio in load-sharing configuration.

*Note: To ensure an optimum EMC behavior of the VCC3 regulator when the VCC3 output is leaving the PCB, it is necessary to optimize the PCB layout to have the PNP very close to the SBC. If this is not sufficient or possible, an external capacitance should be placed to the off-board connector (see also **Chapter 16.1**).*

8.4 Calculation of R_{SHUNT}

As a independent regulator, the maximum current I_{CC3max} where the limit starts and the bit $I_{CC3} > I_{CC3max}$ is set is determined by the shunt resistor R_{SHUNT} and the Output Current Shunt Voltage Threshold $V_{shunt_threshold}$.

The resistor can be calculated as following:

$$R_{SHUNT} = \frac{U_{shunt_threshold}}{I_{CC3\,max}} \tag{8.1}$$

If VCC3 is configured for load sharing, then the shunt resistor determines the load sharing ratio between VCC1 and VCC3. The ratio can be calculated as following:

$$\frac{I_{CC\ 3}}{I_{CC\ 1}} = \frac{110\ \ \Omega\ /105\ \ -\ 15\ \ mV\ \ /I_{CC\ 1}}{R_{SHUNT}} \qquad (a) \tag{8.2}$$

$$I_{CC\ 3} = \frac{I_{CC\ 1} \cdot 110\ \ \Omega\ /105\ \ -\ 15\ \ mV}{R_{SHUNT}} \qquad (b)$$

Example: A shunt resistor with 470mΩ and a load current of 100mA out of VCC1 would result in I_{CC3} = 191mA.

8.5 Unused Pins

In case the VCC3 is not used in the application, it is recommended to connect the unused pins of VCC3 as followed:

- Connect VCC3SH to VS or leave open;
- Leave VCC3B open;
- Leave VCC3REF open
- Do not enable the VCC3 via SPI as this leads to increased current consumption

8.6 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all outputs open; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Table 21 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Parameters independent from Test Set-up							
External Regulator Control Drive Current Capability	$I_{VCC3base}$	40	60	80	mA	$V_{VCC3base}$ = 13.5 V	P_8.6.1
Input Current V_{CC3ref}	$I_{VCC3ref}$	0	3	10	µA	$V_{VCC3ref}$ = 5 V	P_8.6.2
Input Current V_{CC3} Shunt Pin	$I_{VCC3shunt}$	0	3	10	µA	$V_{VCC3shunt}$ = V_S	P_8.6.3
Output Current Shunt Voltage Threshold	$V_{shunt_threshold}$	180	245	310	mV	1)	P_8.6.6
Current increase regulation reaction time	t_{rlinc}	–	–	5	µs	5) V_{CC3} = 5 V to 0 V; $I_{CC3base}$ = 20 mA **Figure 26**	P_8.6.7
Current decrease regulation reaction time	t_{rldec}	–	–	5	µs	5) V_{CC3} = 0 V to 5V; $I_{CC3base}$ = 20 mA **Figure 26**	P_8.6.8
Leakage current of VCC3base when VCC3 disabled	$I_{VCC3base_lk}$	–	–	5	µA	$V_{CC3base}$ = V_S; T_j = 25°C	P_8.6.9
Leakage current of $V_{CC3shunt}$ when VCC3 disabled	$I_{VCC3shunt_lk}$	–	–	5	µA	$V_{CC3shunt}$ = V_S; T_j = 25°C	P_8.6.11
Base to emitter resistor	R_{BE}	120	150	185	kΩ	V_{CC3} = OFF;	P_8.6.12
Active Peak Threshold VCC3 (Transition threshold between low-power and high-power mode regulator)	$I_{VCC3base,Ipeak,r}$	–	50	65	µA	5) Drive current $I_{VCC3base}$; $I_{VCC3base}$ rising V_S =13.5V; -40°C < T_j < 150°C	P_8.6.33
Active Peak Threshold VCC3 (Transition threshold between high-power and low-power mode regulator)	$I_{VCC3base,Ipeak,f}$	15	30	–	µA	5) Drive current $I_{VCC3base}$; $I_{VCC3base}$ falling V_S =13.5V; -40°C < T_j < 150°C	P_8.6.34
Parameters dependent on the Test Set-up (with external PNP device MJD-253)							
External Regulator Output Voltage (VCC3 = 5.0V)	$V_{CC3.out1}$	4.9	5	5.1	V	2) SBC Normal Mode; load sharing configuration with 470 mΩ shunt resistor; 10 µA < I_{VCC1} + I_{VCC3} < 300 mA;	P_8.6.13

Table 21 Electrical Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
External Regulator Output Voltage (VCC3 = 5.0V)	$V_{CC3,out2}$	4.9	5	5.1	V	[2]SBC Normal Mode; stand-alone configuration 10 mA < I_{VCC3} < 300 mA;	P_8.6.14
External Regulator Output Voltage (VCC3 = 5.0V)	$V_{CC3,out3}$	4.8	5	5.2[4]	V	[2]SBC Stop-, Sleep Mode; Stand-alone configuration 10µA < I_{VCC3} < $I_{VCC3_peak,r}$[3]	P_8.6.15
External Regulator Output Voltage (VCC3 = 3.3V)	$V_{CC3,out4}$	3.23	3.3V	3.37	V	[2]SBC Normal Mode; stand-alone configuration 10 mA < I_{VCC3} < 300 mA;	P_8.6.22
External Regulator Output Voltage (VCC3 = 3.3V)	$V_{CC3,out5}$	3.15	3.3V	3.45[4]	V	[2]SBC Stop-, Sleep Mode; Stand-alone configuration 10µA < I_{VCC3} < $I_{VCC3_peak,r}$[3]	P_8.6.23
Load Sharing Ratio ICC1 : ICC3	$Ratio_{LS_1,VCC3}$	1 : 1.35	1 : 1.9	1 : 2.45	–	[5][6]6.0V < V_S < 28V; SBC Normal Mode; LS ratio for a 470 mΩ shunt resistor and total load current of 300mA	P_8.6.16
Load Sharing Ratio ICC1 : ICC3	$Ratio_{LS_2,VCC3}$	1 : 0.67	1 : 0.95	1 : 1.23	–	[5][6]6.0V < V_S < 28V; SBC Normal Mode; LS ratio for a 1 Ω shunt resistor and total load current of 300mA	P_8.6.20
Load Sharing Ratio ICC1 : ICC3	$Ratio_{LS_3,VCC3}$	1 : 1.50	1 : 1.95	1 : 2.40	–	[5][6] T_j = 150°C; 8.0V < V_S < 18V; SBC Normal Mode; LS ratio for a 470 mΩ shunt resistor and total load current of 300mA	P_8.6.27
Load Sharing Ratio ICC1 : ICC3	$Ratio_{LS_4,VCC3}$	1 : 0.75	1 : 0.98	1 : 1.21	–	[5][6] T_j = 150°C; 8.0V < V_S < 18V; SBC Normal Mode; LS ratio for a 1 Ω shunt resistor and total load current of 300mA	P_8.6.28

1) Threshold at which the current limitation starts to operate. This threshold is only active when VCC3 is configured for stand-alone configuration.

2) Tolerance includes load regulation and line regulation.

3) I_{VCC3_peak} refers to the load current out of the collector of the external PNP device. This value can be calculated by multiplying the VCC3base active peak threshold ($I_{VCC3base,Ipeak}$) with the current gain of the PNP

4) At Tj > 125°C, the power transistor leakage could be increased, which has to be added to the quiescent current of the application independently if the regulator is turned on/off. To prevent an overvoltage condition at no load due to this increased leakage, an internal clamping structure will automatically turn on at typ. 200mV above the upper limit of the programmed output voltage.
5) Not subject to production test, specified by design.
6) a) Ratio will change depending on the chosen shunt resistor which value is correlating to the maximum power dissipation of the PNP pass device. See **Chapter 8.4** for the ratio calculation. The ratio will also change at low-drop operation.
For supply voltages of 5.5V < VS < 6V the accuracy applies only for a total load current of 250mA.
The load sharing ratio in SBC Stop Mode has +/-10% wider limits than specified.

   b) The output voltage precision in load sharing in SBC Stop Mode is according to VCC1 +/-4% or better for loads up to 20mA and +/-2% with loads greater than 20mA.
In SBC Normal the +/-2% precision for 5V/3.3V tolerance is valid regardless of the applied load.

Note: There is no thermal protection available for the external PNP transistor. Therefore, the application must be designed to avoid overheating of the PNP via the shunt current limitation in stand alone configuration and by selecting the proper ICC1/ICC3 ratio in load-sharing configuration.

Note: In SBC Stop Mode, the same output voltage tolerance applies as in SBC Normal Mode when I_{VCC3} has exceeded the selected active peak threshold ($I_{VCC3base,Ipeak}$) but with increased current consumption.

Timing diagram for regulator reaction time “current increase regulation reaction time” and “current decrease regulation reaction time”

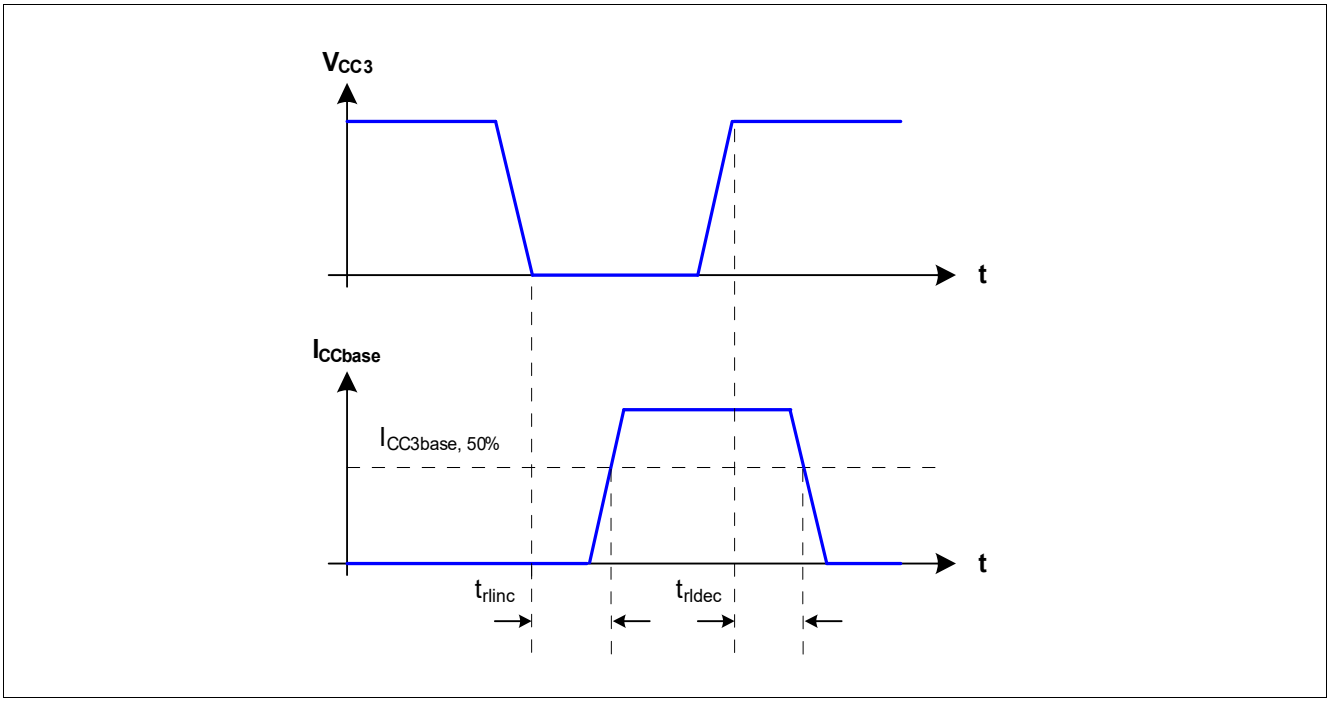

Figure 26 Regulator Reaction Time

Typical Load Sharing Characteristics using the BCP52-16 PNP transistor and a 1 Ω shunt resistor

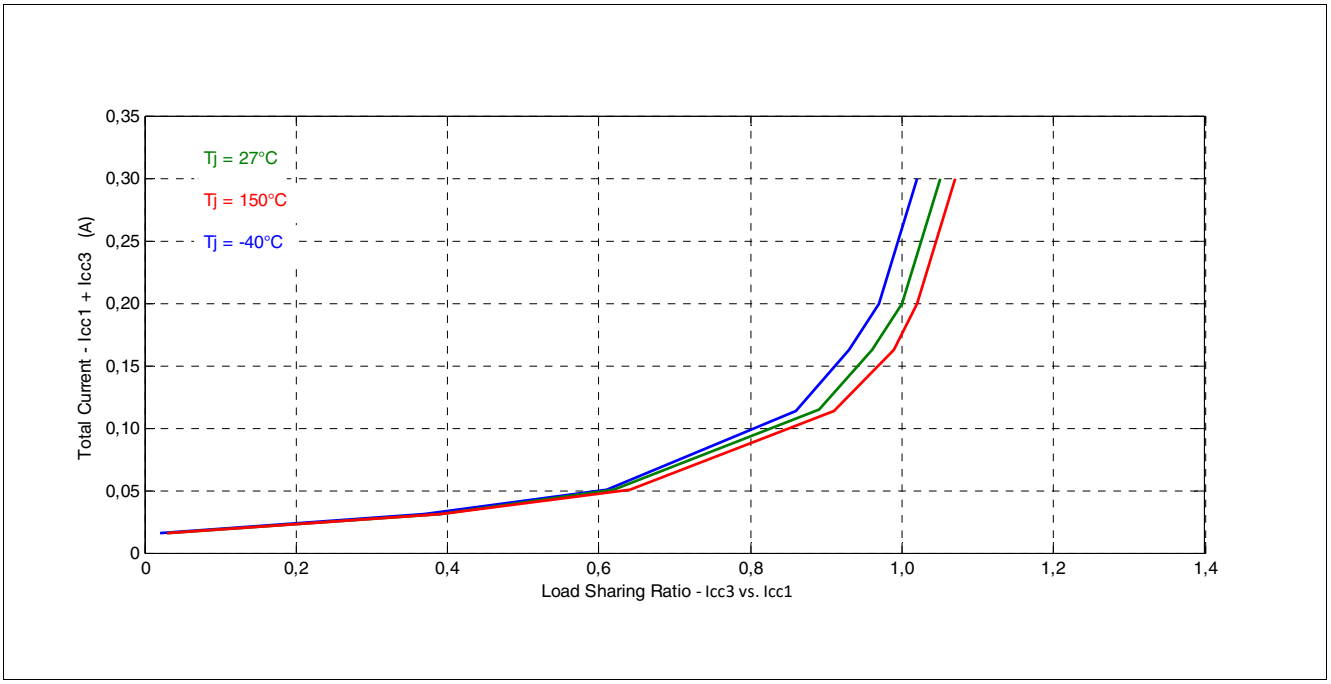

Figure 27 Load Sharing Ratio ICC1 : ICC3 vs. the total load current

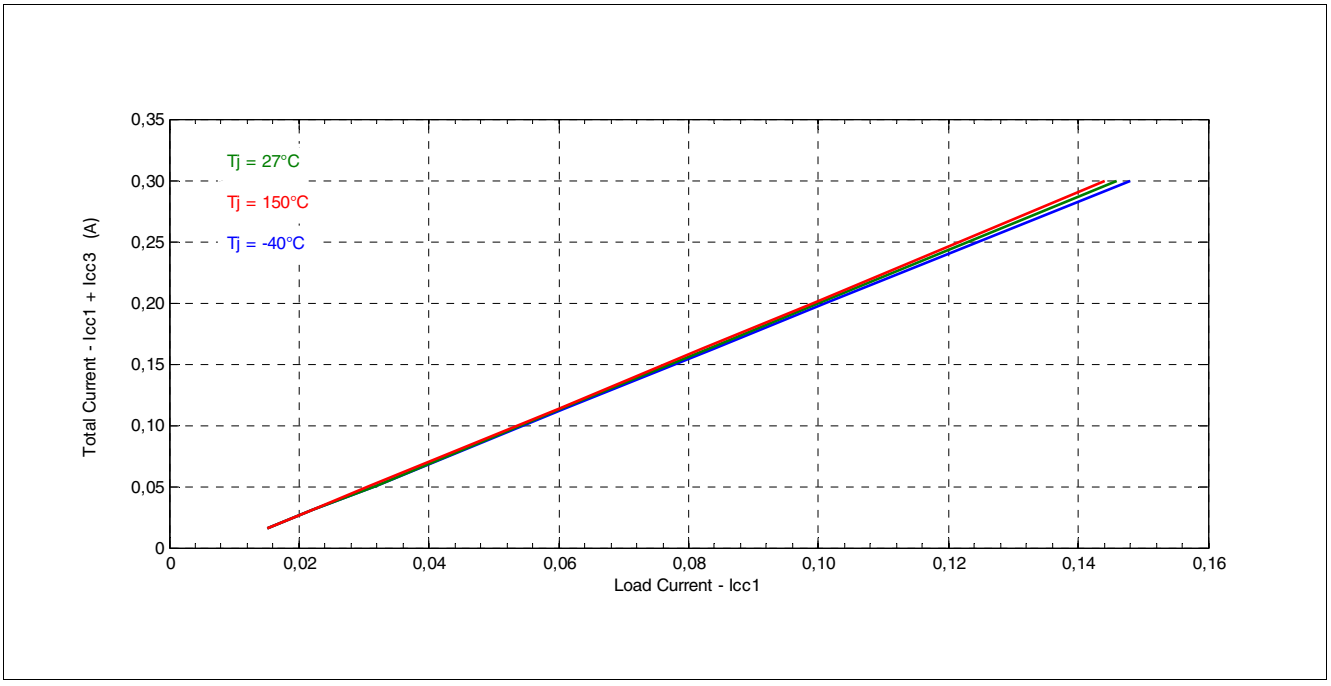

Figure 28 Load Sharing Behavior of ICC1 vs. the total load current

9 High-Side Switch

9.1 Block Description

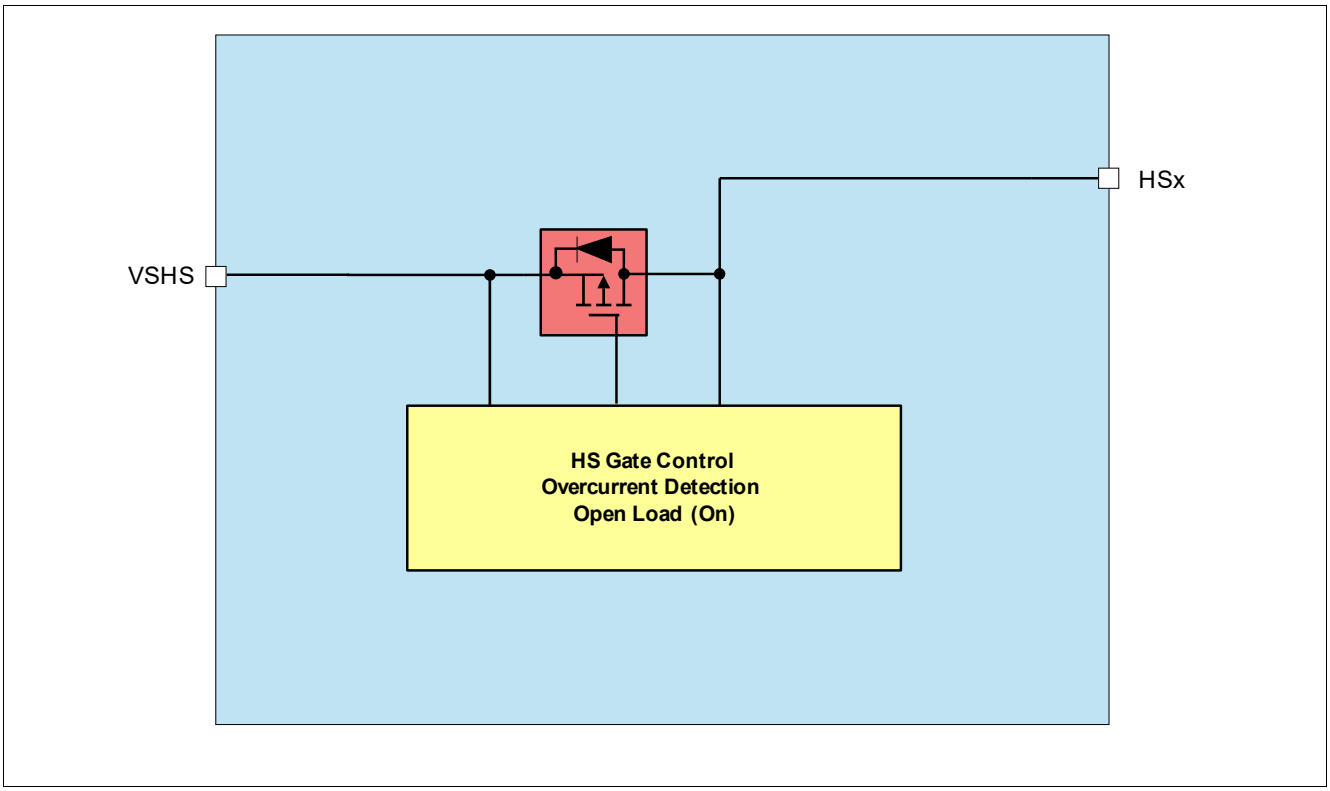

Figure 29 High-Side Module Block Diagram

Features

- Dedicated supply pin VSHS for high-side outputs
- Overvoltage and undervoltage switch off - configurable via SPI
- Overcurrent detection and switch off
- Open load detection in ON-state
- PWM capability with internal timer configurable via SPI
- Switch recovery after removal of OV or UV condition configurable via SPI

9.2 Functional Description

The High-Side switches can be used for control of LEDs, as supply for the wake inputs and for other loads. The High-Side outputs can be controlled either directly via SPI by (**HS_CTRL1**, **HS_CTRL2**), by the integrated timers or by the integrated PWM generators.

The high-side outputs are supplied by a dedicated supply pin VSHS (different to VS). The topology supports improved cranking condition behavior.

The configuration of the High-Side (Permanent On, PWM, cyclic sense, etc.) drivers must be done in SBC Normal Mode. The configuration is taken over in SBC Stop- or SBC Sleep Mode and cannot be modified. When entering SBC Restart Mode or SBC Fail-Safe Mode the HSx outputs are disabled.

9.2.1 Over- and Undervoltage Switch Off

All HS drivers in on-state are switched off in case of overvoltage on VSHS ($V_{SHS,OVD}$). If the voltage drops below the overvoltage threshold the HS drivers are activated again. The feature can be disabled by setting the SPI bit **HS_OV_SD_EN**.

The HS drivers are switched off in case of undervoltage on VSHS ($V_{SHS,UVD}$). If the voltage rises above the undervoltage threshold the HS drivers are activated again. The feature can be disabled by setting the SPI bit **HS_UV_SD_EN**.

So after release of undervoltage or overvoltage condition the HS switch goes back to programmed state in which it was configured via SPI. This behavior is only valid if the bit **HS_OV_UV_REC** is set to '1'. Otherwise the switches will stay off and the respective SPI control bits are cleared.

The overvoltage and undervoltage is signaled in the bits **VSHS_OV** and **VSHS_UV**, no other error bits are set.

9.2.2 Overcurrent Detection and Switch Off

If the load current exceeds the overcurrent shutdown threshold for a time longer then the overcurrent shutdown filter time the output is switched off.

The overcurrent condition and the switch off is signaled with the respective HSx_OC_OT bit in the register **HS_OC_OT_STAT**. The HSx configuration is then reset to 000 by the SBC. To activate the High-Side again the HSx configuration has to be set to ON (001) or be programmed to a timer function. It is recommended to clear the overcurrent bit before activation the High-Side switch, as the bits are not cleared automatically by the SBC.

9.2.3 Open Load Detection

Open load detection on the High-Side outputs is done during on state of the output. If the current in the activated output falls below then Open Load Detection current, the open load is detected and signaled via the respective bit HS1_OL, HS2_OL, HS3_OL, or HS4_OL in the register **HS_OL_STAT**. The High-Side output stays activated. If the open load condition disappears the Open Load bit in the SPI can be cleared. The bits are not cleared automatically by the SBC.

9.2.4 HSx Operation in Different SBC Modes

- During SBC Stop and SBC Sleep Mode the HSx outputs can be used for the cyclic sense feature. The open-load detection, overcurrent shut down as well as overvoltage and undervoltage shutdown are available. The overcurrent shutdown protection feature may influence the wake-up behavior[1)].
- the HSx output can also be enabled for SBC Stop and SBC Sleep Mode as well as controlled by the PWMx generator. The HSx outputs must be configured in SBC Normal Mode before entering a low-power mode.
- The HSx outputs are switched off during SBC Restart or SBC Fail-Safe Mode. They can be enabled via SPI if the failure condition is removed.

1) For the wake feature, the forced overcurrent shut down case must be considered in the user software for all SBC Modes, i.e. due to disabled HSx switches a level change might not be detected anymore at WKx pins.

9.2.5 PWM and Timer Function

Two 8-bit PWM generators are dedicated to generate a PWM signal on the HS outputs, e.g. for brightness adjustment or compensation of supply voltage fluctuation. The PWM generators are mapped to the dedicated HS outputs, and the duty cycle can be independently configured with a 8bit resolution via SPI (**PWM1_CTRL**, **PWM2_CTRL**). Two different frequencies (200Hz, 400Hz) can be selected independently for every PWM generator in the register **PWM_FREQ_CTRL**.

PWM Assignment and Configuration:

- Configure duty cycle and frequency for respective PWM generator in **PWM1_CTRL**/**PWM2_CTRL** and **PWM_FREQ_CTRL**
- Assign PWM generator to respective HS switch(es) in HSx_CTRL
- The PWM generation will start right after the HSx is assigned to the PWM generator (**HS_CTRL1**, **HS_CTRL2**)

Assignment options of HS1... HS4

- Timer 1
- Timer 2
- PWM 1
- PWM 2

Minimum On-time during PWM Operation

The min. on-time during PWM is limited by the actual on- and off-time of the respective HS switch, e.g. the PWM setting ‘0000 0001’ could not be realized.

Reliable Open-Load Detection during PWM Operation

The minimum PWM setting for a reliable open-load detection is 3digits for a period of 400Hz and >2 digits for the frequency setting of 200Hz, i.e. the high-side on-time must be longer than $t_{OL,HS}$.

Reliable Overcurrent Detection during PWM Operation

The minimum PWM setting for a reliable overcurrent detection is >1 digit for a period of 400Hz and 1 digit for the frequency setting of 200Hz, i.e. the high-side on-time must be longer than $t_{SD,HS}$.

9.3 Electrical Characteristics

Table 22 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output HS1, HS2, HS3, HS4							
Static Drain-Source ON Resistance HS1...HS4	$R_{ON,HS25}$	–	7	10	Ω	I_{ds} = 60mA, T_j < 25°C	P_9.3.1
Static Drain-Source ON Resistance HS1...HS4	$R_{ON,HS150}$	–	11.5	16	Ω	I_{ds} = 60mA, T_j < 150°C	P_9.3.2
Leakage Current HSx / per channel	$I_{leak,HS}$	–	–	2	µA	[1] 0 V < V_{HSx} < V_{SHS}; T_j < 85°C	P_9.3.11
Output Slew Rate (rising)	$SR_{raise,HS}$	0.8	–	2.5	V/µs	[1] 20 to 80% V_{SHS} = 6 to 18V R_L = 220Ω	P_9.3.3
Output Slew Rate (falling)	$SR_{fall,HS}$	-2.5	–	-0.8	V/µs	[1] 80 to 20% V_{SHS} = 6 to 18V R_L = 220Ω	P_9.3.4
Switch-on time HSx	$t_{ON,HS}$	3	–	30	µs	CSN = HIGH to 0.8*VSHS; R_L = 220Ω; V_{SHS} = 6 to 18V	P_9.3.5
Switch-off time HSx	$t_{OFF,HS}$	3	–	30	µs	CSN = HIGH to 0.2*VSHS; R_L = 220Ω; V_{SHS} = 6 to 18V	P_9.3.6
Short Circuit Shutdown Current	$I_{SD,HS}$	150	245	300	mA	V_{SHS} = 6 to 20V, hysteresis included	P_9.3.7
Short Circuit Shutdown Filter Time	$t_{SD,HS}$	12	16	20	µs	[2], [3]	P_9.3.8
Open Load Detection Current	$I_{OL,HS}$	0.4	–	3	mA	hysteresis included	P_9.3.9
Open Load Detection hysteresis	$I_{OL,HS,hys}$	0.05	0.45	1.0	mA	[1]	P_9.3.14
Open Load Detection Filter Time	$t_{OL,HS}$	50	64	80	µs	[2], [3]	P_9.3.10

1) Not subject to production test, specified by design.

2) Not subject to production test, tolerance defined by internal oscillator tolerance.

3) Configure proper minimum PWM settings for reliable detection of overcurrent and open load measurement (see also **Chapter 9.2.5**).

10 High Speed CAN Transceiver

10.1 Block Description

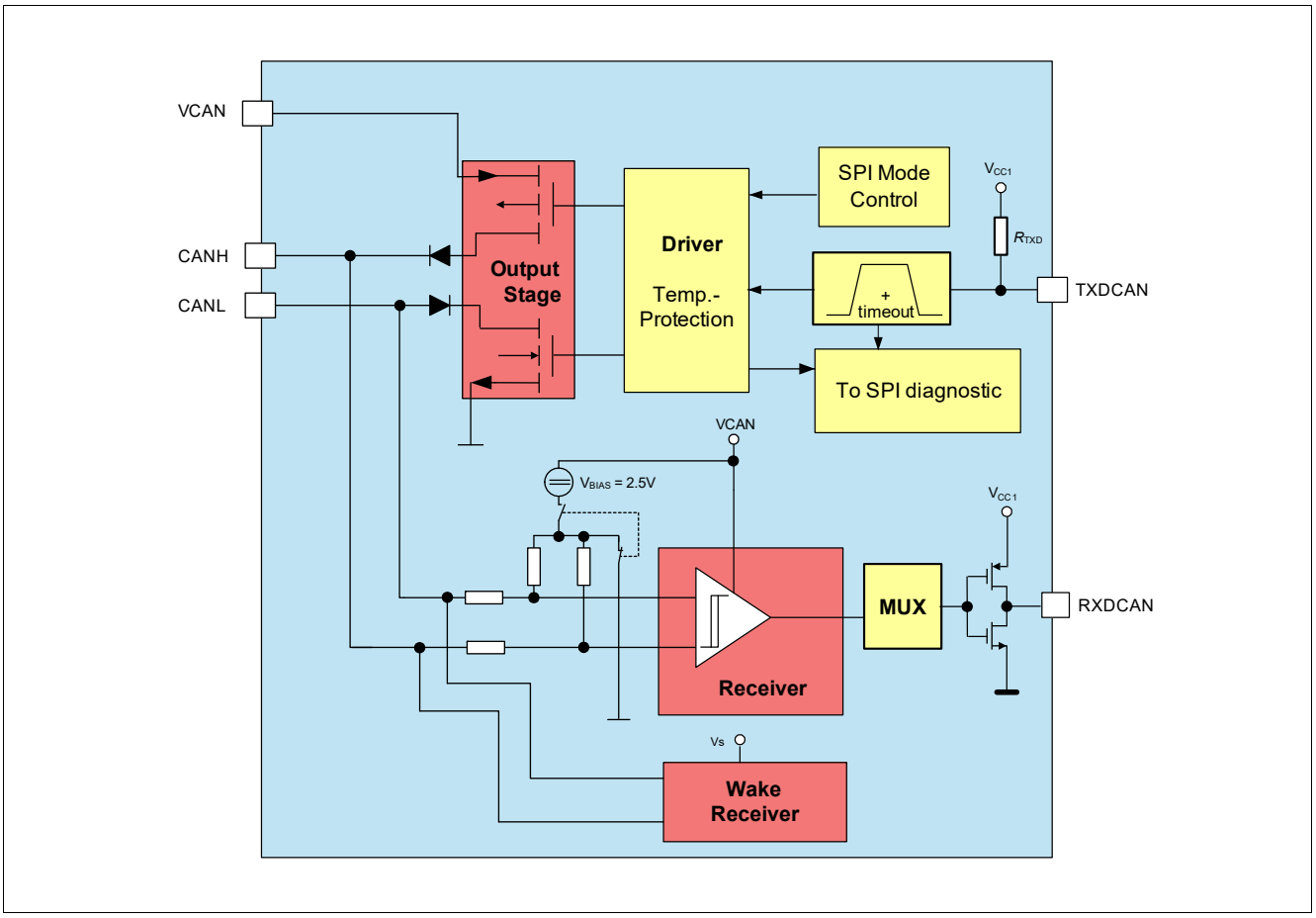

Figure 30 Functional Block Diagram

10.2 Functional Description

The Controller Area Network (CAN) transceiver part of the SBC provides high-speed (HS) differential mode data transmission (up to 2 Mbaud) and reception in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical bus lines compatible to ISO 11898-2:2016 and SAE J2284.

The CAN transceiver offers low power modes to reduce current consumption. This supports networks with partially powered down nodes. To support software diagnostic functions, a CAN Receive-only Mode is implemented.

It is designed to provide excellent passive behavior when the transceiver is switched off (mixed networks, clamp15/30 applications).

A wake-up from the CAN wake capable mode is possible via a message on the bus. Thus, the microcontroller can be powered down or idled and will be woken up by the CAN bus activities.

The CAN transceiver is designed to withstand the severe conditions of automotive applications and to support 12 V applications.

The different transceiver modes can be controlled via the SPI **CAN** bits.

Figure 31 shows the possible transceiver mode transitions when changing the SBC mode.

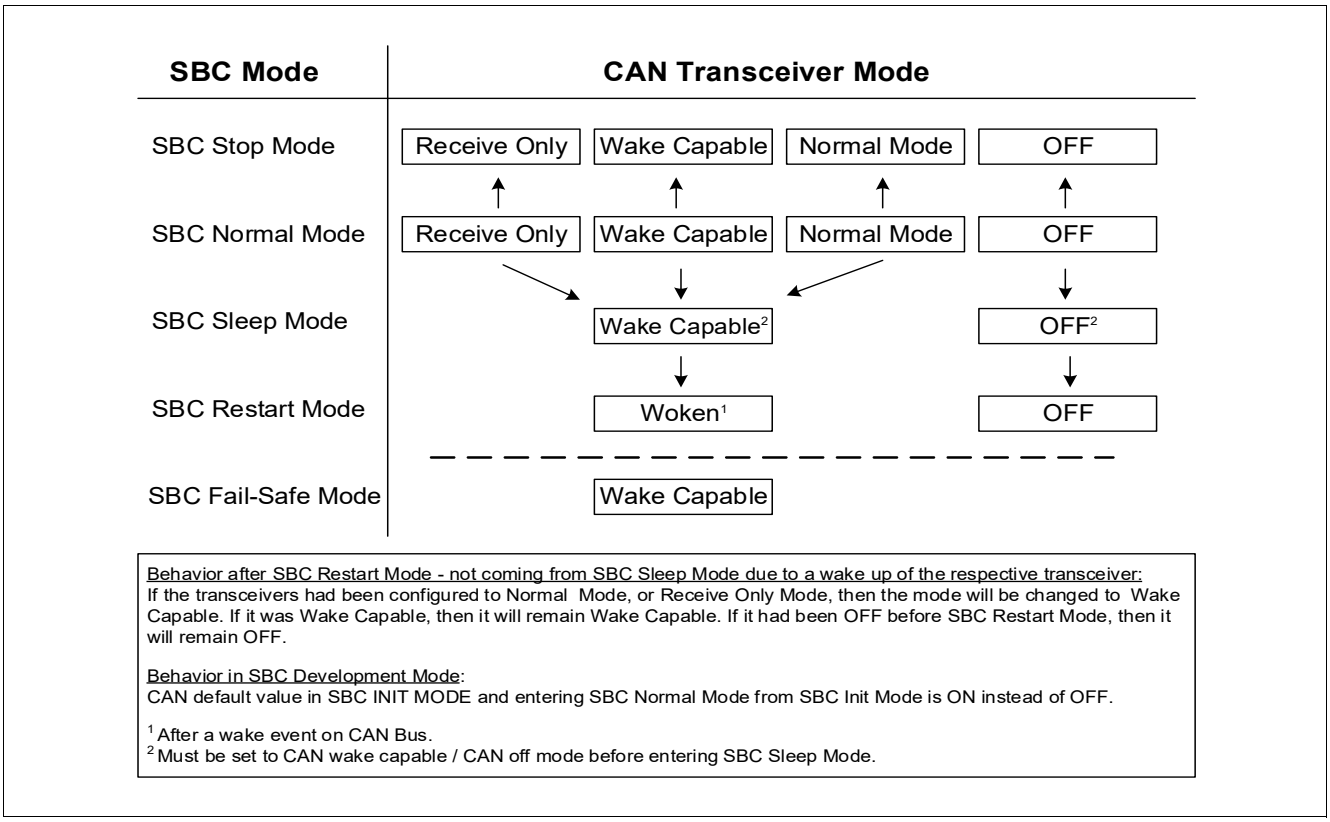

Figure 31 CAN Mode Control Diagram

CAN FD Support

CAN FD stands for 'CAN with Flexible Data Rate'. It is based on the well established CAN protocol as specified in ISO 11898-1. CAN FD still uses the CAN bus arbitration method. The benefit is that the bit rate can be increased by switching to a shorter bit time at the end of the arbitration process and then to return to the longer bit time at the CRC delimiter, before the receivers transmit their acknowledge bits. See also **Figure 32**. In addition, the effective data rate is increased by allowing longer data fields. CAN FD allows the transmission of up to 64 data bytes compared to the 8 data bytes from the standard CAN.

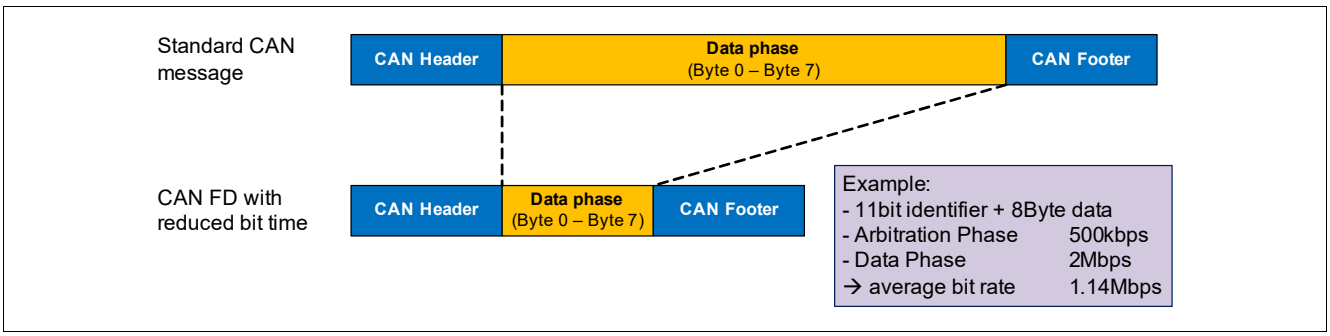

Figure 32 Bite Rate Increase with CAN FD vs. Standard CAN

Not only the physical layer must support CAN FD but also the CAN controller. In case the CAN controller is not able to support CAN FD then the respective CAN node must at least tolerate CAN FD communication. This CAN FD tolerant mode is realized in the physical layer in combination with CAN Partial Networking. The TLE926x-

3QX variants of this family also support the CAN FD tolerant mode. See also **Chapter 5.4.7** for more detailed information on how to enable the CAN FD tolerant mode.

10.2.1 CAN OFF Mode

The CAN OFF Mode is the default mode after power-up of the SBC. It is available in all SBC Modes and is intended to completely stop CAN activities or when CAN communication is not needed. The CANH/L bus interface acts as a high impedance input with a very small leakage current. In CAN OFF Mode, a wake-up event on the bus will be ignored.

10.2.2 CAN Normal Mode

The CAN Transceiver is enabled via SPI in SBC Normal Mode. CAN Normal Mode is designed for normal data transmission/reception within the HS-CAN network. The Mode is available in SBC Normal Mode and in SBC Stop Mode. The bus biasing is set to VCAN/2.

Transmission

The signal from the microcontroller is applied to the TXDCAN input of the SBC. The bus driver switches the CANH/L output stages to transfer this input signal to the CAN bus lines.

Enabling sequence

The CAN transceiver requires an enabling time $t_{CAN,EN}$ before a message can be sent on the bus. This means that the TXDCAN signal can only be pulled LOW after the enabling time. If this is not ensured, then the TXDCAN needs to be set back to HIGH (=recessive) until the enabling time is completed.

Only the next dominant bit will be transmitted on the bus.

Figure 33 shows different scenarios and explanations for CAN enabling.

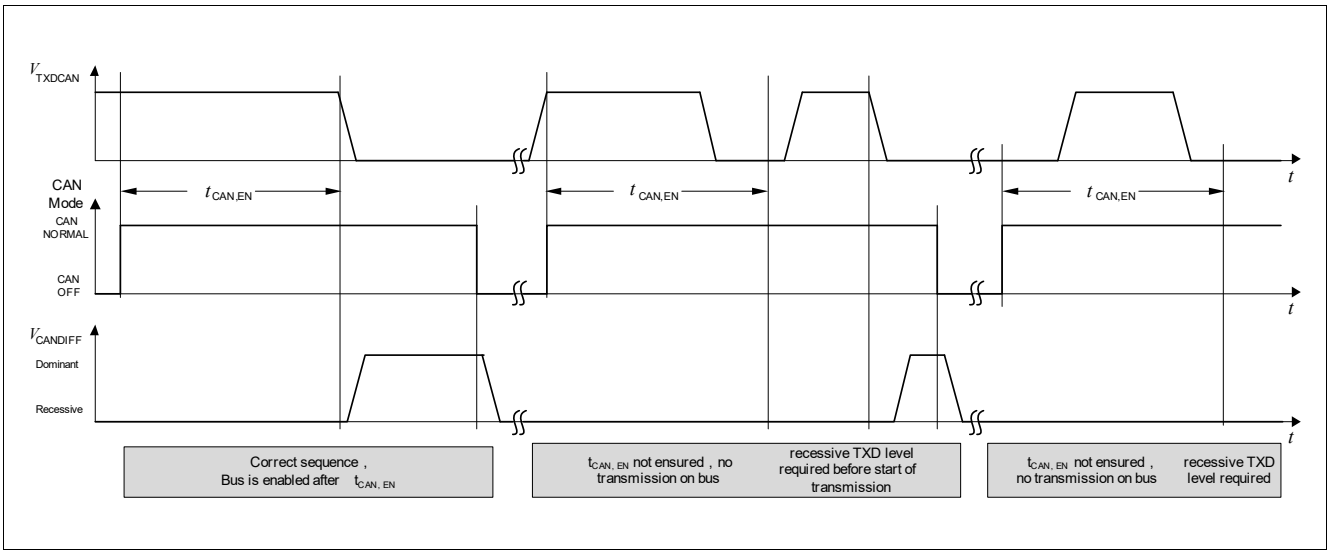

Figure 33 CAN Transceiver Enabling Sequence

Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls CANH/L slopes symmetrically.

Reception

Analog CAN bus signals are converted into digital signals at RXD via the differential input receiver.

10.2.3 CAN Receive Only Mode

In CAN Receive Only Mode (RXD only), the driver stage is de-activated but reception is still operational. This mode is accessible by an SPI command in Normal Mode and in Stop Mode. The bus biasing is set to VCAN/2.

10.2.4 CAN Wake Capable Mode

This mode can be used in SBC Stop, Sleep, Restart and Normal Mode and it is used to monitor bus activities. It is automatically accessed in SBC Fail-Safe Mode. Both bus pins CANH/L are connected to GND via the input resistors.
A wake-up signal on the bus results in a change of behavior of the SBC, as described in **Table 23**. The pins CANH/L are terminated to typ. 2.5V through the input resistors. As a wake-up signalization to the microcontroller, the RXD_CAN pin is set LOW and will stay LOW until the CAN transceiver is changed to any other mode. After a wake-up event, the transceiver can be switched to CAN Normal Mode for communication via SPI.

As shown in **Figure 34**, a wake-up pattern (WUP) is signaled on the bus by two consecutive dominant bus levels for at least t_{Wake1} (filter time $t > t_{Wake1}$) and shorter than t_{Wake2}, each separated by a recessive bus level of greater than t_{Wake1} and shorter than t_{Wake2}.

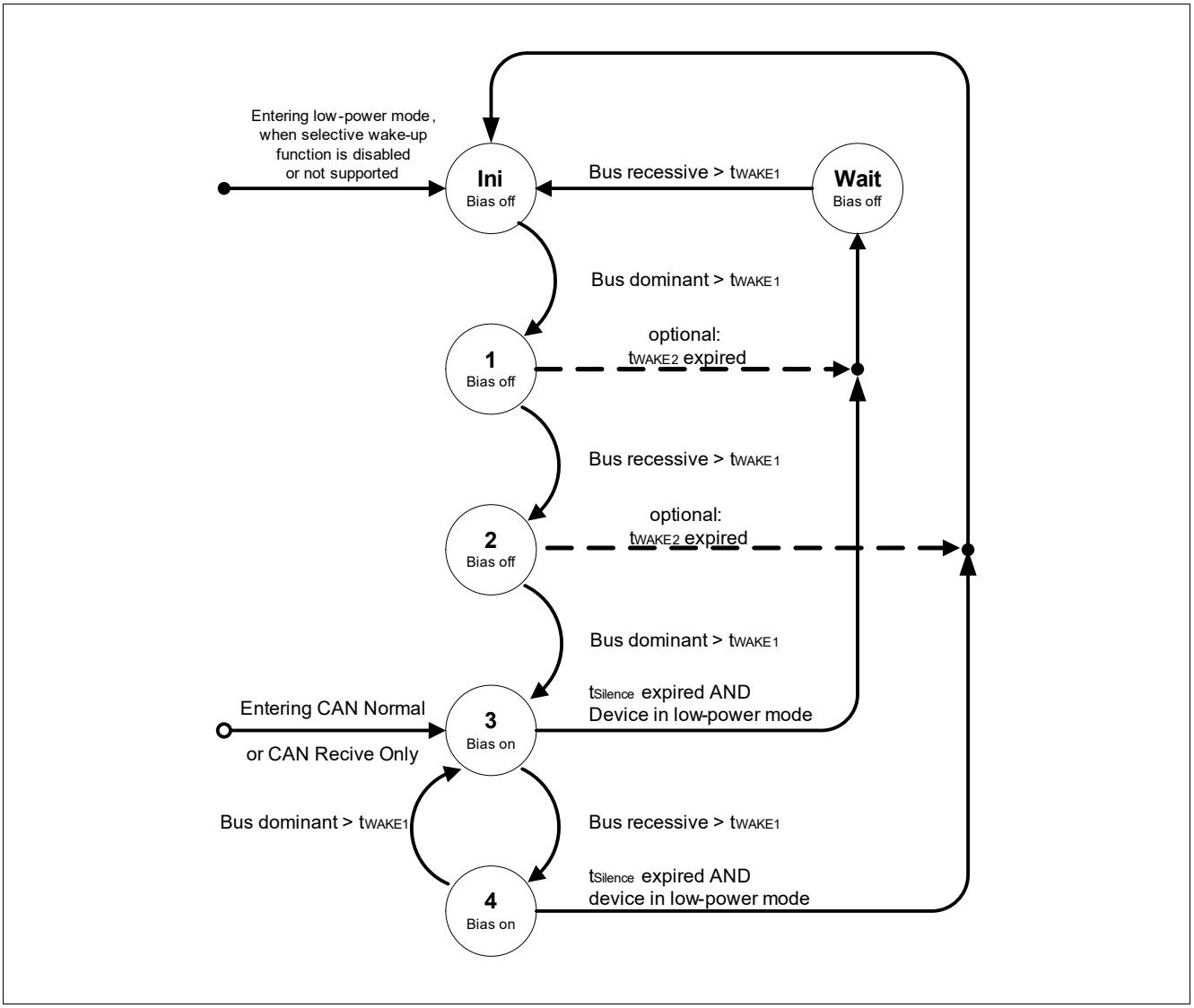

Figure 34 WUP detection following the definition in ISO 11898-2:2016

Rearming the Transceiver for Wake Capability

After a BUS wake-up event, the transceiver is woken. However, the **CAN** transceiver mode bits will still show wake capable (='01') so that the RXD signal will be pulled low. There are two possibilities how the CAN transceiver's wake capable mode is enabled again after a wake event:

- The CAN transceiver mode must be toggled, i.e. switched from Wake Capable Mode to CAN Normal Mode, CAN Receive Only Mode or CAN Off, before switching to CAN Wake Capable Mode again.
- Rearming is done automatically when the SBC is changed to SBC Stop or SBC Fail-Safe Mode to ensure wake-up capability.
- CAN must be set to CAN wake capable / CAN off mode before entering SBC Sleep Mode

*Note: It is not necessary to clear the CAN wake-up bit **CAN_WU** to become wake capable again. It is sufficient to toggle the CAN mode.*

Note: The CAN module is supplied by an internal voltage when in CAN Wake Capable Mode, i.e. the module must not be supplied through the VCAN pin during this time. Before changing the CAN Mode to Normal Mode, the supply of VCAN has to be activated first.

Wake-Up in SBC Stop and Normal Mode

In SBC Stop Mode, if a wake-up is detected, it is always signaled by the INT output and in the **WK_STAT_1** SPI register. It is also signaled by RXDCAN pulled to low. The same applies for the SBC Normal Mode. The microcontroller should set the device from SBC Stop Mode to SBC Normal Mode, there is no automatic transition to Normal Mode.

For functional safety reasons, the watchdog will be automatically enabled in SBC Stop Mode after a Bus wake event in case it was disabled before (if bit **WD_EN_ WK_BUS** was configured to HIGH before).

Wake-Up in SBC Sleep Mode

Wake-up is possible via a CAN message (filter time $t > t_{Wake1}$). The wake-up automatically transfers the SBC into the SBC Restart Mode and from there to Normal Mode the corresponding RXD pin in set to LOW. The microcontroller is able to detect the low signal on RXD and to read the wake source out of the **WK_STAT_1** register via SPI. No interrupt is generated when coming out of Sleep Mode. The microcontroller can now for example switch the CAN transceiver into CAN Normal Mode via SPI to start communication.

Table 23 Action due to CAN Bus Wake-Up

SBC Mode	SBC Mode after Wake	VCC1	INT	RXD
Normal Mode	Normal Mode	ON	LOW	LOW
Stop Mode	Stop Mode	ON	LOW	LOW
Sleep Mode	Restart Mode	Ramping Up	HIGH	LOW
Restart Mode	Restart Mode	ON	HIGH	LOW
Fail-Safe Mode	Restart Mode	Ramping up	HIGH	LOW

10.2.5 TXD Time-out Feature

If the TXD signal is dominant for a time $t > t_{TXD_CAN_TO}$, in CAN Normal Mode, the TXD time-out function deactivates the transmission of the signal at the bus. This is implemented to prevent the bus from being blocked permanently due to an error. The transmitter is disabled and the transceiver is switched to Receive Only Mode. The failure is stored in the SPI flag **CAN_FAIL**. The CAN transmitter stage is activated again after the dominant time-out condition is removed and the transceiver is automatically switched back to CAN Normal Mode. The transceiver configuration stays unchanged.

10.2.6 Bus Dominant Clamping

If the HS CAN bus signal is dominant for a time $t > t_{BUS_CAN_TO}$ in CAN Normal and Receive Only Mode a bus dominant clamping is detected and the SPI bit **CAN_FAIL** is set. The transceiver configuration stays unchanged.

10.2.7 Undervoltage Detection

The voltage at the CAN supply pin is monitored only in CAN Normal and Receive Only Mode for SBC Normal and Stop Mode . In case of VCAN undervoltage a signalization via SPI bit **VCAN_UV** is triggered and the SBC disables the transmitter stage. If the CAN supply reaches a higher level than the undervoltage detection threshold (VCAN > V_{CAN_UV}), the transceiver is automatically switched back to CAN Normal Mode. The transceiver configuration stays unchanged.

10.3 Electrical Characteristics

Table 24 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN Bus Receiver							
Differential Receiver Threshold Voltage, recessive to dominant edge	V_{diff,rd_N}	–	0.80	0.90	V	$V_{diff} = V_{CANH} - V_{CANL}$; -12V ≤ V_{CM}(CAN) ≤ +12V; 0.9 V ≤ V_{diff,D_Range} ≤ 8 V; CAN Normal Mode	P_10.3.2
Dominant state differential input voltage range	$V_{diff_D_range}$	0.9	–	8.0	V	1) $V_{diff} = V_{CANH} - V_{CANL}$; -12V ≤ V_{CM}(CAN) ≤ +12V; CAN Normal Mode	P_10.3.59
Differential Receiver Threshold Voltage, dominant to recessive edge	V_{diff,dr_N}	0.50	0.60	–	V	$V_{diff} = V_{CANH} - V_{CANL}$; -12V ≤ V_{CM}(CAN) ≤ +12V; -3 V ≤ V_{diff,R_Range} ≤ 0.5 V; CAN Normal Mode	P_10.3.3
Recessive state differential input voltage range	$V_{diff_R_range}$	-3.0	–	0.5	V	1) $V_{diff} = V_{CANH} - V_{CANL}$; -12V ≤ V_{CM}(CAN) ≤ +12V; CAN Normal Mode	P_10.3.60
Common Mode Range	CMR	-12	–	12	V	1)	P_10.3.4
CANH, CANL Input Resistance	R_{in}	20	40	50	kΩ	CAN Normal / Wake capable Mode; Recessive state; -2 V ≤ $V_{CANL/H}$ ≤ +7 V	P_10.3.6
Differential Input Resistance	R_{diff}	40	80	100	kΩ	CAN Normal / Wake capable Mode; Recessive state; -2 V ≤ $V_{CANL/H}$ ≤ +7 V	P_10.3.7
Input Resistance Deviation between CANH and CANL	ΔR_i	-3	–	3	%	1) Recessive state; $V_{CANH} = V_{CANL}$ = 5 V	P_10.3.38
Input Capacitance CANH, CANL versus GND	C_{in}	–	20	40	pF	2) V_{TXD} = 5 V	P_10.3.39
Differential Input Capacitance	C_{diff}	–	10	20	pF	2) V_{TXD} = 5 V	P_10.3.40
Wake-up Receiver Threshold Voltage, recessive to dominant edge	$V_{diff,\ rd_W}$	–	0.8	1.15	V	-12V ≤ V_{CM}(CAN) ≤ +12V; 1.15 V ≤ V_{diff,D_Range} ≤ 8 V; CAN Wake Capable Mode	P_10.3.8

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Wake-up Receiver Dominant state differential input voltage range	V_{diff,D_range_W}	1.15	–	8.0	V	[1] -12V ≤ V_{CM}(CAN) ≤ +12V; CAN Wake Capable Mode	P_10.3.61
Wake-up Receiver Threshold Voltage, dominant to recessive edge	$V_{diff,\ dr_W}$	0.4	0.7	–	V	-12V ≤ V_{CM}(CAN) ≤ +12V; -3 V ≤ V_{diff,R_Range} ≤ 0.4 V; CAN Wake Capable Mode	P_10.3.9
Wake-up Receiver Recessive state differential input voltage range	V_{diff,R_range_W}	-3.0	–	0.4	V	[1] -12V ≤ V_{CM}(CAN) ≤ +12V; CAN Wake Capable Mode	P_10.3.62
CAN Bus Transmitter							
CANH/CANL Recessive Output Voltage (CAN Normal Mode)	V_{CANL/H_NM}	2.0	–	3.0	V	CAN Normal Mode; V_{TXD} = V_{CC1}; no load	P_10.3.11
CANH/CANL Recessive Output Voltage (CAN Wake Capable Mode)	V_{CANL/H_LP}	-0.1	–	0.1	V	CAN Wake Capable Mode; V_{TXD} = V_{CC1}; no load	P_10.3.43
CANH, CANL Recessive Output Voltage Difference V_{diff} = V_{CANH} - V_{CANL} (CAN Normal Mode)	$V_{diff_r_N}$	-500	–	50	mV	CAN Normal Mode V_{TXD} = V_{CC1}; no load	P_10.3.12
CANH, CANL Recessive Output Voltage Difference V_{diff} = V_{CANH} - V_{CANL} (CAN Wake Capable Mode)	$V_{diff_r_W}$	-200	–	200	mV	CAN Wake Capable Mode; V_{TXD} = V_{CC1}; no load	P_10.3.41
CANL Dominant Output Voltage	V_{CANL}	0.5	–	2.25	V	CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 50Ω ≤ R_L ≤ 65Ω	P_10.3.13
CANH Dominant Output Voltage	V_{CANH}	2.75	–	4.5	V	CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 50Ω ≤ R_L ≤ 65Ω	P_10.3.14
CANH, CANL Dominant Output Voltage Difference V_{diff} = V_{CANH} - V_{CANL}	$V_{diff_d_N}$	1.5	2.0	2.5	V	CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 50Ω ≤ R_L ≤ 65Ω	P_10.3.16

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff_d_N}$	1.5	–	5.0	V	1)CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; R_L = 2240Ω	P_10.3.55
CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff_d_N}$	1.4	–	3.3	V	1)CAN Normal Mode; VTXD = 0 V; VCAN = 5 V; 45Ω ≤ RL ≤ 70Ω	P_10.3.56
CANH, CANL output voltage difference slope, recessive to dominant	$V_{diff_slope_rd}$	–	–	70	V/us	1)30% to 70% of measured differential bus voltage, C_L = 100 pF, R_L = 60 Ω	P_10.3.57
CANH, CANL output voltage difference slope, dominant to recessive	$V_{diff_slope_dr}$	–	–	70	V/us	1)70% to 30% of measured differential bus voltage, C_L = 100 pF, R_L = 60 Ω	P_10.3.58
Driver Symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	4.5	–	5.5	V	3)CAN Normal Mode; V_{TXD} = 0 V / 5 V; V_{CAN} = 5 V; C_{SPLIT} = 4.7nF; R_L = 60Ω;	P_10.3.42
CANH Short Circuit Current	I_{CANHsc}	-115	-80	-50	mA	CAN Normal Mode; $V_{CANHshort}$ = -3 V	P_10.3.17
CANL Short Circuit Current	I_{CANLsc}	50	80	115	mA	CAN Normal Mode $V_{CANLshort}$ = 18 V	P_10.3.18
Leakage Current (unpowered device)	$I_{CANH,lk}$ $I_{CANL,lk}$	–	5	7.5	µA	$V_S = V_{CAN}$ = 0V; 0V < $V_{CANH,L}$ ≤ 5V; 4)R_{test} = 0 / 47 kΩ	P_10.3.19
Receiver Output RXD							
HIGH level Output Voltage	$V_{RXD,H}$	0.8 × V_{CC1}	–	–	V	CAN Normal Mode $I_{RXD(CAN)}$ = -2 mA;	P_10.3.21
LOW Level Output Voltage	$V_{RXD,L}$	–	–	0.2 × V_{CC1}	V	CAN Normal Mode $I_{RXD(CAN)}$ = 2 mA;	P_10.3.22
Transmission Input TXD							
HIGH Level Input Voltage Threshold	$V_{TXD,H}$	–	–	0.7 × V_{CC1}	V	CAN Normal Mode recessive state	P_10.3.23
LOW Level Input Voltage Threshold	$V_{TXD,L}$	0.3 × V_{CC1}	–	–	V	CAN Normal Mode dominant state	P_10.3.24

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TXD Input Hysteresis	$V_{TXD,hys}$	0.08 × V_{CC1}	0.12 × V_{CC1}	0.5 × V_{CC1}	V	[1]	P_10.3.25
TXD Pull-up Resistance	R_{TXD}	20	40	80	kΩ	–	P_10.3.26
CAN Transceiver Enabling Time	$t_{CAN,EN}$	8	13	18	µs	[5]CSN = HIGH to first valid transmitted TXD dominant	P_10.3.27
Dynamic CAN-Transceiver Characteristics							
Min. Dominant Time for Bus Wake-up	t_{Wake1}	0.50	–	1.8	µs	-12V ≤ V_{CM}(CAN) ≤ +12 V; CAN Wake capable Mode	P_10.3.28
Wake-up Time-out, Recessive Bus	t_{Wake2}	0.8	–	10	ms	[5]CAN Wake capable Mode	P_10.3.29
WUP Wake-up Reaction Time	t_{WU_WUP}	–	–	100	µs	[5][6][7] Wake-up reaction time after a valid WUP on CAN bus;	P_10.3.44
Loop delay (recessive to dominant)	$t_{LOOP,f}$	–	150	255	ns	[3]CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF	P_10.3.30
Loop delay (dominant to recessive)	$t_{LOOP,r}$	–	150	255	ns	[3]CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF	P_10.3.31
Propagation Delay TXD LOW to bus dominant	$t_{d(L),T}$	–	50	–	ns	CAN Normal Mode C_L = 100pF; 50Ω ≤ R_L ≤ 65Ω; V_{CAN} = 5 V;	P_10.3.32
Propagation Delay TXD HIGH to bus recessive	$t_{d(H),T}$	–	50	–	ns	CAN Normal Mode C_L = 100 pF; 50Ω ≤ R_L ≤ 65Ω; V_{CAN} = 5 V;	P_10.3.33
Propagation Delay bus dominant to RXD LOW	$t_{d(L),R}$	–	100	–	ns	CAN Normal Mode C_L = 100pF; 50Ω ≤ R_L ≤ 60Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF	P_10.3.34

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Propagation Delay bus recessive to RXD HIGH	$t_{d(H),R}$	–	100	–	ns	CAN Normal Mode C_L = 100pF; 50Ω ≤ R_L ≤ 60Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF	P_10.3.35
Received Recessive Bit Width (CAN FD up to 2Mbps)	$t_{bit(RXD)}$	400	–	550	ns	CAN Normal Mode C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 500ns; Timing definition according to **Figure 36**	P_10.3.46
TransmittedRecessive Bit Width (CAN FD up to 2Mbps)	$t_{bit(BUS)}$	435	–	530	ns	CAN Normal Mode C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 500ns;Timing definition according to **Figure 36**	P_10.3.47
Receiver Timing Symmetry (CAN FD up to 2Mbps)	Δt_{Rec}	-65	–	40	ns	CAN Normal Mode C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 500ns;Timing definition according to **Figure 36**	P_10.3.48
Received Recessive Bit Width (CAN FD up to 5 Mbps)	$t_{bit(RXD)}$	120	–	220	ns	CAN Normal Mode; C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 36**.	P_10.3.52

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transmitted Recessive Bit Width (CAN FD up to 5 Mbps)	$t_{bit(BUS)}$	155	–	210	ns	CAN Normal Mode; C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 36**.	P_10.3.53
Receiver Timing Symmetry (CAN FD up to 5 Mbps)	Δt_{Rec}	-45	–	15	ns	CAN Normal Mode; C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 36**.	P_10.3.54
TXD Permanent Dominant Time-out	$t_{TxD_CAN_TO}$	1.6	2	2.4	ms	5)CAN Normal Mode	P_10.3.36
BUS Permanent Dominant Time-out	$t_{BUS_CAN_TO}$	1.6	2	2.4	ms	5)CAN Normal Mode	P_10.3.37
Timeout for bus inactivity	$t_{SILENCE}$	0.6	–	1.2	s	5)	P_10.3.50
Bus Bias reaction time	t_{Bias}	–	–	200	µs	5)	P_10.3.51

1) Not subject to production test, specified by design.
2) Not subject to production test, specified by design, S2P - Method; f = 10 MHz.
3) **V_{SYM}** shall be observed during dominant and recessive state and also during the transition dominant to recessive and vice versa while TXD is simulated by a square signal (50% duty cycle) with a frequency of up to 1 MHz (2 MBit/s).
4) R_{test} between supply (VS / VCAN) and 0V (GND).
5) Not subject to production test, tolerance defined by internal oscillator tolerance.
6) Wake-up is signalized via INT pin activation in SBC Stop Mode and via VCC1 ramping up with wake from SBC Sleep Mode.
7) Time starts with end of last dominant phase of WUP.

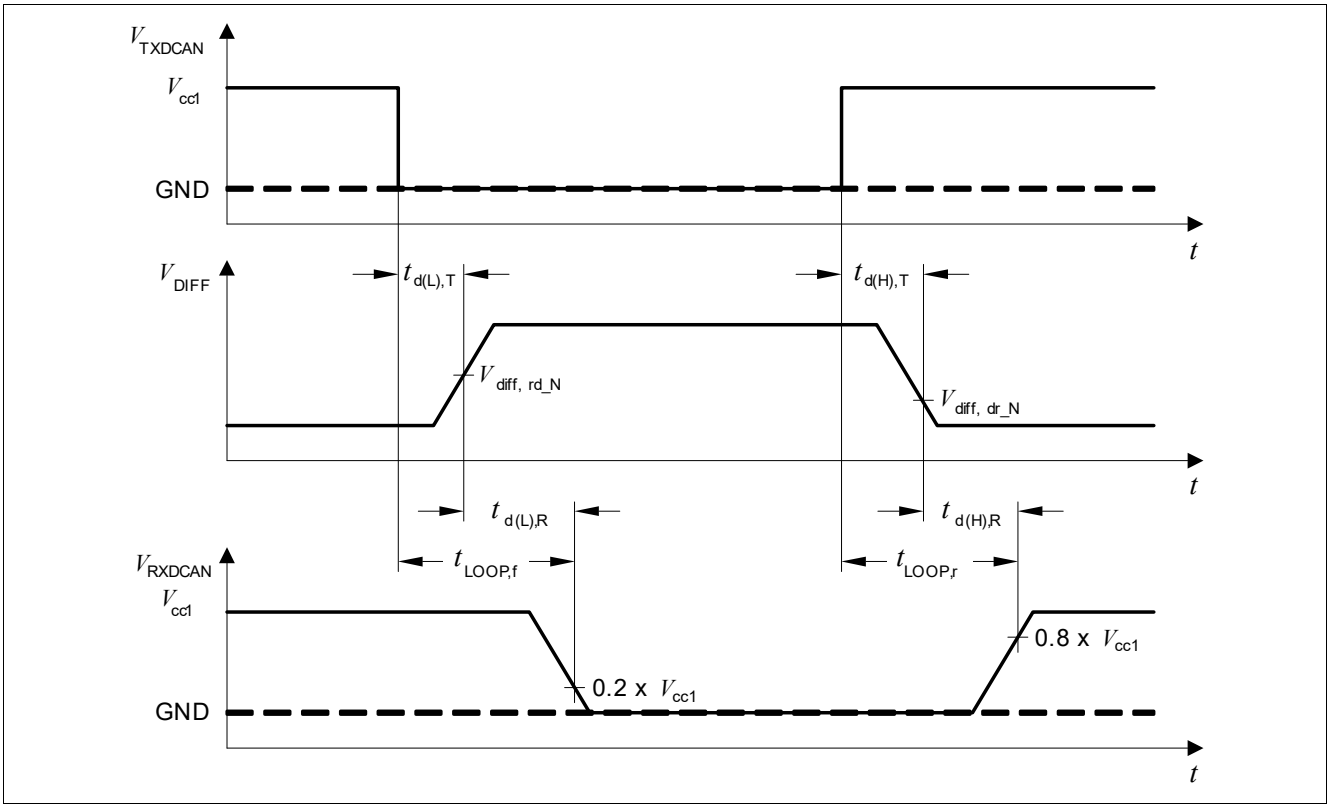

Figure 35 Timing Diagrams for Dynamic Characteristics

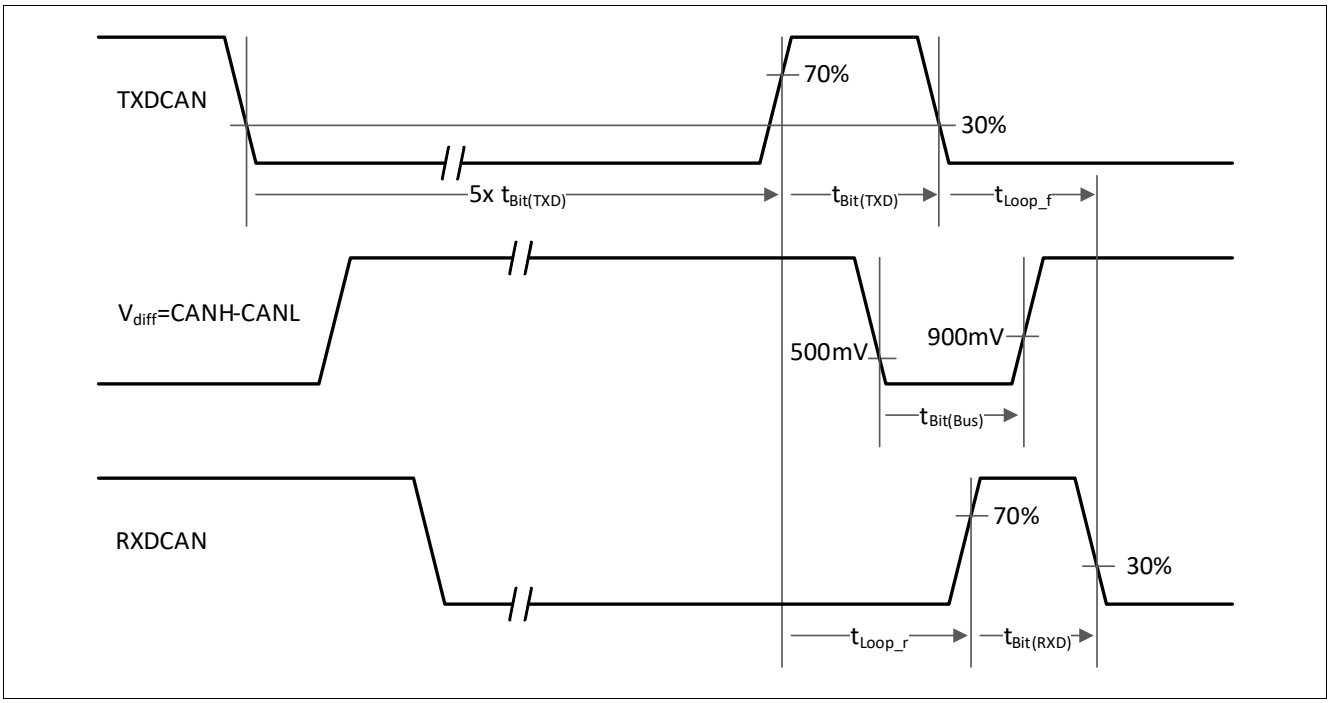

Figure 36 From ISO 11898-2: tloop, tbit(TXD), tbit(Bus), tbit(RXD) definitions

11 Wake and Voltage Monitoring Inputs

11.1 Block Description

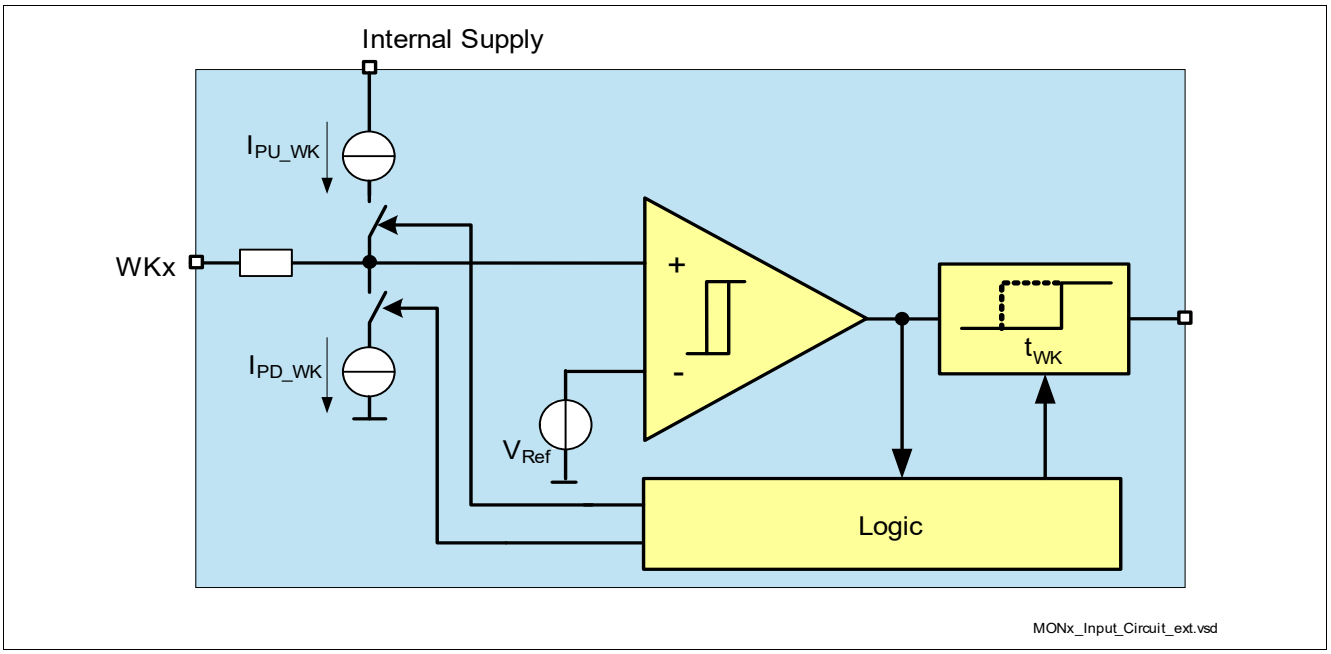

Figure 37 Wake Input Block Diagram

Features

- Three High-Voltage inputs with a 3V (typ.) threshold voltage
- Alternate Measurement function for high-voltage sensing via WK1 and WK2
- Wake-up capability for power saving modes
- Edge sensitive wake feature LOW to HIGH and HIGH to LOW
- Pull-up and Pull-down current sources, configurable via SPI
- Selectable configuration for static sense or cyclic sense working with TIMER1, TIMER2
- In SBC Normal and SBC Stop Mode the level of the WK pin can be read via SPI even if the respective WK is not enabled as a wake source.

11.2 Functional Description

The wake input pins are edge-sensitive inputs with a switching threshold of typically 3V. This means that both transitions, HIGH to LOW and LOW to HIGH, result in a signalization by the SBC. The signalization occurs either in triggering the interrupt in SBC Normal Mode and SBC Stop Mode or by a wake up of the device in SBC Sleep and SBC Fail-Safe Mode.

Two different wake detection modes can be selected via SPI:

- Static sense: WK inputs are always active
- Cyclic sense: WK inputs are only active for a certain time period (see **Chapter 5.2.1**)

Two different filter times of 16µs or 64µs can be selected to avoid a parasitic wake-up due to transients or EMC disturbances in static sense configuration.

The filter time (t_{FWK1}, t_{FWK2}) is triggered by a level change crossing the switching threshold and a wake signal is recognized if the input level will not cross again the threshold during the selected filter time.

Figure 38 shows a typical wake-up timing and parasitic filter.

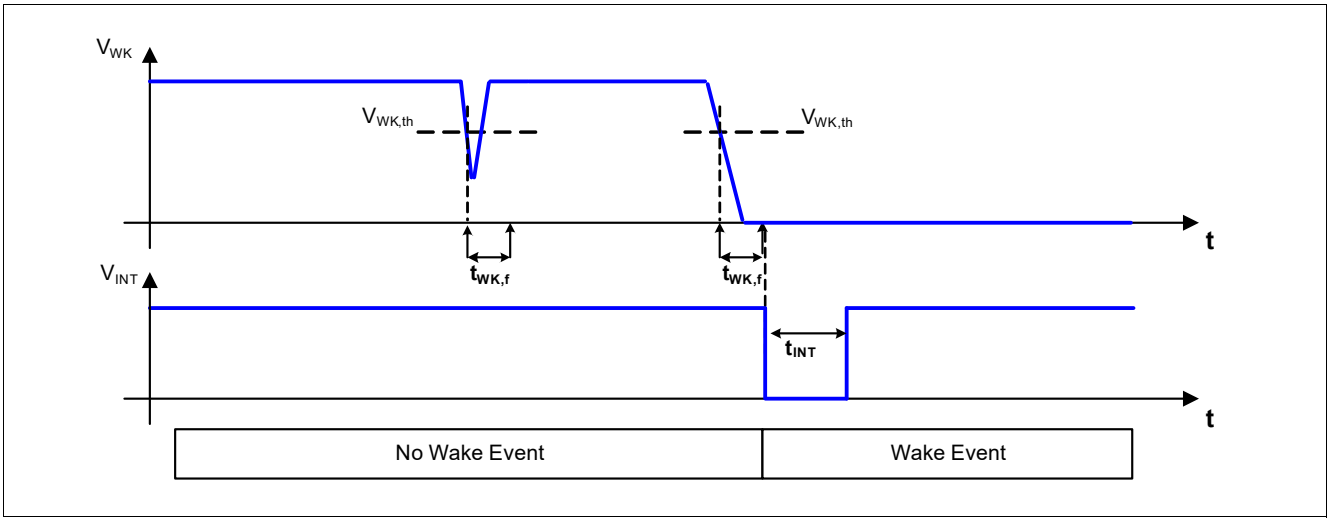

Figure 38 Wake-up Filter Timing for Static Sense

The wake-up capability for each WK pin can be enabled or disabled via SPI command in the **WK_CTRL_2** register.

The wake source for a wake via a WKx pin can always be read in the register **WK_STAT_1** at the bits WK1_WU, WK2_WU, and WK3_WU.

The actual voltage level of the WK pin (LOW or HIGH) can always be read in SBC Normal and SBC Stop Mode in the register **WK_LVL_STAT**. During Cyclic Sense, the register show the sampled levels of the respective WK pin.

If FO2...3 are configured as WK inputs in its alternative function (16µs static filter time), then the wake events will be signalled in the register **WK_STAT_2**.

11.2.1 Wake Input Configuration

To ensure a defined and stable voltage levels at the internal comparator input it is possible to configure integrated current sources via the SPI register **WK_PUPD_CTRL**. In addition, the wake detection modes (including the filter time) can be configured via the SPI register **WK_FLT_CTRL**. An example illustration for the automatic switching configuration is shown in **Figure 39**.

Table 25 Pull-Up / Pull-Down Resistor

WKx_PUPD_1	WKx_PUPD_0	Current Sources	Note
0	0	no current source	WKx input is floating if left open (default setting)
0	1	pull-down	WKx input internally pulled to GND
1	0	pull-up	WKx input internally pulled to internal 5V supply
1	1	Automatic switching	If a high level is detected at the WKx input the pull-up source is activated, if low level is detected the pull down is activated.

Note: If there is no pull-up or pull-down configured on the WK input, then the respective input should be tied to GND or VS on board to avoid unintended floating of the pin and subsequent wake events.

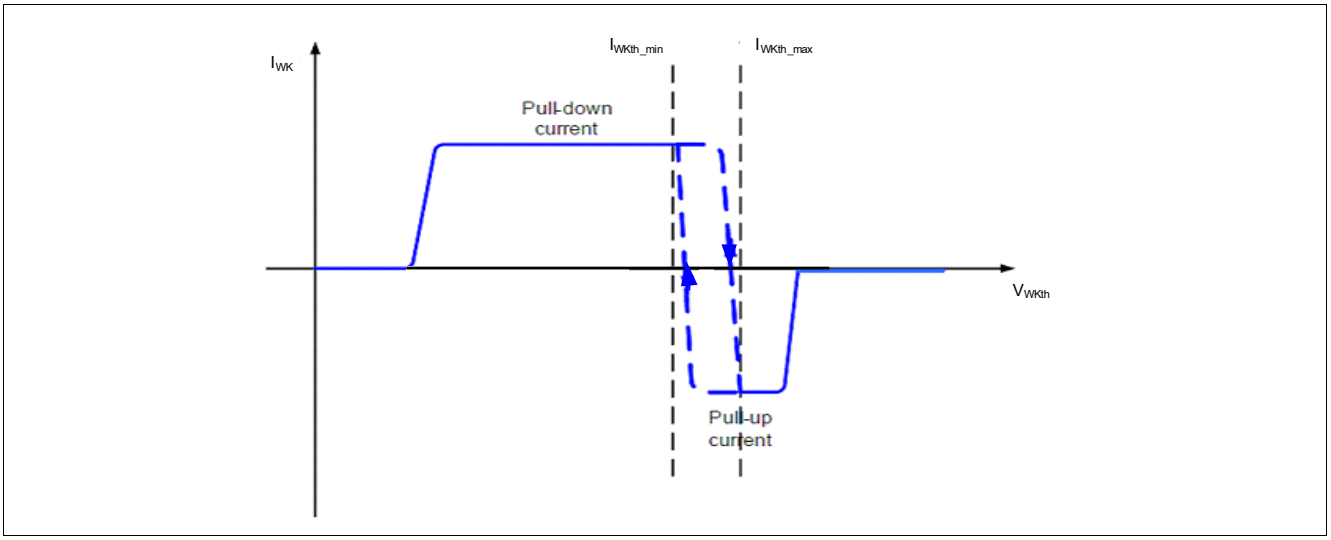

Figure 39 Illustration for Pull-Up / Down Current Sources with Automatic Switching Configuration

Table 26 Wake Detection Configuration and Filter Time

WKx_FLT_1	WKx_FLT_0	Filter Time	Description
0	0	Config A	static sense, 16µs filter time
0	1	Config B	static sense, 64µs filter time
1	0	Config C	Cyclic sense, Timer 1, 16µs filter time. Period, On-time configurable in register **TIMER1_CTRL**
1	1	Config D	Cyclic sense, Timer 2, 16µs filter time. Period, On-time configurable in register **TIMER2_CTRL**

Config A and B are intended for static sense with two different filter times.

Config C or D are intended for cyclic sense configuration. With the filter settings, the respective timer needs to be assigned to one or more HS output, which supplies an external circuit connected to the WKx pin, e.g. HS1 controlled by Timer 2 (HS1 = 010) and connected to WK3 via an switch circuitry - see also **Chapter 5.2**.

11.2.2 Alternate Measurement Function with WK1 and WK2

11.2.2.1 Block Description

This function provides the possibility to measure a voltage, e.g. the unbuffered battery voltage, with the protected WK1 HV-input. The measured voltage is routed out at WK2. It allows for example a voltage compensation for LED lighting by changing the duty cycle of the High-Side outputs. A simple voltage divider needs to be placed externally to provide the correct voltage level to the microcontroller A/D converter input.

The function is available in SBC Normal Mode and it is disabled in all other modes to allow a low-quiescent current operation.The measurement function can be used instead of the WK1 and WK2 wake and level signalling capability.

The benefits of the function is that the signal is measured by a HV-input pin and that there is no current flowing through the resistor divider during low-power modes.
The functionality is shown in a simplified application diagram in **Figure 59**.

11.2.2.2 Functional Description

This measurement function is by default disabled. In this case, WK1 and WK2 have the regular wake and voltage level signalization functionality. The switch S1 is open for this configuration (see **Figure 59**).

The measurement function can be enabled via the SPI bit **WK_MEAS**.

If **WK_MEAS** is set to ‘1’, then the measurement function is enabled and switch S1 is closed in SBC Normal Mode. S1 is open in all other SBC modes. If this function the pull-up and down currents of WK1 and WK2 are disabled, and the internal WK1 and WK2 signals are gated. In addition, the settings for WK1 and WK2 in the registers **WK_PUPD_CTRL**, **WK_FLT_CTRL** and **WK_CTRL_2** are ignored but changing these setting is not prevented. The registers **WK_STAT_1** and **WK_LVL_STAT** are not updated with respect to the inputs WK1 and WK2.
However, if only WK1 or WK2 are set as wake sources and a SBC Sleep Mode command is set, then the **SPI_FAIL** flag will be set and the SBC will be changed into SBC Restart Mode (see **Chapter 5.1** also for wake capability of WK1 and WK2).

Table 27 Differences between Normal WK Function and Measurement Function

Affected Settings/Modules for WK1 and WK2 Inputs	WK_MEAS = 0	WK_MEAS = 1
S1 configuration	‘open’	‘closed’ in SBC Normal Mode, ‘open’ in all other SBC Modes
Internal WK1 & WK2 signal processing	Default wake and level signaling function, **WK_STAT_1**, **WK_STAT_2** are updated accordingly	‘WK1...2 inputs are gated internally, **WK_STAT_1**, **WK_STAT_2** are not updated
WK1_EN, **WK2_EN**	Wake-up via WK1 and WK2 possible if bits are set	setting the bits is ignored and not prevented. If only **WK1_EN**, **WK2_EN** are set while trying to go to SBC Sleep Mode, then the **SPI_FAIL** flag will be set and the SBC will be changed into SBC Restart Mode.
WK_PUPD_CTRL	normal configuration is possible	no pull-up or pull-down enabled
WK_FLT_CTRL	normal configuration is possible	setting the bits is ignored and not prevented

*Note: There is a diode in series to the switch S1 (not shown in the **Figure 59**), which will influence the temperature behavior of the switch.*

11.3 Electrical Characteristics

Table 28 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
WK1...WK3 Input Pin Characteristics							
Wake-up/monitoring threshold voltage	V_{WKth}	2	3	4	V	without external serial resistor R_S (with R_S: $\Delta V = I_{PD/PU} * R_S$); hysteresis included	P_12.3.1
Threshold hysteresis	$V_{WKNth,hys}$	0.1	-	0.7	V	without external serial resistor R_S (with R_S: $\Delta V = I_{PD/PU} * R_S$);	P_12.3.2
WK pin Pull-up Current	I_{PU_WK}	-20	-10	-3	µA	V_{WK_IN} = 4V	P_12.3.3
WK pin Pull-down Current	I_{PD_WK}	3	10	20	µA	V_{WK_IN} = 2V	P_12.3.4
Input leakage current	$I_{LK,I}$	-2		2	µA	0 V < V_{WK_IN} < 40V	P_12.3.5
Drop Voltage across S1 switch	$V_{Drop,S1}$	–	1000	1100	mV	[1)]Drop Voltage between WK1 and WK2 when enabled for voltage measurement; I_{WK1} = 500µA; T_j = 25°C Refer to **Figure 40**	P_12.3.13
Timing							
Wake-up filter time 1	t_{FWK1}	12	16	20	µs	[2)]SPI Setting	P_12.3.6
Wake-up filter time 2	t_{FWK2}	50	64	80	µs	[2)]SPI Setting	P_12.3.7

1) Not subject to production test; specified by design

2) Not subject to production test, tolerance defined by internal oscillator tolerance

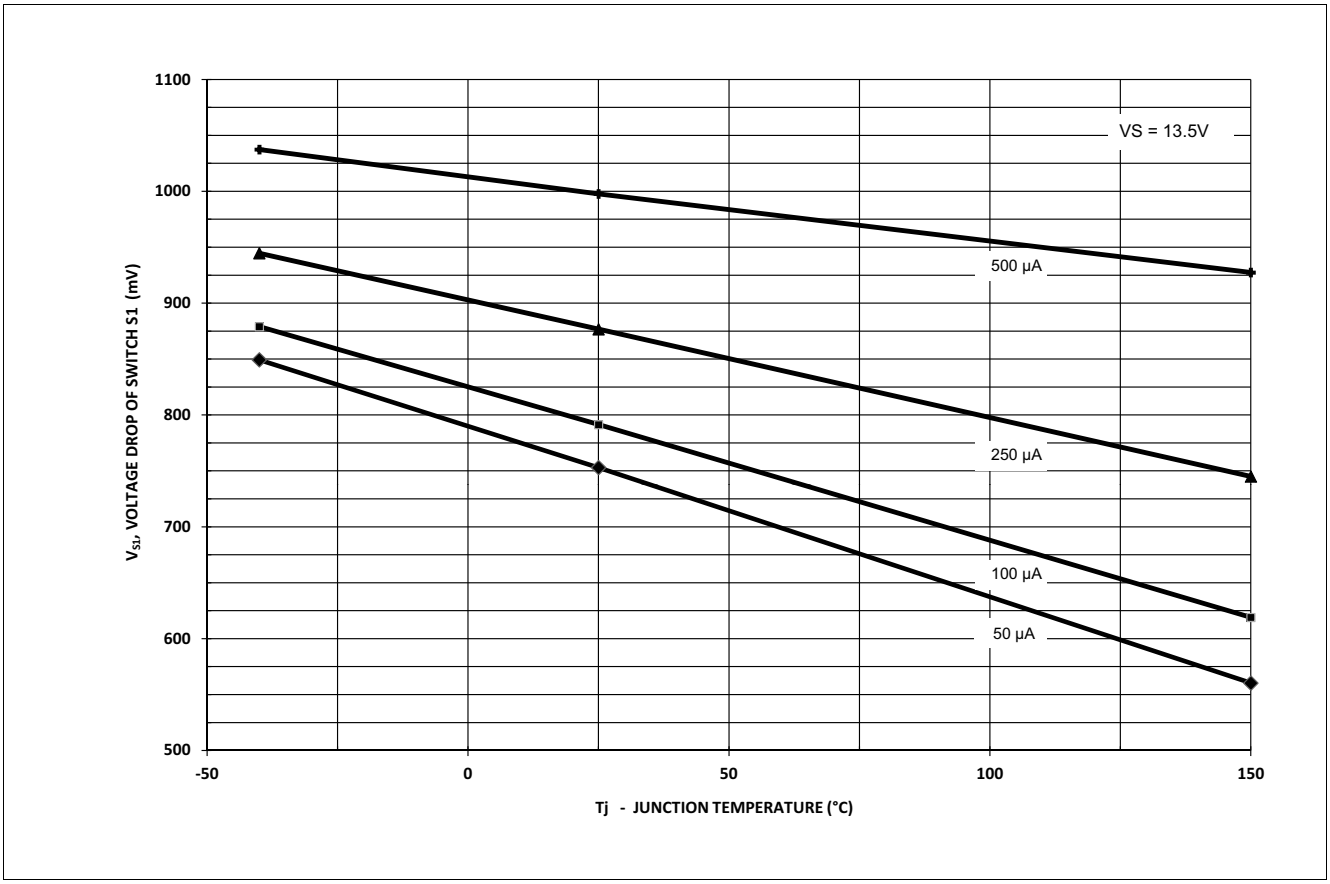

Figure 40 Typical Drop Voltage Characteristics of S1 (between WK1 & WK2)

12 Interrupt Function

12.1 Block and Functional Description

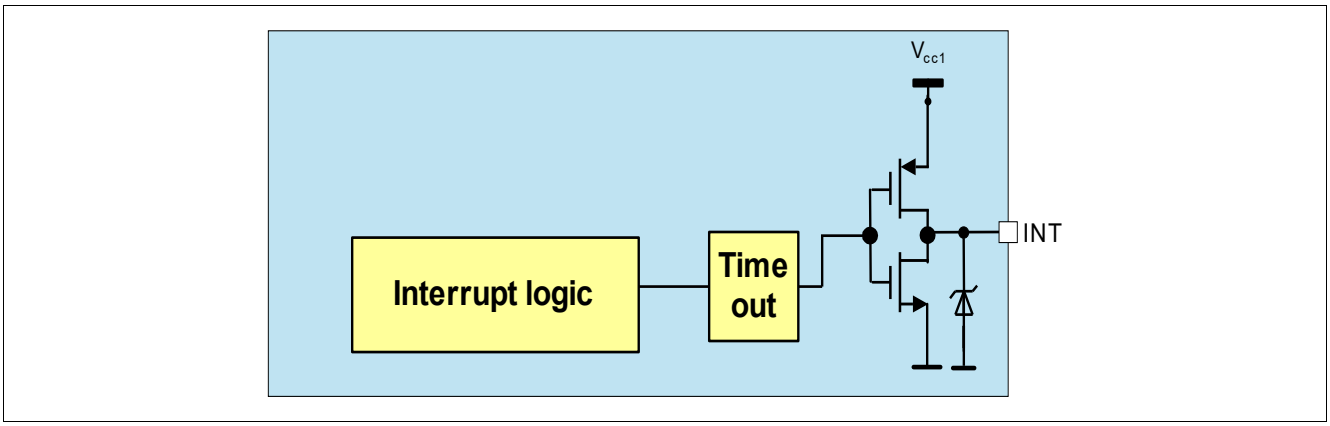

Figure 41 Interrupt Block Diagram

The interrupt is used to signalize special events in real time to the microcontroller. The interrupt block is designed as a push/pull output stage as shown in **Figure 41**. An interrupt is triggered and the INT pin is pulled low (active low) for t_{INT} in SBC Normal and Stop Mode and it is released again once t_{INT} is expired. The minimum HIGH-time of INT between two consecutive interrupts is t_{INTD}. An interrupt does not cause a SBC mode change.

Two different interrupt classes could be selected via the SPI bit **INT_ GLOBAL**:

- Class 1 (wake interrupt - **INT_ GLOBAL**=0): all wake-up events stored in the wake status SPI register (**WK_STAT_1** and **WK_STAT_2**) cause an interrupt (default setting). An interrupt is only triggered if the respective function is also enabled as a wake source (including GPIOx if configured as a wake input). The CAN time out signalization **CANTO** is also considered as a wake source. Therefore, the interrupt mask bit **CANTO_ MASK** has higher priority than the bit **INT_ GLOBAL**, i.e. Integral is not taken into account for CANTO.
- Class 2 (global interrupt - **INT_ GLOBAL**=1): in addition to the wake-up events, all signalled failures stored in the other status registers cause an interrupt (the register **WK_LVL_STAT** is not generating interrupts)

Note: The errors which will cause SBC Restart or SBC Fail-Safe Mode (Vcc1_UV, WD_FAIL, VCC1_SC, TSD2, FAILURE) are the exceptions of an INT generation on status bits. Also POR and DEV_STAT_x and will not generate interrupts.

In addition to this behavior, an INT will be triggered when the SBC is sent to SBC Stop Mode and not all bits were cleared in the **WK_STAT_1** and **WK_STAT_2**register.

The SPI status registers are updated at every falling edge of the INT pulse. All interrupt events are stored in the respective register (except the register **WK_LVL_STAT**) until the register is read and cleared via SPI command. A second SPI read after reading out the respective status register is optional but recommended to verify that the interrupt event is not present anymore. The interrupt behavior is shown in **Figure 42** for class 1 interrupts. The behavior for class 2 is identical.

The INT pin is also used during SBC Init Mode to select the hardware configuration of the device. See **Chapter 5.1.1** for further information.

Interrupt Function

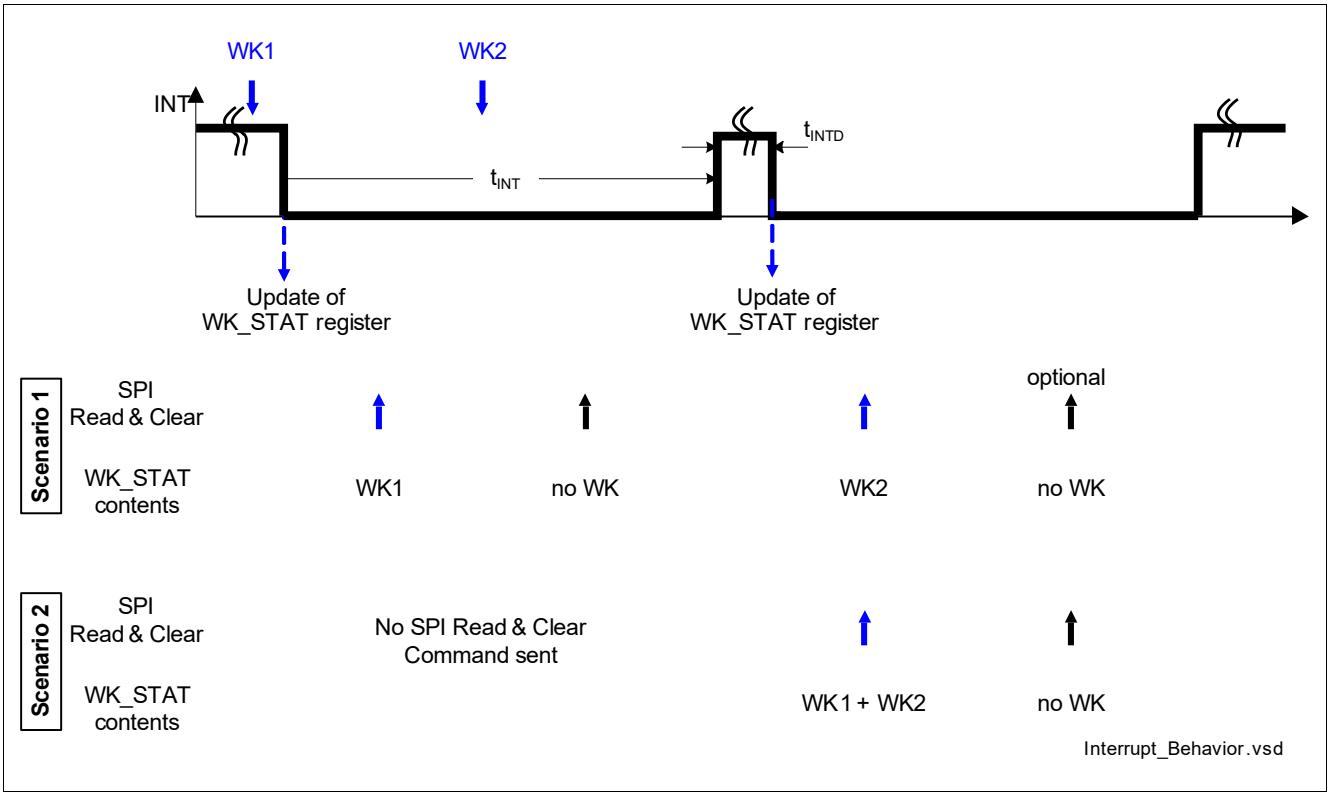

Figure 42 Interrupt Signalization Behavior

12.2 Electrical Characteristics

Table 29 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Interrupt Output; Pin INT							
INT High Output Voltage	$V_{INT,H}$	0.8 × V_{CC1}	–	–	V	1) I_{INT} = -1 mA; INT = OFF	P_13.2.1
INT Low Output Voltage	$V_{INT,L}$	–	–	0.2 × V_{CC1}	V	1) I_{INT} = 1 mA;INT = ON	P_13.2.2
INT Pulse Width	t_{INT}	80	100	120	µs	2)	P_13.2.3
INT Pulse Minimum Delay Time	t_{INTD}	80	100	120	µs	2) between consecutive pulses	P_13.2.4
Configuration Select; Pin INT							
Config Pull-down Resistance	R_{CFG}	180	250	350	kΩ	V_{INT} = 5 V	P_13.2.5
Config Select Filter Time	t_{CFG_F}	5	10	14	µs		P_13.2.6

1) Output Voltage Value also determines device configuration during SBC Init Mode

2) Not subject to production test, tolerance defined by internal oscillator tolerance.

13 Fail Outputs

13.1 Block and Functional Description

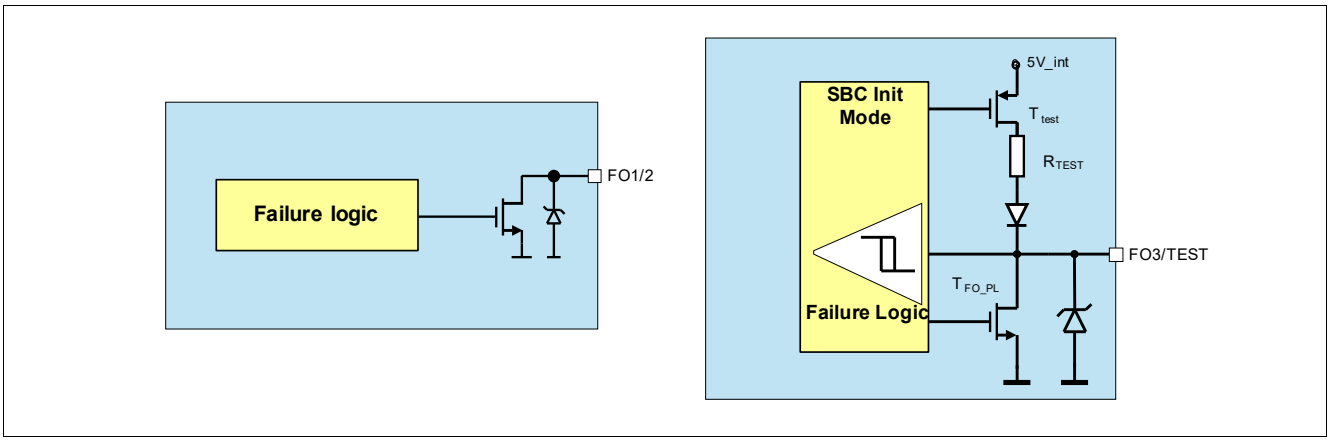

Figure 43 Simplified Fail Output Block Diagram for FO1/2 and for FO3/TEST

The fail outputs consist of a failure logic block and three open-drain outputs (FO1, FO2, FO3) with active-low signalization.

The fail outputs are activated due to following failure conditions:

- Watchdog trigger failure (For config 3&4 only after the 2nd watchdog trigger failure and for config 1&2 after 1st watchdog trigger failure)
- Thermal shutdown TSD2
- VCC1 short to GND
- VCC1 overvoltage (only if the SPI bit **VCC1_OV_RST** is set)
- After 4 consecutive VCC1 undervoltage event (see **Chapter 14.6** for details)

At the same time SBC Fail-Safe Mode is entered (exceptions are watchdog trigger failures depending on selected
configurations - see **Chapter 5.1.1**).

The fail output activation is signalled in the SPI bit **FAILURE** of the register **DEV_STAT**.

For testing purposes only the Fail Outputs can also be activated via SPI by setting the bit **FO_ON**. This bit is independent of the FO failure bits. In case that there is no failure condition, the FO outputs can also be turned off again via SPI, i.e. no successful watchdog trigger is needed.

The entry of SBC Fail-Safe Mode due to a watchdog failure can be configured as described in **Chapter 5.1.1**.

In order to deactivate the fail outputs in SBC Normal Mode the failure conditions must not be present anymore (e.g. TSD2, VCC1 short circuit, etc) and the bit **FAILURE** needs to be cleared via SPI command.
In case of a watchdog failure the correct procedure to deactivate the fail outputs is:

- a successful WD trigger, i.e. **WD_FAIL** must be cleared
- clearing of the **FAILURE** bit

WD_FAIL will also be cleared when going to SBC Sleep or SBC Fail-Safe Mode due to another failure (not a WD failure) or if the watchdog is disabled in SBC Stop Mode

Note: The Fail output pin is triggered for any of the above described failures. No FAILURE is caused for the 1st watchdog failure if selected for Config2.

The three fail outputs are activated simultaneously with following output functionalities:

- FO1: Static fail output
- FO2: 1.25Hz, 50% (typ.) duty cycle, e.g. to generate an indicator signal
- FO3: 100Hz PWM, 20% (typ.) duty cycle, e.g. to generate a dimmed rear light from a break light.

*Note: The duty cycle for FO3 can be configured via SPI option to 20%, 10%, 5% or 2.5%. Default value is 20%. See the register **FO_DC** for configuration.*

13.1.1 General Purpose I/O Functionality of FO2 and FO3 as Alternate Function

In case that FO2 and FO3 are not used in the application, those pins can also be configured with an alternate function as high-voltage (VSHS related) General Purpose I/O pins.

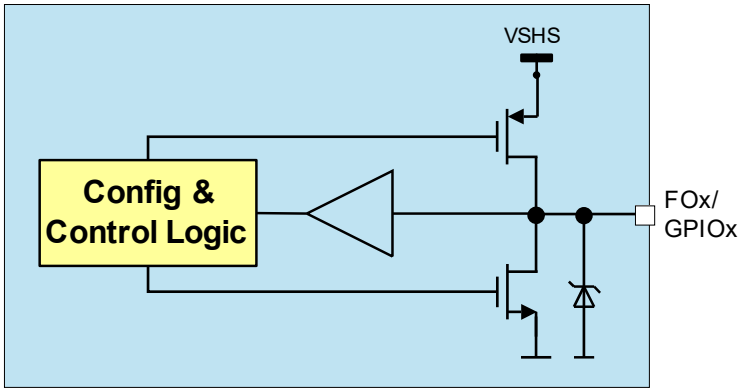

Figure 44 Simplified General Purpose I/O block diagram for FO2 and FO3/TEST

The pins are by default configured as FO pins. The configuration is done via the SPI register **GPIO_CTRL**. The alternate function can be:

- Wake Inputs: The detection threshold $V_{GPIOI,th}$ is similar as for the WK inputs. The wake-up detection behavior is the same as for WKx pins. Wake events are stored and reported in **WK_STAT_2**.
- Low-Side Switches: The switch is able to drive currents of up to 10mA (see also $V_{GPIOL,L1}$). It is self-protected with regards to current limitation. No other diagnosis is implemented.
- High-Side Switches: The switch is able to drive currents up to 10mA (see also $V_{GPIOH,H1}$). It is self-protected with regards to current limitation. No other diagnosis is implemented.
- If configured as GPIO then the respective level at the pin will be shown in **WK_LVL_STAT** in SBC Normal and Stop Mode. This is also the case if configured as LS/HS and can serve as a feedback about the respective state. GPIO2 is shared with the TEST level bit.

Table 30 describes the behavior of the FO/GPIO pins in their different configurations and SBC modes.

Fail Outputs

Table 30 Fail-Output and GPIO configuration behavior during the respective SBC Modes

FOx Configuration	SBC Normal Mode	SBC Stop Mode	SBC Sleep Mode	SBC Restart Mode	SBCFail-SafeMode
FOx (default)	configurable	fixed	fixed	active / fixed	active
OFF		OFF	OFF	OFF	OFF
Wake Input		wake capable	wake capable	wake capable	OFF
Low-Side		fixed	fixed	OFF	OFF
High-Side		fixed	fixed	OFF	OFF

Explanation of FO/GPIO states:

- configurable: settings can be changed in this SBC mode
- fixed: settings stay as configured in SBC Normal Mode
- active: FOx is activated due to a failure leading to SBC Restart or Fail-Safe Mode.

Restart Behavior:

The behavior during SBC Restart and Fail-Safe Mode as well as the transition to SBC Normal Mode is as follows:

- if configured as Wake Input: it will stay wake capable during SBC Restart Mode and OFF while in SBC Fail-Safe Mode. It will resume wake capability when leaving SBC Restart Mode (SPI register is not modified)
- if configured as Low-Side or High-Side: They will be disabled during SBC Restart and Fail-Safe Mode. After leaving SBC Restart Mode the previously configured function will be resumed (SPI register is not modified)
- if configured as FO and activated due to a failure: FO will stay activated during SBC Restart Mode and when entering SBC Normal Mode (SPI register is not modified)

Note: In order to avoid unintentional entry of SBC Development Mode care must be taken that the level of FO3/TEST is HIGH during device power up and SBC Init Mode.

Note: The FOx drivers are supplied via VS. However, the GPIO HS switches (FO2, FO3/TEST) are supplied by VSHS

13.2 Electrical Characteristics

Table 31 Electrical Characteristics

V_{SHS} = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Pin FO1							
FO1 low output voltage (active)	$V_{FO,L1}$	–	–	1.0	V	I_{FO} = 4mA	P_14.2.1
FO1 high output current (inactive)	$I_{FO,H}$	0	–	2	µA	V_{FO} = 28V	P_14.2.2
Pin FO2							
FO2 side indicator frequency	f_{FO2SI}	1.00	1.25	1.50	Hz	3)	P_14.2.3
FO2 side indicator duty cycle	d_{FO2SI}	45	50	55	%	3)	P_14.2.4
Pin FO3/TEST[2)]							
Pull-up Resistance at pin FO3/TEST	R_{TEST}	2.5	5	10	kΩ	V_{TEST} =0V; SBC Init Mode	P_14.2.5
TEST Input Filter Time	t_{TEST}	50	64	80	µs	3)	P_14.2.6
FO3 pulsed light frequency	f_{FO3PL}	80	100	120	Hz	3)	P_14.2.7
FO3 pulsed light duty cycle	d_{FO3PL}	16	20	24	%	3)4)default setting	P_14.2.8
Alternate FO2...3 Electrical Characteristics: GPIO							
GPIO low-side output voltage (active)	$V_{GPIOL,L1}$	–	–	1	V	I_{GPIO} = 10mA	P_14.2.9
GPIO low-side output voltage (active)	$V_{GPIOL,L2}$	–	–	5	mV	5)I_{GPIO} = 50µA	P_14.2.17
GPIO high-side output voltage (active)	$V_{GPIOH,H1}$	VSHS-1	–	–	V	I_{GPO} = -10mA	P_14.2.10
GPIO high-side output voltage (active)	$V_{GPIOH,H2}$	VSHS-5	–	–	mV	5)I_{GPO} = -50µA	P_14.2.18
GPIO input threshold voltage	$V_{GPIOI,th}$	1.5	2.5	3.5	V	6) hysteresis included	P_14.2.11
GPIO input threshold hysteresis	$V_{GPIOI,hys}$	100	400	700	mV	5)	P_14.2.12
GPIO low-side current limitation	$I_{GPIOL,max}$	10	–	30	mA	V_{GPIO} = 28V	P_14.2.13
GPIO high-side current limitation	$I_{GPIOH,max}$	-45	–	-10	mA	V_{GPIO} = 0V	P_14.2.14

Fail Outputs

1) The FOx drivers are supplied via VS. However, the GPIO HS switches (FO2, FO3/TEST) are supplied by VSHS
2) The external capacitance on this pin must be limited to less than 10nF to ensure proper detection of SBC Development Mode and SBC User Mode operation.
3) Not subject to production test, tolerance defined by internal oscillator tolerance.
4) The duty cyclic is adjustable via the SPI bits **FO_DC**.
5) Not subject to production test, specified by design.
6) Applies also for TEST voltage input level

14 Supervision Functions

14.1 Reset Function

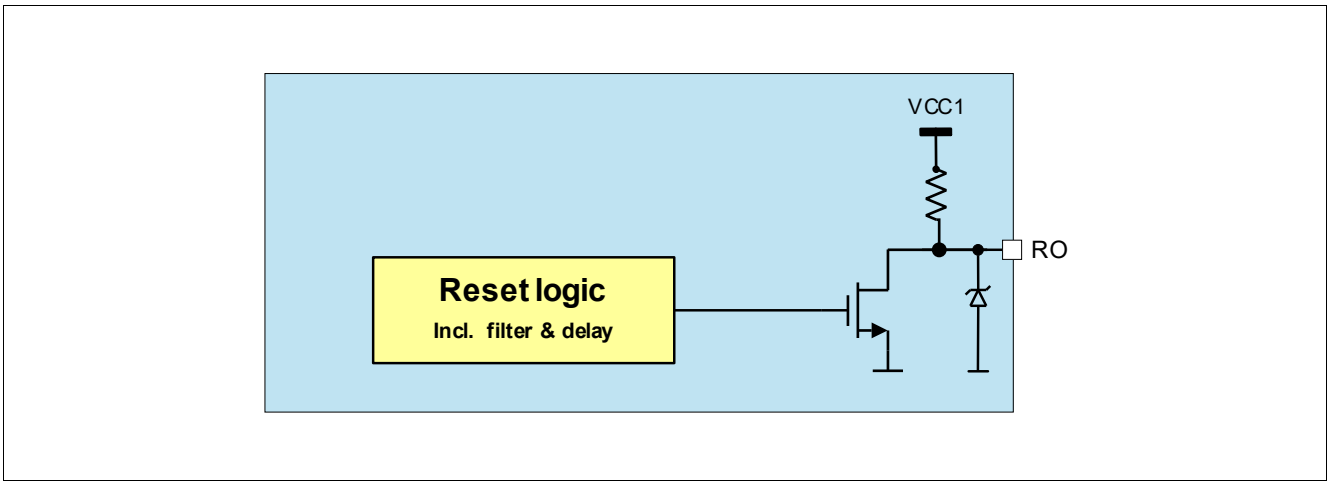

Figure 45 Reset Block Diagram

14.1.1 Reset Output Description

The reset output pin RO provides a reset information to the microcontroller, for example, in the event that the output voltage has fallen below the undervoltage threshold $V_{RT1/2/3/4}$. In case of a reset event, the reset output RO is pulled to low after the filter time **t_{RF}** and stays low as long as the reset event is present plus a reset delay time **t_{RD1}**. When connecting the SBC to battery voltage, the reset signal remains LOW initially. When the output voltage V_{cc1} has reached the reset default threshold $V_{RT1,r}$, the reset output RO is released to HIGH after the reset delay time t_{RD1}. A reset can also occur due to a watchdog trigger failure. The reset threshold can be adjusted via SPI, the default reset threshold is **$V_{RT1,f}$**. The RO pin has an integrated pull-up resistor. In case reset is triggered, it will be pulled low for **V_{cc1}** ≥ 1V and for VS ≥ **$V_{POR,f}$** (see also **Chapter 14.3**).

The timings for the RO triggering regarding VCC1 undervoltage and watchdog trigger is shown in **Figure 46**.

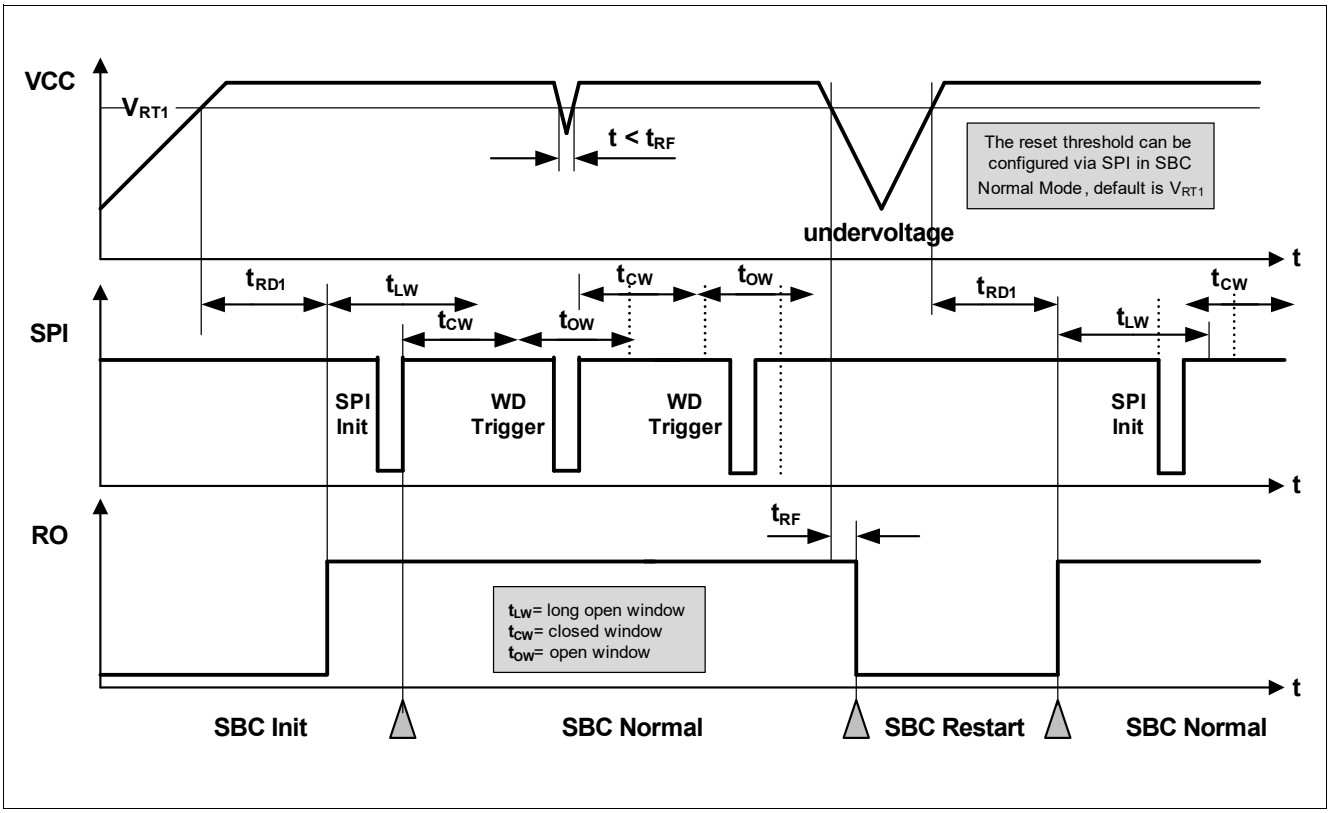

Figure 46 Reset Timing Diagram

14.1.2 Soft Reset Description

In SBC Normal and SBC Stop Mode, it is also possible to trigger a device internal reset via a SPI command in order to bring the SBC into a defined state in case of failures. In this case the microcontroller must send a SPI command and set the **MODE** bits to '11' in the **M_S_CTRL** register. As soon as this command becomes valid, the SBC is set back to SBC INIT Mode and all SPI registers are set to their default values (see SPI **Chapter 15.5** and **Chapter 15.6**).

Two different soft reset configurations are possible via the SPI bit **SOFT_ RESET_RO**:

- The reset output (RO) is triggered when the soft reset is executed (default setting, the same reset delay time **t_{RD1}** applies)
- The reset output (RO) is not triggered when the soft reset is executed

Note: The device must be in SBC Normal Mode or SBC Stop Mode when sending this command. Otherwise, the command will be ignored.

14.2 Watchdog Function

The watchdog is used to monitor the software execution of the microcontroller and to trigger a reset if the microcontroller stops serving the watchdog due to a lock up in the software.

Two different types of watchdog functions are implemented and can be selected via the bit **WD_WIN**:

- Time-Out Watchdog (default value)
- Window Watchdog

The respective watchdog functions can be selected and programmed in SBC Normal Mode. The configuration stays unchanged in SBC Stop Mode.

Please refer to **Table 32** to match the SBC Modes with the respective watchdog modes.

Table 32 Watchdog Functionality by SBC Modes

SBC Mode	Watchdog Mode	Remarks
INIT Mode	Starts with Long Open Window	Watchdog starts with Long Open Window after RO is released
Normal Mode	WD Programmable	Window Watchdog, Time-Out watchdog or switched OFF for SBC Stop Mode
Stop Mode	Watchdog is fixed or OFF	
Sleep Mode	OFF	SBC will start with Long Open Window when entering SBC Normal Mode.
Restart Mode	OFF	SBC will start with Long Open Window when entering SBC Normal Mode.

The watchdog timing is programmed via SPI command. As soon as the watchdog is programmed, the timer starts with the new setting and the watchdog must be served. The watchdog is triggered by sending a valid SPI-write command to the watchdog configuration register. The trigger SPI command is executed when the Chip Select input (CSN) becomes HIGH.

When coming from SBC Init, SBC Restart Mode or in certain cases from SBC Stop Mode, the watchdog timer is always started with a long open window. The long open window (t_{LW} = 200ms) allows the microcontroller to run its initialization sequences and then to trigger the watchdog via SPI.

The watchdog timer period can be selected via the watchdog timing bit field (**WD_TIMER**) and is in the range of 10 ms to 1000 ms. This setting is valid for both watchdog types.

The following watchdog timer periods are available:

- WD Setting 1: 10ms
- WD Setting 2: 20ms
- WD Setting 3: 50ms
- WD Setting 4: 100ms
- WD Setting 5: 200ms
- WD Setting 6: 500ms
- WD Setting 7: 1000ms

In case of a watchdog reset, SBC Restart or SBC Fail-Safe Mode is entered according to the configuration and the SPI bits **WD_FAIL** are set. Once the RO goes HIGH again the watchdog immediately starts with a long open window the SBC enters automatically SBC Normal Mode.

In SBC Development Mode the watchdog is OFF and therefore no reset and interrupt are generated due to a watchdog failure.

Depending on the configuration, the **WD_FAIL** bits will be set after a watchdog trigger failure as follows:

- In case an incorrect WD trigger is received (triggering in the closed watchdog window or when the watchdog counter expires without a valid trigger) then the **WD_FAIL** bits will be increased (showing the number of incorrect WD triggers)
- For config 2: the bits can have the maximum value of ‘01’
- For config 1, 3 and 4: the bits can have the maximum value of ‘10’

The **WD_FAIL** bits are cleared automatically when following conditions apply:

- After a successful watchdog trigger
- When the watchdog is OFF: in SBC Stop Mode after successfully disabling it, in SBC Sleep Mode, or in SBC Fail-Safe Mode (except for a watchdog failure)

14.2.1 Time-Out Watchdog

The time-out watchdog is an easier and less secure watchdog than a window watchdog as the watchdog trigger can be done at any time within the configured watchdog timer period.

A correct watchdog service immediately results in starting a new watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the safe trigger area as defined in **Figure 47**.

If the time-out watchdog period elapses, a watchdog reset is created by setting the reset output RO low and the SBC switches to SBC Restart or SBC Fail-Safe Mode.

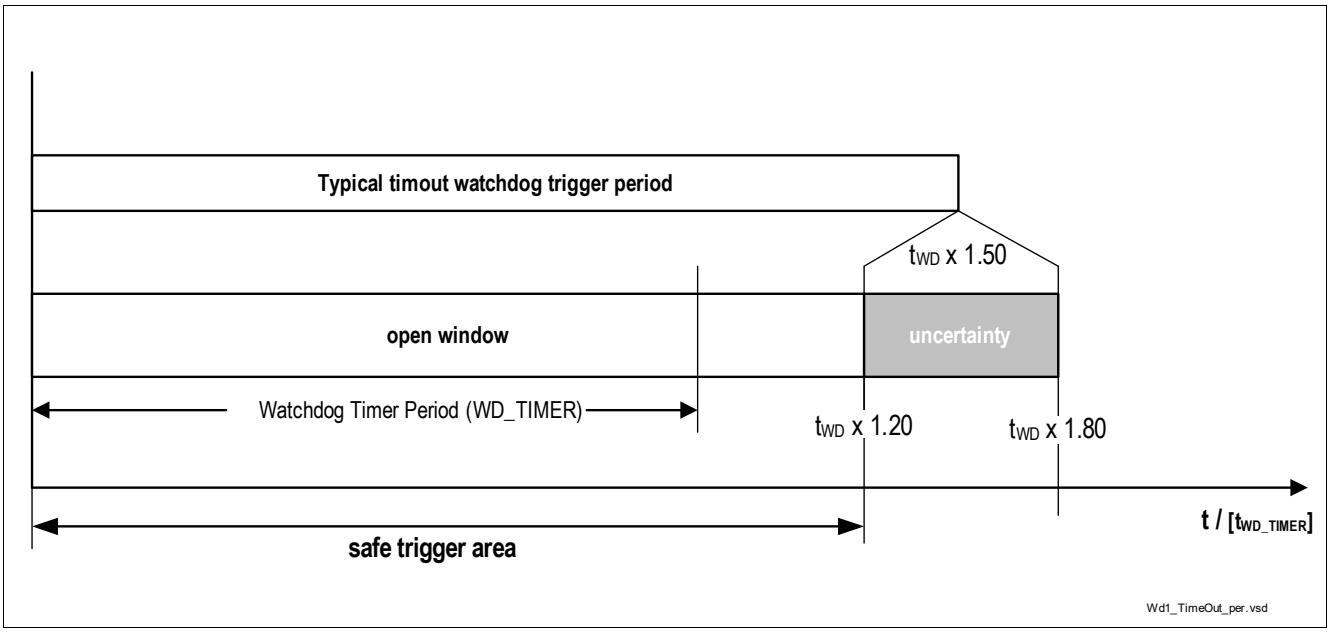

Figure 47 Time-out Watchdog Definition

14.2.2 Window Watchdog

Compared to the time-out watchdog the characteristic of the window watchdog is that the watchdog timer period is divided between an closed and an open window. The watchdog must be triggered within the open window.

A correct watchdog trigger results in starting the window watchdog period by a closed window followed by an open window.

The watchdog timer period is at the same time the typical trigger time and defines the middle of the open window. Taking the oscillator tolerances into account leads to a safe trigger area of:

t_{WD} x 0.72 < safe trigger area < t_{WD} x 1.20.

The typical closed window is defined to a width of 60% of the selected window watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the timings as defined in **Figure 48**.

A correct watchdog service immediately results in starting the next closed window.

Should the trigger signal meet the closed window or should the watchdog timer period elapse, then a watchdog reset is created by setting the reset output RO low and the SBC switches to SBC Restart or SBC Fail-Safe Mode.

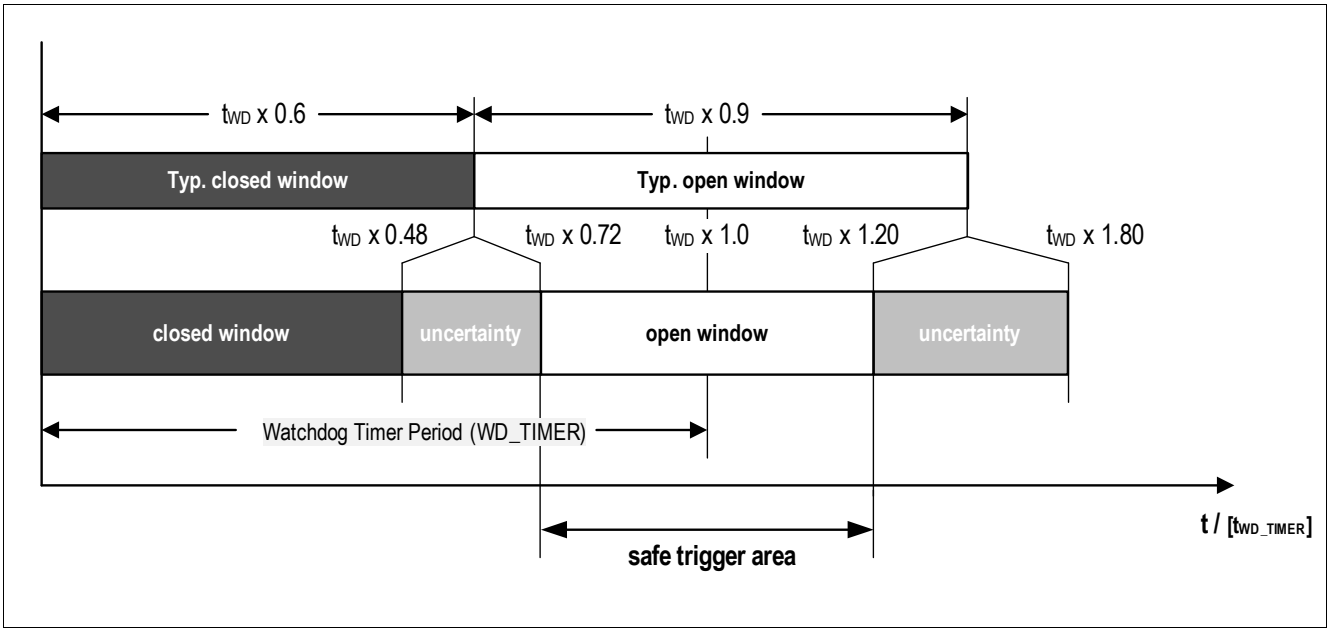

Figure 48 Window Watchdog Definition

14.2.3 Watchdog Setting Check Sum

A check sum bit is part of the SPI commend to trigger the watchdog and to set the watchdog setting.

The sum of the 8 data bits in the register WWD_CTRL needs to have even parity (see **Equation (14.1)**). This is realized by either setting the bit **CHECKSUM** to 0 or 1. If the check sum is wrong, then the SPI command is ignored, i.e. the watchdog is not triggered or the settings are not changed and the bit SPI_FAIL is set.

The checksum is calculated by taking all 8 data bits into account. The written value of the reserved bit 3 of the WWD_CTRL register is considered (even if read as '0' in the SPI output) for checksum calculation, i.e. if a 1 is written on the reserved bit position, then a 1 will be used in the checksum calculation.

(14.1)

$$CHKSUM = Bit15 \oplus \ldots \oplus Bit8$$

14.2.4 Watchdog during SBC Stop Mode

The watchdog can be disabled for SBC Stop Mode in SBC Normal Mode. For safety reasons, there is a special sequence to be followed in order to disable the watchdog as described in **Figure 49**. Two different SPI bits (**WD_STM_ EN_0**, **WD_STM_ EN_1**) in the registers **WK_CTRL_1** and **WD_CTRL** need to be set.

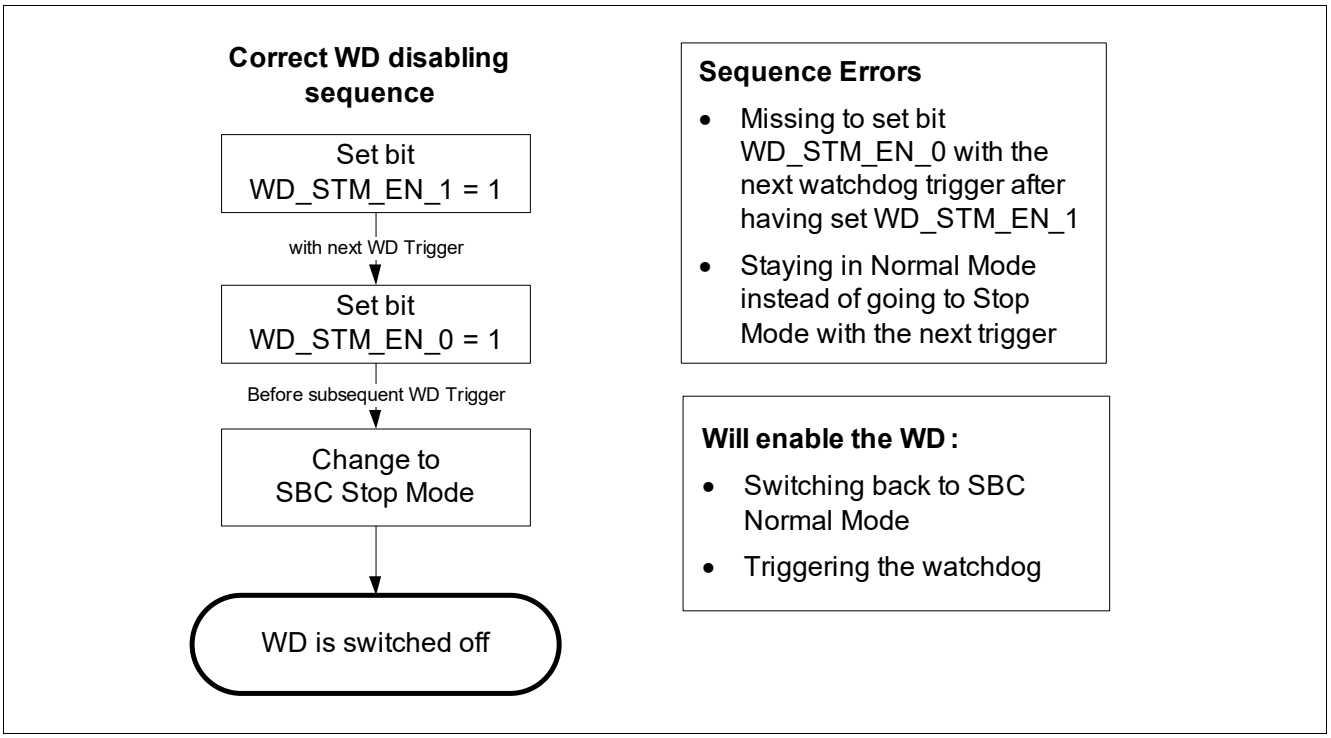

Figure 49 Watchdog disabling sequence in SBC Stop Mode

If a sequence error occurs, then the bit **WD_STM_ EN_1** will be cleared and the sequence has to be started again.

The watchdog can be enabled by triggering the watchdog in SBC Stop Mode or by switching back to SBC Normal Mode via SPI command. In both cases the watchdog will start with a long open window and the bits WD_STM_EN_1 and WD_STM_ EN_0 are cleared. After the long open window the watchdog has to be served as configured in the **WD_CTRL** register.

*Note: The bit **WD_STM_ EN_0** will be cleared automatically when the sequence is started and it was 1 before.*

14.2.5 Watchdog Start in SBC Stop Mode due to Bus Wake

In SBC Stop Mode the Watchdog can be disabled. In addition a feature is available which will start the watchdog with any BUS wake (CAN) during SBC Stop Mode. The feature is enabled by setting the bit **WD_EN_WK_BUS** = 1
(= default value after POR). The bit can only be changed in SBC Normal Mode and needs to be programmed before starting the watchdog disable sequence.

A wake on CAN will generate an interrupt and the RXD pin for CAN is pulled to low. By these signals the microcontroller is informed that the watchdog is startedwith a long open window. After the long open window the watchdog has to be served as configured in the **WD_CTRL** register.

To disable the watchdog again, the SBC needs to be switched to Normal Mode and the sequence needs to be sent again.

14.3 VS Power On Reset

At power up of the device, the VS Power on Reset is detected when VS > **$V_{POR,r}$** and the SPI bit **POR** is set to indicate that all SPI registers are set to POR default settings. VCC1 is starting up and the reset output will be kept LOW and will only be released once VCC1 has crossed **$V_{RT1,r}$** and after **t_{RD1}** has elapsed.
In case VS < **$V_{POR,f}$**, an device internal reset will be generated and the SBC is switched OFF and will restart in INIT mode at the next VS rising. This is shown in **Figure 50**.

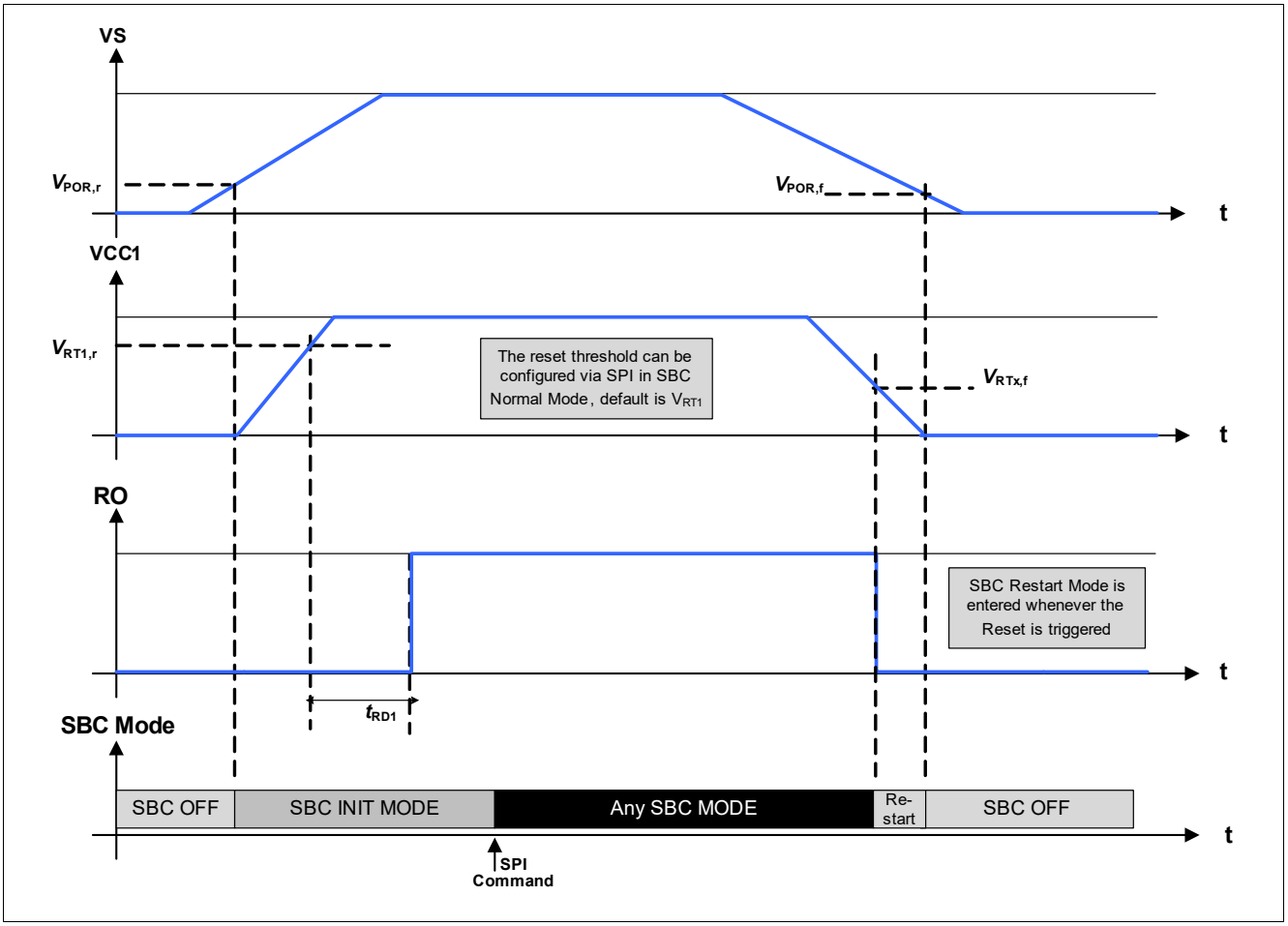

Figure 50 Ramp up / down example of Supply Voltage

14.4 Undervoltage VS and VSHS

If the supply voltage VS reaches the undervoltage threshold **$V_{S,UV}$** then the SBC does the following measures:

- SPI bit **VS_UV** is set. No other error bits are set. The bit can be cleared once the condition is not present anymore,
- VCC3 is disabled (see **Chapter 8.2**) unless the control bit **VCC3_VS_ UV_OFF** is set
- The VCC1 short circuit protection becomes inactive (see **Chapter 14.7**). However, the thermal protection of the device remains active.

If the undervoltage threshold is exceeded (VS rising) then functions will be automatically enabled again.

If the supply voltage VSHS passes below the undervoltage threshold (**$V_{SHS,UVD}$**) the SBC does the following measures:

- HS1...4 are acting accordingly to the SPI setting (see **Chapter 9**)
- see **Chapter 13.2.7**
- SPI bit **VSHS_UV** is set. No other error bits are set. The bit can be cleared once the condition is not present anymore,
- VCC1, VCC2, WKx and CAN are not affected by VSHS undervoltage

14.5 Overvoltage VSHS

If the supply voltage VSHS reaches the overvoltage threshold (**$V_{SHS,OVD}$**) the SBC triggers the following measures:

- HS1...4 are acting accordingly to the SPI setting (see **Chapter 9**)
- SPI bit **VSHS_OV** is set. No other error bits are set. The bit can be cleared once the condition is not present anymore,
- VCC1, VCC2, VCC3, WKx and CAN are not affected by VS overvoltage

14.6 VCC1 Over-/ Undervoltage and Undervoltage Prewarning

14.6.1 VCC1 Undervoltage and Undervoltage Prewarning

A first-level voltage detection threshold is implemented as a prewarning for the microcontroller. The prewarning event is signaled with the bit **VCC1_ WARN**. No other actions are taken.

As described in **Chapter 14.1** and **Figure 51**, a reset will be triggered (RO pulled ‘low’) when the V_{CC1} output voltage falls below the selected undervoltage threshold (V_{RTx}). The bit **VCC1_UV** is set and the SBC will enter SBC Restart Mode.

*Note: The **VCC1_ WARN** or **VCC1_UV** bits are not set in Sleep Mode as V_{CC1} = 0V in this case*

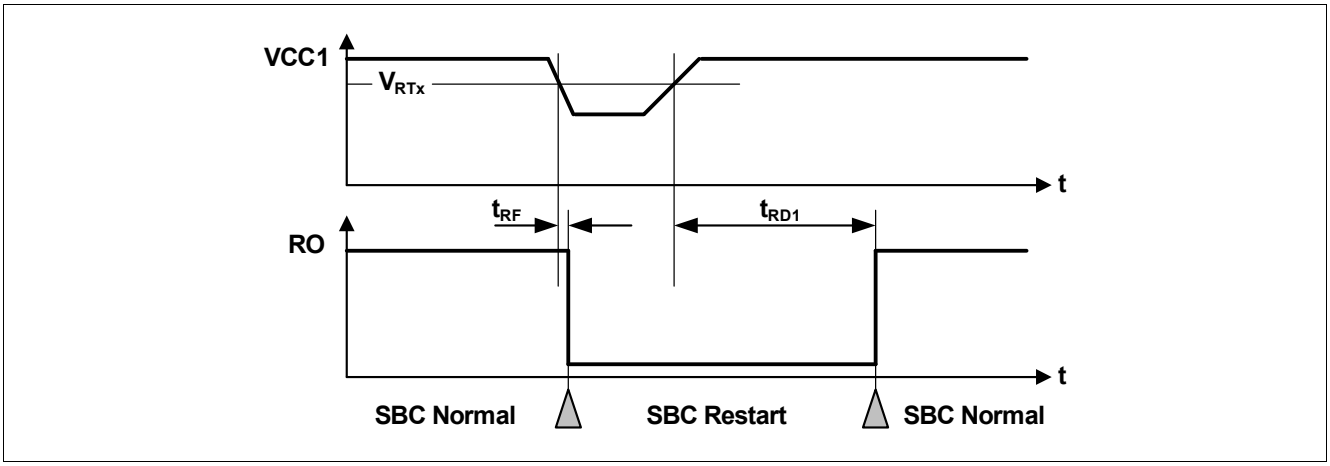

Figure 51 VCC1 Undervoltage Timing Diagram

An additional safety mechanism is implemented to avoid repetitive VCC1 undervoltage resets due to high dynamic loads on VCC1:

- A counter is increased for every consecutive VCC1 undervoltage event (regardless on the selected reset threshold),
- The counter is active in SBC Init-, Normal-, and Stop Mode,
- For VS < **$V_{S,UV}$** the counter will be stopped in SBC Normal Mode (i.e. the VS UV comparator is always enabled in SBC Normal Mode),
- A 4th consecutive VCC1 undervoltage event will lead to SBC Fail-Safe Mode entry and to setting the bit **VCC1_UV _FS**
- This counter is cleared:
  - when SBC Fail-Safe Mode is entered,
  - when the bit **VCC1_UV** is cleared,
  - when a Soft Reset is triggered.

Note: It is recommended to clear the VCC1_UV bit once it was set and detected.

14.6.2 VCC1 Overvoltage

For fail-safe reasons a configurable VCC1 overvoltage detection feature is implemented for SBC Init- and Normal Mode.

In case the **$V_{CC1,OV,r}$** threshold is crossed, the SBC triggers following measures depending on the configuration:

- The bit **VCC1_ OV** is always set;
- If the bit **VCC1_OV_RST** is set and **CFGP** = '1', then SBC Restart Mode is entered. The FOx outputs are activated. After the reset delay time (**t_{RD1}**), the SBC Restart Mode is left and SBC Normal Mode is resumed even if the VCC1 overvoltage event is still present (see also **Figure 52**). The **VCC1_OV_RST** bit is cleared automatically;
- If the bit **VCC1_OV_RST** is set and **CFGP** = '0', then SBC Fail-Safe Mode is entered and FOx outputs are activated.

*Note: Before entering SBC Stop Mode the bit **VCC1_OV_RST** must be set to '0' to avoid unintentional SBC Restart or Fail-Safe Mode entry. The status bit **VCC1_ OV** could be set unintentionally. The reason is*

that external noise could be coupled into the VCC1 supply line. Especially, in case the VCC1 output current in SBC STOP Mode is below the active peak threshold ($I_{VCC1,Ipeak}$).

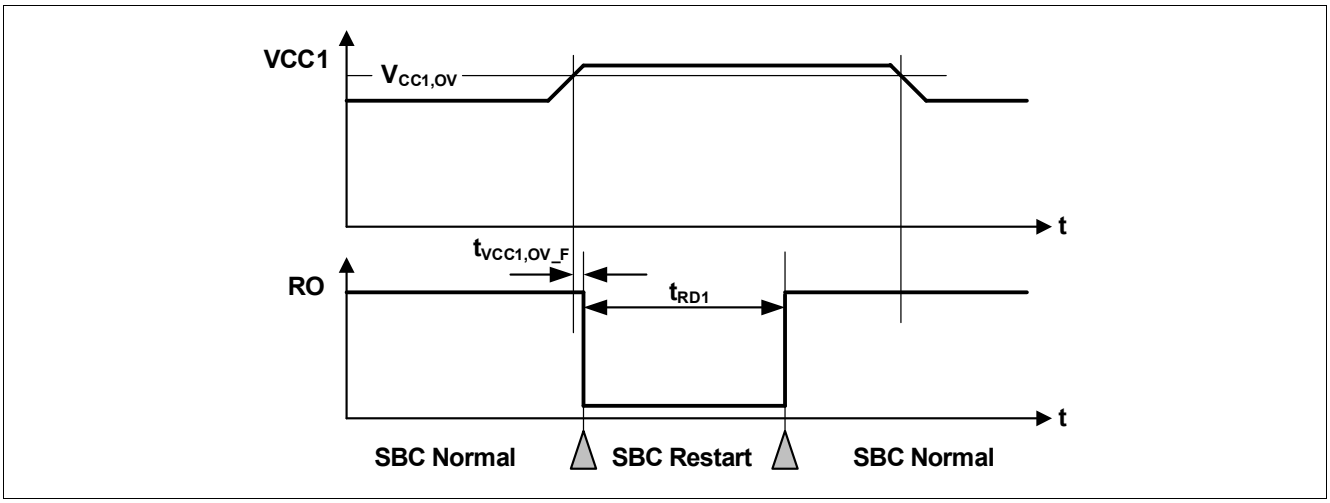

Figure 52 VCC1 Overvoltage Timing Diagram

14.7 VCC1 Short Circuit and VCC3 Diagnostics

The short circuit protection feature for V_{CC1} is implemented as follows (VS needs to be higher than **$V_{S,UV}$**):

- If VCC1 is not above the V_{RTx} within **$t_{VCC1,SC}$** after device power up or after waking from SBC Sleep Mode then the SPI bit **VCC1_SC** bit is set, VCC1 is turned OFF, the FOx pins are enabled, **FAILURE** is set and SBC Fail-Safe Mode is entered. The SBC can be activated again via wake on CAN, WKx.
- The same behavior applies, if V_{CC1} falls below V_{RTx} for longer than **$t_{VCC1,SC}$**.

VCC3 diagnosis features are implemented as follows:

- Load Sharing: The external PNP is disabled when VS < **$V_{S,UV}$** if VCC3_VS_ UV_OFF = 0 or when in SBC Stop Mode if **VCC3_LS_ STP_ON** = '0'. All other diagnostic features are disabled because they are provided via VCC1.
- Stand-alone configuration: The external PNP is disabled when VCC3 < **$V_{S,UV}$** if VCC3_VS_ UV_OFF = 0. The overcurrent limitation is signalled via the bit **VCC3_OC** according to the selected shunt resistor, VCC3 undervoltage is signalled via the bit **VCC3_UV** and the regulator is disabled due to VS undervoltage when **$V_{S,UV}$** is reached.

*Note: Neither **VCC1_SC** nor **VCC3_UV** flags are set during power up of V_{CC1} or turn on of V_{CC3} respectively.*

14.8 VCC2 Undervoltage and VCAN Undervoltage

An undervoltage warning is implemented for VCC2 and VCAN as follows:

- V_{CC2} undervoltage Detection: In case V_{CC2} will drop below the $V_{CC2,UV,f}$ threshold, then the SPI bit **VCC2_UV** is set and can be only cleared via SPI.
- V_{CAN} undervoltage Detection: In case the voltage on V_{CAN} will drop below the V_{CAN_UV} threshold, then the SPI bit **VCAN_UV** is set and can be only cleared via SPI.

Note: The VCC2_UV flag is not set during turn-on or turn-off of $V_{CC2.}$

14.9 Thermal Protection

Three independent and different thermal protection features are implemented in the SBC according to the system impact:

- Individual thermal shutdown of specific blocks
- Temperature prewarning of main microcontroller supply VCC1
- SBC thermal shutdown due to VCC1 overtemperature

14.9.1 Individual Thermal Shutdown

As a first-level protection measure the output stages VCC2, CAN, and HSx are independently switched OFF if the respective block reaches the temperature threshold T_{jTSD1}. Then the **TSD1** bit is set. This bit can only be cleared via SPI once the overtemperature is not present anymore. Independent of the SBC Mode the thermal shutdown protection is only active if the respective block is ON.

The respective modules behave as follows:

- VCC2: Is switched to OFF and the control bits **VCC2_ON** are cleared. The status bit **VCC2_OT** is set. Once the overtemperature condition is not present anymore, then VCC2 has to be configured again by SPI.
- VCC3 as a stand-alone regulator: Is switched to OFF and the control bits **VCC3_ON** are cleared. The status bit **VCC3_OT** is set. Once the overtemperature condition is not present anymore VCC3 has to be configured again by SPI. It is recommended to clear the **VCC3_OT** bit before enabling the regulator again.
- VCC3 in load sharing configuration: in case of overtemperature at VCC3 the bit **VCC3_OT** is set and VCC3 is switched off. The regulator will be switched on again automatically once the overtemperature event is not present anymore. Also in this case it is recommended to clear the **VCC3_OT** bit right away.
- CAN: The transmitter is disabled and stays in CAN Normal Mode acting like CAN Receive only mode. The status bits **CAN_FAIL** = '01' are set. Once the overtemperature condition is not present anymore, then the CAN transmitter is automatically switched on.
- HSx: If one or more HSx switches reach the TSD1 threshold, then all HSx switches are turned OFF and the control bits for HSx are cleared (see registers **HS_CTRL1** and **HS_CTRL2**). The status bits HSx_OC_OT are set (see register **HS_OC_OT_STAT**). Once the overtemperature condition is not present anymore, then HSx has to be configured again by SPI.

Note: The diagnosis bits are not cleared automatically and have to be cleared via SPI once the overtemperature condition is not present anymore.

14.9.2 Temperature Prewarning

As a next level of thermal protection a temperature prewarning is implemented if the main supply VCC1 reaches the thermal prewarning temperature threshold **T_{jPW}**. Then the status bit **TPW** is set. This bit can only be cleared via SPI once the overtemperature is not present anymore. Independent of the SBC Mode the thermal prewarning is only active if the VCC1 is ON.

14.9.3 SBC Thermal Shutdown

As a highest level of thermal protection a temperature shutdown of the SBC is implemented if the main supply VCC1 reaches the thermal shutdown temperature threshold **T_{jTSD2}**. Once a TSD2 event is detected SBC Fail-Safe Mode is entered for **t_{TSD2}** to allow the device to cool down. After this time has expired, the SBC will automatically change via SBC Restart Mode to SBC Normal Mode (see also **Chapter 5.1.6**).

When a TSD2 event is detected, then the status bit **TSD2** is set. This bit can only be cleared via SPI in SBC Normal Mode once the overtemperature is not present anymore. Independent of the SBC Mode the thermal shutdown is only active if VCC1 is ON.

14.10 Electrical Characteristics

Table 33 Electrical Specification

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VCC1 Monitoring; VCC1 = 5.0V Version							
Undervoltage Prewarning Threshold Voltage PW,f	$V_{PW,f}$	4.6	4.7	4.85	V	VCC1 falling, SPI bit is set	P_15.10.1
Undervoltage Prewarning Threshold Voltage PW,r	$V_{PW,r}$	4.65	4.80	4.90	V	VCC1 rising	P_15.10.2
Reset Threshold Voltage RT1,f	$V_{RT1,f}$	4.5	4.6	4.75	V	default setting; VCC1 falling	P_15.10.3
Reset Threshold Voltage RT1,r	$V_{RT1,r}$	4.6	4.7	4.85	V	default setting; VCC1 rising	P_15.10.4
Reset Threshold Voltage RT2,f	$V_{RT2,f}$	3.75	3.9	4.05	V	VCC1 falling	P_15.10.5
Reset Threshold Voltage RT2,r	$V_{RT2,r}$	3.85	4.0	4.15	V	VCC1 rising	P_15.10.6
Reset Threshold Voltage RT3,f	$V_{RT3,f}$	3.15	3.3	3.45	V	VS ≥ 4V; VCC1 falling	P_15.10.7
Reset Threshold Voltage RT3,r	$V_{RT3,r}$	3.25	3.4	3.55	V	VS ≥ 4V; VCC1 rising	P_15.10.8
Reset Threshold Voltage RT4,f	$V_{RT4,f}$	2.4	2.65	2.8	V	VS ≥ 4V; VCC1 falling	P_15.10.9
Reset Threshold Voltage RT4,r	$V_{RT4,r}$	2.5	2.75	2.9	V	VS ≥ 4V; VCC1 rising	P_15.10.10
Reset Threshold Hysteresis	$V_{RT,hys}$	50	100	200	mV	–	P_15.10.11
VCC1 Overvoltage Detection Threshold Voltage	$V_{CC1,OV,r}$	5.3	–	5.6	V	[1)]rising VCC1	P_15.10.50
VCC1 Overvoltage Detection Threshold Voltage	$V_{CC1,OV,f}$	5.2	–	5.5	V	falling VCC1	P_15.10.72
VCC1 OV Detection Filter Time	t_{VCC1,OV_F}	5	10	14	us	[3)]	P_15.10.51
VCC1 Short to GND Filter Time	$t_{VCC1,SC}$	3.2	4	4.8	ms	[3)]	P_15.10.12
Reset Generator; Pin RO							
Reset Low Output Voltage	$V_{RO,L}$	–	0.2	0.4	V	I_{RO} = 1 mA for V_{CC1} ≥ 1 V & $V_S \geq V_{POR,f}$	P_15.10.14
Reset High Output Voltage	$V_{RO,H}$	0.8 x V_{CC1}	–	V_{CC1} + 0.3 V	V	I_{RO} = -20 µA	P_15.10.15

Table 33 Electrical Specification (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset Pull-up Resistor	R_{RO}	10	20	40	kΩ	V_{RO} = 0 V	P_15.10.16
Reset Filter Time	t_{RF}	4	10	26	µs	[3] $V_{CC1} < V_{RT1x}$ to RO = L see also **Chapter 14.3**	P_15.10.17
Reset Delay Time	t_{RD1}	1.5	2	2.5	ms	[2] [3]	P_15.10.18
VCC2 Monitoring							
VCC2 Undervoltage Threshold Voltage (falling)	$V_{CC2,UV,f}$	4.5	–	4.75	V	VCC2 falling	P_15.10.19
VCC2 Undervoltage Threshold Voltage (rising)	$V_{CC2,UV,r}$	4.6	–	4.9	V	VCC2 rising	P_15.10.77
VCC2 Undervoltage detection hysteresis	$V_{CC2,UV, hys}$	20	100	250	mV	–	P_15.10.20
VCC3 Monitoring							
VCC3 Undervoltage Detection	$V_{CC3,UV}$	4.0	4.25	4.5	V	**VCC3_ V_CFG**=0 hysteresis included	P_15.10.21
VCC3 Undervoltage Detection	$V_{CC3,UV}$	2.65	2.85	3.00	V	3.3V option or **VCC3_ V_CFG**=1 hysteresis included	P_15.10.47
VCC3 Undervoltage detection hysteresis	$V_{CC3,UV, hys}$	20	100	250	mV	–	P_15.10.22
VCAN Monitoring							
CAN Supply undervoltage detection threshold	V_{CAN_UV}	4.45	–	4.85	V	CAN Normal Mode, hysteresis included;	P_15.10.23
Watchdog Generator							
Long Open Window	t_{LW}	160	200	240	ms	[3]	P_15.10.24
Internal Oscillator	f_{CLKSBC}	0.8	1.0	1.2	MHz	–	P_15.10.25
Minimum Waiting time during SBC Fail-Safe Mode							
Min. waiting time Fail-Safe	$t_{FS,min}$	80	100	120	ms	[3][4]	P_15.10.75
Power-on Reset, Over- / Undervoltage Protection							
VS Power on reset rising	$V_{POR,r}$	–		4.5	V	VS increasing	P_15.10.26
VS Power on reset falling	$V_{POR,f}$	–		3	V	VS decreasing	P_15.10.27

Table 33 Electrical Specification (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VS Undervoltage Detection Threshold	$V_{S,UV}$	5.3	–	6.0	V	Supply UV threshold for VCC3 and VCC1 SC detection; hysteresis included	P_15.10.13
VSHS Overvoltage Detection Threshold	$V_{SHS,OVD}$	20		22	V	Supply OV supervision for HSx; hysteresis included	P_15.10.28
VSHS Overvoltage Detection hysteresis	$V_{SHS,OVD,hys}$	100	500	–	mV	5)	P_15.10.29
VSHS Undervoltage Detection Threshold	$V_{SHS,UVD}$	4.8		5.5	V	Supply UV supervision for HSx, and HS of GPIOx; hysteresis included	P_15.10.30
VSHS Undervoltage Detection hysteresis	$V_{SHS,UVD,hys}$	50	200	350	mV	5)	P_15.10.31
Overtemperature Shutdown[5]							
Thermal Prewarning Temperature	T_{jPW}	125	145	165	°C		P_15.10.32
Thermal Shutdown TSD1	T_{jTSD1}	165	185	200	°C		P_15.10.33
Thermal Shutdown TSD2	T_{jTSD2}	165	185	200	°C		P_15.10.34
Thermal Shutdown hysteresis	$T_{jTSD,hys}$	5	15	25	°C		P_15.10.68
Deactivation time after thermal shutdown TSD2	t_{TSD2}	0.8	1	1.2	s	3)	P_15.10.35

1) It is ensured that the threshold $V_{CC1,OV,r}$ is always higher than the highest regulated V_{CC1} output voltage $V_{CC1,out42}$.

2) The reset delay time will start when VCC1 crosses above the selected Vrtx threshold

3) Not subject to production test, tolerance defined by internal oscillator tolerance.

4) This time applies for all failure entries except a device thermal shutdown (TSD2 has a typ. 1s waiting time t_{TSD2})

5) Not subject to production test, specified by design.

15 Serial Peripheral Interface

15.1 SPI Block Description

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input CLK provided by the microcontroller. The output word appears synchronously at the data output SDO (see **Figure 53**).

The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), LOW active. After the CSN input returns from LOW to HIGH, the word that has been read is interpreted according to the content. The SDO output switches to tristate status (high impedance) at this point, thereby releasing the SDO bus for other use.The state of SDI is shifted into the input register with every falling edge on CLK. The state of SDO is shifted out of the output register after every rising edge on CLK. The SPI of the SBC is not daisy chain capable.

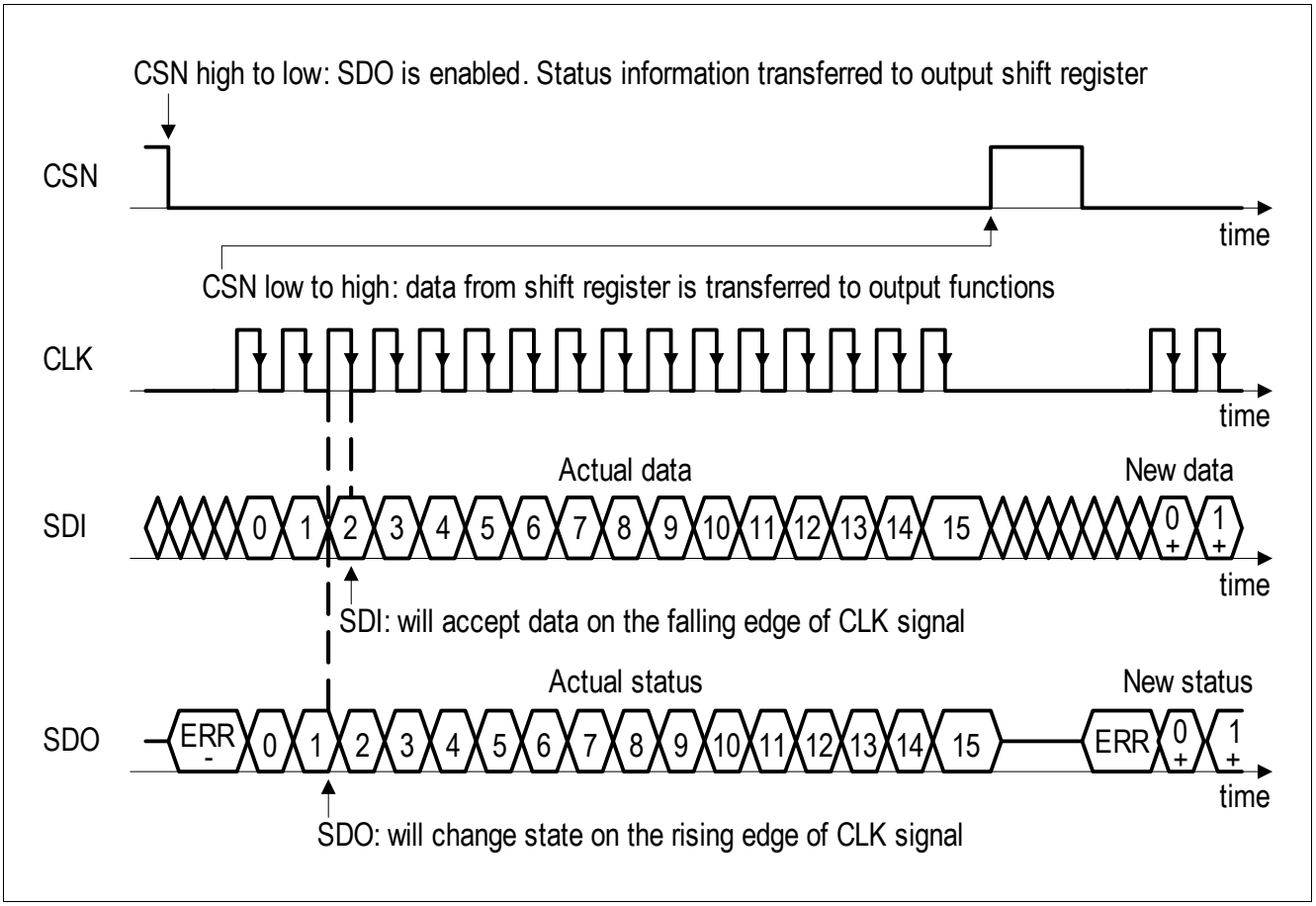

Figure 53 SPI Data Transfer Timing (note the reversed order of LSB and MSB shown in this figure compared to the register description)

15.2 Failure Signalization in the SPI Data Output

When the microcontroller sends a wrong SPI command to the SBC, the SBC ignores the information. Wrong SPI commands are either invalid SBC mode commands or commands which are prohibited by the state machine to avoid undesired device or system states (see below). In this case the diagnosis bit '**SPI_FAIL**' is set and the SPI Write command is ignored (mostly no partial interpretation). This bit can be only reset by actively clearing it via a SPI command.

Invalid SPI Commands leading to SPI_FAIL are listed below:

- Illegal state transitions: Going from SBC Stop to SBC Sleep Mode. In this case the SBC enters in addition the SBC Restart Mode;
  Trying to go to SBC Stop or SBC Sleep mode from SBC Init Mode. In this case SBC Normal Mode is entered;
- Uneven parity in the data bit of the **WD_CTRL** register. In this case the watchdog trigger is ignored or the new watchdog settings are ignored respectively;
- In SBC Stop Mode: attempting to change any SPI settings, e.g. changing the watchdog configuration, PWM settings and HS configuration settings during SBC Stop Mode, etc.;
  the SPI command is ignored in this case;
  only WD trigger, returning to Normal Mode, triggering a SBC Soft Reset, and Read & Clear status registers commands are valid SPI commands in SBC Stop Mode;
- When entering SBC Stop Mode and **WK_STAT_1** and **WK_STAT_2** are not cleared; **SPI_FAIL** will not be set but the INT pin will be triggered;
- Changing from SBC Stop to Normal Mode and changing the other bits of the **M_S_CTRL** register. The other modifications will be ignored;
- SBC Sleep Mode: attempt to go to Sleep Mode when all bits in the **BUS_CTRL_1** and **WK_CTRL_2** registers are cleared. In this case the **SPI_FAIL** bit is set and the SBC enters Restart Mode.
  Even though the Sleep Mode command is not entered in this case, the rest of the command (e.g modifying VCC2 or VCC3) is executed and the values stay unchanged during SBC Restart Mode;
  Note: At least one wake source must be activated in order to avoid a deadlock situation in SBC Sleep Mode, i.e. the SBC would not be able to wake up anymore.
  If the only wake source is a timer and the timer is OFF then the SBC will wake immediately from Sleep Mode and enter Restart Mode;
  No failure handling is done for the attempt to go to SBC STOP Mode when all bits in the registers **BUS_CTRL_1** and **WK_CTRL_2** are cleared because the microcontroller can leave this mode via SPI;
- If VCC3 load sharing **VCC3_LS** is enabled and the microcontroller tries to clear the bit, then the rest of the command executed but **VCC3_LS** will remain set;
- Attempt to enter SBC Sleep Mode if WK_MEAS is set to '1' and only WK1_EN or WK2_EN are set as wake sources. Also in this case the **SPI_FAIL** bit is set and the SBC enters Restart Mode;
- Setting a longer or equal on-time than the timer period of the respective timer;
- SDI stuck at HIGH or LOW, e.g. SDI received all '0' or all '1';

Note: There is no SPI fail information for unused addresses.

Signalization of the ERR Flag (high active) in the SPI Data Output (see Figure 53):

The ERR flag presents an additional diagnosis possibility for the SPI communication. The ERR flag is being set for following conditions:

- in case the number of received SPI clocks is not 0 or 16,
- in case RO is LOW and SPI frames are being sent at the same time.

Note: In order to read the SPI ERR flag properly, CLK must be low when CSN is triggered, i.e. the ERR bit is not valid if the CLK is high on a falling edge of CSN

The number of received SPI clocks is not 0 or 16:

The number of received input clocks is supervised to be 0- or 16 clock cycles and the input word is discarded in case of a mismatch (0 clock cycle to enable ERR signalization). The error logic also recognizes if CLK was high during CSN edges. Both errors - 0 bit and 16 bit CLK mismatch or CLK high during CSN edges - are flagged in the following SPI output by a “HIGH” at the data output (SDO pin, bit ERR) before the first rising edge of the clock is received. The complete SPI command is ignored in this case.

RO is LOW and SPI frames are being sent at the same time:

The ERR flag will be set when the RO pin is triggered (during SBC Restart) and SPI frames are being sent to the SBC at the same time. The behavior of the ERR flag will be signalized at the next SPI command for below conditions:

- if the command begins when RO is HIGH and it ends when RO is LOW,
- if a SPI command will be sent while RO is LOW,
- If a SPI command begins when RO is LOW and it ends when RO is HIGH.

and the SDO output will behave as follows:

- always when RO is LOW then SDO will be HIGH,
- when a SPI command begins with RO is LOW and ends when RO is HIGH, then the SDO should be ignored because wrong data will be sent.

Note: It is possible to quickly check for the ERR flag without sending any data bits. i.e. only the CSN is pulled low and SDO is observed - no SPI Clocks are sent in this case

Note: The ERR flag could also be set after the SBC has entered SBC Fail-Safe Mode because the SPI communication is stopped immediately.

15.3 SPI Programming

For the TLE9261-3BQX, 7 bits are used or the address selection (BIT6...0). Bit 7 is used to decide between Read Only and Read & Clear for the status bits, and between Write and Read Only for configuration bits. For the actual configuration and status information, 8 data bits (BIT15...8) are used.

Writing, clearing and reading is done byte wise. The SPI status bits are not cleared automatically and must be cleared by the microcontroller, e.g. if the TSD2 was set due to overtemperature. The configuration bits will be partially automatically cleared by the SBC - please refer to the individual registers description for detailed information. During SBC Restart Mode the SPI communication is ignored by the SBC, i.e. it is not interpreted.

There are two types of SPI registers:

- Control registers: Those are the registers to configure the SBC, e.g. SBC mode, watchdog trigger, etc
- Status registers: Those are the registers where the status of the SBC is signalled, e.g. wake events, warnings, failures, etc.

For the status registers, the requested information is given in the same SPI command in DO.
For the control registers, also the status of the respective byte is shown in the same SPI command. However, if the setting is changed this is only shown with the next SPI command (it is only valid after CSN high) of the same register.

The SBC status information from the SPI status registers, is transmitted in a compressed way with each SPI response on SDO in the so called Status Information Field register (see also **Figure 54**). The purpose of this register is to quickly signal the information to the microcontroller if there was a change in one of the SPI status registers. In this way, the microcontroller does not need to read constantly all the SPI status registers but only those registers, which were changed.

Each bit in the Status Information Field represents a SPI status register (see **Table 34**). As soon as one bit is set in one of the status registers, then the respective bit in the Status Information Field register will be set. The register **WK_LVL_STAT** is not included in the status Information field. This is listed in **Table 34**.

For Example if bit 0 in the Status Information Field is set to 1, one or more bits of the register 100 0001 (**SUP_STAT_1**) is set to 1. Then this register needs to be read in a second SPI command. The bit in the Status Information Field will be set to 0 when all bits in the register 100 0001 are set back to 0.

Table 34 Status Information Field

Bit in Status Information Field	CorrespondingAddress Bit	Status Register Description
0	100 0001	SUP_STAT_1: Supply Status -VSHS fail, VCCx fail, POR
1	100 0010	THERM_STAT: Thermal Protection Status
2	100 0011	DEV_STAT: Device Status - Mode before Wake, WD Fail, SPI Fail, Failure
3	100 0100	BUS_STAT: Bus Failure Status: CAN;
4	100 0110	WK_STAT_1, WK_STAT_2: Wake Source Status; Status bit is set as combinational OR of both registers
5	100 0000	SUP_STAT_2: VCC1_WARN/OV, VCC3 Status
6	101 0100	HS_OC_OT_STAT: High-Side Over Load Status
7	101 0101	HS_OL_STAT: High-Side Open Load Status

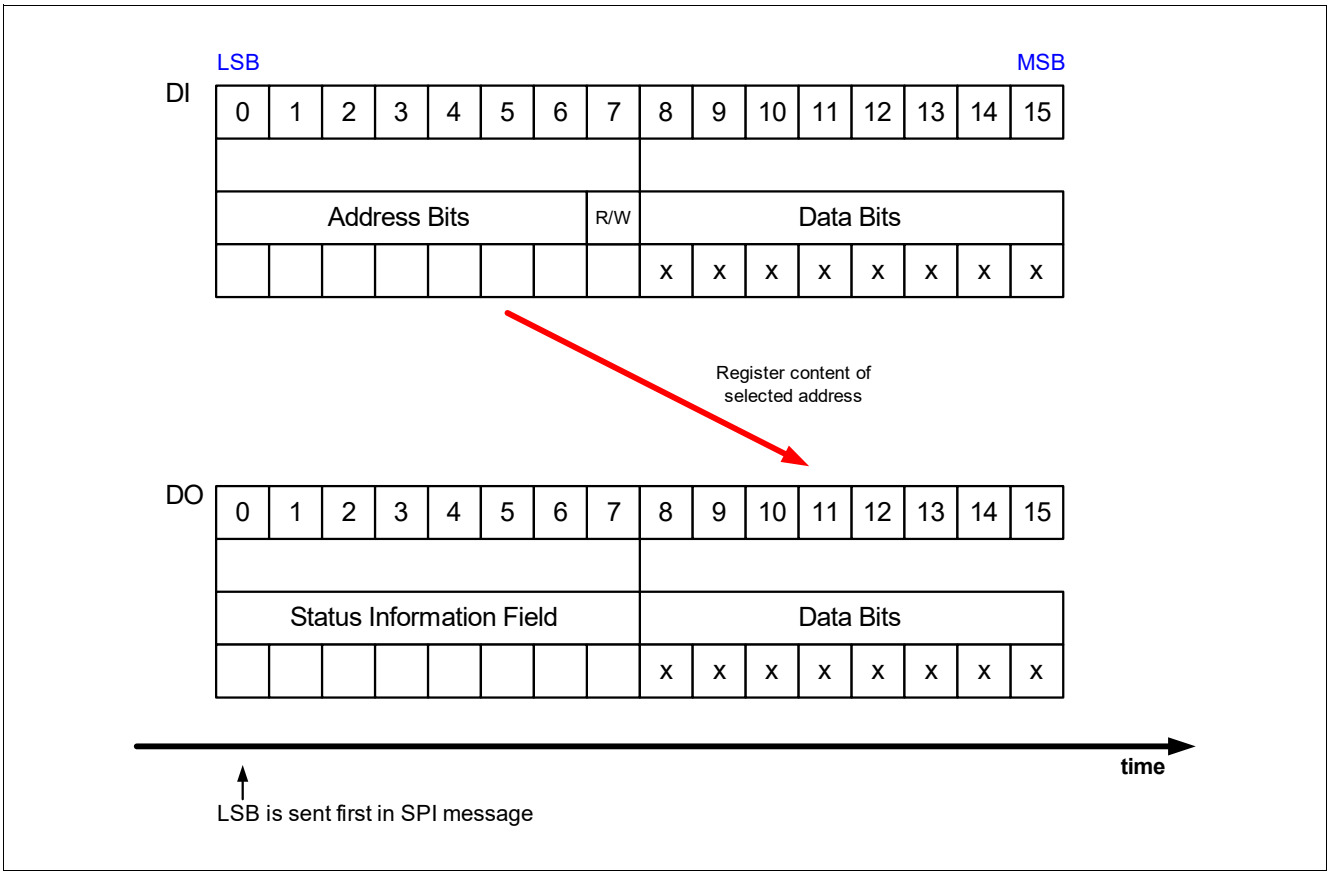

Figure 54 SPI Operation Mode

15.4 SPI Bit Mapping

The following figures show the mapping of the registers and the SPI bits of the respective registers.

The Control Registers ‘000 0000’ to ‘001 1110’ are Read/Write Register. Depending on bit 7 the bits are only read (setting bit 7 to ‘0’) or also written (setting bit 7 to ‘1’). The new setting of the bit after write can be seen with a new read / write command.

The registers ‘100 0000’ to ‘111 1110’ are Status Registers and can be read or read with clearing the bit (if possible) depending on bit 7. To clear a Data Byte of one of the Status Registers bit 7 must be set to 1. The registers **WK_LVL_STAT**, and **FAM_PROD_STAT**, **SWK_OSC_CAL_H_STAT**, **SWK_OSC_CAL_L_STAT**, **SWK_STAT**, **SWK_ECNT_STAT**, **SWK_CDR_STAT1**, **SWK_CDR_STAT2** are an exception as they show the actual voltage level at the respective WK pin (LOW/HIGH), or a fixed family/ product ID respectively and can thus not be cleared. It is recommended for proper diagnosis to clear respective status bits for wake events or failure. However, in general it is possible to enable drivers without clearing the respective failure flags.

When changing to a different SBC Mode, certain configurations bits will be cleared automatically or modified:

- The SBC Mode bits are updated to the actual status, e.g. when returning to Normal Mode
- When changing to a low-power mode (Stop/Sleep), the diagnosis bits of the switches and transceivers are not cleared. FOx will stay activated if it was triggered before.
- When changing to SBC Stop Mode, the CAN control bits will not be modified.
- When changing to SBC Sleep Mode, the CAN control bits will be modified if they were not OFF or wake capable before.
- HSx, VCC2 and VCC3 will stay on when going to Sleep-/Stop Mode (configuration can only be done in Normal Mode). Diagnosis is active (OC, OL, OT). In case of a failure the switch is turned off and no wake-up is issued
- The configuration bits for HSx and VCC2 in stand-alone configuration are cleared in SBC Restart Mode. FOx will stay activated if it was triggered before. Depending on the respective configuration, CAN transceivers will be either OFF, woken or still wake capable.

*Note: The detailed behavior of the respective SPI bits and control functions is described in **Chapter 15.5**, **Chapter 15.6**.and in the respective module chapter. The bit type be marked as ‘rwh’ in case the SBC will modify respective control bits.*

	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0		
	8 Data Bits [bits 8...15] for Configuration & Status Information								Reg. Type	7 Address Bits [bits 0...6] for Register Selection								
Control Registers	M_S_CTRL								rw	0	0	0	0	0	0	1		
	HW_CTRL								rw	0	0	0	0	0	1	0		
	WD_CTRL								rw	0	0	0	0	0	1	1		
	BUS_CTRL_1								rw	0	0	0	0	1	0	0		
	BUS_CTRL_2								rw	0	0	0	0	1	0	1		
	WK_CTRL_1								rw	0	0	0	0	1	1	0		
	WK_CTRL_2								rw	0	0	0	0	1	1	1		
	WK_PUPD_CTRL								rw	0	0	0	1	0	0	0		
	WK_FLT_CTRL								rw	0	0	0	1	0	0	1		
	TIMER1_CTRL								rw	0	0	0	1	1	0	0		
	TIMER2_CTRL								rw	0	0	0	1	1	0	1		
	SW_SD_CTRL								rw	0	0	1	0	0	0	0		
	HS_CTRL_1								rw	0	0	1	0	1	0	0		
	HS_CTRL_2								rw	0	0	1	0	1	0	1		
	GPIO_CTRL								rw	0	0	1	0	1	1	1		
	PWM1_CTRL								rw	0	0	1	1	0	0	0		
	PWM2_CTRL								rw	0	0	1	1	0	0	1		
	PWM_FREQ_CTRL								rw	0	0	1	1	1	0	0		
	SYS_STAT_CTRL								rw	0	0	1	1	1	1	0		
Selective Wake Control Registers	SWK_CTRL								rw	0	1	0	0	0	0	0		
	SWK_BTL1_CTRL								rw	0	1	0	0	0	0	1		
	SWK_BTL2_CTRL								rw	0	1	0	0	0	1	0		
	SWK_ID3_CTRL								rw	0	1	0	0	0	1	1		
	SWK_ID2_CTRL								rw	0	1	0	0	1	0	0		
	SWK_ID1_CTRL								rw	0	1	0	0	1	0	1		
	SWK_ID0_CTRL								rw	0	1	0	0	1	1	0		
	SWK_MASK_ID3_CTRL								rw	0	1	0	0	1	1	1		
	SWK_MASK_ID2_CTRL								rw	0	1	0	1	0	0	0		
	SWK_MASK_ID1_CTRL								rw	0	1	0	1	0	0	1		
	SWK_MASK_ID0_CTRL								rw	0	1	0	1	0	1	0		
	SWK_DLC_CTRL								rw	0	1	0	1	0	1	1		
	SWK_DATA7_CTRL								rw	0	1	0	1	1	0	0		
	SWK_DATA6_CTRL								rw	0	1	0	1	1	0	1		
	SWK_DATA5_CTRL								rw	0	1	0	1	1	1	0		
	SWK_DATA4_CTRL								rw	0	1	0	1	1	1	1		
	SWK_DATA3_CTRL								rw	0	1	1	0	0	0	0		
	SWK_DATA2_CTRL								rw	0	1	1	0	0	0	1		
	SWK_DATA1_CTRL								rw	0	1	1	0	0	1	0		
	SWK_DATA0_CTRL								rw	0	1	1	0	0	1	1		
	SWK_CAN_FD_CTRL								rw	0	1	1	0	1	0	0		
	SWK_OSC_TRIM_CTRL								rw	0	1	1	1	0	0	0		
	SWK_OPT_CTRL								rw	0	1	1	1	0	0	1		
	SWK_OSC_CAL_H_STAT								r	0	1	1	1	0	1	0		
	SWK_OSC_CAL_L_STAT								r	0	1	1	1	0	1	1		
	SWK_CDR_CTRL1								rw	0	1	1	1	1	0	0		
	SWK_CDR_CTRL2								rw	0	1	1	1	1	0	1		
	SWK_CDR_LIMIT_H_CTRL								rw	0	1	1	1	1	1	0		
	SWK_CDR_LIMIT_L_CTRL								rw	0	1	1	1	1	1	1		
Status Registers	SUP_STAT_2								rc	1	0	0	0	0	0	0	5	Status Information Field Bit
	SUP_STAT_1								rc	1	0	0	0	0	0	1	0	
	THERM_STAT								rc	1	0	0	0	0	1	0	1	
	DEV_STAT								rc	1	0	0	0	0	1	1	2	
	BUS_STAT_1								rc	1	0	0	0	1	0	0	3	
	WK_STAT_1								rc	1	0	0	0	1	1	0	4	
	WK_STAT_2								rc	1	0	0	0	1	1	1	4	
	WK_LVL_STAT								r	1	0	0	1	0	0	0	-	
	HS_OC_OT_STAT								rc	1	0	1	0	1	0	0	6	
	HS_OL_STAT								rc	1	0	1	0	1	0	1	7	
	SWK_STAT								r	1	1	1	0	0	0	0		
	SWK_ECNT_STAT								r	1	1	1	0	0	0	1		
	SWK_CDR_STAT1								r	1	1	1	0	0	1	0		
	SWK_CDR_STAT2								r	1	1	1	0	0	1	1		
	FAM_PROD_STAT								r	1	1	1	1	1	1	0		

Figure 55 SPI Register Mapping including Selective Wake

Register Short Name	15	14	13	12	11	10	9	8	7	6...0
	Data Bit 15...8								Access Mode	Address A6...A0
	D7	D6	D5	D4	D3	D2	D1	D0		
CONTROL REGISTERS										
M_S_CTRL	MODE_1	MODE_0	VCC3_ON	VCC2_ON_1	VCC2_ON_0	VCC1_OV_RST	VCC1_RT_1	VCC1_RT_0	read/write	0000001
HW_CTRL	VCC3_V_CFG	SOFT_RESET_RO	FO_ON	VCC3_VS_UV_OFF	VCC3_LS	reserved	VCC3_LS_STP_ON	CFG	read/write	0000010
WD_CTRL	CHECKSUM	WD_STM_EN_0	WD_WIN	WD_EN_WK_BUS	reserved	WD_TIMER_2	WD_TIMER_1	WD_TIMER_0	read/write	0000011
BUS_CTRL_1	reserved	reserved	reserved	reserved	reserved	CAN_2	CAN_1	CAN_0	read/write	0000100
BUS_CTRL_2	reserved	reserved	I_PEAK_TH	reserved	reserved	reserved	reserved	reserved	read/write	0000101
WK_CTRL_1	TIMER2_WK_EN	TIMER1_WK_EN	reserved	reserved	reserved	WD_STM_EN_1	reserved	reserved	read/write	0000110
WK_CTRL_2	INT_GLOBAL	reserved	WK_MEAS	reserved	reserved	WK3_EN	WK2_EN	WK1_EN	read/write	0000111
WK_PUPD_CTRL	reserved	reserved	WK3_PUPD_1	WK3_PUPD_0	WK2_PUPD_1	WK2_PUPD_0	WK1_PUPD_1	WK1_PUPD_0	read/write	0001000
WK_FLT_CTRL	reserved	reserved	WK3_FLT_1	WK3_FLT_0	WK2_FLT_1	WK2_FLT_0	WK1_FLT_1	WK1_FLT_0	read/write	0001001
TIMER1_CTRL	reserved	TIMER1_ON_2	TIMER1_ON_1	TIMER1_ON_0	reserved	TIMER1_PER_2	TIMER1_PER_1	TIMER1_PER_0	read/write	0001100
TIMER2_CTRL	reserved	TIMER2_ON_2	TIMER2_ON_1	TIMER2_ON_0	reserved	TIMER2_PER_2	TIMER2_PER_1	TIMER2_PER_0	read/write	0001101
SW_SD_CTRL	reserved	HS_OV_SD_EN	HS_UV_SD_EN	HS_OV_UV_REC	reserved	reserved	reserved	reserved	read/write	0010000
HS_CTRL_1	reserved	HS2_2	HS2_1	HS2_0	reserved	HS1_2	HS1_1	HS1_0	read/write	0010100
HS_CTRL_2	reserved	HS4_2	HS4_1	HS4_0	reserved	HS3_2	HS3_1	HS3_0	read/write	0010101
GPIO_CTRL	FO_DC_1	FO_DC_0	GPIO2_2	GPIO2_1	GPIO2_0	GPIO1_2	GPIO1_1	GPIO1_0	read/write	0010111
PWM1_CTRL	PWM1_DC_7	PWM1_DC_6	PWM1_DC_5	PWM1_DC_4	PWM1_DC_3	PWM1_DC_2	PWM1_DC_1	PWM1_DC_0	read/write	0011000
PWM2_CTRL	PWM2_DC_7	PWM2_DC_6	PWM2_DC_5	PWM2_DC_4	PWM2_DC_3	PWM2_DC_2	PWM2_DC_1	PWM2_DC_0	read/write	0011001
PWM_FREQ_CTRL	reserved	reserved	reserved	reserved	reserved	PWM2_FREQ_0	reserved	PWM1_FREQ_0	read/write	0011100
SYS_STAT_CTRL	SYS_STAT_7	SYS_STAT_6	SYS_STAT_5	SYS_STAT_4	SYS_STAT_3	SYS_STAT_2	SYS_STAT_1	SYS_STAT_0	read/write	0011110
SELECTIVE WAKE REGISTERS										
SWK_CTRL	OSC_CAL	TRIM_EN_1	TRIM_EN_0	CANTO_MASK	reserved	reserved	reserved	CFG_VAL	read/write	0100000
SWK_BTL1_CTRL	TBIT_7	TBIT_6	TBIT_5	TBIT_4	TBIT_3	TBIT_2	TBIT_1	TBIT_0	read/write	0100001
SWK_BTL2_CTRL	reserved	reserved	SP_5	SP_4	SP_3	SP_2	SP_1	SP_0	read/write	0100010
SWK_ID3_CTRL	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	read/write	0100011
SWK_ID2_CTRL	ID20	ID19	ID18	ID17	ID16	ID15	ID14	ID13	read/write	0100100
SWK_ID1_CTRL	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	read/write	0100101
SWK_ID0_CTRL	reserved	ID4	ID3	ID2	ID1	ID0	RTR	IDE	read/write	0100110
SWK_MASK_ID3_CTRL	MASK_ID28	MASK_ID27	MASK_ID26	MASK_ID25	MASK_ID24	MASK_ID23	MASK_ID22	MASK_ID21	read/write	0100111
SWK_MASK_ID2_CTRL	MASK_ID20	MASK_ID19	MASK_ID18	MASK_ID17	MASK_ID16	MASK_ID15	MASK_ID14	MASK_ID13	read/write	0101000
SWK_MASK_ID1_CTRL	MASK_ID12	MASK_ID11	MASK_ID10	MASK_ID9	MASK_ID8	MASK_ID7	MASK_ID6	MASK_ID5	read/write	0101001
SWK_MASK_ID0_CTRL	reserved	MASK_ID4	MASK_ID3	MASK_ID2	MASK_ID1	MASK_ID0	reserved	reserved	read/write	0101010
SWK_DLC_CTRL	reserved	reserved	reserved	reserved	DLC_3	DLC_2	DLC_1	DLC_0	read/write	0101011
SWK_DATA7_CTRL	DATA7_7	DATA7_6	DATA7_5	DATA7_4	DATA7_3	DATA7_2	DATA7_1	DATA7_0	read/write	0101100
SWK_DATA6_CTRL	DATA6_7	DATA6_6	DATA6_5	DATA6_4	DATA6_3	DATA6_2	DATA6_1	DATA6_0	read/write	0101101
SWK_DATA5_CTRL	DATA5_7	DATA5_6	DATA5_5	DATA5_4	DATA5_3	DATA5_2	DATA5_1	DATA5_0	read/write	0101110
SWK_DATA4_CTRL	DATA4_7	DATA4_6	DATA4_5	DATA4_4	DATA4_3	DATA4_2	DATA4_1	DATA4_0	read/write	0101111
SWK_DATA3_CTRL	DATA3_7	DATA3_6	DATA3_5	DATA3_4	DATA3_3	DATA3_2	DATA3_1	DATA3_0	read/write	0110000
SWK_DATA2_CTRL	DATA2_7	DATA2_6	DATA2_5	DATA2_4	DATA2_3	DATA2_2	DATA2_1	DATA2_0	read/write	0110001
SWK_DATA1_CTRL	DATA1_7	DATA1_6	DATA1_5	DATA1_4	DATA1_3	DATA1_2	DATA1_1	DATA1_0	read/write	0110010
SWK_DATA0_CTRL	DATA0_7	DATA0_6	DATA0_5	DATA0_4	DATA0_3	DATA0_2	DATA0_1	DATA0_0	read/write	0110011
SWK_CAN_FD_CTRL	reserved	reserved	DIS_ERR_CNT	RX_FILT_BYP	FD_FILTER_2	FD_FILTER_1	FD_FILTER_0	CAN_FD_EN	read/write	0110100
SELECTIVE WAKE TRIM &CONFIGURATIONS REGISTERS										
SWK_OSC_TRIM_CTRL	TRIM_OSC_7	TRIM_OSC_6	TRIM_OSC_5	TRIM_OSC_4	TRIM_OSC_3	TRIM_OSC_2	TRIM_OSC_1	TRIM_OSC_0	read/write	0111000
SWK_OPT_CTRL	RX_WK_SEL	reserved	reserved	TRIM_OSC_12	TRIM_OSC_11	TRIM_OSC_10	TRIM_OSC_9	TRIM_OSC_8	read/write	0111001
SWK_OSC_CAL_H_STAT	OSC_CAL_H_7	OSC_CAL_H_6	OSC_CAL_H_5	OSC_CAL_H_4	OSC_CAL_H_3	OSC_CAL_H_2	OSC_CAL_H_1	OSC_CAL_H_0	read	0111010
SWK_OSC_CAL_L_STAT	OSC_CAL_L_7	OSC_CAL_L_6	OSC_CAL_L_5	OSC_CAL_L_4	OSC_CAL_L_3	OSC_CAL_L_2	OSC_CAL_L_1	OSC_CAL_L_0	read	0111011
SWK_CDR_CTRL1	reserved	reserved	reserved	reserved	SELFILT_1	SELFILT_0	reserved	CDR_EN	read/write	0111100
SWK_CDR_CTRL2	reserved	reserved	reserved	reserved	reserved	reserved	SEL_OSC_CLK_1	SEL_OSC_CLK_0	read/write	0111101
SWK_CDR_LIMIT_HIGH	CDR_LIM_H_7	CDR_LIM_H_6	CDR_LIM_H_5	CDR_LIM_H_4	CDR_LIM_H_3	CDR_LIM_H_2	CDR_LIM_H_1	CDR_LIM_H_0	read/write	0111110
SWK_CDR_LIMIT_LOW	CDR_LIM_L_7	CDR_LIM_L_6	CDR_LIM_L_5	CDR_LIM_L_4	CDR_LIM_L_3	CDR_LIM_L_2	CDR_LIM_L_1	CDR_LIM_L_0	read/write	0111111
STATUS REGISTERS										
SUP_STAT_2	reserved	VS_UV	reserved	VCC3_OC	VCC3_UV	VCC3_OT	VCC1_OV	VCC1_WARN	read/clear	1000000
SUP_STAT_1	POR	VSHS_UV	VSHS_OV	VCC2_OT	VCC2_UV	VCC1_SC	VCC1_UV_FS	VCC1_UV	read/clear	1000001
THERM_STAT	reserved	reserved	reserved	reserved	reserved	TSD2	TSD1	TPW	read/clear	1000010
DEV_STAT	DEV_STAT_1	DEV_STAT_0	reserved	reserved	WD_FAIL_1	WD_FAIL_0	SPI_FAIL	FAILURE	read/clear	1000011
BUS_STAT_1	reserved	reserved	reserved	CANTO	SYSERR	CAN_FAIL_1	CAN_FAIL_0	VCAN_UV	read/clear	1000100
BUS_STAT_2	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved	read/clear	1000101
WK_STAT_1	reserved	reserved	CAN_WU	TIMER_WU	reserved	WK3_WU	WK2_WU	WK1_WU	read/clear	1000110
WK_STAT_2	reserved	reserved	GPIO2_WU	GPIO1_WU	reserved	reserved	reserved	reserved	read/clear	1000111
WK_LVL_STAT	SBC_DEV_LVL	CFGP	GPIO2_LVL	GPIO1_LVL	reserved	WK3_LVL	WK2_LVL	WK1_LVL	read	1001000
HS_OC_OT_STAT	reserved	reserved	reserved	reserved	HS4_OC_OT	HS3_OC_OT	HS2_OC_OT	HS1_OC_OT	read/clear	1010100
HS_OL_STAT	reserved	reserved			HS4_OL	HS3_OL	HS2_OL	HS1_OL	read/clear	1010101
SELECTIVE WAKE STATUS REGISTERS										
SWK_STAT	reserved	SYNC	reserved	reserved	CANSIL	SWK_SET	WUP	WUF	read	1110000
SWK_ECNT_STAT	reserved	reserved	ECNT_5	ECNT_4	ECNT_3	ECNT_2	ECNT_1	ECNT_0	read	1110001
SWK_CDR_STAT1	N_AVG_11	N_AVG_10	N_AVG_9	N_AVG_8	N_AVG_7	N_AVG_6	N_AVG_5	N_AVG_4	read	1110010
SWK_CDR_STAT2	N_AVG_3	N_AVG_2	N_AVG_1	N_AVG_0	reserved	reserved	reserved	reserved	read	1110011
FAMILY AND PRODUCT REGISTERS										
FAM_PROD_STAT	FAM_3	FAM_2	FAM_1	FAM_0	PROD_3	PROD_2	PROD_1	PROD_0	read	1111110

Figure 56 TLE9261-3BQX SPI Bit Mapping including Selective Wake

15.5 SPI Control Registers

READ/WRITE Operation (see also **Chapter 15.3**):

- The ‘POR / Soft Reset Value’ defines the register content after POR or SBC Reset.
- The ‘Restart Value’ defines the register content after SBC Restart, where ‘x’ means the bit is unchanged.
- One 16-bit SPI command consist of two bytes:
  - the 7-bit address and one additional bit for the register access mode and
  - following the data byte
  The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...15 (see also figure before).
- There are three different bit types:
  - ‘r’ = READ: read only bits (or reserved bits)
  - ‘rw’ = READ/WRITE: readable and writable bits
  - ‘rwh’ = READ/WRITE/Hardware: readable/writable bits, which can also be modified by the SBC hardware
- Reserved bits are marked as “Reserved” and always read as “0”. The respective bits shall also be programmed as “0”.
- Reading a register is done byte wise by setting the SPI bit 7 to “0” (= Read Only).
- Writing to a register is done byte wise by setting the SPI bit 7 to “1”.
- SPI control bits are in general not cleared or changed automatically. This must be done by the microcontroller via SPI programming. Exceptions to this behavior are stated at the respective register description and the respective bit type is marked with a ‘h’ meaning that the SBC is able to change the register content.

The registers are addressed wordwise.

15.5.1 General Control Registers

M_S_CTRL
Mode- and Supply Control (Address 000 0001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00x0 00xx$_B$

7	6	5	4	3	2	1	0
MODE_1	**MODE_0**	**VCC3_ON**	**VCC2_ON_1**	**VCC2_ON_0**	**VCC1_OV_RST**	**VCC1_RT_1**	**VCC1_RT_0**
rwh	rwh	rwh	rwh	rwh	rwh	rw	rw

Field	Bits	Type	Description
MODE	7:6	rwh	**SBC Mode Control** 00B , SBC Normal Mode 01B , SBC Sleep Mode 10B , SBC Stop Mode 11B , SBC Reset: Soft Reset is executed (configuration of RO triggering in bit **SOFT_ RESET_RO**)
VCC3_ON	5	rwh	**VCC3 Mode Control** 0B , VCC3 OFF 1B , VCC3 is enabled (as independent voltage regulator)
VCC2_ON	4:3	rwh	**VCC2 Mode Control** 00B , VCC2 off 01B , VCC2 on in Normal Mode 10B , VCC2 on in Normal and Stop Mode 11B , VCC2 always on (except in SBC Fail-Safe Mode)
VCC1_OV_RST	2	rwh	**VCC1 Overvoltage leading to Restart / Fail-Safe Mode enable** 0B , **VCC1_ OV** is set in case of VCC1_OV; no SBC Restart or Fail-Safe is entered for VCC1_OV 1B , **VCC1_ OV** is set in case of VCC1_OV; depending on the device configuration SBC Restart or SBC Fail-Safe Mode is entered (see **Chapter 5.1.1**);
VCC1_RT	1:0	rw	**VCC1 Reset Threshold Control** 00B , Vrt1 selected (highest threshold) 01B , Vrt2 selected 10B , Vrt3 selected 11B , Vrt4 selected

Notes

1. *It is not possible to change from Stop to Sleep Mode via SPI Command. See also the State Machine Chapter*
2. *After entering SBC Restart Mode, the MODE bits will be automatically set to SBC Normal Mode. The VCC2_ON bits will be automatically set to OFF after entering SBC Restart Mode and after OT.*
3. *The SPI output will always show the previously written state with a Write Command (what has been programmed before)*

HW_CTRL
Mode- and Supply Control (Address 000 0010$_B$)
POR / Soft Reset Value: y000 y000$_B$; Restart Value: xx0x x00x$_B$

7	6	5	4	3	2	1	0
VCC3_V_CFG	**SOFT_RESET_RO**	**FO_ON**	**VCC3_VS_UV_OFF**	**VCC3_LS**	**Reserved**	**VCC3_LS_STP_ON**	**CFG**
rw	rw	rwh	rw	rw	r	rw	rw

Field	Bits	Type	Description
VCC3_V_CFG	7	rw	**VCC3OutputVoltageConfiguration(ifconfiguredasindependent voltage regulator)** 0B , VCC3 has same output voltage as VCC1 1B , VCC3 is configured to either 3.3V or 1.8V (depending on VCC1 derivative)
SOFT_RESET_RO	6	rw	**Soft Reset Configuration** 0B , RO will be triggered (pulled low) during a Soft Reset 1B , No RO triggering during a Soft Reset
FO_ON	5	rwh	**Failure Output Activation (FO1..3)** 0B , FOx not activated by software, FO can be activated by defined failures (see **Chapter 13**) 1B , FOx activated by software (via SPI)
VCC3_VS_UV_OFF	4	rw	**VCC3 VS_UV shutdown configuration** 0B , VCC3 will be disabled automatically at VS_UV 1B , VCC3 will stay enabled even below VS_UV
VCC3_LS	3	rw	**VCC3 Configuration** 0B , VCC3 operating as a stand-alone regulator 1B , VCC3 in load sharing operation with VCC1
Reserved	2	r	**Reserved, always reads as 0**
VCC3_LS_STP_ON	1	rw	**VCC3 Load Sharing in SBC Stop Mode configuration** 0B , VCC3 in LS configuration during SBC Stop Mode and high-power mode: disabled 1B , VCC3 in LS configuration during SBC Stop Mode and high-power mode: enabled
CFG	0	rw	**Configuration Select (see also Table 5)** 0B , Depending on hardware configuration, SBC Restart or Fail-Safe Mode is reached after the 2. watchdog trigger failure (=default) - Config 3/4 1B , Depending on hardware configuration, SBC Restart or Fail-Safe Mode is reached after the 1. watchdog trigger failure - Config 1/2

Notes

1. *Clearing the FO_ON bit will not disable the FOx outputs for the case a failure occurred which triggered the FOx outputs. In this case the FOx outputs have to be disabled by clearing the FAILURE bit.*

*If the FO_ON bit is set by the software then it will be cleared by the SBC after SBC Restart Mode was entered and the FOx outputs will be disabled. See also **Chapter 13** for FOx activation and deactivation.*

2. *After triggering a SBC Soft Reset the bits VCC3_V_CFG and VCC3_LS are not reset if they were set before, i.e. it stays unchanged, which is stated by the 'y' in the POR / Soft Reset Value. POR value: 0000 0000 and Soft Reset value: xx00 x00x*
3. *VCC3_LS_STP_ON: Is a combination of load sharing and VCC1 active peak in Stop mode*

WD_CTRL
Watchdog Control (Address 000 0011$_B$)
POR / Soft Reset Value: 0001 0100$_B$; Restart Value: x0xx 0100$_B$

7	6	5	4	3	2	1	0
CHECKSUM	**WD_STM_EN_0**	**WD_WIN**	**WD_EN_WK_BUS**	**Reserved**	**WD_TIMER_2**	**WD_TIMER_1**	**WD_TIMER_0**
rw	rwh	rw	rw	r	rwh	rwh	rwh

Field	Bits	Type	Description
CHECKSUM	7	rw	**Watchdog Setting Check Sum Bit** The sum of bits 7:0 needs to have even parity (see **Chapter 14.2.3**) 0B , Counts as 0 for checksum calculation 1B , Counts as 1 for checksum calculation
WD_STM_EN_0	6	rwh	**Watchdog Deactivation during Stop Mode, bit 0 (Chapter 14.2.4)** 0B , Watchdog is active in Stop Mode 1B , Watchdog is deactivated in Stop Mode
WD_WIN	5	rw	**Watchdog Type Selection** 0B , Watchdog works as a Time-Out watchdog 1B , Watchdog works as a Window watchdog
WD_EN_WK_BUS	4	rw	**Watchdog Enable after Bus (CAN) Wake in SBC Stop Mode** 0B , Watchdog will not start after a CAN wake 1B , Watchdog starts with a long open window after CAN Wake
Reserved	3	r	**Reserved, always reads as 0**
WD_TIMER	2:0	rwh	**Watchdog Timer Period** 000B , 10ms 001B , 20ms 010B , 50ms 011B , 100ms 100B , 200ms 101B , 500ms 110B , 1000ms 111B , reserved

Notes

1. *See also **Chapter 14.2.4** for more information on disabling the watchdog in SBC Stop Mode.*
2. *See **Chapter 14.2.5** for more information on the effect of the bit WD_EN_WK_BUS.*
3. *See **Chapter 14.2.3** for calculation of checksum.*

BUS_CTRL_1
Bus Control (Address 000 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0yyy$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**CAN_2**	**CAN_1**	**CAN_0**
r	r	r	r	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
CAN	2:0	rwh	**HS-CAN Module Modes** 000B , CAN OFF 001B , CAN is wake capable (no SWK) 010B , CAN Receive Only Mode (no SWK) 011B , CAN Normal Mode (no SWK) 100B , CAN OFF 101B , CAN is wake capable with SWK 110B , CAN Receive Only Mode with SWK 111B , CAN Normal Mode with SWK

Notes

1. *The reset values for the CAN transceivers are marked with 'y' because they will vary depending on the cause of change - see below.*
2. *see **Figure 31** for detailed state changes of CAN Transceiver for different SBC modes.*
3. *The bit CAN_2 is not modified by the SBC but can only be changed by the user. Therefore, the access type is 'rw' compared to bits CAN_0 and CAN_1.*
4. *In case SYSERR = 0 and the CAN transceiver is configured to 'x11' while going to SBC Sleep Mode, it will be automatically set to wake capable ('x01'). The SPI bits will be changed to wake capable. If configured to 'x10' and SBC Sleep Mode is entered, then the transceiver is set to wake capable, while it will stay in Receive Only Mode when it had been configured to 'x10' when going to SBC Stop Mode. If it had been configured to wake capable or OFF then the mode will remain unchanged.The Receive Only Mode has to be selected by the user before entering SBC Stop Mode. Please refer to **Chapter 5.4.4** for detailed information on the Selective Wake mode changes.*
5. *Failure Handling Mechanism: When the device enters Fail-Safe Mode due to a failure (TSD2, WD-Failure,...), then the wake registers **BUS_CTRL_1** and **WK_CTRL_2** are reset to following values (=wake sources) 'xxx0 0001' and 'x0x0 0111' in order to ensure that the device can be woken again.*

BUS_CTRL_2
Bus Control (Address 000 0101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00x0 0000$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**I_PEAK_TH**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
r	r	rw	r	r	r	r	r

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
I_PEAK_TH	5	rw	**VCC1 Active Peak Threshold Selection** 0B , low VCC1 active peak threshold selected (ICC1,peak_1) 1B , higher VCC1 active peak threshold selected (ICC1,peak_2)
Reserved	4:0	r	**Reserved, always reads as 0**

Notes

1. *The bit **I_PEAK_TH** can be modified in SBC Init and Normal Mode. In SBC Stop Mode this bit is Read only but SPI_FAIL will not be set when trying to modify the bit in SBC STOP Mode and no INT is triggered in case **INT_GLOBAL** is set.*
2. *see **Figure 31** for detailed state changes of CAN Transceiver for different SBC modes*
3. *Failure Handling Mechanism: When the device enters Fail-Safe Mode due to a failure (TSD2, WD-Failure,...), then the wake registers **BUS_CTRL_1**, and **WK_CTRL_2** are reset to following values (=wake sources) 'xxx0 1001', and 'x0x0 0111' in order to ensure that the device can be woken again.*

WK_CTRL_1
Internal Wake Input Control (Address 000 0110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xx00 0000$_B$**

7	6	5	4	3	2	1	0
TIMER2_WK_EN	**TIMER1_WK_EN**	**Reserved**	**Reserved**	**Reserved**	**WD_STM_EN_1**	**Reserved**	**Reserved**
rw	rw	r	r	r	rwh	r	r

Field	Bits	Type	Description
TIMER2_WK_EN	7	rw	**Timer2 Wake Source Control (for cyclic wake)** 0B , Timer2 wake disabled 1B , Timer2 is enabled as a wake source
TIMER1_WK_EN	6	rw	**Timer1 Wake Source Control (for cyclic wake)** 0B , Timer1 wake disabled 1B , Timer1 is enabled as a wake source
Reserved	5:3	r	**Reserved, always reads as 0**
WD_STM_EN_1	2	rwh	**Watchdog Deactivation during Stop Mode, bit 1 (Chapter 14.2.4)** 0B , Watchdog is active in Stop Mode 1B , Watchdog is deactivated in Stop Mode
Reserved	1:0	r	**Reserved, always reads as 0**

WK_CTRL_2
External Wake Source Control (Address 000 0111$_B$)
POR / Soft Reset Value: 0000 0111$_B$; Restart Value: x0x0 0xxx$_B$

7	6	5	4	3	2	1	0
INT_GLOBAL	**Reserved**	**WK_MEAS**	**Reserved**	**Reserved**	**WK3_EN**	**WK2_EN**	**WK1_EN**
rw	r	rw	r	r	rw	rw	rw

Field	Bits	Type	Description
INT_ GLOBAL	7	rw	**Global Interrupt Configuration (see also Chapter 12.1)** 0B , Only wake sources trigger INT (default) 1B , All status information register bits will trigger INT (including all wake sources)
Reserved	6	r	**Reserved, always reads as 0**
WK_MEAS	5	rw	**WK / Measurement selection (see also Chapter 11.2.2)** 0B , WK functionality enabled for WK1 and WK2 1B , Measurement functionality enabled; WK1 & WK2 are disabled as wake sources, i.e. bits WK1/2_EN bits are ignored
Reserved	4:3	r	**Reserved, always reads as 0**
WK3_EN	2	rw	**WK3 Wake Source Control** 0B , WK3 wake disabled 1B , WK3 is enabled as a wake source
WK2_EN	1	rw	**WK2 Wake Source Control** 0B , WK2 wake disabled 1B , WK2 is enabled as a wake source
WK1_EN	0	rw	**WK1 Wake Source Control** 0B , WK1 wake disabled 1B , WK1 is enabled as a wake source

Notes

1. *WK_MEAS is by default configured for standard WK functionality (WK1 and WK2). The bits WK1_EN and WK2_EN are ignored in case WK_MEAS is activated. If the bit is set to '1' then the measurement function is enabled during Normal Mode & the bits WK1_EN and WK2_EN are ignored. The bits WK1/"_LVL bits need to be ignored as well.*
2. *The wake sources CAN are selected in the register **BUS_CTRL_1** by setting the respective bits to 'wake capable'*
3. *Failure Handling Mechanism: When the device enters Fail-Safe Mode due to a failure (TSD2, WD-Failure,...), then the wake registers **BUS_CTRL_1** and **WK_CTRL_2** are reset to following values (=wake sources) 'xxx0 0001' and 'x0x0 0111' in order to ensure that the device can be woken again.*

WK_PUPD_CTRL
Wake Input Level Control (Address 000 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 00xx xxxx$_B$**

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**WK3_PUPD_1**	**WK3_PUPD_0**	**WK2_PUPD_1**	**WK2_PUPD_0**	**WK1_PUPD_1**	**WK1_PUPD_0**
r	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
WK3_PUPD	5:4	rw	**WK3 Pull-Up / Pull-Down Configuration** 00B , No pull-up / pull-down selected 01B , Pull-down resistor selected 10B , Pull-up resistor selected 11B , Automatic switching to pull-up or pull-down
WK2_PUPD	3:2	rw	**WK2 Pull-Up / Pull-Down Configuration** 00B , No pull-up / pull-down selected 01B , Pull-down resistor selected 10B , Pull-up resistor selected 11B , Automatic switching to pull-up or pull-down
WK1_PUPD	1:0	rw	**WK1 Pull-Up / Pull-Down Configuration** 00B , No pull-up / pull-down selected 01B , Pull-down resistor selected 10B , Pull-up resistor selected 11B , Automatic switching to pull-up or pull-down

WK_FLT_CTRL
Wake Input Filter Time Control (Address 000 1001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 00xx xxxx$_B$**

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**WK3_FLT_1**	**WK3_FLT_0**	**WK2_FLT_1**	**WK2_FLT_0**	**WK1_FLT_1**	**WK1_FLT_0**
r	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
WK3_FLT	5:4	rw	**WK3 Filter Time Configuration** 00B , Configuration A: Filter with 16µs filter time (static sensing) 01B , Configuration B: Filter with 64µs filter time (static sensing) 10B , Configuration C: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer1 11B , Configuration D: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer2
WK2_FLT	3:2	rw	**WK2 Filter Time Configuration** 00B , Configuration A: Filter with 16µs filter time (static sensing) 01B , Configuration B: Filter with 64µs filter time (static sensing) 10B , Configuration C: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer1 11B , Configuration D: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer2
WK1_FLT	1:0	rw	**WK1 Filter Time Configuration** 00B , Configuration A: Filter with 16µs filter time (static sensing) 01B , Configuration B: Filter with 64µs filter time (static sensing) 10B , Configuration C: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer1 11B , Configuration D: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer2

Note: When selecting a filter time configuration, the user must make sure to also assign the respective timer to at least one HS switch during cyclic sense operation

TIMER1_CTRL
Timer1 Control and Selection (Address 000 1100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0000 0000$_B$**

7	6	5	4	3	2	1	0
Reserved	**TIMER1_ ON_2**	**TIMER1_ ON_1**	**TIMER1_ ON_0**	**Reserved**	**TIMER1_ PER_2**	**TIMER1_ PER_1**	**TIMER1_ PER_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
TIMER1_ ON	6:4	rwh	**Timer1 On-Time Configuration** 000B , OFF / Low (timer not running, HSx output is low) 001B , 0.1ms on-time 010B , 0.3ms on-time 011B , 1.0ms on-time 100B , 10ms on-time 101B , 20ms on-time 110B , OFF / HIGH (timer not running, HSx output is high) 111B , reserved
Reserved	3	r	**Reserved, always reads as 0**
TIMER1_ PER	2:0	rwh	**Timer1 Period Configuration** 000B , 10ms 001B , 20ms 010B , 50ms 011B , 100ms 100B , 200ms 101B , 1s 110B , 2s 111B , reserved

Notes

1. *A timer must be first assigned and is then automatically activated as soon as the on-time is configured.*
2. *If cyclic sense is selected and the HS switches are cleared during SBC Restart Mode, then also the timer settings (period and on-time) are cleared to avoid incorrect switch detection.*
3. *In case the timer are set as wake sources and cyclic sense is running, then both cyclic sense and cyclic wake will be active at the same time.*

TIMER2_CTRL
Timer2 Control and selection (Address 000 1101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0000 0000$_B$**

7	6	5	4	3	2	1	0
Reserved	**TIMER2_ ON_2**	**TIMER2_ ON_1**	**TIMER2_ ON_0**	**Reserved**	**TIMER2_ PER_2**	**TIMER2_ PER_1**	**TIMER2_ PER_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
TIMER2_ ON	6:4	rwh	**Timer2 On-Time Configuration** 000B , OFF / Low (timer not running, HSx output is low) 001B , 0.1ms on-time 010B , 0.3ms on-time 011B , 1.0ms on-time 100B , 10ms on-time 101B , 20ms on-time 110B , OFF / HIGH (timer not running, HSx output is high) 111B , reserved
Reserved	3	r	**Reserved, always reads as 0**
TIMER2_ PER	2:0	rwh	**Timer2 Period Configuration** 000B , 10ms 001B , 20ms 010B , 50ms 011B , 100ms 100B , 200ms 101B , 1s 110B , 2s 111B , reserved

Notes

1. *A timer must be first assigned and is then automatically activated as soon as the on-time is configured.*
2. *If cyclic sense is selected and the HS switches are cleared during SBC Restart Mode, then also the timer settings (period and on-time) are cleared to avoid incorrect switch detection.*

SW_SD_CTRL
Switch Shutdown Control (Address 001 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0xxx 0000$_B$**

7	6	5	4	3	2	1	0
Reserved	**HS_OV_SD_EN**	**HS_UV_SD_EN**	**HS_OV_UV_REC**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
r	rw	rw	rw	r	r	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
HS_OV_SD_EN	6	rw	**Shutdown Disabling of HS1...4 in case of VSHS OV** 0B , shutdown enabled in case of VSHS OV 1B , shutdown disabled in case of VSHS OV
HS_UV_SD_EN	5	rw	**Shutdown Disabling of HS1...4 in case of VSHS UV** 0B , shutdown enabled in case of VSHS UV 1B , shutdown disabled in case of VSHS UV
HS_OV_UV_REC	4	rw	**Switch Recovery after Removal of VSHS OV/UV for HS1...4** 0B , Switch recovery is disabled 1B , Previous state before VSHS OV/UV is enabled after OV/UV condition is removed
Reserved	3:0	r	**Reserved, always reads as 0**

HS_CTRL1
High-Side Switch Control 1 (Address 001 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0000 0000$_B$**

7	6	5	4	3	2	1	0
Reserved	**HS2_2**	**HS2_1**	**HS2_0**	**Reserved**	**HS1_2**	**HS1_1**	**HS1_0**
rw	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
HS2	6:4	rwh	**HS2 Configuration** 000B , Off 001B , On 010B , Controlled by Timer1 011B , Controlled by Timer2 100B , Controlled by PWM1 101B , Controlled by PWM2 110B , Reserved 111B , Reserved
Reserved	3	r	**Reserved, always reads as 0**
HS1	2:0	rwh	**HS1 Configuration** 000B , Off 001B , On 010B , Controlled by Timer1 011B , Controlled by Timer2 100B , Controlled by PWM1 101B , Controlled by PWM2 110B , Reserved 111B , Reserved

Note: The bits for the switches are also reset in case of overcurrent and overtemperature.

HS_CTRL2
High-Side Switch Control 2 (Address 001 0101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0000 0000$_B$**

7	6	5	4	3	2	1	0
Reserved	**HS4_2**	**HS4_1**	**HS4_0**	**Reserved**	**HS3_2**	**HS3_1**	**HS3_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
HS4	6:4	rwh	**HS4 Configuration** 000B , Off 001B , On 010B , Controlled by Timer1 011B , Controlled by Timer2 100B , Controlled by PWM1 101B , Controlled by PWM2 110B , Reserved 111B , Reserved
Reserved	3	r	**Reserved, always reads as 0**
HS3	2:0	rwh	**HS3 Configuration** 000B , Off 001B , On 010B , Controlled by Timer1 011B , Controlled by Timer2 100B , Controlled by PWM1 101B , Controlled by PWM2 110B , Reserved 111B , Reserved

Note: The bits for the switches are also reset in case of overcurrent and overtemperature.

GPIO_CTRL
GPIO Configuration Control (Address 001 0111$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xxxx xxxx$_B$**

7	6	5	4	3	2	1	0
FO_DC_1	**FO_DC_0**	**GPIO2_2**	**GPIO2_1**	**GPIO2_0**	**GPIO1_2**	**GPIO1_1**	**GPIO1_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FO_DC	7:6	rw	**Duty Cycle Configuration of FO3 (if selected)** 00B , 20% 01B , 10% 10B , 5% 11B , 2.5%
GPIO2	5:3	rw	**GPIO2 Configuration** 000B , FO3 selected 001B , FO3 selected 010B , FO3 selected 011B , FO3 selected 100B , OFF 101B , Wake input enabled (16µs static filter) 110B , Low-Side Switch ON 111B , High-Side Switch ON
GPIO1	2:0	rw	**GPIO1 Configuration** 000B , FO2 selected 001B , FO2 selected 010B , FO2 selected 011B , FO2 selected 100B , OFF 101B , Wake input enabled (16µs static filter) 110B , Low-Side Switch ON 111B , High-Side Switch ON

Note: When selecting a filter time configuration, the user must make sure to also assign the respective timer to at least one HS switch during cyclic sense operation

PWM1_CTRL
PWM1 Configuration Control (Address 001 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xxxx xxxx$_B$**

7	6	5	4	3	2	1	0
PWM1_DC_7	**PWM1_DC_6**	**PWM1_DC_5**	**PWM1_DC_4**	**PWM1_DC_3**	**PWM1_DC_2**	**PWM1_DC_1**	**PWM1_DC_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM1_DC	7:0	rw	**PWM1 Duty Cycle (bit0=LSB; bit7=MSB)** 0000 0000B, 100% OFF xxxx xxxx B, ON with DC fraction of 255 1111 1111B, 100% ON

Note: The min. On-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting '000 0001' could not be realized.

PWM2_CTRL
PWM2 Configuration Control (Address 001 1001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xxxx xxxx$_B$**

7	6	5	4	3	2	1	0
PWM2_DC_7	**PWM2_DC_6**	**PWM2_DC_5**	**PWM2_DC_4**	**PWM2_DC_3**	**PWM2_DC_2**	**PWM2_DC_1**	**PWM2_DC_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM2_DC	7:0	rw	**PWM2 Duty Cycle (bit0=LSB; bit7=MSB)** 0000 0000B, 100% OFF xxxx xxxxB, ON with DC fraction of 255 1111 1111B, 100% ON

Note: The min. On-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting '000 0001' could not be realized.

PWM_FREQ_CTRL
PWM Frequency Configuration Control (Address 001 1100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0000 0x0x$_B$**

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**PWM2_FREQ**	**Reserved**	**PWM1_FREQ**
r	r	r	r	r	rw	r	rw

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
PWM2_ FREQ	2	rw	**PWM2 Frequency Selection** 0B , 200Hz configuration 1B , 400Hz configuration
Reserved	1	r	**Reserved, always reads as 0**
PWM1_ FREQ	0	rw	**PWM1 Frequency Selection** 0B , 200Hz configuration 1B , 400Hz configuration

Note: The min. On-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting '000 0001' could not be realized.

SYS_STATUS_CTRL
System Status Control (Address 001 1110$_B$)
POR Value: 0000 0000$_B$; **Restart Value/Soft Reset Value: xxxx xxxx$_B$**

7	6	5	4	3	2	1	0
SYS_STAT_7	**SYS_STAT_6**	**SYS_STAT_5**	**SYS_STAT_4**	**SYS_STAT_3**	**SYS_STAT_2**	**SYS_STAT_1**	**SYS_STAT_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SYS_STAT	7:0	rw	**System Status Control Byte (bit0=LSB; bit7=MSB)** Dedicated byte for system configuration, access only by microcontroller. Cleared after power up and Soft Reset

Notes

1. *The **SYS_STATUS_CTRL** register is an exception for the default values, i.e. it will keep its configured value also after a Soft Reset.*
2. *This byte is intended for storing system configurations of the ECU by the microcontroller and is only accessible in SBC Normal Mode. The byte is not accessible by the SBC and is also not cleared after Fail-Safe or SBC Restart Mode. It allows the microcontroller to quickly store system configuration without loosing the data.*

15.5.2 Selective Wake Control Registers

SWK_CTRL
CAN Selective Wake Control (Address 010 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xxxx 0000$_B$**

7	6	5	4	3	2	1	0
OSC_CAL	**TRIM_EN_1**	**TRIM_EN_0**	**CANTO_ MASK**	**Reserved**	**Reserved**	**Reserved**	**CFG_VAL**
rw	rw	rw	rw	r	r	r	rwh

Field	Bits	Type	Description
OSC_CAL	7	rw	**Oscillator Calibration Mode** 0B , Oscillator Calibration is disabled 1B , Oscillator Calibration is enabled
TRIM_EN	6:5	rw	**(Un)locking mechanism of oscillator recalibration** 00B , locked 01B , locked 10B , locked 11B , unlocked
CANTO_ MASK	4	rw	**CAN Time Out Masking** 0B , CAN time-out is masked - no interrupt (on pin INT) is triggered 1B , CAN time-out is signaled on INT
Reserved	3:1	r	**Reserved, always reads as 0**
CFG_VAL	0	rwh	**SWK Configuration valid** 0B , Configuration is not valid (SWK not possible) 1B , SWK configuration valid, needs to be set to enable SWK

Notes

1. *TRIM_EN unlocks the oscillation calibration mode. Only the bit combination '11' is the valid unlock. The pin TXDCAN is used for oscillator synchronisation (trimming).*
2. *The microcontroller needs to validate the SWK configuration and set 'CFG_VAL' to '1'. The SBC will only enable SWK if CFG_VAL' to '1'. The bit will be cleared automatically by the SBC after a wake up or POR or if a SWK configuration data is changed by the microcontroller.*
3. *CANTO bit will only be updated inside BUS_STAT while CAN_2 is set. Therefore, an interrupt is only signaled upon occurrence of CANTO while CAN_2 (SWK is enabled) is set in SBC Normal and Stop Mode.*
4. *TRIM_EN also unlocks the writing to the SWK_OPT_CTRL register in order to enable the alternate low-power Receiver for Selective wake to optimize the quiescent current consumption. Only the bit combination '11' unlocks the calibrations / configurations.*
5. *In SBC stop-mode, any write command to a CAN or SWK configuration register will lead to CFG_VAL be set to '0' (SWK becomes invalid).*

SWK_BTL1_CTRL
SWK Bit Timing Logic Control1 (Address 010 0001$_B$)
POR / Soft Reset Value: 1010 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
TBIT_7	**TBIT_6**	**TBIT_5**	**TBIT_4**	**TBIT_3**	**TBIT_2**	**TBIT_1**	**TBIT_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TBIT	7:0	rw	**Number of Time Quanta in a Bit Time** Represents the number of time quanta in a bit time. Quanta is depending on **SEL_OSC_CLK**<1:0> from the **SWK_CDR_CTRL2** register.

SWK_BTL2_CTRL
SWK Bit Timing Control2 (Address 010 0010$_B$)
POR / Soft Reset Value: 0011 0011$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
reserved	**reserved**	**SP_5**	**SP_4**	**SP_3**	**SP_2**	**SP_1**	**SP_0**
r	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
SP	5:0	rw	**Sampling Point Position** Represents the sampling point position (fractional number < 1). Example: 0011 0011 = 0.796875 (~80%)

SWK_ID3_CTRL
SWK WUF Identifier bits 28...21 (Address 010 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
ID28	**ID27**	**ID26**	**ID25**	**ID24**	**ID23**	**ID22**	**ID21**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ID28_21	7:0	rw	**WUF Identifier Bits 28...21**

Note: Please note the configuration of the standard identifier and extended identifier. The standard identifier is configured to the bits ID18...ID28

SWK_ID2_CTRL
SWK WUF Identifier bits 20...13 (Address 010 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
ID20	**ID19**	**ID18**	**ID17**	**ID16**	**ID15**	**ID14**	**ID13**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ID20_13	7:0	rw	**WUF Identifier Bits 20...13**

SWK_ID1_CTRL
SWK WUF Identifier bits 12...5 (Address 010 0101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
ID12	**ID11**	**ID10**	**ID9**	**ID8**	**ID7**	**ID6**	**ID5**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ID12_5	7:0	rw	**WUF Identifier Bits 12...5**

SWK_ID0_CTRL
SWK WUF Identifier bits 4...0 (Address 010 0110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0xxx xxxx$_B$

7	6	5	4	3	2	1	0
reserved	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**	**RTR**	**IDE**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
ID4_0	6:2	rw	**WUF Identifier Bits 4..0**
RTR	1	rw	**Remote Transmission Request Field (acc. ISO 11898-1)** 0B , Normal Data Frame 1B , Remote Transmission Request
IDE	0	rw	**Identifier Extension Bit** 0B , Standard Identifier Length (11 bit) 1B , Extended Identifier Length (29 bit)

Note: The setting RTR = 1 is not allowed for wake-up frames according to the ISO11898-2:2016

SWK_MASK_ID3_CTRL
SWK WUF Identifier Mask bits 28...21 (Address 010 0111$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
MASK_ID28	**MASK_ID27**	**MASK_ID26**	**MASK_ID25**	**MASK_ID24**	**MASK_ID23**	**MASK_ID22**	**MASK_ID21**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MASK_ID28_21	7:0	rw	**WUF Identifier Mask Bits 28...21** 0B , Unmasked - bit is ignored 1B , Masked - bit is compared in CAN frame

Note: Masking WUF bits is done by setting the respective MASK bit to '1'

SWK_MASK_ID2_CTRL
SWK WUF Identifier Mask bits 20...13 (Address 010 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
MASK_ID20	**MASK_ID19**	**MASK_ID18**	**MASK_ID17**	**MASK_ID16**	**MASK_ID15**	**MASK_ID14**	**MASK_ID13**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MASK_ID20_13	7:0	rw	**WUF Identifier Mask Bits 20...13** 0B , Unmasked - bit is ignored 1B , Masked - bit is compared in CAN frame

SWK_MASK_ID1_CTRL
SWK WUF Identifier Mask bits 12...5 (Address 010 1001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
MASK_ID12	**MASK_ID11**	**MASK_ID10**	**MASK_ID9**	**MASK_ID8**	**MASK_ID7**	**MASK_ID6**	**MASK_ID5**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MASK_ID12_5	7:0	rw	**WUF Identifier Mask Bits 12...5** 0B , Unmasked - bit is ignored 1B , Masked - bit is compared in CAN frame

SWK_MASK_ID0_CTRL
SWK WUF Identifier bits 4...0 (Address 010 1010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0xxx xx00$_B$

7	6	5	4	3	2	1	0
Reserved	**MASK_ID4**	**MASK_ID3**	**MASK_ID2**	**MASK_ID1**	**MASK_ID0**	**Reserved**	**Reserved**
rw	rw	rw	rw	rw	rw	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
MASK_ID4_0	6:2	rw	**WUF Identifier MASK Bits 4..0** 0B , Unmasked - bit is ignored 1B , Masked - bit is compared in CAN frame
Reserved	1:0	r	**Reserved, always reads as 0**

SWK_DLC_CTRL
SWK Frame Data Length Code Control (Address 010 1011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**DLC_3**	**DLC_2**	**DLC_1**	**DLC_0**
r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
DLC	3:0	rw	**Payload length in number of bytes** 0000B, Frame Data Length = 0 or cleared 0001B, Frame Data Length = 1 0010B, Frame Data Length = 2 0011B, Frame Data Length = 3 0100B, Frame Data Length = 4 0101B, Frame Data Length = 5 0110B, Frame Data Length = 6 0111B, Frame Data Length = 7 from 1000B to 1111B Frame Data Length = 8

*Note: The number of bytes in the data field has to be indicated by the DLC. The DLC consists of four bits. The admissible number of data bytes for a data frame ranges from zero to eight. DLCs in the range of zero to seven shall indicate data fields of length of zero to seven bytes. DLCs in the range from eight to fifteen indicate data fields of length of eight byte. The configured DLC value has to match bit by bit with the DLC in the received wake-up frame (refer also to **Chapter 5.4.2.3**).*

SWK_DATA7_CTRL
SWK Data7 Register (Address 010 1100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA7_7	**DATA7_6**	**DATA7_5**	**DATA7_4**	**DATA7_3**	**DATA7_2**	**DATA7_1**	**DATA7_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA7	7:0	rw	**Data7 byte content(bit0=LSB; bit7=MSB)**

SWK_DATA6_CTRL

SWK Data6 Register (Address 010 1101$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA6_7	**DATA6_6**	**DATA6_5**	**DATA6_4**	**DATA6_3**	**DATA6_2**	**DATA6_1**	**DATA6_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA6	7:0	rw	**Data6 byte content (bit0=LSB; bit7=MSB)**

SWK_DATA5_CTRL

SWK Data5 Register (Address 010 1110$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA5_7	**DATA5_6**	**DATA5_5**	**DATA5_4**	**DATA5_3**	**DATA5_2**	**DATA5_1**	**DATA5_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA5	7:0	rw	**Data5 byte content (bit0=LSB; bit7=MSB)**

SWK_DATA4_CTRL

SWK Data4 Register (Address 010 1111$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA4_7	**DATA4_6**	**DATA4_5**	**DATA4_4**	**DATA4_3**	**DATA4_2**	**DATA4_1**	**DATA4_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA4	7:0	rw	**Data4 byte content (bit0=LSB; bit7=MSB)**

SWK_DATA3_CTRL

SWK Data3 Register (Address 011 0000$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA3_7	**DATA3_6**	**DATA3_5**	**DATA3_4**	**DATA3_3**	**DATA3_2**	**DATA3_1**	**DATA3_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA3	7:0	rw	**Data3 byte content (bit0=LSB; bit7=MSB)**

SWK_DATA2_CTRL

SWK Data2 Register (Address 011 0001$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA2_7	**DATA2_6**	**DATA2_5**	**DATA2_4**	**DATA2_3**	**DATA2_2**	**DATA2_1**	**DATA2_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA2	7:0	rw	**Data2 byte content (bit0=LSB; bit7=MSB)**

SWK_DATA1_CTRL

SWK Data1 Register (Address 011 0010$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA1_7	**DATA1_6**	**DATA1_5**	**DATA1_4**	**DATA1_3**	**DATA1_2**	**DATA1_1**	**DATA1_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA1	7:0	rw	**Data1 byte content (bit0=LSB; bit7=MSB)**

SWK_DATA0_CTRL

SWK Data0 Register (Address 011 0011$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA0_7	**DATA0_6**	**DATA0_5**	**DATA0_4**	**DATA0_3**	**DATA0_2**	**DATA0_1**	**DATA0_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA0	7:0	rw	**Data0 byte content (bit0=LSB; bit7=MSB)**

SWK_CAN_FD_CTRL

CAN FD Configuration Control Register (Address 011 0100$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00xx xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**DIS_ERR_CNT**	**RX_FILT_BYP**	**FD_FILTER_2**	**FD_FILTER_1**	**FD_FILTER_0**	**CAN_FD_EN**
r	r	rwh	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
DIS_ERR_ CNT	5	rwh	**Error Counter Disable Function** 0B , Error Counter is enabled during SWK 1B , Error counter is disabled during SWK only if CAN_FD_EN = '1'
RX_FILT_ BYP	4	rw	**RX Receiver Filter Bypass** 0B , RX Filter not bypassed 1B , RX Filter bypassed
FD_FILTER	3:1	rw	**CAN FD Dominant Filter Time** 000B , 50 ns 001B , 100 ns 010B , 150 ns 011B , 200 ns 100B , 250 ns 101B , 300 ns 110B , 350 ns 111B , 775 ns
CAN_FD_ EN	0	rw	**Enable CAN FD Tolerant Mode** 0B , CAN FD Tolerant Mode disabled 1B , CAN FD Tolerant Mode enabled

*Note: The bit **RX_FILT_ BYP** is bypassing the analog filter in the CAN receiver path; The **FD_FILTER** is not in the analog path of the CAN receiver and is not bypassed.*

*Note: **DIS_ERR_ CNT** is cleared by the SBC at tsilence expiration.*

15.5.3 Selective Wake Trimming and Calibration Control Registers

SWK_OSC_TRIM_CTRL
SWK Oscillator Trimming Register (Address 011 1000$_B$)
POR / Soft Reset Value: xxxx xxxx$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
TRIM_OSC_7	**TRIM_OSC_6**	**TRIM_OSC_5**	**TRIM_OSC_4**	**TRIM_OSC_3**	**TRIM_OSC_2**	**TRIM_OSC_1**	**TRIM_OSC_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TRIM_OSC	7:0	rw	**Oscillator trimming (bit0=LSB; bit7=MSB); (only writable if TRIM_EN = '11')**

Note: TRIM_OSC[0:4] represent the 32-steps fine trimming range with a monotonous behavior from slower to faster frequency. The step width is ~0.25MHz.
TRIM_OSC[5:7] are modifying the oscillator temperature coefficient. It is strongly recommended to not change these values.
Due to CDR functionality, it is not required to change these values.

SWK_OPT_CTRL
Selective Wake Options Register (Address 011 1001$_B$)
POR / Soft Reset Value: 000x xxxx$_B$; Restart Value: x00x xxxx$_B$

7	6	5	4	3	2	1	0
RX_WK_SEL	**Reserved**	**Reserved**	**TRIM_OSC_12**	**TRIM_OSC_11**	**TRIM_OSC_10**	**TRIM_OSC_9**	**TRIM_OSC_8**
rw	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RX_WK_SEL	7	rw	**SWK Receiver selection (only accessible if TRIM_EN = '11')** 0B , Standard Receiver selected during SWK 1B , Low-Power Receiver selected during SWK
Reserved	6:5	r	**Reserved, always reads as 0**
TRIM_OSC	4:0	rw	**Oscillator trimming (bit8=LSB; bit12=MSB); (only writable if TRIM_EN = '11')**

Note: The bit RX_WK_SEL is used to select the respective receiver during Selective Wake operation. To reduce the quiescent current during Frame Detect Mode it is recommended to select the Low-Power Receiver, i.e. RX_WK_SEL = '1'.
Important: If the RX_WK_SEL bit is changed, then it must be ensured that the values of TRIM_OSC [8:12] bits remain unchanged to avoid a change of oscillator frequency.

Note: TRIM_OSC[8:12] represent the 32-steps coarse trimming range, which is not monotonous. It is not recommended to change these values.

SWK_OSC_CAL_H_STAT
SWK Oscillator Calibration High Register (Address 011 1010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
OSC_CAL_H_7	**OSC_CAL_H_6**	**OSC_CAL_H_5**	**OSC_CAL_H_4**	**OSC_CAL_H_3**	**OSC_CAL_H_2**	**OSC_CAL_H_1**	**OSC_CAL_H_0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
OSC_CAL_H	7:0	r	**Oscillator Calibration High Register**

SWK_OSC_CAL_L_STAT
SWK Oscillator Calibration Low Register (Address 011 1011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
OSC_CAL_L_7	**OSC_CAL_L_6**	**OSC_CAL_L_5**	**OSC_CAL_L_4**	**OSC_CAL_L_3**	**OSC_CAL_L_2**	**OSC_CAL_L_1**	**OSC_CAL_L_0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
OSC_CAL_L	7:0	r	**Oscillator Calibration Low Register**

SWK_CDR_CTRL1
CDR Control 1 Register (Address 011 1100$_B$)
POR / Soft Reset Value: 0000 0100$_B$; Restart Value: 0000 xx0x$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**SEL_FILT_1**	**SEL_FILT_0**	**Reserved**	**CDR_EN**
r	r	r	r	rw	rw	r	rw

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
SEL_FILT	3:2	rw	**Select Time Constant of Filter** 00B , Time constant 8 01B , Time constant 16 (default) 10B , Time constant 32 11B , adapt distance between falling edges 2, 3 bit: Time constant 32 distance between f. edges 4, 5, 6, 7, 8 bit: Time constant 16 distance between falling edges 9, 10 bit: Time constant 8
Reserved	1	r	**Reserved, always reads as 0**
CDR_EN	0	rw	**Enable CDR** 0B , CDR disabled 1B , CDR enabled

SWK_CDR_CTRL2
CDR Control 2Register (Address 011 1101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 00xx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**SEL_OSC_CLK_1**	**SEL_OSC_CLK_0**
r	r	r	r	r	r	rw	rw

Field	Bits	Type	Description
Reserved	7:2	r	**Reserved, always reads as 0**
SEL_OSC_CLK	1:0	rw	**Input Frequency for CDR module** See **Table 35** and **Table 36**.

Table 35 Frequency Settings of Internal Clock for the CDR

SEL_OSC_CLK[1:0]	int. Clock for CDR
00	80 MHz
01	40 MHz

Table 35 Frequency Settings of Internal Clock for the CDR (cont'd)

SEL_OSC_CLK[1:0]	int. Clock for CDR
10	20 MHz
11	10 MHz

Table 36 Recommended CDR Settings for Different Baud Rates

SEL_OSC_CLK [1:0]	Baudrate	SWK_BTL1_CTRL Value	SWK_CDR_LIMIT_HIGH _CTRL Value	SWK_CDR_LIMIT_LOW_ CTRL Value
00	500k	1010 0000	1010 1000	1001 1000
01	500k	0101 0000	0101 0100	0100 1100
10	500k	CDR Setting not recommended for this baudrate due to insufficient precision		
11	500k	CDR Setting not recommended for this baudrate due to insufficient precision		
00	250k	CDR Setting not to be used due to excessive time quanta (counter overflow)		
01	250k	1010 0000	1010 1000	1001 1000
10	250k	0101 0000	0101 0100	0100 1100
11	250k	CDR Setting not recommended for this baudrate due to insufficient precision		
00	125k	CDR Setting not to be used due to excessive time quanta (counter overflow)		
01	125k	CDR Setting not to be used due to excessive time quanta (counter overflow)		
10	125k	1010 0000	1010 1000	1001 1000
11	125k	0101 0000	0101 0100	0100 1100

SWK_CDR_LIMIT_HIGH_CTRL
SWK CDR Upper Limit Control (Address 011 1110$_B$)
POR / Soft Reset Value: 1010 1000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
CDR_LIM_ H_7	CDR_LIM_ H_6	CDR_LIM_ H_5	CDR_LIM_ H_4	CDR_LIM_ H_3	CDR_LIM_ H_2	CDR_LIM_ H_1	CDR_LIM_ H_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CDR_LIM_H	7:0	rw	**Upper Bit Time Detection Range of Clock and Data Recovery** SWK_BTL1_CTRL values > + 5% will be clamped

SWK_CDR_LIMIT_LOW_CTRL
SWK CDR Lower Limit Control (Address 011 1111$_B$)
POR / Soft Reset Value: 1001 1000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
CDR_LIM_ L_7	CDR_LIM_ L_6	CDR_LIM_ L_5	CDR_LIM_ L_4	CDR_LIM_ L_3	CDR_LIM_ L_2	CDR_LIM_ L_1	CDR_LIM_ L_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CDR_LIM_L	7:0	rw	**Lower Bit Time Detection Range of Clock and Data Recovery** **SWK_BTL1_CTRL** values < - 5% will be clamped

15.6 SPI Status Information Registers

READ/CLEAR Operation (see also **Chapter 15.3**):

- One 16-bit SPI command consist of two bytes:
  - the 7-bit address and one additional bit for the register access mode and
  - following the data byte
  The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...15 (see also figure).
- There are two different bit types:
  - ‘r’ = READ: read only bits (or reserved bits)
  - ‘rc’ = READ/CLEAR: readable and clearable bits
- Reading a register is done byte wise by setting the SPI bit 7 to “0” (= Read Only)
- Clearing a register is done byte wise by setting the SPI bit 7 to “1”
- SPI status registers are in general not cleared or changed automatically (an exception are the **WD_FAIL** bits). This must be done by the microcontroller via SPI command

The registers are addressed wordwise.

15.6.1 General Status Registers

SUP_STAT_2
Supply Voltage Fail Status (Address 100 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0x0x xxxx$_B$**

7	6	5	4	3	2	1	0
Reserved	**VS_UV**	**Reserved**	**VCC3_OC**	**VCC3_UV**	**VCC3_OT**	**VCC1_OV**	**VCC1_WARN**
r	rc	r	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
VS_UV	6	rc	**VS Undervoltage Detection ($V_{S,UV}$)** 0B , No VS undervoltage detected 1B , VS undervoltage detected
Reserved	5	r	**Reserved, always reads as 0**
VCC3_OC	4	rc	**VCC3 Overcurrent Detection** 0B , No OC 1B , OC detected
VCC3_UV	3	rc	**VCC3 Undervoltage Detection** 0B , No VCC3 UV detection 1B , VCC3 UV Fail detected
VCC3_OT	2	rc	**VCC3 Overtemperature Detection** 0B , No overtemperature 1B , VCC3 overtemperature detected
VCC1_ OV	1	rc	**VCC1 Overvoltage Detection ($V_{CC1,OV,r}$)** 0B , No VCC1 overvoltage warning 1B , VCC1 overvoltage detected
VCC1_ WARN	0	rc	**VCC1 Undervoltage Prewarning ($V_{PW,f}$)** 0B , No VCC1 undervoltage prewarning 1B , VCC1 undervoltage prewarning detected

Notes

1. *The VCC1 undervoltage prewarning threshold $V_{PW,f}$ / $V_{PW,r}$ is a fixed threshold and independent of the VCC1 undervoltage reset thresholds.*

SUP_STAT_1
Supply Voltage Fail Status (Address 100 0001$_B$)
POR / Soft Reset Value: y000 0000$_B$; **Restart Value: xxxx xx0x$_B$**

7	6	5	4	3	2	1	0
POR	**VSHS_UV**	**VSHS_OV**	**VCC2_OT**	**VCC2_UV**	**VCC1_SC**	**VCC1_UV_FS**	**VCC1_UV**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
POR	7	rc	**Power-On Reset Detection** 0B , No POR 1B , POR occurred
VSHS_UV	6	rc	**VSHS Undervoltage Detection ($V_{SHS,UVD}$)** 0B , No VSHS-UV 1B , VSHS-UV detected
VSHS_OV	5	rc	**VSHS Overvoltage Detection ($V_{SHS,OVD}$)** 0B , No VSHS-OV 1B , VSHS-OV detected
VCC2_OT	4	rc	**VCC2 Overtemperature Detection** 0B , No overtemperature 1B , VCC2 overtemperature detected
VCC2_UV	3	rc	**VCC2 Undervoltage Detection ($V_{CC2,UV,f}$)** 0B , No VCC2 undervoltage 1B , VCC2 undervoltage detected
VCC1_SC	2	rc	**VCC1 Short to GND Detection (<Vrtx for t>4ms after switch on)** 0B , No short 1B , VCC1 short to GND detected
VCC1_UV_FS	1	rc	**VCC1 UV-Detection (due to Vrtx reset)** 0B , No Fail-Safe Mode entry due to 4th consecutive VCC1_UV 1B , Fail-Safe Mode entry due to 4th consecutive VCC1_UV
VCC1_UV	0	rc	**VCC1 UV-Detection (due to Vrtx reset)** 0B , No VCC1_UV detection 1B , VCC1 UV-Fail detected

Notes

1. *The MSB of the POR/Soft Reset value is marked as 'y': the default value of the POR bit is set after Power-on reset (POR value = 1000 0000). However it will be cleared after a SBC Soft Reset command (Soft Reset value = 0000 0000).*
2. *During Sleep Mode, the bits VCC1_SC,VCC1_OV and VCC1_UV will not be set when VCC1 is off*
3. *The VCC1_UV bit is never updated in SBC Restart Mode, in SBC Init Mode it is only updated after RO was released for the first time, it is always updated in SBC Normal and Stop Mode, and it is always updated in any SBC modes in a VCC1_SC condition (after VCC1_UV = 1 for >4ms).*

THERM_STAT
Thermal Protection Status (Address 100 0010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0xxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**TSD2**	**TSD1**	**TPW**
r	r	r	r	r	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
TSD2	2	rc	**TSD2 Thermal Shut-Down Detection** 0B , No TSD2 event 1B , TSD2 OT detected - leading to SBC Fail-Safe Mode
TSD1	1	rc	**TSD1 Thermal Shut-Down Detection** 0B , No TSD1 fail 1B , TSD1 OT detected
TPW	0	rc	**Thermal Pre Warning** 0B , No Thermal Pre warning 1B , Thermal Pre warning detected

Note: TSD1 and TSD2 are not reset automatically, even if the temperature pre warning or TSD1 OT condition is not present anymore. Also TSD2 is not reset.

DEV_STAT
Device Information Status (Address 100 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xx00 xxxx$_B$**

7	6	5	4	3	2	1	0
DEV_STAT_1	**DEV_STAT_0**	**Reserved**	**Reserved**	**WD_FAIL_1**	**WD_FAIL_0**	**SPI_FAIL**	**FAILURE**
rc	rc	r	r	rh	rh	rc	rc

Field	Bits	Type	Description
DEV_STAT	7:6	rc	**Device Status before Restart Mode** 00B , Cleared (Register must be actively cleared) 01B , Restart due to failure (WD fail, TSD2, VCC1_UV); also after a wake from Fail-Safe Mode 10B , Sleep Mode 11B , Reserved
Reserved	5:4	r	**Reserved, always reads as 0**
WD_FAIL	3:2	rh	**Number of WD-Failure Events (1/2 WD failures depending on CFG)** 00B , No WD Fail 01B , 1x WD Fail, FOx activation - Config 2 selected 10B , 2x WD Fail, FOx activation - Config 1 / 3 / 4 selected 11B , Reserved (never reached)
SPI_FAIL	1	rc	**SPI Fail Information** 0B , No SPI fail 1B , Invalid SPI command detected
FAILURE	0	rc	**Activation of Fail Output FO** 0B , No Failure 1B , Failure occurred

Notes

1. *The bits **DEV_STAT** show the status of the device before it went through Restart. Either the device came from regular Sleep Mode (‘10’) or a failure (‘01’ - SBC Restart or SBC Fail-Safe Mode: WD fail, TSD2 fail, VCC_UV fail or VCC1_OV if bit **VCC1_OV_RST** is set) occurred. Failure is also an illegal command from SBC Stop to SBC Sleep Mode or going to SBC Sleep Mode without activation of any wake source. Coming from SBC Sleep Mode (‘10’) will also be shown if there was a trial to enter SBC Sleep Mode without having cleared all wake flags before.*
2. *The **WD_FAIL** bits are configured as a counter and are the only status bits, which are cleared automatically by the SBC. They are cleared after a successful watchdog trigger and when the watchdog is stopped (also in SBC Sleep and Fail-Safe Mode unless it was reached due to a watchdog failure). See also **Chapter 13.1**.*
3. *The SPI_FAIL bit is cleared only by SPI command*
4. *In case of Config 2/4 the WD_Fail counter is frozen in case of WD trigger failure until a successful WD trigger.*
5. *If CFG = ‘0’ then a 1st watchdog failure will not trigger the FO outputs or the FAILURE bit but only force the SBC into SBC Restart Mode.*

BUS_STAT_1
Bus Communication Status (Address 100 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 000x xxxx$_B$**

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**CANTO**	**SYSERR**	**CAN_FAIL_1**	**CAN_FAIL_0**	**VCAN_UV**
r	r	r	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
Reserved	6:5	r	**Reserved, always reads as 0**
CANTO	4	rc	**CAN Time Out Detection** 0B , Normal operation 1B , CAN Time Out detected
SYSERR	3	rc	**SWK System Error** 0B , Selective Wake Mode is possible 1B , System Error detected, SWK enabling not possible
CAN_FAIL	2:1	rc	**CAN Failure Status** 00B , No error 01B , CAN TSD shutdown 10B , CAN_TXD_DOM: TXD dominant time out for longer than $t_{TxD_CAN_TO}$ 11B , CAN_BUS_DOM: BUS dominant time out for longer than $t_{TxD_CAN_TO}$
VCAN_UV	0	rc	**Undervoltage CAN Bus Supply** 0B , Normal operation 1B , CAN Supply undervoltage detected. Transmitter disabled

Notes

1. *CAN Recovery Conditions:*
   1.) TXD Time Out: TXD goes HIGH or transmitter is set to wake capable or switched off;
   2.) Bus dominant time out: Bus will become recessive or transceiver is set to wake capable or switched off.
   3.) Supply undervoltage: as soon as the threshold is crossed again, i.e. VCAN > VCAN_UV for CAN
   4.)In all cases (also for TSD shutdown): to enable the Bus transmission again, TXD needs to be HIGH for a certain time (transmitter enable time).
2. *The VCAN_UV comparator is enabled if the mode bit CAN_1 = '1', i.e. in CAN Normal or CAN Receive Only Mode.*
3. *CANTO will be set only if CAN2 = 1 (=SWK Mode enabled). It will be set as soon as CANSIL was set and will stay set even in CANSIL it is reset. An interrupt is issued in SBC Stop- and SBC Normal Mode as soon as CANTO is set and the interrupt is not masked out, i.e. CANTO_MASK must be set to 1.*
4. *The SYSERR Flag is set in case of a configuration error and in case of an error counter overflow (n>32). It is only updated if SWK is enabled (CAN_2 = '1'). See also **Chapter 5.4.3**.*
5. *CANTO is set asynchronously to the INT pulse. In order to prevent undesired clearing of CANTO and thus possibly missing this interrupt, the bit will be prevented from clearing (i.e. cannot be cleared) until the next falling edge of INT.*

WK_STAT_1
Wake-up Source and Information Status (Address 100 0110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 00xx 0xxx$_B$**

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**CAN_WU**	**TIMER_WU**	**Reserved**	**WK3_WU**	**WK2_WU**	**WK1_WU**
r	r	rc	rc	r	rc	rc	rc

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
Reserved	6	r	**Reserved, always reads as 0**
CAN_WU	5	rc	**Wake up via CAN Bus** 0B , No Wake up 1B , Wake up
TIMER_WU	4	rc	**Wake up via TimerX** 0B , No Wake up 1B , Wake up
Reserved	3	r	**Reserved, always reads as 0**
WK3_WU	2	rc	**Wake up via WK3** 0B , No Wake up 1B , Wake up
WK2_WU	1	rc	**Wake up via WK2** 0B , No Wake up 1B , Wake up
WK1_WU	0	rc	**Wake up via WK1** 0B , No Wake up 1B , Wake up

Note: The respective wake source bit will also be set when the device is woken from SBC Fail-Safe Mode

WK_STAT_2
Wake-up Source and Information Status (Address 100 0111$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 00xx 0000$_B$**

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**GPIO2_WU**	**GPIO1_WU**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
r	r	rc	rc	r	r	r	r

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
GPIO2_WU	5	rc	**Wake up via GPIO2** 0B , No Wake up 1B , Wake up
GPIO1_WU	4	rc	**Wake up via GPIO1** 0B , No Wake up 1B , Wake up
Reserved	3:0	r	**Reserved, always reads as 0**

WK_LVL_STAT
WK Input Level (Address 100 1000_B)
POR / Soft Reset Value: xx00 $0xxx_B$; Restart Value: xxxx $0xxx_B$

7	6	5	4	3	2	1	0
SBC_DEV_LVL	**CFGP**	**GPIO2_LVL**	**GPIO1_LVL**	**Reserved**	**WK3_LVL**	**WK2_LVL**	**WK1_LVL**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
SBC_DEV_LVL	7	r	**Status of SBC Operating Mode at FO3/TEST Pin** 0B , User Mode activated 1B , SBC Development Mode activated
CFGP	6	r	**Device Configuration Status** 0B , No external pull-up resistor connected on INT (Config 2/4) 1B , External pull-up resistor connected on INT (Config 1/3)
GPIO2_LVL	5	r	**Status of GPIO2 (if selected as GPIO)** 0B , Low Level (=0) 1B , High Level (=1)
GPIO1_LVL	4	r	**Status of GPIO1 (if selected as GPIO)** 0B , Low Level (=0) 1B , High Level (=1)
Reserved	3	r	**Reserved, always reads as 0**
WK3_LVL	2	r	**Status of WK3** 0B , Low Level (=0) 1B , High Level (=1)
WK2_LVL	1	r	**Status of WK2** 0B , Low Level (=0) 1B , High Level (=1)
WK1_LVL	0	r	**Status of WK1** 0B , Low Level (=0) 1B , High Level (=1)

Note: GPIOx_LVL is updated in SBC Normal and Stop Mode if configured as wake input, low-side switch or high-side switch.
In cyclic sense or wake mode, the registers contain the sampled level, i.e. the registers are updated after every sampling. The GPIOs are not capable of cyclic sensing.
If selected as GPIO then the respective level is shown even if configured as low-side or high-side.

HS_OC_OT_STAT
High-Side Switch Overload Status (Address 101 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**HS4_OC_OT**	**HS3_OC_OT**	**HS2_OC_OT**	**HS1_OC_OT**
r	r	r	r	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
HS4_OC_OT	3	rc	**Overcurrent & Overtemperature Detection HS4** 0B , No OC or OT 1B , OC or OT detected
HS3_OC_OT	2	rc	**Overcurrent & Overtemperature Detection HS3** 0B , No OC or OT 1B , OC or OT detected
HS2_OC_OT	1	rc	**Overcurrent & Overtemperature Detection HS2** 0B , No OC or OT 1B , OC or OT detected
HS1_OC_OT	0	rc	**Overcurrent & Overtemperature Detection HS1** 0B , No OC or OT 1B , OC or OT detected

*Note: The OC/OT bit might be set for $V_{POR,f} < VS < 5.5V$ (see also **Chapter 4.2**)*

HS_OL_STAT
High-Side Switch Open-Load Status (Address 101 0101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**HS4_OL**	**HS3_OL**	**HS2_OL**	**HS1_OL**
r	r	r	r	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
HS4_OL	3	rc	**Open-Load Detection HS4** 0B , No OL 1B , OL detected
HS3_OL	2	rc	**Open-Load Detection HS3** 0B , No OL 1B , OL detected
HS2_OL	1	rc	**Open-Load Detection HS2** 0B , No OL 1B , OL detected
HS1_OL	0	rc	**Open-Load Detection HS1** 0B , No OL 1B , OL detected

15.6.2 Selective Wake Status Registers

SWK_STAT
Selective Wake Status (Address 111 0000_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $0x00\ xxxx_B$

7	6	5	4	3	2	1	0
Reserved	**SYNC**	**Reserved**	**Reserved**	**CANSIL**	**SWK_SET**	**WUP**	**WUF**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
SYNC	6	r	**Synchronisation (at least one CAN frame without fail must have been received)** 0B , SWK function not working or not synchronous to CAN bus 1B , Valid CAN frame received, SWK function is synchronous to CAN bus
Reserved	5:4	r	**Reserved, always reads as 0**
CANSIL	3	r	**CAN Silent Time during SWK operation** 0B , tsilence not exceeded 1B , set if tsilence is exceeded.
SWK_SET	2	r	**Selective Wake Activity** 0B , Selective Wake is not active 1B , Selective Wake is activated
WUP	1	r	**Wake-up Pattern Detection** 0B , No WUP 1B , WUP detected
WUF	0	r	**SWK Wake-up Frame Detection (acc. ISO 11898-2:2016)** 0B , No WUF 1B , WUF detected

Note: SWK_SET is set to flag that the selective wake functionality is activated (SYSERR = 0, CFG_VAL = 1, CAN_2 = 1). The selective wake function is activated via a CAN mode change, except if CAN = '100'.

SWK_ECNT_STAT
SWK Status (Address 111 0001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00xx xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**ECNT_5**	**ECNT_4**	**ECNT_3**	**ECNT_2**	**ECNT_1**	**ECNT_0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
ECNT	5:0	r	**SWK CAN Frame Error Counter** 00 0000B, No Frame Error 01 1111B, 31 Frame Errors have been counted 10 0000B, Error counter overflow - SWK function will be disabled

Note: If a frame has been received that is valid according to ISO 11898-1 and the counter is not zero, then the counter shall be decremented. If the counter has reached a value of 32, the following actions shall be performed: Selective Wake function shall be disabled, SYSERR shall be set and CAN wake capable function shall be enabled, which leads to a wake with the next WUP.

SWK_CDR_STAT1
CDR Status 1 Register (Address 111 0010$_B$)
POR / Soft Reset Value: 1010 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
N_AVG_11	**N_AVG_10**	**N_AVG_9**	**N_AVG_8**	**N_AVG_7**	**N_AVG_6**	**N_AVG_5**	**N_AVG_4**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
NAVG_SAT	7:0	r	**Output Value from Filter Block** N_AVG is representing the integer part of the number of selected input clock frequency per CAN bus bit. N_AVG[11:4] e.g.160.75

SWK_CDR_STAT2
CDR Status 2 Register (Address 111 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
N_AVG_3	**N_AVG_2**	**N_AVG_1**	**N_AVG_0**	**reserved**	**reserved**	**reserved**	**reserved**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
NAVG_SAT	7:4	r	**Output Value from Filter Block** N_AVG is representing the fractional part of the number of selected input clock frequency per CAN bus bit. N_AVG[3:0] e.g.160.75
Reserved	3:0	r	**Reserved, always reads as 0**

15.6.3 Family and Product Information Register

FAM_PROD_STAT
Family and Product Identification Register (Address 111 1110$_B$)
POR / Soft Reset Value: 0011 yyyy $_B$; Restart Value: 0011 yyyy$_B$

7	6	5	4	3	2	1	0
FAM_3	**FAM_2**	**FAM_1**	**FAM_0**	**PROD_3**	**PROD_2**	**PROD_1**	**PROD_0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FAM	7:4	r	**SBC Family Identifier (bit4=LSB; bit7=MSB)** 0 001B, Driver SBC Family 0 010B, DC/DC-SBC Family 0 011B, Mid-Range SBC Family 0 100B, Multi-CAN SBC Family 0 101B, Lite-CAN SBC Family 0 111B, Mid-Range+ SBC Family x x x xB, reserved for future products
PROD	3:0	r	**SBC Product Identifier (bit0=LSB; bit3=MSB)** 0 0 1 0B, reserved 0 1 1 0B, TLE9261-3QX (VCC1 = 5V, no LIN, VCC3, SWK) 1 0 1 0B, TLE9262-3QX (VCC1 = 5V, 1 LIN, VCC3, SWK) 1 1 1 0B, TLE9263-3QX (VCC1 = 5V, 2 LIN, VCC3, SWK) (default device when untrimmed)

Notes

1. *The actual default register value after POR, Soft Reset or Restart of PROD will depend on the respective product. Therefore the value ‘y’ is specified.*
2. *SWK = Selective Wake feature in CAN Partial Networking standard*

15.7 Electrical Characteristics

Table 37 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	4.0	MHz	1)	P_16.7.1
SPI Interface; Logic Inputs SDI, CLK and CSN							
H-input Voltage Threshold	V_{IH}	–	–	0.7* V_{CC1}	V	–	P_16.7.2
L-input Voltage Threshold	V_{IL}	0.3* V_{CC1}	–	–	V	–	P_16.7.3
Hysteresis of input Voltage	V_{IHY}	0.08 × V_{CC1}	0.12 × V_{CC1}	0.5 × V_{CC1}	V	1)	P_16.7.4
Pull-up Resistance at pin CSN	R_{ICSN}	20	40	80	kΩ	V_{CSN} = 0.7 x V_{CC1}	P_16.7.5
Pull-down Resistance at pin SDI and CLK	$R_{ICLK/SDI}$	20	40	80	kΩ	$V_{SDI/CLK}$ = 0.2 x V_{CC1}	P_16.7.6
Input Capacitance at pin CSN, SDI or CLK	C_I	–	10	–	pF	1)	P_16.7.7
Logic Output SDO							
H-output Voltage Level	V_{SDOH}	V_{CC1} - 0.4	V_{CC1} - 0.2	–	V	I_{DOH} = -1.6 mA	P_16.7.8
L-output Voltage Level	V_{SDOL}	–	0.2	0.4	V	I_{DOL} = 1.6 mA	P_16.7.9
Tristate Leakage Current	I_{SDOLK}	-10	–	10	µA	V_{CSN} = V_{CC1}; 0 V < V_{DO} < V_{CC1}	P_16.7.10
Tristate Input Capacitance	C_{SDO}	–	10	15	pF	1)	P_16.7.11
Data Input Timing[1)]							
Clock Period	t_{pCLK}	250	–	–	ns	–	P_16.7.12
Clock High Time	t_{CLKH}	125	–	–	ns	–	P_16.7.13
Clock Low Time	t_{CLKL}	125	–	–	ns	–	P_16.7.14
Clock Low before CSN Low	t_{bef}	125	–	–	ns	–	P_16.7.15
CSN Setup Time	t_{lead}	250	–	–	ns	–	P_16.7.16
CLK Setup Time	t_{lag}	250	–	–	ns	–	P_16.7.17
Clock Low after CSN High	t_{beh}	125	–	–	ns	–	P_16.7.18
SDI Set-up Time	t_{DISU}	100	–	–	ns	–	P_16.7.19
SDI Hold Time	t_{DIHO}	50	–	–	ns	–	P_16.7.20
Input Signal Rise Time at pin SDI, CLK and CSN	t_{rIN}	–	–	50	ns	–	P_16.7.21

Table 37 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Signal Fall Time at pin SDI, CLK and CSN	t_{fIN}	–	–	50	ns	–	P_16.7.22
Delay Time for Mode Changes[2)]	$t_{Del,Mode}$	–	–	6	µs	includes internal oscillator tolerance	P_16.7.23
CSN High Time	$t_{CSN(high)}$	3	–	–	µs	–	P_16.7.24
Data Output Timing[1)]							
SDO Rise Time	t_{rSDO}	–	30	80	ns	C_L = 100 pF	P_16.7.25
SDO Fall Time	t_{fSDO}	–	30	80	ns	C_L = 100 pF	P_16.7.26
SDO Enable Time	t_{ENSDO}	–	–	50	ns	low impedance	P_16.7.27
SDO Disable Time	t_{DISSDO}	–	–	50	ns	high impedance	P_16.7.28
SDO Valid Time	t_{VASDO}	–	–	50	ns	C_L = 100 pF	P_16.7.29

1) Not subject to production test; specified by design

2) Applies to all mode changes triggered via SPI commands

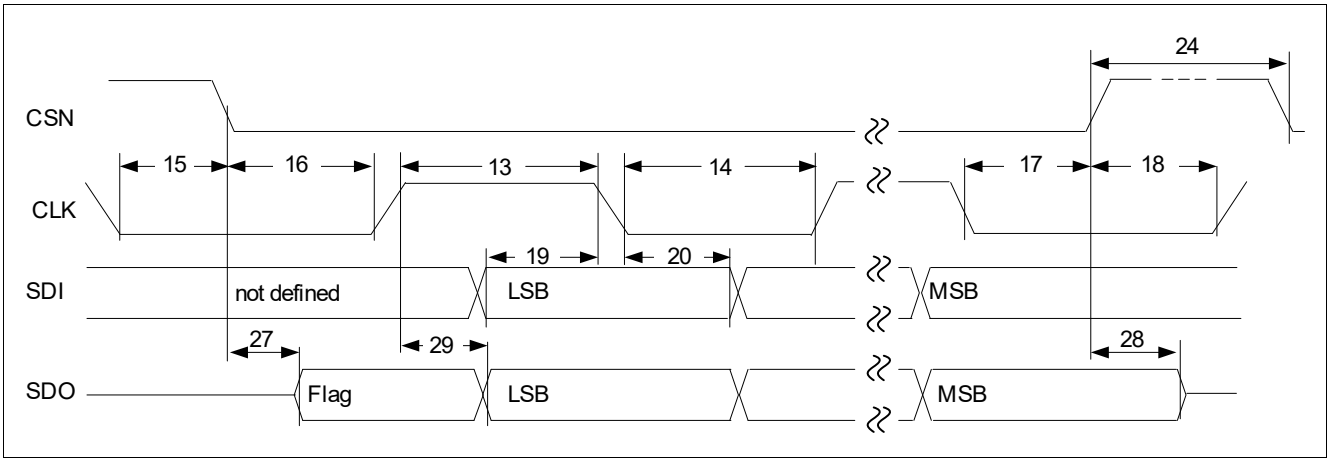

Figure 57 SPI Timing Diagram

Note: Numbers in drawing correlate to the last 2 digits of the Number field in the Electrical Characteristics table.

16 Application Information

16.1 Application Diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

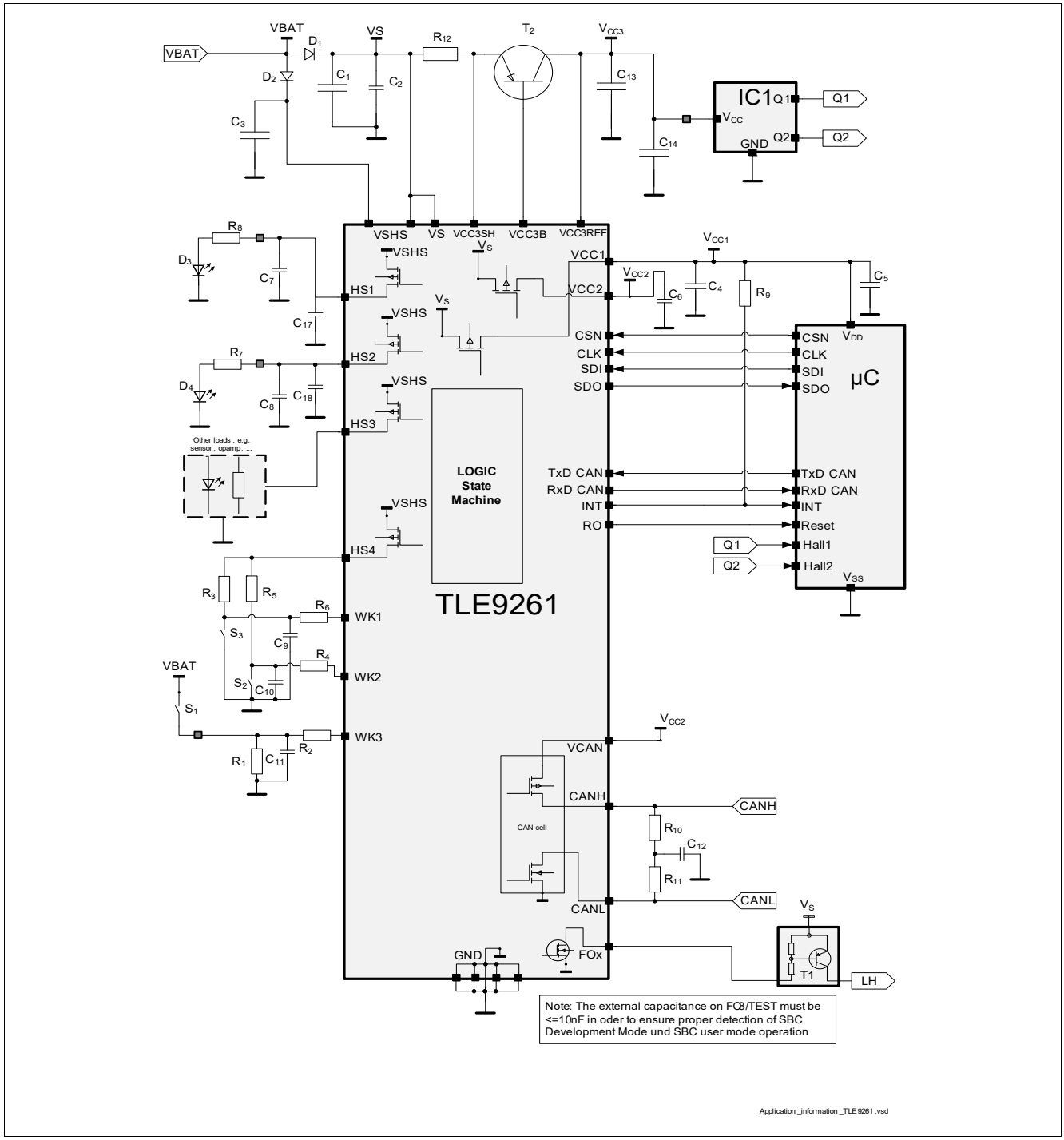

Figure 58 Simplified Application Diagram

Application Information

Note: Unused outputs are recommended to be left unconnected on the application board. If unused output pins are routed to an external connector which leaves the ECU, then these pins should have provision for a zero ohm jumper (depopulated if unused) or ESD protection.

Table 38 Bill of Material for Simplified Application Diagram

Ref.	Typical Value	Purpose / Comment
Capacitances		
C1	68µF	Buffering capacitor to cut off battery spikes, depending on application
C2	100nF	EMC, blocking capacitor
C3	22µF	Buffering capacitor to cut off battery spikes from VSHS as separate supply input; Depending on application, only needed if VSHS is not connected to VS;
C4	2.2µF low ESR	As required by application, min. 470nF for stability and max. 68µF recommended
C5	100nF ceramic	Spike filtering, improve stability of supply for microcontroller; not needed for SBC
C6	2.2µF low ESR	Blocking capacitor, min. 470nF for stability; if used for CAN supply place a 100nF ceramic capacitor in addition very close to VCAN pin for optimum EMC behavior
C7	33nF	As required by application, mandatory protection for off-board connections
C8	33nF	As required by application, mandatory protection for off-board connections
C17	47pF	Only required in case of off-board connection to optimize EMC behavior, place close to pin
C18	47pF	Only required in case of off-board connection to optimize EMC behavior, place close to pin
C9	10nF	Spike filtering, as required by application, mandatory protection for off-board connections (see also Simplified Application Diagram with the Alternate Measurement Function)
C10	10nF	Spike filtering, as required by application, mandatory protection for off-board connections
C11	10nF	Spike filtering, as required by application, mandatory protection for off-board connections
C12	4.7nF / OEM dependent	Split termination stability
C13	10µF low ESR	Stability of VCC3, ceramic capacitor, e.g. Murata 10 µF/10 V GCM31CR71A106K64L or 2x 4.7 µF/10 V
C14	47nF	Only required in case of off-board connection to optimize EMC behavior, place close to connector
Resistances		
R1	10kΩ	Wetting current of the switch, as required by application
R2	10kΩ	Limit the WK pin current, e.g. for ISO pulses
R3	10kΩ	Wetting current of the switch, as required by application

Table 38 Bill of Material for Simplified Application Diagram (cont'd)

Ref.	Typical Value	Purpose / Comment
R4	10kΩ	Limit the WK pin current, e.g. for ISO pulses
R5	10kΩ	Wetting current of the switch, as required by application
R6	10kΩ	Limit the WK pin current, e.g. for ISO pulses
R7	depending on LED config.	LED current limitation, as required by application
R8	depending on LED config.	LED current limitation, as required by application
R9	47kΩ	Selection of hardware configuration 1/3, i.e. in case of WD failure SBC Restart Mode is entered. If not connected, then hardware configuration 2/4 is selected
R10	60Ω / OEM dependent	CAN bus termination
R11	60Ω / OEM dependent	CAN bus termination
R12	1Ω shunt, depending on required current limitation or load sharing ratio	Sense shunt for ICC3 current limitation (configured to typ. 235mA with 1Ω shunt) for stand-alone configuration; Setting of load sharing ratio (here ICC3/ICC1 = 1) in load sharing configuration.
R15	10kΩ	WK1 pin current limitation, e.g. for ISO pulses, for alternate measurement function (see also Simplified Application Diagram with the Alternate Measurement Function)
R16	depending on application and microcontroller	Voltage Divider resistor to adjust measurement voltage to microcontroller ADC input range (see also Simplified Application Diagram with the Alternate Measurement Function)
R17	depending on application and microcontroller	Voltage Divider resistor to adjust measurement voltage to microcontroller ADC input range (see also Simplified Application Diagram with the Alternate Measurement Function)
Active Components		
D1	e.g. BAS 3010A, Infineon	Reverse polarity protection for VS supply pins
D2	e.g. BAS 3010A, Infineon	Reverse polarity protection for VSHS supply pin; if separate supplies are not needed, then connect VSHS to VS pins
D3	LED	As required by application, configure series resistor accordingly
D4	LED	As required by application, configure series resistor accordingly
T1	e.g. BCR191W	High active FO control
T2	BCP 52-16, Infineon	Power element of VCC3, current limit or load sharing ratio to be configured via shunt
	MJD 253, ON Semi	Alternative power element of VCC3
µC	e.g. TC2xxx	Microcontroller

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

Application Information

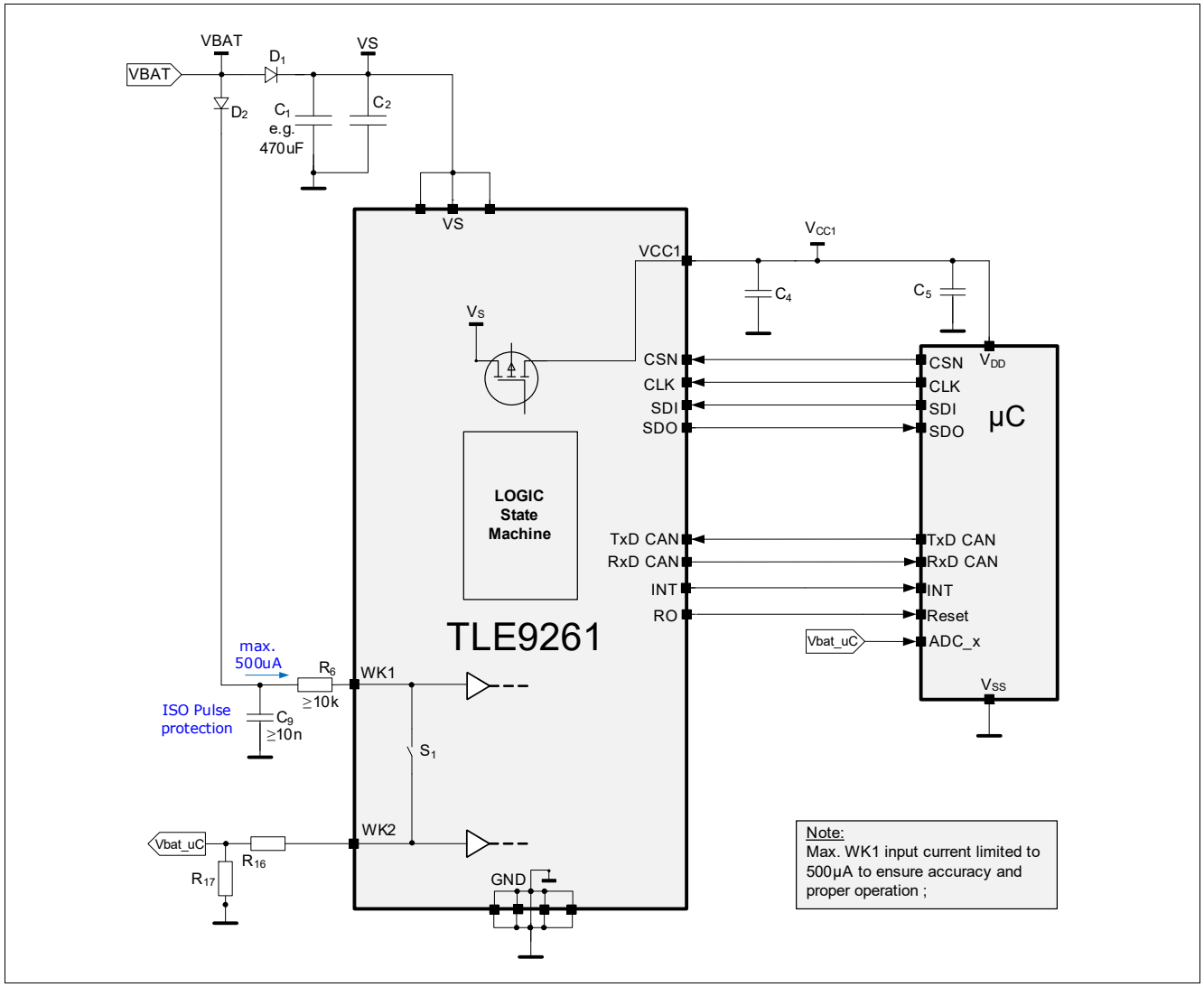

Figure 59 Simplified Application Diagram with the Alternate Measurement Function via WK1 and WK2

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.WK1 must be connected to signal to be measured and WK2 is the output to the microcontroller supervision function. The maximum current into WK1 must be <500uA. The minimum current into WK1 should be >5uA to ensure proper operation.

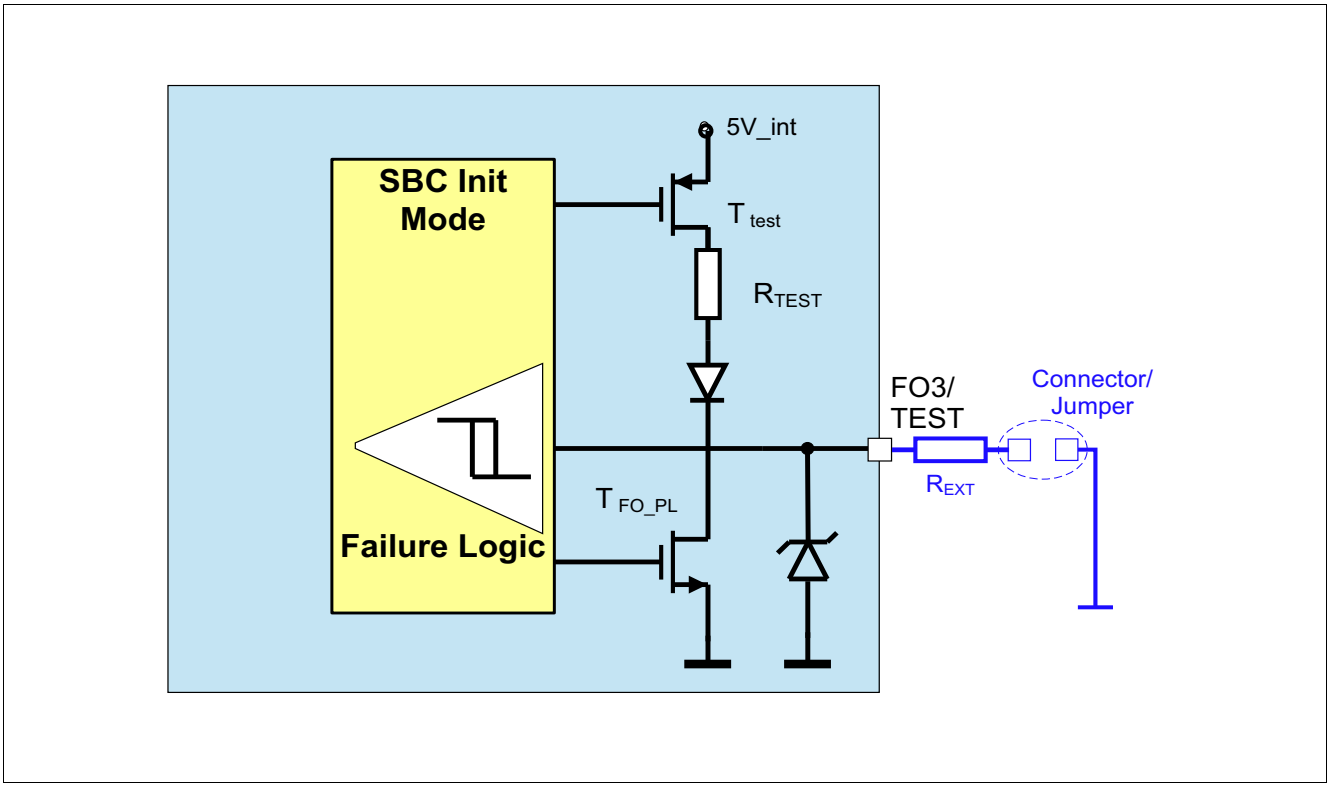

Figure 60 Hint for Increasing the Robustness of pin FO3/TEST during Debugging or Programming

16.2 ESD Tests

*Note: Tests for ESD robustness according to IEC61000-4-2 “gun test” (150pF, 330Ω) has been performed. The results and test conditions are available in a test report. The target values for the test are listed in **Table 39** below.*

Table 39 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin CANH, CANL, VS, WK1..3, HSx, VCC2, VCC3 versus GND	>6	kV	1)2) positive pulse
ESD at pin CANH, CANL, VS, WK1..3, HSx, VCC2, VCC3 versus GND	< -6	kV	1)2) negative pulse

1) ESD Test “Gun Test” is specified with external components for pins VS, WK1..3, HSx, VCC3 and VCC2. See the application diagram in **Chapter 16.1** for more information.

2) ESD susceptibility “ESD GUN” according LIN EMC 1.3 Test Specification, Section 4.3 (IEC 61000-4-2). Tested by external test house (IBEE Zwickau, EMC Test report Nr. 04-01-17)

EMC and ESD susceptibility tests according to SAE J2962-2 (2010) have been performed. Tested by external test house (UL LLC).

16.3 Thermal Behavior of Package

Below figure shows the thermal resistance (R_{th_JA}) of the device vs. the cooling area on the bottom of the PCB for Ta = 85°C. Every line reflects a different PCB and thermal via design.

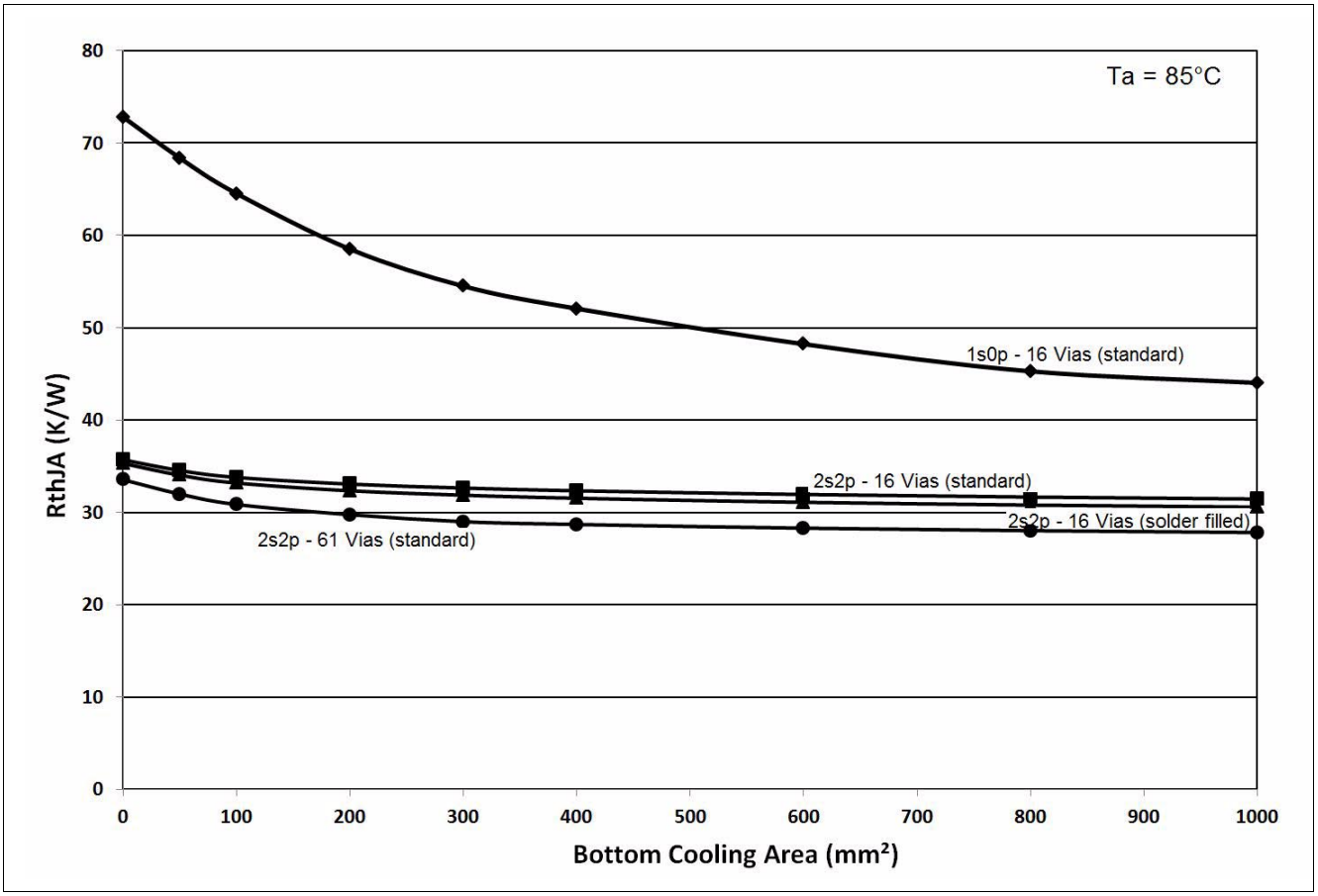

Figure 61 Thermal Resistance (R_{th_JA}) vs. Cooling Area

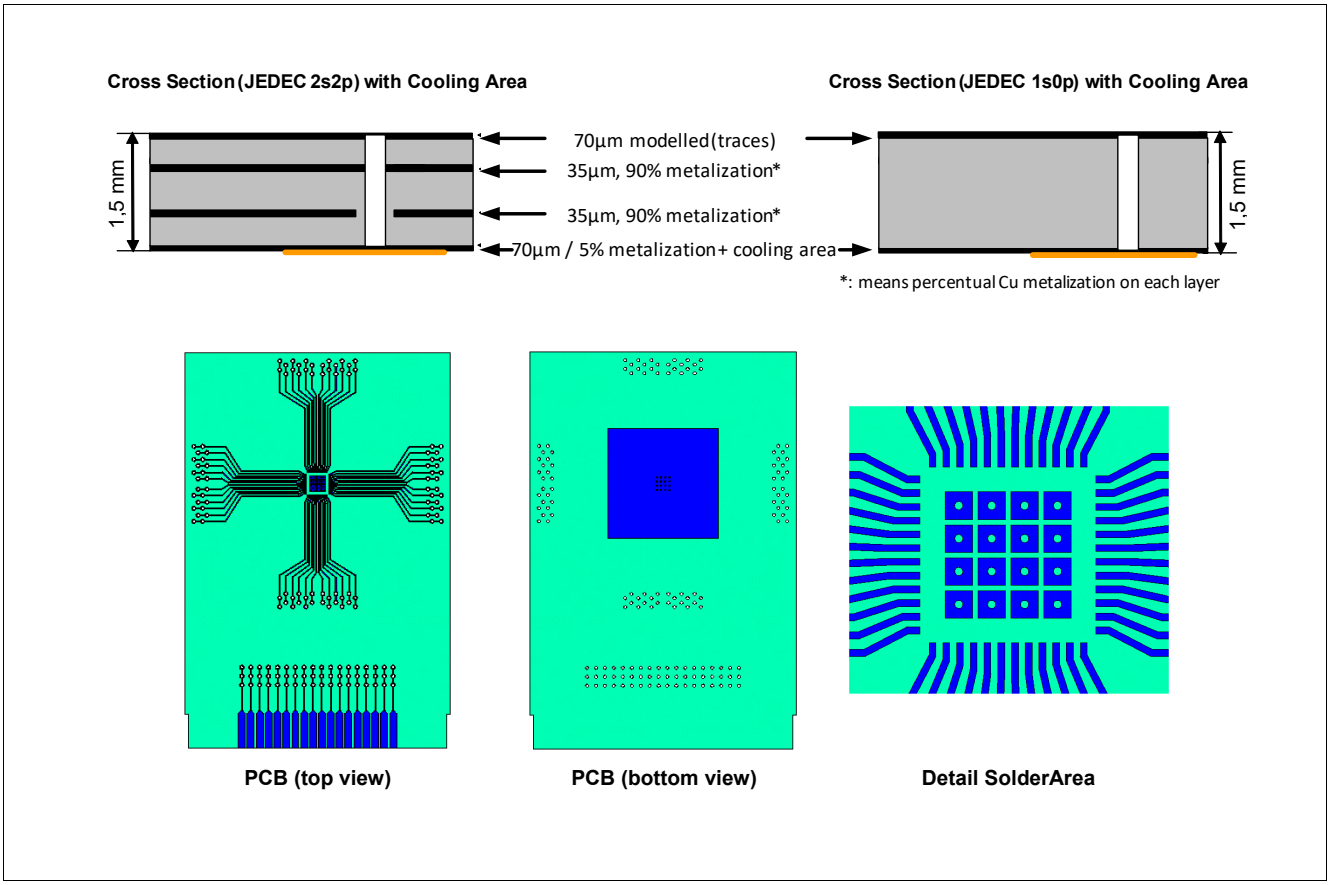

Figure 62 Board Setup

Board setup is defined according to JESD 51-2,-5,-7.
Board: 76.2x114.3x1.5mm^3 with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer (70µm).

17 Package Outlines

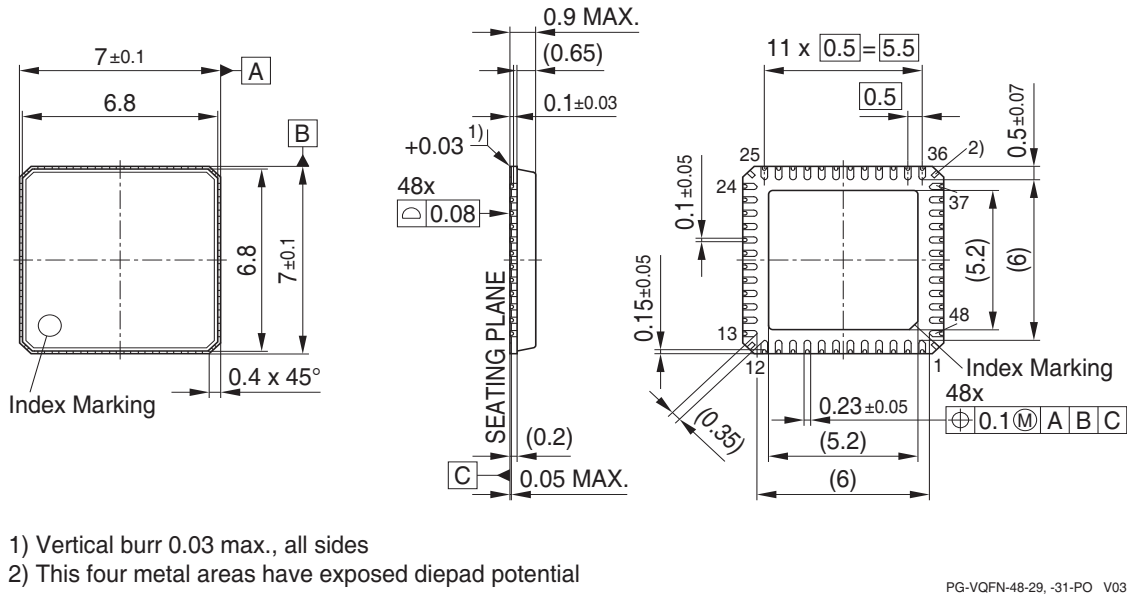

Figure 63 PG-VQFN-48-31

Note: Dimensions in mm.
The tie bars have an internal connection to the exposed pad.
*For assembly recommendations please also refer to the documents "Recommendations for Board Assembly (VQFN and IQFN)" and "VQFN48 Layout Hints" on the Infineon website (**www.infineon.com**).*

The PG-VQFN-48-31 package is a leadless exposed pad power package featuring Lead Tip Inspection (LTI) to support Automatic Optical Inspection (AOI).

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

18 Revision History

Revision	Date	Changes
Rev. 1.1	2019-09-27	Datasheet updated: • Editorial changes • Updated **Table 4** – corrected footnote 9) to match P_4.4.33, i.e changed 525µA to 550µA • **Chapter 5.1.4** “SBC Sleep Mode”: added condition for CAN mode handling before SBC Sleep Mode entry • **Table 9** “CAN Modes ...”: CAN_x bits for CAN Receive Only (no SWK) • **Figure 3** “State Diagram ...”: added footnote with condition for CAN mode handling before SBC Sleep Mode entry • **Figure 31** “CAN Mode Control Diagram”: added Footnote 2) with condition for CAN mode handling before SBC Sleep Mode entry • Updated **Table 24** – added P_10.3.57 and P_10.3.58 (no product change) – added P_10.3.59, P_10.3.60, P_10.3.61 and P_10.3.62 – tightened P_10.3.16 – tightened P_10.3.39 and P_10.3.40 by additional footnote • **Figure 10.2.4** “CAN Wake Capable Mode”, rearming the transceiver for wake capability: added condition for CAN mode handling before SBC Sleep Mode entry • **SWK_CTRL**: added note (5.) to SWK_CTRL register
Rev. 1.0	2017-07-31	Initial Release

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