



Integrated  
Circuit  
Systems, Inc.

**PRELIMINARY**

# ICS8430252-45

## FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

### GENERAL DESCRIPTION

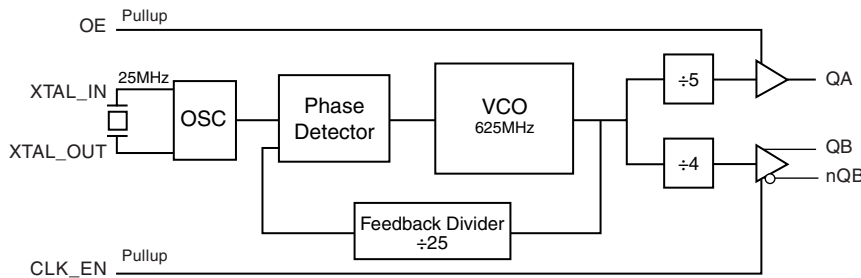


The ICS8430252-45 is a 2 output LVPECL and LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated: 156.25MHz LVPECL output and, 125MHz LVCMOS output. The 8430252-45 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS8430252-45 is packaged in a small 16-pin TSSOP package.

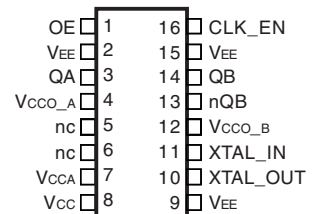
### FEATURES

- One differential 3.3V LVPECL output and One LVCMOS/LVTTL output
- Crystal oscillator interface designed for a 25MHz, 18pF parallel resonant crystal
- A 25MHz crystal generates both an output frequency of 156.25MHz (LVPECL) and 125MHz (LVCMOS)
- VCO frequency: 625MHz
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz) using a 25MHz crystal: 0.39ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request
- Available in both standard and lead-free RoHS compliant packages

### BLOCK DIAGRAM



### PIN ASSIGNMENT



### ICS8430252-45 16-Lead TSSOP

4.4mm x 5.0mm x 0.92mm  
package body  
**G Package**  
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



**TABLE 1. PIN DESCRIPTIONS**

| Number   | Name                 | Type   |        | Description  |
|----------|----------------------|--------|--------|--|
| 1        | OE                   | Input  | Pullup | Output enable pin. LVCMOS/LVTTL interface levels. See Table 3A Function Table. |
| 2, 9, 15 | V <sub>EE</sub>      | Power  |        | Negative supply pin.   |
| 3        | QA                   | Output |        | LVCMOS/LVTTL clock output.   |
| 4        | V <sub>CCO_A</sub>   | Power  |        | Output supply pin for QA output.   |
| 5, 6     | nc                   | Unused |        | No connect.  |
| 7        | V <sub>CCA</sub>     | Power  |        | Analog supply pin.   |
| 8        | V <sub>CC</sub>      | Power  |        | Core supply pin.   |
| 10, 11   | XTAL_OUT,<br>XTAL_IN | Input  |        | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.    |
| 12       | V <sub>CCO_B</sub>   | Power  |        | Output supply pin for QB, nQB outputs.   |
| 13, 14   | nQB, QB              | Output |        | Differential clock outputs. LVPECL interface levels.                           |
| 16       | CLK_EN               | Input  | Pullup | Clock enable pin. LVCMOS/LVTTL interface levels. See Table 3B Function Table.  |

**TABLE 2. PIN CHARACTERISTICS**

| Symbol              | Parameter                     | Test Conditions   | Minimum | Typical | Maximum | Units |
|---------------------|-------------------------------|---|---------|---------|---------|-------|
| C <sub>IN</sub>     | Input Capacitance             |   |         | 4       |         | pF    |
| C <sub>PD</sub>     | Power Dissipation Capacitance | V <sub>CC</sub> , V <sub>CCA</sub> , V <sub>CCO_A</sub> , V <sub>CCO_B</sub> = 3.465V |         | 10      |         | pF    |
| R <sub>PULLUP</sub> | Input Pullup Resistor         |   |         | 51      |         | kΩ    |

**TABLE 3A. OE SELECT FUNCTION TABLE**

| Input | Output |
|-------|--------|
| OE    | QA     |
| 0     | Hi-Z   |
| 1     | Active |

**TABLE 3B. CLK\_EN SELECT FUNCTION TABLE**

| Input  | Outputs |        |
|--------|---------|--------|
|        | QB      | nQB    |
| CLK_EN |         |        |
| 0      | Low     | High   |
| 1      | Active  | Active |



**ABSOLUTE MAXIMUM RATINGS**

|  |                          |
|--|--------------------------|
| Supply Voltage, $V_{CC}$                 | 4.6V                     |
| Inputs, $V_i$                            | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_o$                           |                          |
| Continuous Current                       | 50mA                     |
| Surge Current                            | 100mA                    |
| Package Thermal Impedance, $\theta_{JA}$ | 89°C/W (0 lfpm)          |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol                   | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------------------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$                 | Core Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{CCA}$                | Analog Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{CCO\_A}, V_{CCO\_B}$ | Output Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{EE}$                 | Power Supply Current  |                 |         | 75      |         | mA    |
| $I_{CCA}$                | Analog Supply Current |                 |         | 8       |         | mA    |

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO\_A} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol   | Parameter                   | Test Conditions                              | Minimum | Typical | Maximum        | Units |
|----------|-----------------------------|--|---------|---------|----------------|-------|
| $V_{IH}$ | Input High Voltage          |  | 2       |         | $V_{CC} + 0.3$ | V     |
| $V_{IL}$ | Input Low Voltage           |  | -0.3    |         | 0.8            | V     |
| $I_{IH}$ | Input High Current          | OE, CLK_EN<br>$V_{CC} = V_{IN} = 3.465V$     |         |         | 5              |       |
| $I_{IL}$ | Input Low Current           | OE, CLK_EN<br>$V_{CC} = 3.465V, V_{IN} = 0V$ | -150    |         |                |       |
| $V_{OH}$ | Output High Voltage; NOTE 1 |  | 2.6     |         |                | V     |
| $V_{OL}$ | Output Low Voltage; NOTE 1  |  |         |         | 0.5            | V     |

NOTE 1: Outputs terminated with 50Ω to  $V_{CCO\_A}/2$ . See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

**TABLE 4C. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO\_B} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol      | Parameter                         | Test Conditions | Minimum         | Typical | Maximum         | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CCO} - 1.4$ |         | $V_{CCO} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CCO} - 2.0$ |         | $V_{CCO} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6             |         | 1.0             | V     |

NOTE 1: Outputs terminated with 50Ω to  $V_{CCO\_B} - 2V$ .



**TABLE 5. CRYSTAL CHARACTERISTICS**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|-------|
| Mode of Oscillation                |                 | Fundamental |         |         |       |
| Frequency                          |                 |             | 25      |         | MHz   |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | Ω     |
| Shunt Capacitance                  |                 |             |         | 7       | pF    |
| Drive Level                        |                 |             |         | 1       | mW    |

NOTE: Characterized using an 18pF parallel resonant crystal.

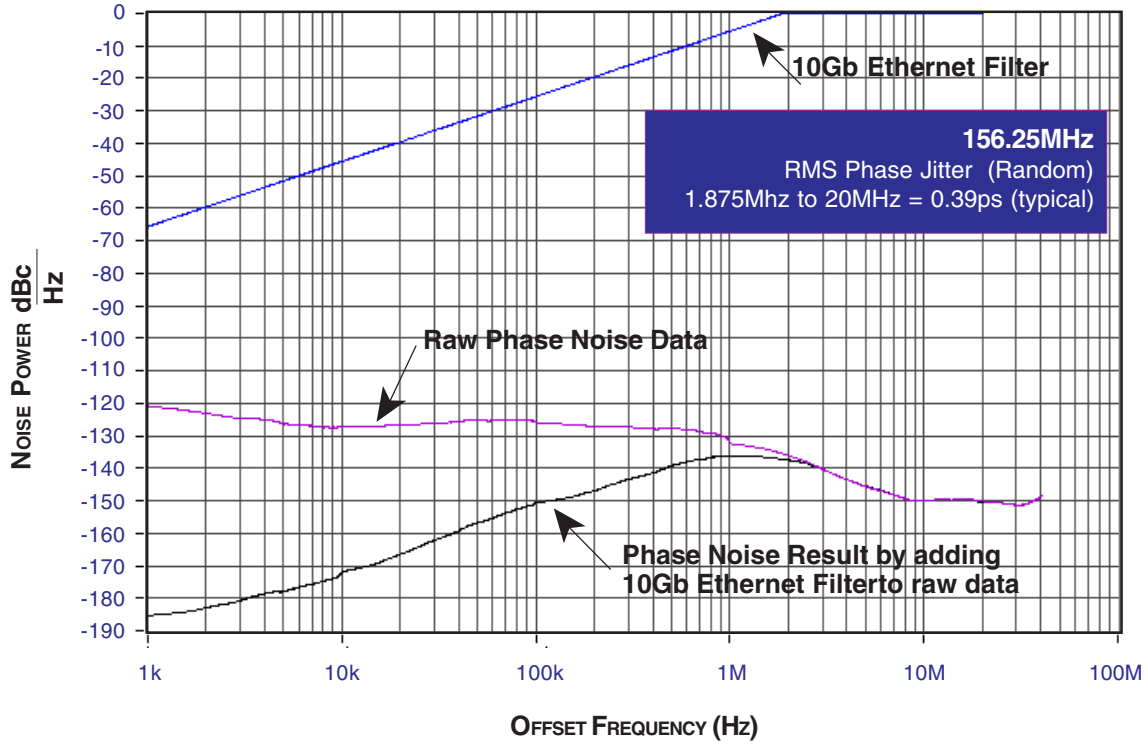
**TABLE 6. AC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO_A}, V_{CCO_B} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

| Symbol               | Parameter                         | Test Conditions | Minimum                      | Typical | Maximum | Units |
|----------------------|-----------------------------------|-----------------|------------------------------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency Range            |                 |                              | 156.25  |         | MHz   |
|                      |                                   |                 |                              | 125     |         | MHz   |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 1 | QA              | 125MHz (1.875MHz - 20MHz)    | 0.41    |         | ps    |
|                      |                                   | QB, nQB         | 156.25MHz (1.875MHz - 20MHz) | 0.39    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time             | QA              | 20% to 80%                   | 775     |         | ps    |
|                      |                                   | QB, nQB         |                              | 390     |         | ps    |
| odc                  | Output Duty Cycle                 | QA              |                              | 50      |         | %     |
|                      |                                   | QB, nQB         |                              | 50      |         | %     |

NOTE 1: Please refer to the Phase Noise Plots.

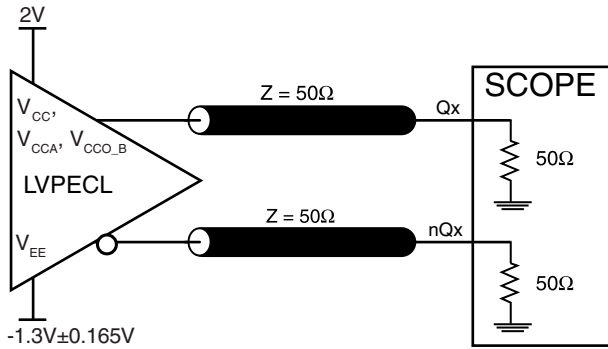


**TYPICAL PHASE NOISE AT 156.25MHz**

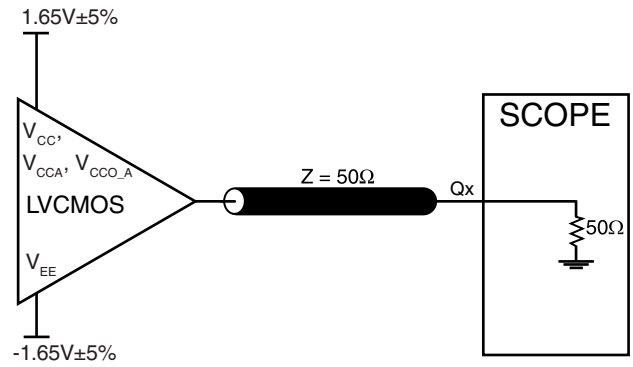




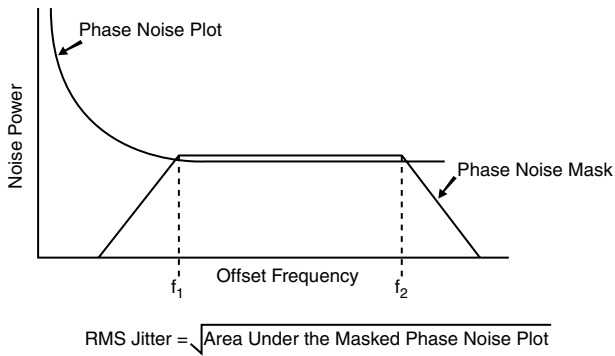
**PARAMETER MEASUREMENT INFORMATION**



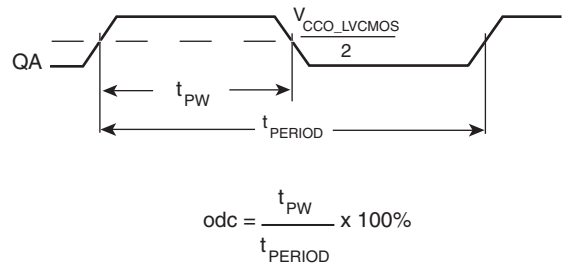
**3.3V CORE/3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT**



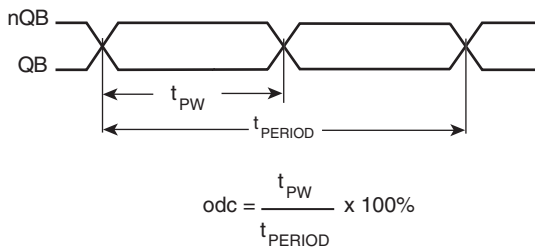
**3.3V CORE/3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT**



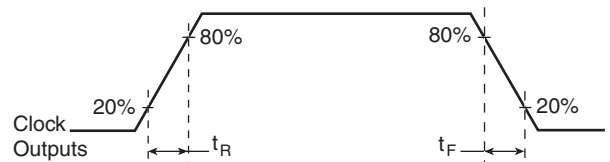
**RMS PHASE JITTER**



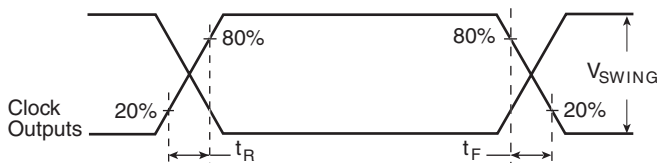
**LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**LVPECL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**LVCMOS OUTPUT RISE/FALL TIME**



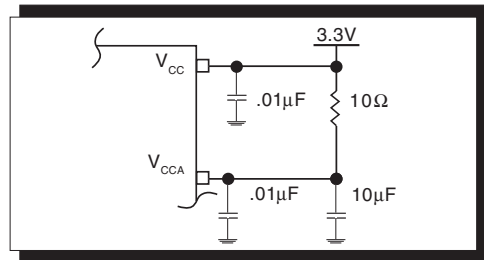
**LVPECL OUTPUT RISE/FALL TIME**



## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8430252-45 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$ , and  $V_{CCO_X}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{CCA}$  pin.

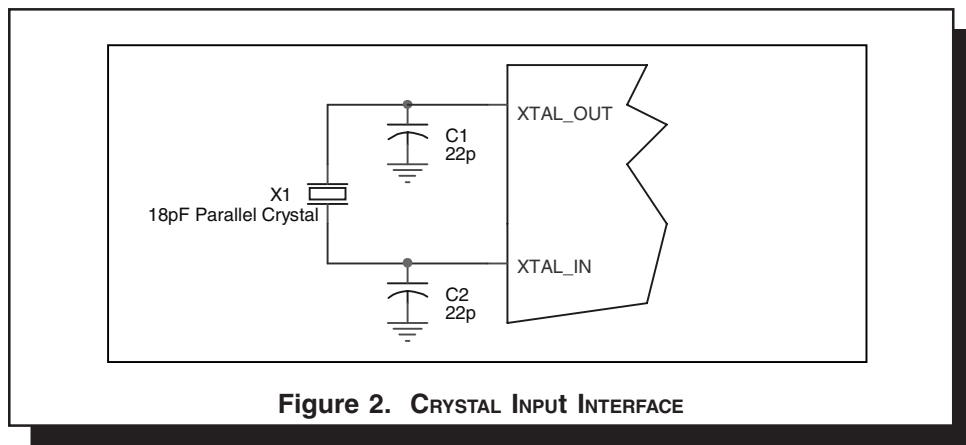


**FIGURE 1. POWER SUPPLY FILTERING**

### CRYSTAL INPUT INTERFACE

The ICS8430252-45 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF

parallel resonant crystal and were chosen to minimize the ppm error.



**Figure 2. CRYSTAL INPUT INTERFACE**



**RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS**

**INPUTS:**

**SELECT PINS:**

All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

**OUTPUTS:**

**LVC MOS OUTPUT:**

All unused LVC MOS output can be left floating. We recommend that there is no trace attached.

**LVPECL OUTPUT**

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

**TERMINATION FOR 3.3V LVPECL OUTPUT**

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

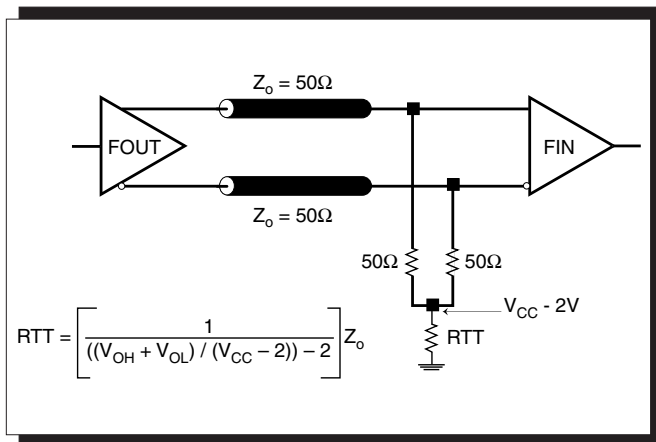


FIGURE 3A. LVPECL OUTPUT TERMINATION

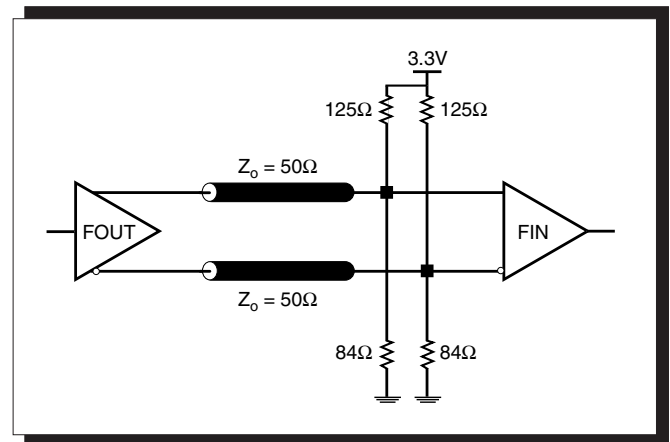


FIGURE 3B. LVPECL OUTPUT TERMINATION





## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8430252-45. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8430252-45 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 75mA = 259.88mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 30mW = 90mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $259.9mW + 60mW = 319.9mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 81.8°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$70°C + 0.320W * 81.8°C/W = 96.2°C$ . This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 7. THERMAL RESISTANCE  $\theta_{JA}$  FOR 16-PIN TSSOP, FORCED CONVECTION**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |           |           |           |
|--|-----------|-----------|-----------|
|  | 0         | 200       | 500       |
| Single-Layer PCB, JEDEC Standard Test Boards       | 137.1°C/W | 118.2°C/W | 106.8°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 89.0°C/W  | 81.8°C/W  | 78.1°C/W  |

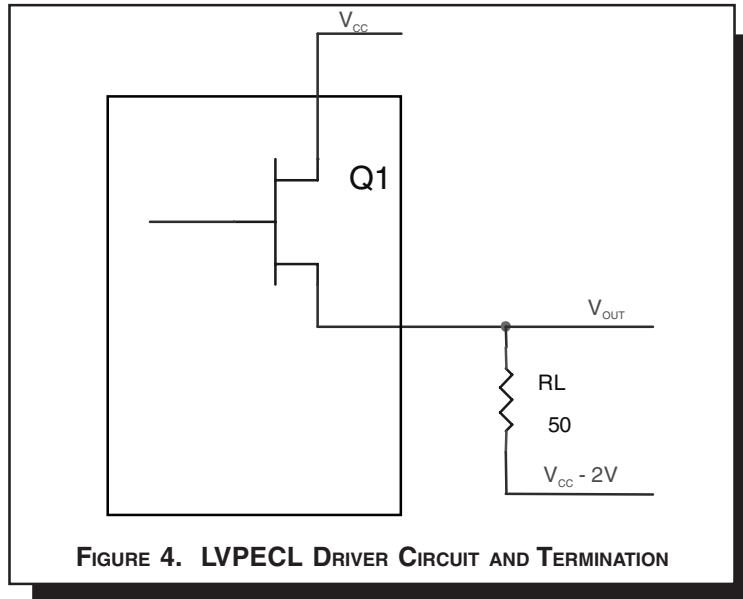
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 4.



**FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$$

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = Pd\_H + Pd\_L = 30mW



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## RELIABILITY INFORMATION

TABLE 8.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 16 LEAD TSSOP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |           |           |           |
|--|-----------|-----------|-----------|
|  | 0         | 200       | 500       |
| Single-Layer PCB, JEDEC Standard Test Boards       | 137.1°C/W | 118.2°C/W | 106.8°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 89.0°C/W  | 81.8°C/W  | 78.1°C/W  |

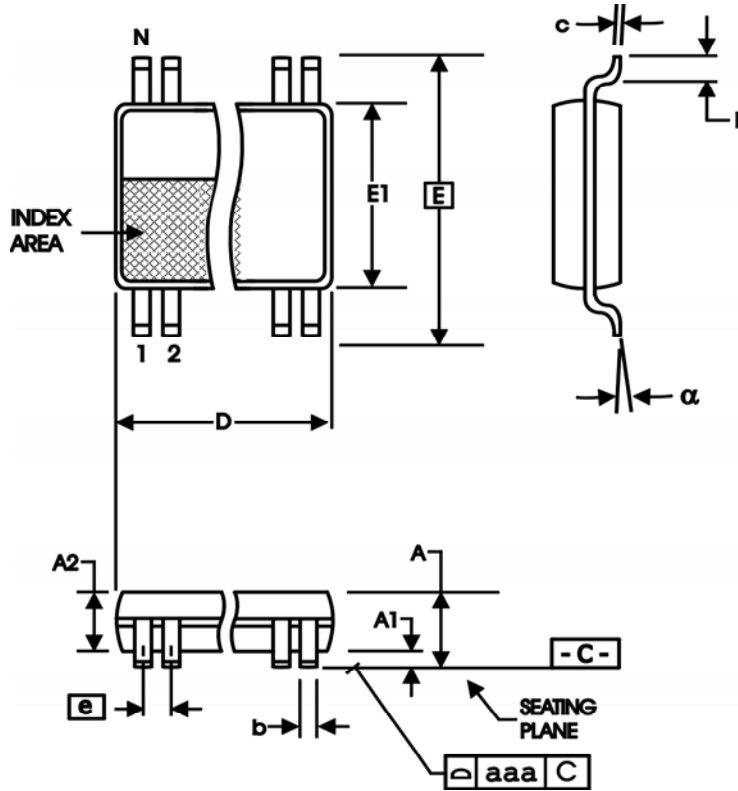
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8430252-45 is: 2070



**PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP**



**TABLE 9. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters |         |
|--------|-------------|---------|
|        | Minimum     | Maximum |
| N      | 16          |         |
| A      | --          | 1.20    |
| A1     | 0.05        | 0.15    |
| A2     | 0.80        | 1.05    |
| b      | 0.19        | 0.30    |
| c      | 0.09        | 0.20    |
| D      | 4.90        | 5.10    |
| E      | 6.40 BASIC  |         |
| E1     | 4.30        | 4.50    |
| e      | 0.65 BASIC  |         |
| L      | 0.45        | 0.75    |
| alpha  | 0°          | 8°      |
| aaa    | --          | 0.10    |

Reference Document: JEDEC Publication 95, MO-153



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**TABLE 10. ORDERING INFORMATION**

| Part/Order Number  | Marking  | Package                   | Shipping Packaging | Temperature |
|--------------------|----------|---------------------------|--------------------|-------------|
| ICS8430252CG-45    | 30252C45 | 16 Lead TSSOP             | tube               | 0°C to 70°C |
| ICS8430252CG-45T   | 30252C45 | 16 Lead TSSOP             | 2500 tape & reel   | 0°C to 70°C |
| ICS8430252CG-45LF  | TBD      | 16 Lead "Lead-Free" TSSOP | tube               | 0°C to 70°C |
| ICS8430252CG-45LFT | TBD      | 16 Lead "Lead-Free" TSSOP | 2500 tape & reel   | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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