M52758SP/FP

Wide Band Analog Switch

REJ03F0196-0200
Rev.2.00
Sep 14, 2006

Description

The M52758 is a semiconductor integrated circuit for the RGBHV interface. The device features switching signals input from two types of image and outputting them to CRT display etc.

Synchronous signal meeting the frequency band of 10 kHz to 200 kHz are output at TTL. The frequency band of video signals is 250 MHz, acquiring high-resolution images, and are optimum as an interface IC with high-resolution CRT display and various new media.

Features

- Frequency band: RGB 250 MHz
  HV 10 Hz to 200 kHz
- Input level: RGB 0.7 V_{P-P} (typ.)
  HV TTL input 2.0 V_{O-P} (both channel)
- Only the G channel is provided with sync-on video output.
- The TTL format is adopted for HV output.

Application

Display monitor

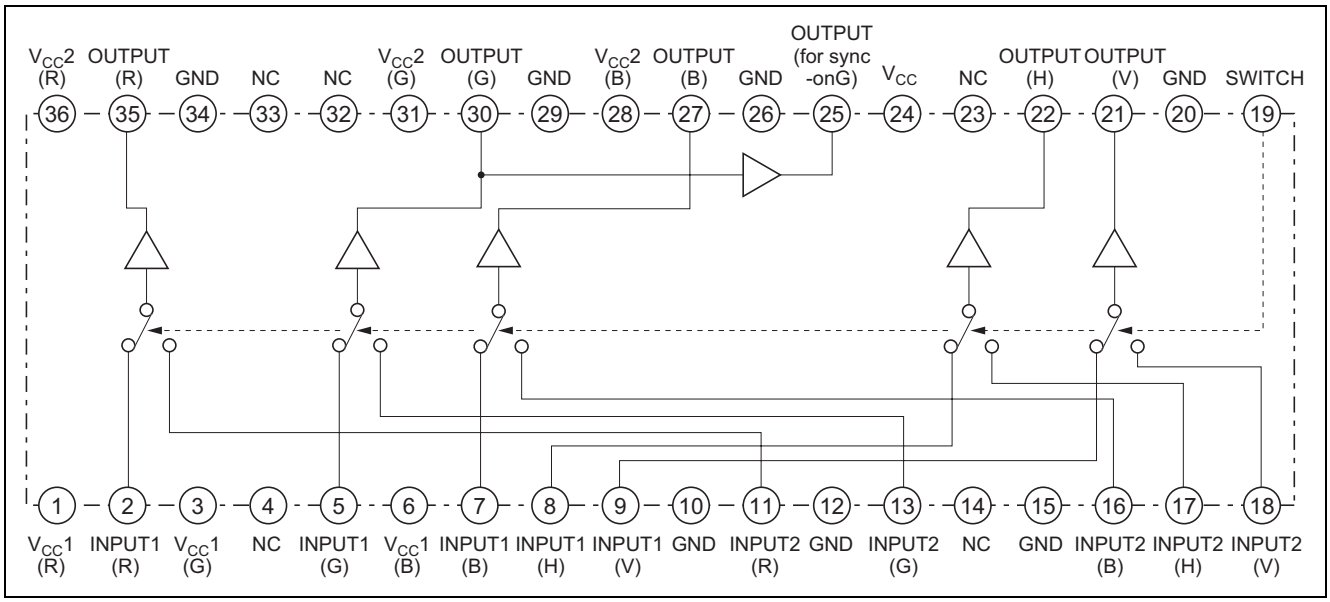
Recommended Operating Condition

Supply voltage range: 4.75 to 5.5 V

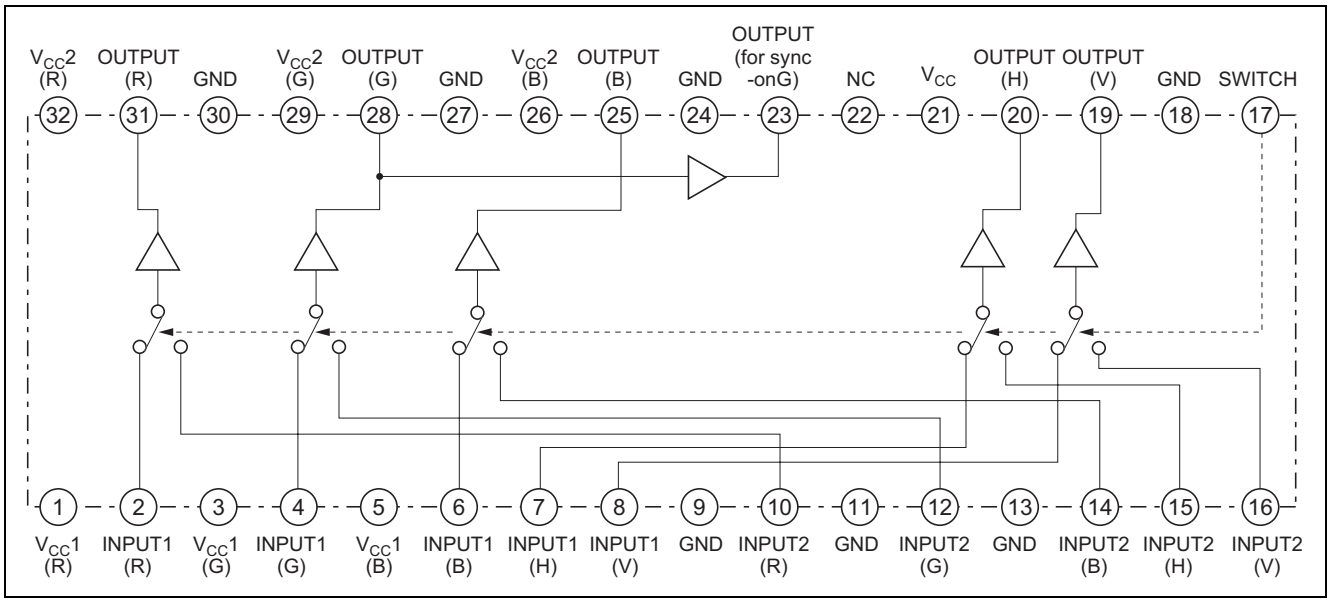
Rated supply voltage: 5.0 V

Block Diagram

M52758FP

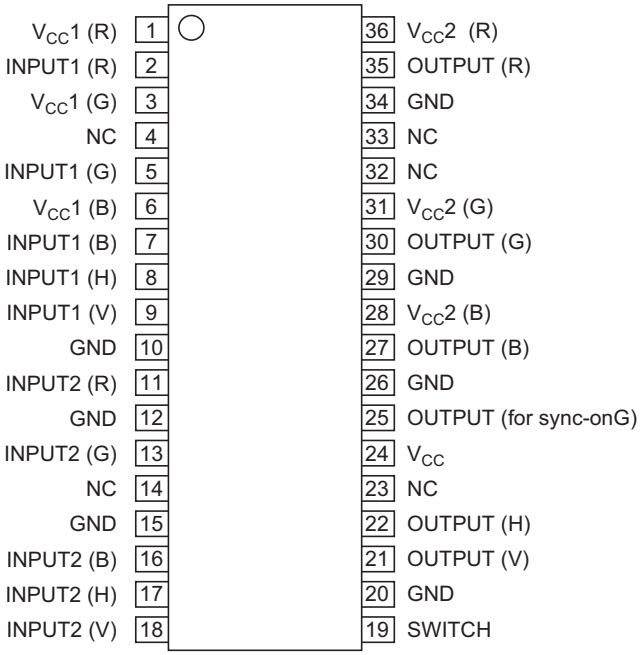


M52758SP



Pin Arrangement

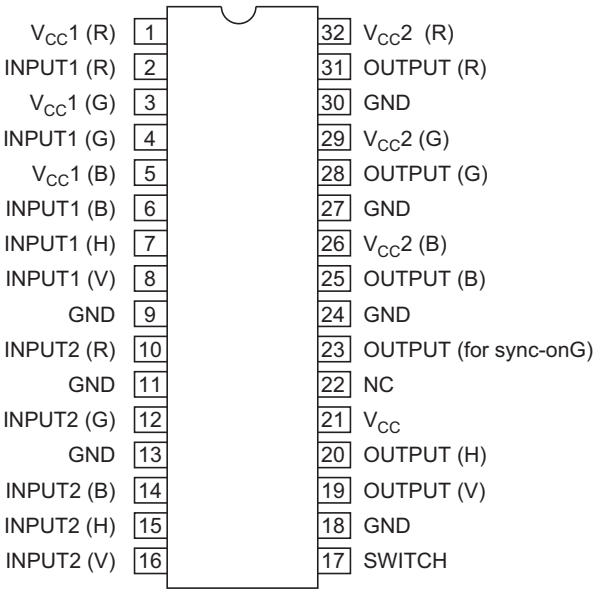
M52758FP



(Top view)

Outline: PRSP0036GA-B (36P2R-D)

M52758SP



(Top view)

NC: No connection

Outline: PRDP0032BA-A (32P4B)

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7.0	V
Power dissipation	Pd	1068 (FP) 1603 (SP)	mW
Ambient temperature	Topr	–20 to +85	°C
Storage temperature	Tstg	–40 to +150	°C
Recommended supply voltage	Vopr	5.0	V
Recommended supply voltage range	Vopr'	4.75 to 5.5	V
Electrostatic discharge	Surge	±200	V

Electrical Characteristics

Pin No is FP (V_{CC} = 5 V, Ta = 25°C, unless otherwise noted)

Item	Symbol	Limits			Unit	Test Point (s)	V_{CC} (V)	Input										SW
		Min.	Typ.	Max.			V_{CC}	SW2 Rin1	SW5 Gin1	SW7 Bin1	SW8 Hin1	SW9 Vin1	SW11 Rin2	SW13 Gin2	SW16 Bin2	SW17 Hin2	SW18 Vin2	SW19 Switch
Circuit current1 (no signal)	$I_{CC}1$	46	66	86	mA	A	5	b	b	b	b	b	b	b	b	b	b	b
Circuit current2 (no signal)	$I_{CC}2$	46	66	86	mA	A	5	b	b	b	b	b	b	b	b	b	b	a
(RGB SW)																		
Output DC voltage1	V_{DC1}	1.85	2.05	2.25	V	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	b	b	b	b	b	b
Output DC voltage2	V_{DC2}	1.85	2.05	2.25	V	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	b	b	b	b	b	a
Output DC voltage3	V_{DC3}	0.75	1.15	1.55	V	T.P.25	5	b	b	b	b	b	b	b	b	b	b	b
Output DC voltage4	V_{DC4}	0.75	1.15	1.55	V	T.P.25	5	b	b	b	b	b	b	b	b	b	b	a
Maximum allowable input1	Vimax1	2.0	2.4	—	V_{P-P}	T.P.2 T.P.5 T.P.7	5	abb SG1	bab SG1	bba SG1	b	b	b	b	b	b	b	b
Maximum allowable input2	Vimax2	2.0	2.4	—	V_{P-P}	T.P.11 T.P.13 T.P.16	5	b	b	b	b	b	abb SG1	bab SG1	bba SG1	b	b	a
Voltage gain1	G_{V1}	0.3	0.9	1.5	dB	T.P.35 T.P.30 T.P.27	5	abb SG2	bab SG2	bba SG2	b	b	b	b	b	b	b	b
Relative voltage gain1	ΔG_{V1}	–0.4	0	0.4	dB	Relative to measured values above												
Voltage gain2	G_{V2}	0.3	0.9	1.5	dB	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	abb SG2	bab SG2	bba SG2	b	b	a
Relative voltage gain2	ΔG_{V2}	–0.4	0	0.4	dB	Relative to measured values above												
Voltage gain3	G_{V3}	–0.4	0.2	0.8	dB	T.P.25	5	b	a SG2	b	b	b	b	b	b	b	b	b
Voltage gain4	G_{V4}	–0.4	0.2	0.8	dB	T.P.25	5	b	b	b	b	b	b	a SG2	b	b	b	a
Frequency characteristic1 (100 MHz)	F_{C1}	–1.0	0	1.0	dB	T.P.31 T.P.28 T.P.25	5	abb SG4	bab SG4	bba SG4	b	b	b	b	b	b	b	b
Relative frequency characteristic1 (100 MHz)	ΔF_{C1}	–1.0	0	1.0	dB	Relative to measured values above												
Frequency characteristic2 (100 MHz)	F_{C2}	–1.0	0	1.0	dB	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	abb SG4	bab SG4	bba SG4	b	b	a
Relative frequency characteristic2 (100 MHz)	ΔF_{C2}	–1.0	0	1.0	dB	Relative to measured values above												
Frequency characteristic3 (250 MHz)	F_{C3}	–3.0	–1.5	1.0	dB	T.P.35 T.P.30 T.P.27	5	abb SG5	bab SG5	bba SG5	b	b	b	b	b	b	b	b
Frequency characteristic4 (250 MHz)	F_{C4}	–3.0	–1.5	1.0	dB	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	abb SG5	bab SG5	bba SG5	b	b	a

Electrical Characteristics (cont.)

Item	Symbol	Limits			Unit	Test Point (s)	V_{CC} (V)	Input									SW
		Min.	Typ.	Max.			V_{CC}	SW2 Rin1	SW5 Gin1	SW7 Bin1	SW8 Hin1	SW9 Vin1	SW11 Rin2	SW13 Gin2	SW16 Bin2	SW17 Hin2	SW18 Vin2	SW19 Switch
Crosstalk between two inputs1 (10 MHz)	C.T.I.1	—	–60	–50	dB	T.P.35 T.P.30 T.P.27	5	abb SG3	bab SG3	bba SG3	b	b	b	b	b	b	b	b ↓ a
Crosstalk between two inputs2 (10 MHz)	C.T.I.2	—	–60	–50	dB	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	abb SG3	bab SG3	bba SG3	b	b	a ↓ b
Crosstalk between two inputs3 (100 MHz)	C.T.I.3	—	–40	–35	dB	T.P.35 T.P.30 T.P.27	5	abb SG4	bab SG4	bba SG4	b	b	b	b	b	b	b	b ↓ a
Crosstalk between two inputs4 (100 MHz)	C.T.I.4	—	–40	–35	dB	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	abb SG4	bab SG4	bba SG4	b	b	a ↓ b
Crosstalk between channels1 (10 MHz)	C.T.C.1	—	–50	–40	dB	T.P.35 T.P.30 T.P.27	5	abb SG3	bab SG3	bba SG3	b	b	b	b	b	b	b	b
Crosstalk between channels2 (10 MHz)	C.T.C.2	—	–50	–40	dB	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	abb SG3	bab SG3	bba SG3	b	b	a
Crosstalk between channels3 (100 MHz)	C.T.C.3	—	–30	–25	dB	T.P.35 T.P.30 T.P.27	5	abb SG4	bab SG4	bba SG4	b	b	b	b	b	b	b	b
Crosstalk between channels4 (100 MHz)	C.T.C.4	—	–30	–25	dB	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	abb SG4	bab SG4	bba SG4	b	b	a
Pulse characteristic1	Tr1	—	1.6	2.5	ns	T.P.35 T.P.30 T.P.27	5	a SG6	a SG6	a SG6	b	b	b	b	b	b	b	b
	Tf1	—	1.6	2.5	ns	T.P.35 T.P.30 T.P.27	5	a SG6	a SG6	a SG6	b	b	b	b	b	b	b	b
Pulse characteristic2	Tr2	—	1.6	2.5	ns	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	a SG6	a SG6	a SG6	b	b	a
	Tf2	—	1.6	2.5	ns	T.P.35 T.P.30 T.P.27	5	b	b	b	b	b	a SG6	a SG6	a SG6	b	b	a
(HV SW)																		
High level output voltage1	V_{OH1}	4.5	0.5	—	dB	T.P.21 T.P.22	5	b	b	b	c 5.0 V	c 5.0 V	b	b	b	b	b	b
High level output voltage2	V_{OH2}	4.5	0.5	—	dB	T.P.21 T.P.22	5	b	b	b	b	b	b	b	b	c 5.0 V	c 5.0 V	a
Low level output voltage1	V_{OL1}	—	0.2	0.5	dB	T.P.21 T.P.22	5	b	b	b	c 0 V	c 0 V	b	b	b	b	b	b
Low level output voltage2	V_{OL2}	—	0.2	0.5	dB	T.P.21 T.P.22	5	b	b	b	b	b	b	b	b	c 0 V	c 0 V	a
Input selectional voltage1	Vith1	1.4	1.8	2.0	dB	T.P.8 T.P.9	5	b	b	b	c Variable	c Variable	b	b	b	b	b	b
Input selectional voltage2	Vith2	1.4	1.8	2.0	dB	T.P.17 T.P.18	5	b	b	b	b	b	b	b	b	c Variable	c Variable	a
Rising delay time1	Trd1	—	100	150	ns	T.P.21 T.P.22	5	b	b	b	a SG7	a SG7	b	b	b	b	b	b
Rising delay time2	Trd2	—	100	150	ns	T.P.21 T.P.22	5	b	b	b	b	b	b	b	b	a SG7	a SG7	a
Falling delay time1	Tfd1	—	50	100	ns	T.P.21 T.P.22	5	b	b	b	a SG7	a SG7	b	b	b	b	b	b
Falling delay time2	Tfd2	—	50	100	ns	T.P.21 T.P.22	5	b	b	b	b	b	b	b	b	a SG7	a SG7	a
Switching selectional voltage1	Vsth1	0.5	1.5	2.0	V	T.P.19	5	a SG1	a SG1	a SG1	a SG7	a SG7	b	b	b	b	b	c
Switching selectional voltage2	Vsth2	0.5	1.5	2.0	V	T.P.19	5	b	b	b	b	b	a SG1	a SG1	a SG1	a SG7	a SG7	c

Electrical Characteristics Test Method (Pin No is FP)

It omits the SW.No accorded with signal input pin because it is already written in Table.

SW A, SW1, SW3, SW5 is in side a if there is not defined specially.

$I_{CC}1$, $I_{CC}2$, Circuit Current (no signal)

The condition is shown as Table. Set SW19 to GND (or OPEN) and SW A to side b, measure the current by current meter A. The current is as $I_{CC}1$ ($I_{CC}2$).

V_{DC1}, V_{DC2} Output DC Voltage

Set SW19 to GND (or OPEN), measure the DC voltage of T.P.35 (T.P.30, T.P.27) when there is no signal input. The DC voltage is as V_{DC1} (or V_{DC2}).

V_{DC3}, V_{DC4} Output DC Voltage

Measure the DC voltage of T.P.25 same as Table, the DC voltage is as V_{DC3} (or V_{DC4}).

Vimax1, Vimax2 Maximum Allowable Input

Set SW19 to GND, SG1 as the input signal of pin 2. Rising up the amplitude of SG1 slowly, read the amplitude of input signal when the output waveform is distorted. The amplitude is as Vimax1. And measure Vimax1 when SG2 as the input signal of pin 5, pin 7 in same way. Next, set SW to OPEN, measure Vimax2 when SG2 as the input signal of pin 11, 13, 16.

G_{V1}, ΔG_{V1}, G_{V2}, ΔG_{V2}

1. The condition is shown as Table.
2. Set SW19 to GND, SG2 as the input signal of pin 2. At this time, read the amplitude output from T.P.35. The amplitude is as $V_{OR}1$.
3. Voltage gain G_{V1} is

$$G_{V1} = 20\log \frac{V_{OR}1\ [V_{P\text{-}P}]}{0.7\ [V_{P\text{-}P}]} \quad [dB]$$

4. The method as same as 2 and 3, measure the voltage gain G_{V1} when SG2 as the input signal of pin 5, 7.
5. The difference of each channel relative voltage gain is as ΔG_{V1}.
6. Set SW19 to OPEN, measure G_{V2}, ΔG_{V12} in the same way.

G_{V3}, G_{V4}, Voltage Gain

1. The condition is shown as Table. This test is by active probe.
2. Measure the amplitude output from T.P.25.
3. Measure the G_{V3}, G_{V4} by the same way as G_{V1}, ΔG_{V1}, G_{V2}, ΔG_{V2}.

F_{C1}, ΔF_{C1}, F_{C2}, ΔF_{C2}

1. The condition is shown as Table. This test is by active probe.
2. Set SW19 to GND, SG2 as the input signal of pin 2. Measure the amplitude output from T.P.35. The amplitude is as $V_{OR}1$. By the same way, measure the output when SG4 is as input signal of pin 2, the output is as $V_{OR}2$.
3. The frequency characteristic F_{C1} is

$$F_{C1} = 20\log \frac{V_{OR}2\ [V_{P\text{-}P}]}{V_{OR}1\ [V_{P\text{-}P}]} \quad [dB]$$

4. The method as same as 2 and 3, measure the frequency F_{C1} when input signal to pin 5, 7.
5. The difference between of each channel frequency characteristic is as ΔF_{C1}.
6. Set SW19 to OPEN, measure F_{C2}, ΔF_{C2}.

F_{C3}, F_{C4} Frequency Characteristic

By the same way as Table measure the F_{C3}, F_{C4} when SG5 of input signal.

C.T.I.1, C.T.I.2 Crosstalk between Two Input

1. The condition is shown as Table. This test is by active prove.
2. Set SW19 to GND, SG3 as the input signal of pin 2. Measure the amplitude output from T.P.35.The amplitude is as $V_{OR}3$.
3. Set SW19 to OPEN, measure the amplitude output from T.P.35. The amplitude is as $V_{OR}3'$.
4 The crosstalk between two inputs C.T.I.1 is

$$C.T.I.1 = 20\log \frac{V_{OR}3' \, [V_{P-P}]}{V_{OR}3 \, [V_{P-P}]} \quad [dB]$$

5. By the same way, measure the crosstalk between two inputs when SG3 as the input signal of pin 5, pin 7.
6. Next, set SW19 to OPEN, SG3 as the input signal of pin 11, measure the amplitude output from T.P.35. The amplitude is as $V_{OR}4$.
7. Set SW19 to GND, measure the amplitude output from T.P.35. The amplitude is as $V_{OR}4'$.
8 The crosstalk between two inputs C.T.I.2 is

$$C.T.I.2 = 20\log \frac{V_{OR}4' \, [V_{P-P}]}{V_{OR}4 \, [V_{P-P}]} \quad [dB]$$

9. By the same way, measure the crosstalk between channels when SG3 as the input signal of pin 13, 16.

C.T.I.3, C.T.I.4 Crosstalk between Two Input

Set SG4 as the input signal, and then the same method as Table, measure C.T.I.3. C.T.I.4.

C.T.C.1, C.T.C.2 Crosstalk between Channel

1. The condition is as Table. This test is by active prove.
2. Set SW19 to GND, SG3 as the input signal of pin 2. Measure the amplitude output from T.P.35. The amplitude is as $V_{OR}5$.
3. Next, measure T.P.30, T.P.27 in the same state, and the amplitude is as $V_{OG}5$, $V_{OB}5$.
4. The crosstalk between channels C.T.C.1 is

$$C.T.C.1 = 20\log \frac{V_{OG}5 \text{ or } V_{OB}5}{V_{OR}5} \quad [dB]$$

5. Measure the crosstalk between channels when SG3 is as the input signal of pin 5, pin 7.
6. Next, set SW19 to OPEN, SG3 as the input signal of pin 11, measure the amplitude output from T.P.35. The amplitude is as $V_{OR}6$.
7. Next, measure the amplitude output from T.P.30, T.P.27 in the same state. The amplitude is as $V_{OG}6$, $V_{OB}6$.
8. The crosstalk between channels C.T.C.2 is

$$C.T.C.2 = 20\log \frac{V_{OG}6 \text{ or } V_{OB}6}{V_{OR}6} \quad [dB]$$

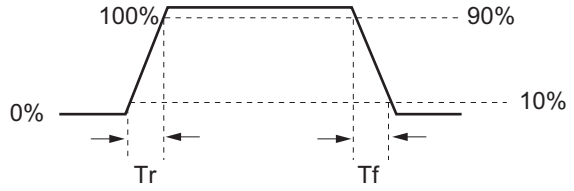
9. By the same way, measure the crosstalk between channels when input signal to pin 13, 16.

C.T.C.3, C.T.C.4 Crosstalk between Channel

Set SG4 as the input signal, and the same method as Table, measure C.T.C.3, C.T.C.4.

Tr1, Tf1, Tr2, Tf2 Pulse Characteristic

1. The condition is as Table. Set SW19 to GND (or OPEN).
2. The rising of 10% to 90% for input pulse is Tri, the falling of 10% to 90% for input pulse is Tfi.
3. Next, the rising of 10% to 90% for output pulse is Tro, the falling of 10% to 90% for output pulse is Tfo.
4. The pulse characteristic Tr1, Tf1 (Tr2, Tf2) is



$$Tr1\ (Tr2) = \sqrt{(Tro)^2 - (Tri)^2} \quad (ns)$$

$$Tf1\ (Tf2) = \sqrt{(Tfo)^2 - (Tfi)^2} \quad (ns)$$

V_{OH1}, V_{OH2} High Level Output Voltage

The condition is as Table. Set SW19 to GND (OPEN), input 5 V at input terminal. Measure the output voltage, the voltage is as V_{OH1} (V_{OH2}).

V_{OL1}, V_{OL2} Low Level Output Voltage

The condition is as Table. Set SW19 to GND (OPEN), input 0 V at input terminal. Measure the output voltage, the voltage is as V_{OL1} (V_{OL2}).

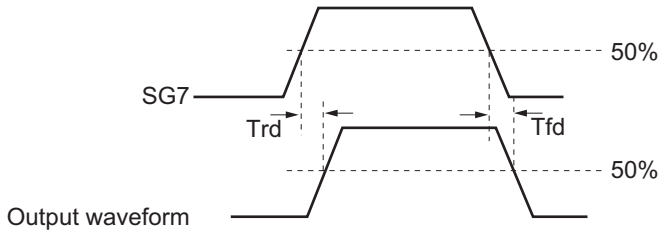
Vith1, Vith2 Input Selectional Voltage

The condition is as Table. Set SW19 to GND (OPEN), increasing gradually the voltage of input terminal from 0 V, measure the voltage of input terminal when output terminal is 4.5 V. The input voltage is as Vith1 (Vith2).

Trd1, Trd2 Rising Delay Time, Tfd1, Tfd2 Falling delay time

The condition is as Table. Set SW19 to GND (OPEN), SG7 is as the input signal of input terminal, measure the waveform of output.

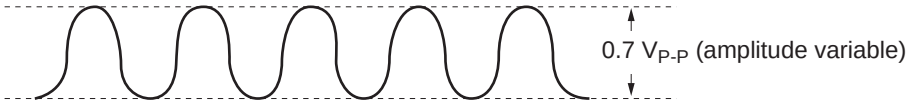
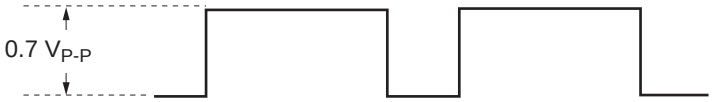
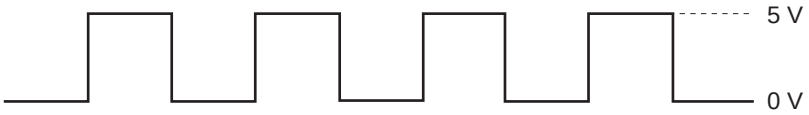
Rising delay time is as Trd1 (Trd2). Falling delay time is as Tfd1 (Tfd2). Reference to the Figure as shown below.



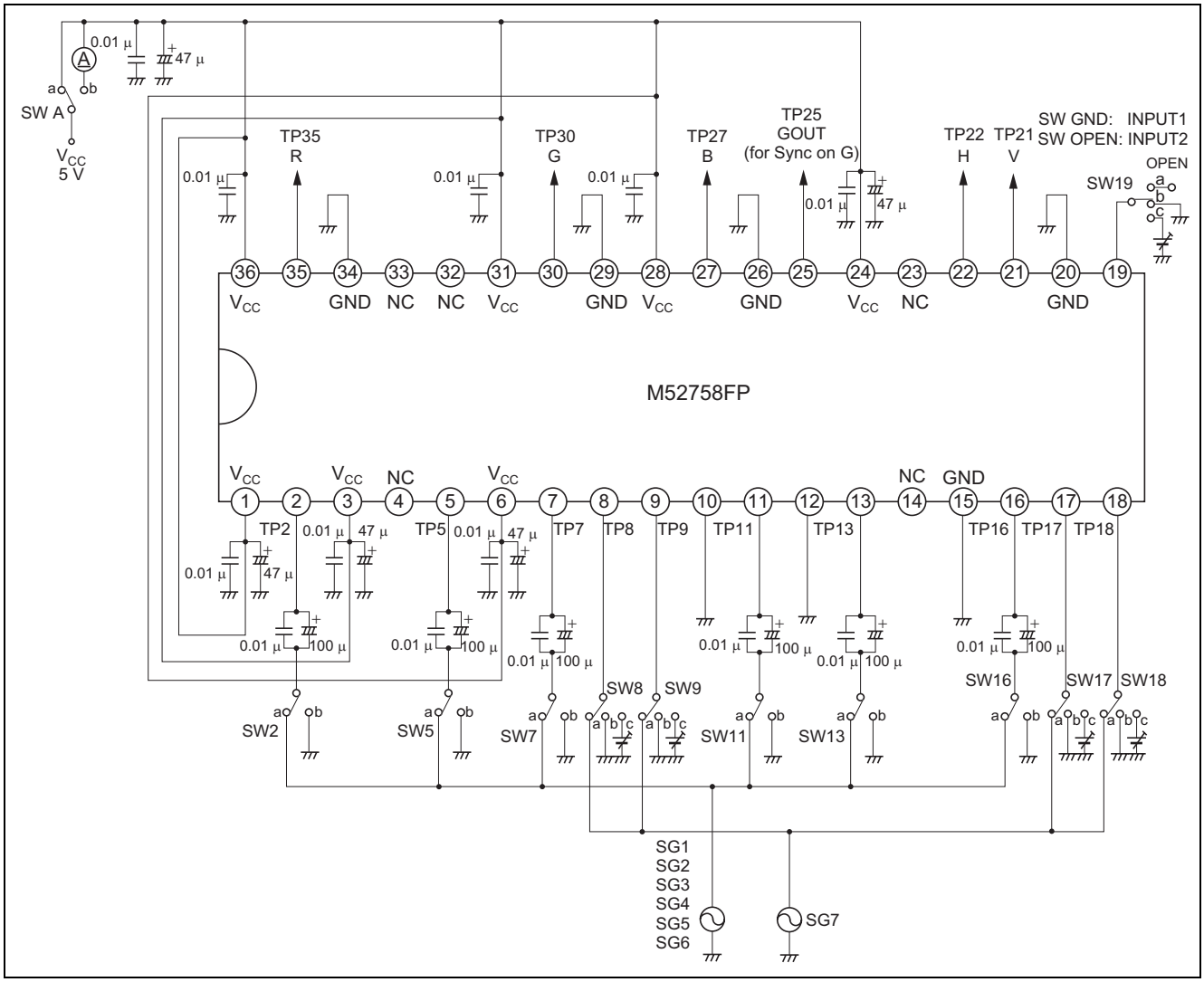
Vsth1, Vsth2 Switching Selectional Voltage

1. The condition is as Table. SG1 is as the input signal of pin 2, pin 5, pin 7, and SG7 is as the input signal of pin 8, pin 9. There is no input at another pins.
2. Input 0 V at pin 19, confirm that there are signals output from T.P.21, T.P.22, T.P.25, T.P.27, T.P.30, T.P.35.
3. Increase gradually the voltage of terminal pin 19. Read the voltage when there is no signal output from the terminals listed as above.
   The voltage is as Vsth1.
4. SG1 as the input signal of pin 11, pin 13, pin 16, and SG7 as the input signal of pin 17, pin 18. There is no input at another pins.
5. Inputs 5 V at pin 19, confirm that there is no signal output from T.P.21, T.P.22, T.P.25, T.P.27, T.P.30, T.P.35.
6. Decreasing gradually the voltage of terminal pin 19. Read the voltage when there are signals output from the terminals listed as above. The voltage is as Vsth2.

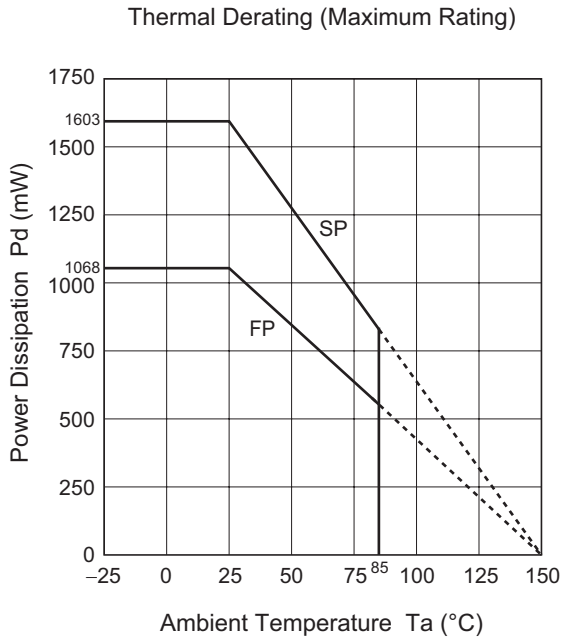
Input Signal

SG No.	Input Signal
SG1	Sine wave (f = 60 kHz, 0.7 V_{P-P}, amplitude variable) 
SG2	Sine wave (f = 1 MHz, amplitude 0.7 V_{P-P})
SG3	Sine wave (f = 10 MHz, amplitude 0.7 V_{P-P})
SG4	Sine wave (f = 100 MHz, amplitude 0.7 V_{P-P})
SG5	Sine wave (f = 250 MHz, amplitude 0.7 V_{P-P})
SG6	Pulse with amplitude 0.7 V_{P-P} (f = 60 kHz, duty 80%) 
SG7	Square wave (Amplitude 5.0 V_{O-P} TTL, f = 60 kHz, duty 50%) 

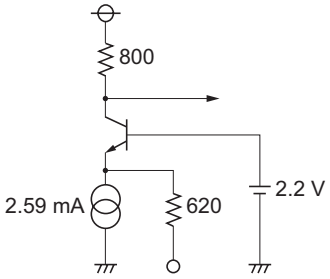
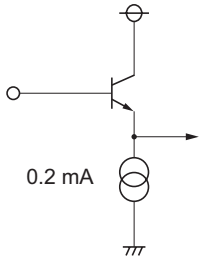
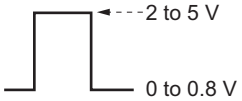
Test Circuit (FP)



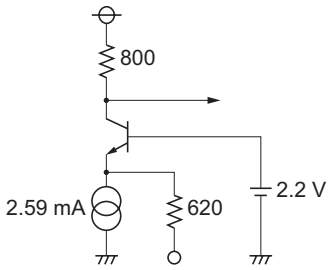
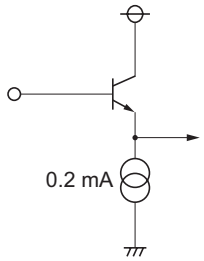
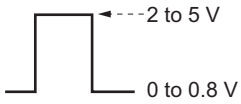
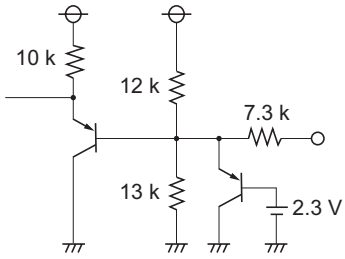
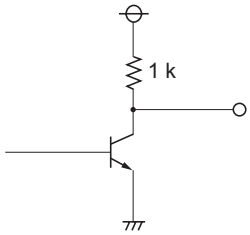
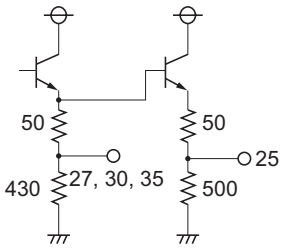
Typical Characteristics



Pin Description

Pin No. (FP)	Name	DC Voltage (V)	Peripheral Circuit	Function
1 3 6	$V_{CC}1$ (R) $V_{CC}1$ (G) $V_{CC}1$ (B)	5.0	—	—
2 5 7	Input1 (R) Input1 (G) Input1 (B)	1.5		Input signal with low impedance
8 9	Input1 (H) Input1 (V)	—		Input pulse between 2 V and 5 V 
10, 12, 15, 20, 26, 29, 34	GND	GND	—	—

Pin Description (cont.)

Pin No. (FP)	Name	DC Voltage (V)	Peripheral Circuit	Function
11 13 16	Input2 (R) Input2 (G) Input2 (B)	1.5		Input signal with low impedance.
17 18	Input2 (H) Input2 (V)	—		Input pulse between 2 V and 5 V. 
19	Switch	2.6		Switch by OPEN and GND.
21 22	Output (V) Output (H)	—		Output impedance is built-in
24	V_{CC} (H, V, Switch)	5	—	—
4, 14, 23, 32, 33	NC	—	—	—
25 27 30 35	Output (sync on G) Output (B) Output (G) Output (R)	1.15 2.05		Output impedance is built-in
28 31 36	$V_{CC}2$ (R) $V_{CC}2$ (G) $V_{CC}2$ (B)	5	—	—

Note How to Use This IC (Pin No is FP)

1. R, G, B input signal is 0.7 V_{P-P} of standard video signal.
2. H, V input is 2.0 V (min.) TTL type.
3. Input signal with sufficient low impedance to input terminal.
4. The terminal of H, V output pin are shown as Figure 1. It is possible to reduce rise time by insert the resister between V_{CC} line and H, V output pin, but set the value of resister in order that the current is under 7.5 mA. Setting the value of R is more than 2 kΩ as shown in Figure 1.

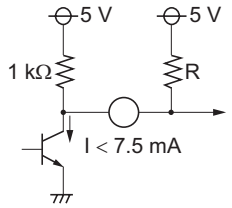


Figure 1

5. The terminal of R, G, B output pin (pin 27, 30, 35). It is possible to add a pull-up resister according as drive ability. But set the value of resister in order that the current is under 10 mA. Setting the value of R is more than 500 Ω as shown in Figure 2.

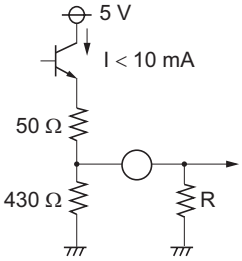


Figure 2

6. Switch (pin 19) can be changed when this terminal is GND or OPEN
   When GND: Signal output from input 1
   When OPEN: Signal output from input 2
   When the switch is being used as Figure 3
   0 to 0.5 V: Signal output from input 1
   2 to 5 V: Signal output from input 2
   It is not allowable to set voltage higher than V_{CC}.

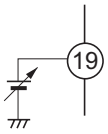


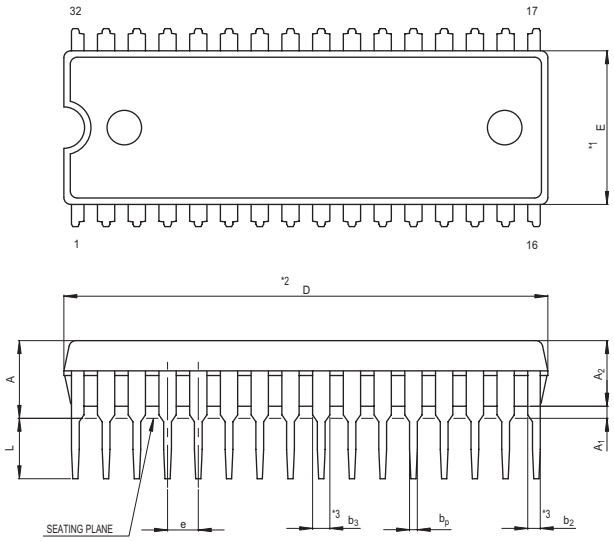
Figure 3

Notice of Making Printed Circuit Board

- Please notice following as shown below. It will maybe cause something oscillation because of the P.C.B. layout of the wide band analog switch.
- The distance between resister and output pin is as short as possible when insert a output pull-down resister.
- The capacitance of output terminal as small as possible.
- Set the capacitance between V_{CC} and GND near the pins if possible.
- Using stable power-source (if possible the separated power-source will be better).
- It will reduce the oscillation when add a resister that is tens of ohms between output pin and next stage.
- Assign an area as large as possible for grounding.

Package Dimensions

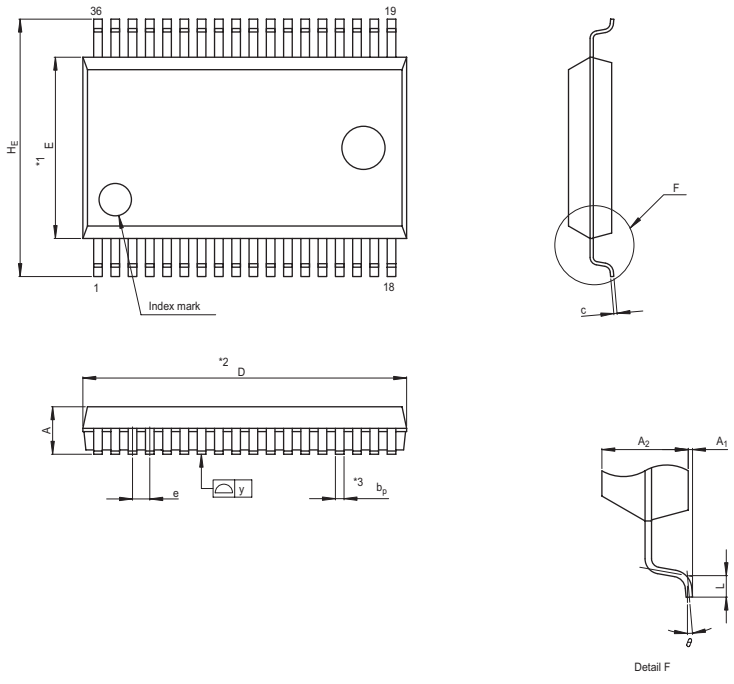
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP32-8.9x28-1.78	PRDP0032BA-A	32P4B	2.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	9.86	10.16	10.46
D	27.8	28.0	28.2
E	8.75	8.9	9.05
A	—	—	5.08
A_1	0.51	—	—
A_2	—	3.8	—
b_p	0.35	0.45	0.55
b_2	0.63	0.73	1.03
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP36-8.4x15-0.80	PRSP0036GA-B	36P2R-D	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.8	15.0	15.2
E	8.2	8.4	8.6
A_2	—	2.05	—
A	—	—	2.35
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.10
L	0.3	0.5	0.7

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