LINEAR SYSTEMS

SST402
LOW NOISE, LOW DRIFT
MONOLITHIC DUAL
N-CHANNEL JFET

micross

Linear Systems replaces discontinued Siliconix SST402

The SST402 is a Low Noise, Low Drift, Monolithic Dual N-Channel JFET

The SST402 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The SST402 features a 5-mV offset and 10-µV/°C drift. The SST402 is a direct replacement for discontinued Siliconix SST402.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

SST402 Applications:

- Wideband Differential Amps
- High-Speed,Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES	
LOW DRIFT	$\lvert V_{GS1-2} / T \rvert$ = 10µV/°C TYP.
LOW NOISE	e_n = 6nV/Hz @ 10Hz TYP.
LOW PINCHOFF	V_p = 2.5V TYP.

ABSOLUTE MAXIMUM RATINGS
@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C

Maximum Voltage and Current for Each Transistor – Note 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	50V
$-V_{DSO}$	Drain to Source Voltage	50V
$-I_{G(f)}$	Gate Forward Current	10mA

Maximum Power Dissipation	
Device Dissipation @ Free Air – Total	300mW

MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$\lvert V_{GS1-2} / T \rvert$ max.	DRIFT VS. TEMPERATURE	10	µV/°C	V_{DG}=10V, I_D=200µA T_A=-55°C to +125°C
$\lvert V_{GS1-2} \rvert$ max.	OFFSET VOLTAGE	10	mV	V_{DG}=10V, I_D=200µA

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	50	60	--	V	V_{DS} = 0 I_D=1nA
BV_{GGO}	Gate-To-Gate Breakdown	±50	--	--	V	I_G= 1nA I_D= 0 I_S= 0
	TRANSCONDUCTANCE					
Y_{fss}	Full Conduction	2000	--	7000	µmho	V_{DG}= 10V V_{GS}= 0V f = 1kHz
Y_{fs}	Typical Operation	1000	--	2000	µmho	V_{DG}= 15V I_D= 200µA f = 1kHz
$\lvert Y_{FS1-2} / Y_{FS} \rvert$	Mismatch	--	0.6	3	%	
	DRAIN CURRENT					
I_{DSS}	Full Conduction	0.5	--	10	mA	V_{DG}= 10V V_{GS}= 0V
$\lvert I_{DSS1-2} / I_{DSS} \rvert$	Mismatch at Full Conduction	--	1	5	%	
	GATE VOLTAGE					
V_{GS}(off) or V_p	Pinchoff voltage	-0.5	--	-2.5	V	V_{DS}= 15V I_D= 1nA
V_{GS}(on)	Operating Range	--	--	-2.3	V	V_{DS}=15V I_D=200µA
	GATE CURRENT					
$-I_G$max.	Operating	--	-4	-15	pA	V_{DG}= 15V I_D= 200µA
$-I_G$max.	High Temperature	--	--	-10	nA	T_A= +125°C
$-I_{GSS}$max.	At Full Conduction	--	--	100	pA	V_{DS} =0
$-I_{GSS}$max.	High Temperature	5	5	5	pA	V_{DG}= 15V T_A= +125°C
	OUTPUT CONDUCTANCE					
Y_{OSS}	Full Conduction	--	--	20	µmho	V_{DG}= 10V V_{GS}= 0V
Y_{OS}	Operating	--	0.2	2	µmho	V_{DG}= 15V I_D= 500µA
	COMMON MODE REJECTION					
CMR	-20 log $\lvert V_{GS1-2} / V_{DS} \rvert$	95	--	--	dB	V_{DS} = 10 to 20V I_D=30µA
	NOISE					V_{DS}= 15V V_{GS}= 0V R_G= 10M
NF	Figure	--	--	0.5	dB	f= 100Hz NBW= 6Hz
e_n	Voltage	--	20	--	nV/√Hz	V_{DS}=15V I_D=200µA f=10Hz NBW=1Hz
	CAPACITANCE					
C_{ISS}	Input	--	--	8	pF	V_{DS}= 15V I_D= 200µA f= 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	

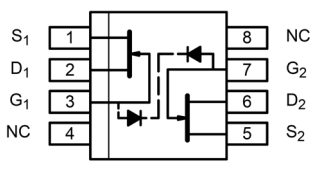
Click To Buy

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

SST402 in PDIP / SOIC
SST402 available as bare die
Please contact Micross for full package and die dimensions

PDIP / SOIC (Top View)



Micross Components Europe

micross

Tel: +44 1603 788967
Email: chipcomponents@micross.com
Web: http://www.micross.com/distribution

Information furnished by Linear Integrated Systems and Micross Components is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.