



LP5907-Q1 用于 RF 和模拟电路的超低噪声、250mA 线性稳压器 - 无需旁路电容

1 特性

- 符合 AEC-Q100 1 级标准
- 与 1 μ F 陶瓷输入和输出电容搭配使用，性能稳定
- 无需噪声旁路电容
- 支持远距离安置输出电容
- 热过载保护和短路保护
- 运行结温范围：-40°C 到 125°C
- 输入电压范围：2.2V 至 5.5V
- 输出电压范围：1.2V 至 4.5V
- 输出电流：250mA
- 低输出电压噪声：< 10 μ V_{RMS}
- 电源抑制比 (PSRR)：1kHz 频率时为 82dB
- 输出电压容差： \pm 2%
- 几乎零 IQ（禁用时）：< 1 μ A
- 极低 I_Q（使能时）：12 μ A
- 启动时间：80 μ s
- 低压降：120mV（典型值）

2 应用范围

- 信息娱乐
- 仪表
- 车身电子装置

3 说明

LP5907-Q1 是一款能够提供 250mA 输出电流的线性稳压器。此器件专门针对 RF 和模拟电路而设计，可满足其低噪声、高 PSRR、低静态电流以及低线路或负载瞬态响应系数等诸多要求。LP5907-Q1 采用创新的设计技术，无需噪声旁路电容便可提供出色的噪声性能，并且支持远距离安置输出电容。

此器件设计为与 1 μ F 输入和 1 μ F 输出陶瓷电容搭配使用（无需独立的噪声旁路电容）。

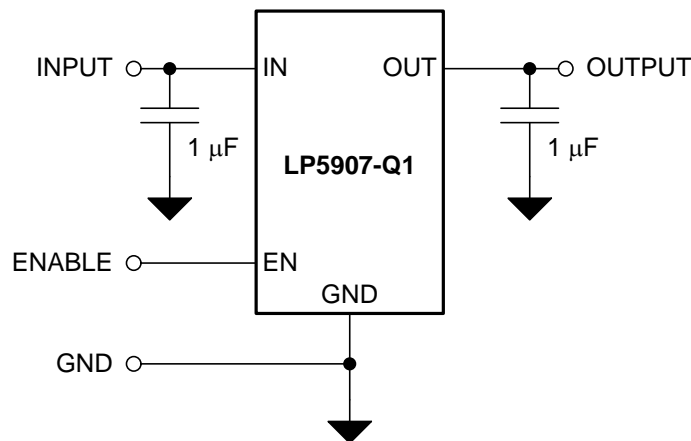
其固定输出电压介于 1.20V 和 4.50V 之间（以 25mV 为单位增量）。如需特定的电压选项，请联系德州仪器 (TI) 销售代表。

器件信息⁽¹⁾

| 器件型号 | 封装 | 封装尺寸（标称值） |
|-----------|------------|-----------------|
| LP5907-Q1 | SOT-23 (5) | 2.90mm x 1.60mm |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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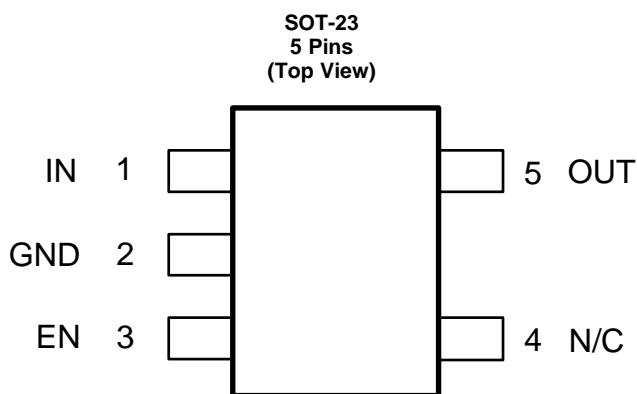
4 修订历史记录

| 日期 | 修订版本 | 注释 |
|------------|------|-------|
| 2014 年 9 月 | * | 最初发布。 |

5 Device Comparison Table

| SOT-23 PACKAGE ORDER NUMBER | VOLTAGE OPTION (V) |
|-----------------------------|--------------------|
| LP5907QMF1-1.2Q1 | 1.2 |
| LP5907QMF1-1.8Q1 | 1.8 |
| LP5907QMF1-2.5Q1 | 2.5 |
| LP5907QMF1-2.8Q1 | 2.8 |
| LP5907QMF1-3.0Q1 | 3.0 |
| LP5907QMF1-3.3Q1 | 3.3 |
| LP5907QMF1-3.8Q1 | 3.8 |
| LP5907QMF1-4.5Q1 | 4.5 |

6 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|--------|------|-----|--|
| NUMBER | NAME | | |
| 1 | IN | I | Input voltage supply. A 1-μF capacitor should be connected at this input. |
| 2 | GND | – | Common ground |
| 3 | EN | I | Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off and discharges the output pin to GND through an internal 230-Ω pull-down resistor. A high voltage ($> V_{IH}$) on this pin enables the regulator output. This pin has an internal 1-MΩ pull-down resistor to hold the regulator off by default. |
| 4 | N/C | – | No internal electrical connection. |
| 5 | OUT | O | Regulated output voltage. A minimum 1-μF low-ESR capacitor should be connected to this pin. Connect this output to the load circuit. An internal 230-Ω (typical) pull-down resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low). |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-------------------|---|--------------------|--------------------|------|
| V _{IN} | Input voltage | −0.3 | 6 | V |
| V _{OUT} | Output voltage | −0.3 | See ⁽³⁾ | |
| V _{EN} | Enable input voltage | −0.3 | 6 | |
| | Continuous power dissipation ⁽⁴⁾ | Internally Limited | | W |
| T _{JMAX} | Junction temperature | | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the GND pin.
- (3) Abs Max V_{OUT} is the lessor of V_{IN} + 0.3 V, or 6 V.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage.

7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|--------------------|---------------------------|---|-------|------|------|
| T _{stg} | Storage temperature range | | −65 | 150 | °C |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | −2000 | 2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | | | |
| | | Corner pins (1,3,4,5) | −1000 | 1000 | |
| | | Other pin (2) | −1000 | 1000 | |

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------------------|---|-----|-----|------|
| V _{IN} | Input supply voltage | 2.2 | 5.5 | V |
| V _{EN} | Enable input voltage | 0 | 5.5 | |
| I _{OUT} | Output current | 0 | 250 | mA |
| T _{J-MAX-OP} | Operating junction temperature ⁽³⁾ | −40 | 125 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the GND pin.
- (3) T_{J-MAX-OP} = (T_{A(MAX)} + (P_{D(MAX)} × R_{θJA})).

7.4 Thermal Information⁽¹⁾

| THERMAL METRIC ⁽²⁾ | | SOT-23 (DBV) | UNIT |
|-------------------------------|--|--------------|------|
| | | 5 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 193.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 102.1 | |
| R _{θJB} | Junction-to-board thermal resistance | 45.8 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 8.4 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 45.3 | |

- (1) Thermal performance is based on the JEDEC standard: *JESD51-7 High Effective Thermal Conductivity Test Board for Leadless Surface Mount Packages*.
- (2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾

 $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise stated.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------------|---|---|---------------------------|-------|-----|-----|-------------------|
| V _{IN} | Input voltage | T _A = 25°C | | 2.2 | | 5.5 | V |
| ΔV _{OUT} | Output voltage tolerance | V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA to 250 mA, V _{OUT} ≥ 1.8 V | | −2 | | 2 | %V _{OUT} |
| | | V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA to 250 mA, V _{OUT} < 1.8 V | | −3 | | 3 | |
| | Line regulation | V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA | | 0.02 | | | %/V |
| | Load regulation | I _{OUT} = 1 mA to 250 mA | | 0.001 | | | %/mA |
| I _{LOAD} | Output load current | | | 0 | | 250 | mA |
| I _Q | Quiescent current ⁽⁴⁾ | V _{EN} = 1.2 V, I _{OUT} = 0 mA | | 12 | | 25 | μA |
| | | V _{EN} = 1.2 V, I _{OUT} = 250 mA | | 250 | | 425 | |
| | | V _{EN} = 0.3 V (Disabled) | | 0.2 | | 1 | |
| I _G | Ground current ⁽⁵⁾ | V _{EN} = 1.2 V, I _{OUT} = 0 mA | | 14 | | | μA |
| V _{DO} | Dropout voltage ⁽⁶⁾ | I _{OUT} = 100 mA | | 50 | | | mV |
| | | I _{OUT} = 250 mA | | | | 250 | |
| I _{SC} | Short circuit current limit | T _A = 25°C ⁽⁷⁾ | | 250 | 500 | | mA |
| PSRR | Power supply rejection ratio ⁽⁸⁾ | f = 100 Hz, I _{OUT} = 20 mA | | 90 | | | dB |
| | | f = 1 kHz, I _{OUT} = 20 mA | | 82 | | | |
| | | f = 10 kHz, I _{OUT} = 20 mA | | 65 | | | |
| | | f = 100 kHz, I _{OUT} = 20 mA | | 60 | | | |
| e _N | Output noise voltage ⁽⁸⁾ | BW = 10 Hz to 100 kHz | I _{OUT} = 1 mA | 10 | | | μV _{RMS} |
| | | | I _{OUT} = 250 mA | 6.5 | | | |
| R _{AD} | Output Automatic Discharge pull-down resistance | V _{EN} < V _{IL} (output disabled) | | 230 | | | Ω |
| T _{SD} | Thermal shutdown | T _J rising | | 160 | | | °C |
| | Thermal hysteresis | T _J falling from shutdown | | 15 | | | |
| LOGIC INPUT THRESHOLDS | | | | | | | |
| V _{IL} | Low input threshold | V _{IN} = 2.2 V to 5.5 V V _{EN} falling until the output is disabled | | 0.4 | | | V |
| V _{IH} | High input threshold | V _{IN} = 2.2 V to 5.5 V V _{EN} rising until the output is enabled | | 1.2 | | | V |
| I _{EN} | Input current at EN pin ⁽⁹⁾ | V _{EN} = 5.5 V and V _{IN} = 5.5 V | | 5.5 | | | μA |
| | | V _{EN} = 0 V and V _{IN} = 5.5 V | | 0.001 | | | |

- (1) All voltages are with respect to the device GND terminal, unless otherwise stated.
- (2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of -40°C to 125°C , unless otherwise stated. Typical values represent the most likely parametric norm at $T_A = 25^\circ\text{C}$, and are provided for reference purposes only.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$. See [Applications and Implementation](#).
- (4) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT} .
- (5) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
- (6) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
- (7) Short-circuit current (I_{SC}) for the LP5907-Q1 is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.
- (8) This specification is verified by design.
- (9) There is a 1-M Ω resistor between EN and ground on the device.

Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾ (continued)

$V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise stated.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|-------------------------------|---|--|-----|-----|---------------|
| TRANSIENT CHARACTERISTICS | | | | | | |
| ΔV_{OUT} | Line transient ⁽⁸⁾ | $V_{IN} = (V_{OUT(NOM)} + 1\text{ V})$ to $(V_{OUT(NOM)} + 1.6\text{ V})$ in 30 μs | -1 | | | mV |
| | | $V_{IN} = (V_{OUT(NOM)} + 1.6\text{ V})$ to $(V_{OUT(NOM)} + 1\text{ V})$ in 30 μs | | 1 | | |
| | Load transient ⁽⁸⁾ | $I_{OUT} = 1\text{ mA}$ to 250 mA in 10 μs | -40 | | | mV |
| | | $I_{OUT} = 250\text{ mA}$ to 1mA in 10 μs | | | 40 | |
| | | Overshoot on start-up ⁽⁸⁾ | Stated as a percentage of $V_{OUT(NOM)}$ | | | 5% |
| t_{ON} | Turnon time | From $V_{EN} > V_{IH}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$ $T_A = 25^{\circ}\text{C}$ | | 80 | 150 | μs |

7.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP | MAX | UNIT |
|-----------|---|---------------------------|--------------------|-----|-----|---------------|
| C_{IN} | Input capacitance ⁽²⁾ | Capacitance for stability | 0.7 | 1 | | μF |
| C_{OUT} | Output capacitance ⁽²⁾ | | 0.7 | 1 | 10 | |
| ESR | Output/Input capacitance ⁽²⁾ | | 5 | | 500 | m Ω |

- (1) The minimum capacitance should be greater than $0.5\text{ }\mu\text{F}$ over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.
- (2) This specification is verified by design.

7.7 Typical Characteristics

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$

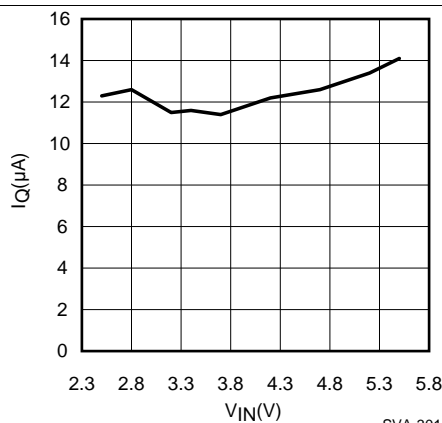


Figure 1. Quiescent Current vs Input Voltage

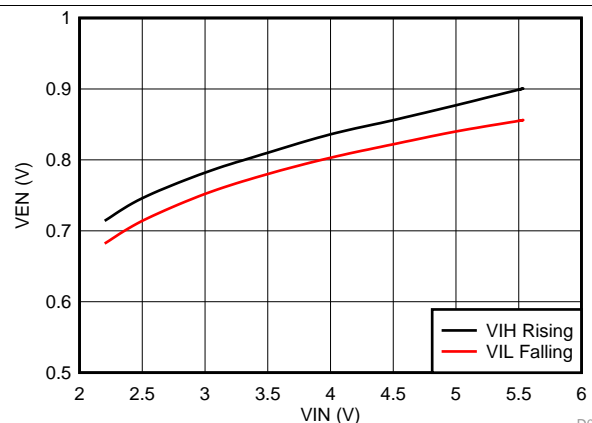


Figure 2. V_{EN} Thresholds vs V_{IN}

Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$

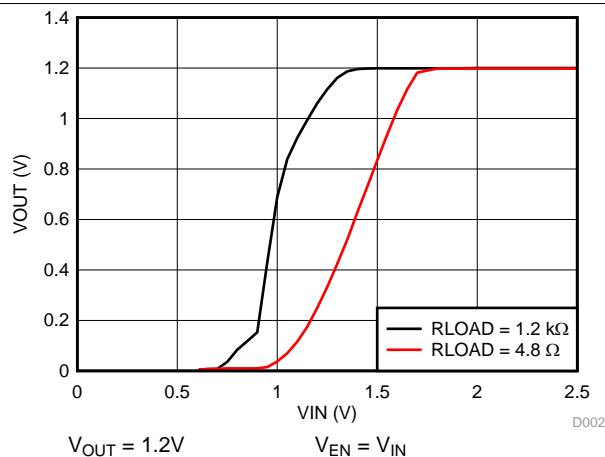


Figure 3. V_{OUT} vs V_{IN}

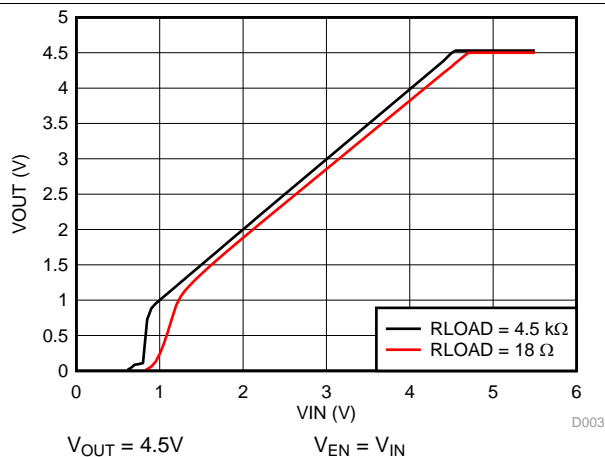


Figure 4. V_{OUT} vs V_{IN}

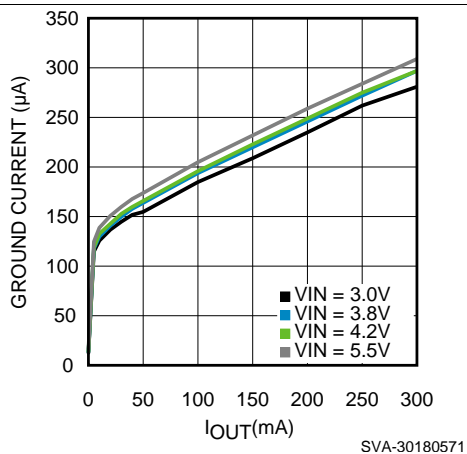


Figure 5. Ground Current vs Output Current

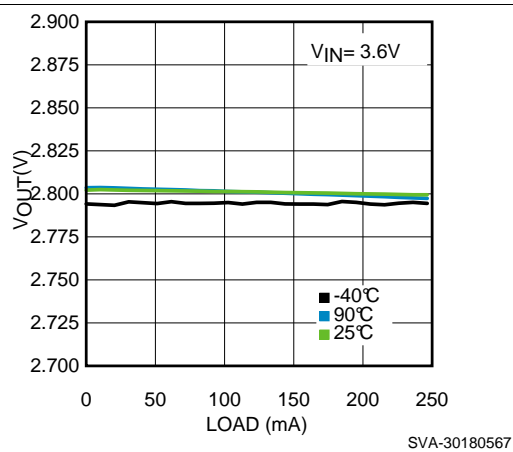


Figure 6. Load Regulation

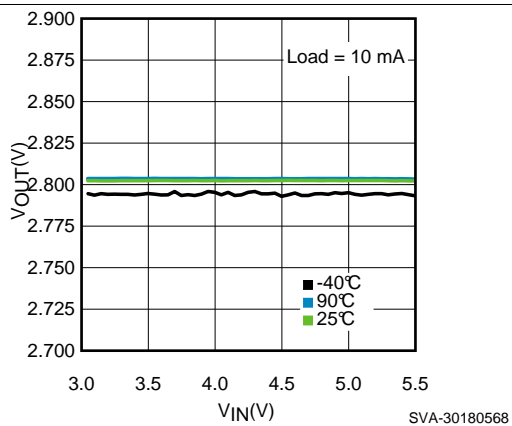


Figure 7. Line Regulation

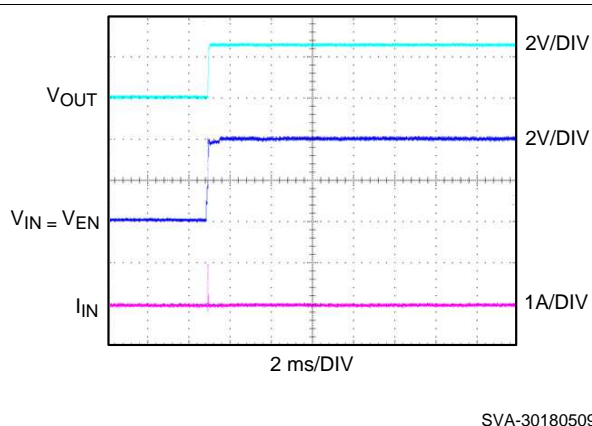
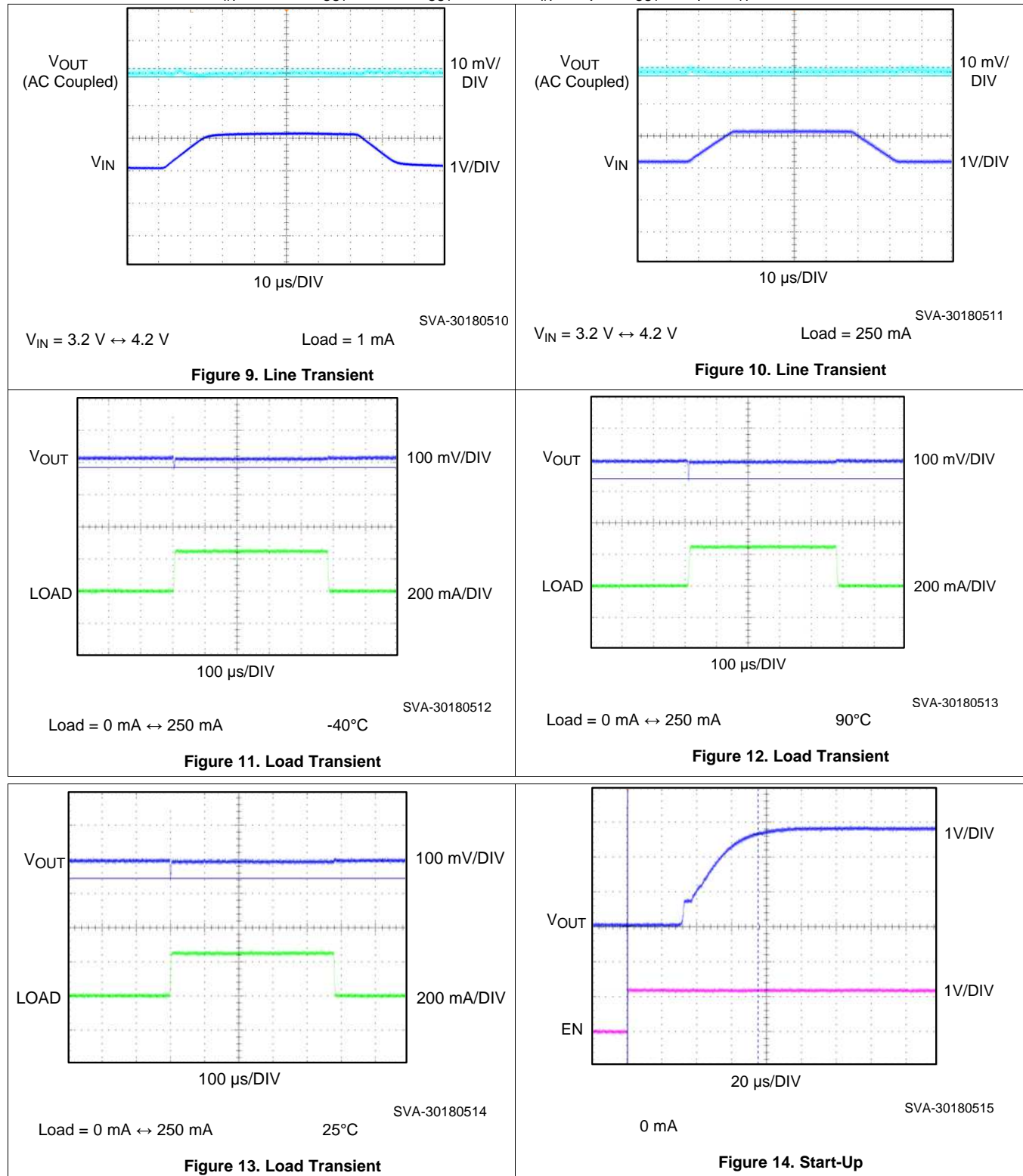


Figure 8. Inrush Current

Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$



Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$

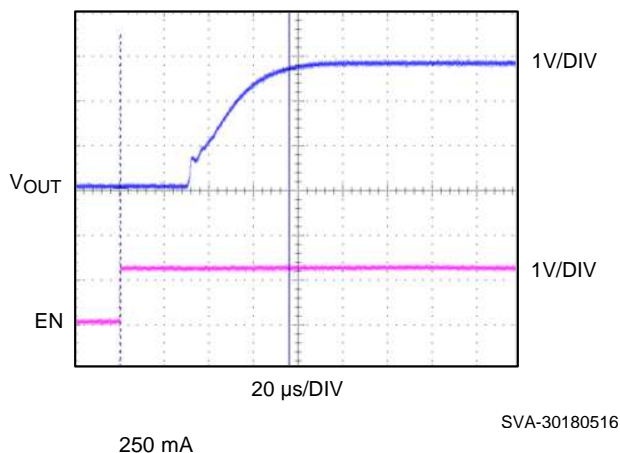


Figure 15. Start-Up

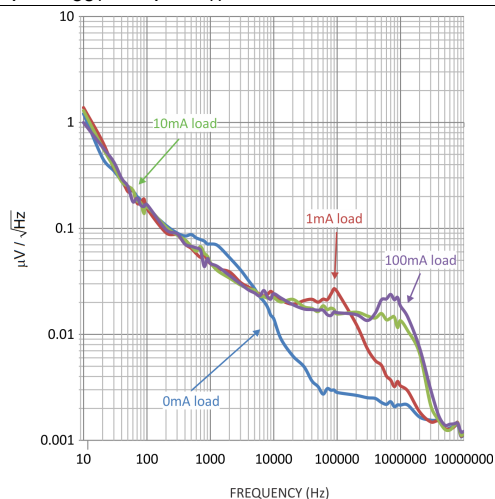


Figure 16. Noise Density Test

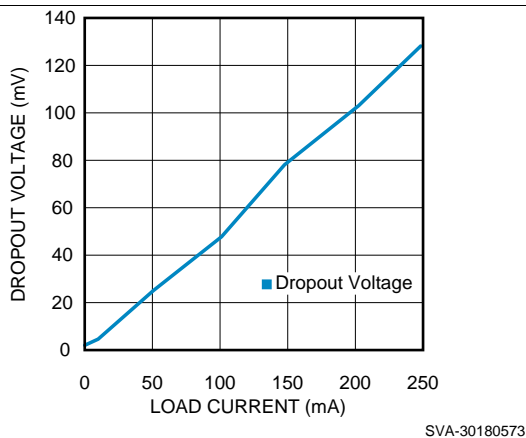


Figure 17. Dropout Voltage vs Load Current

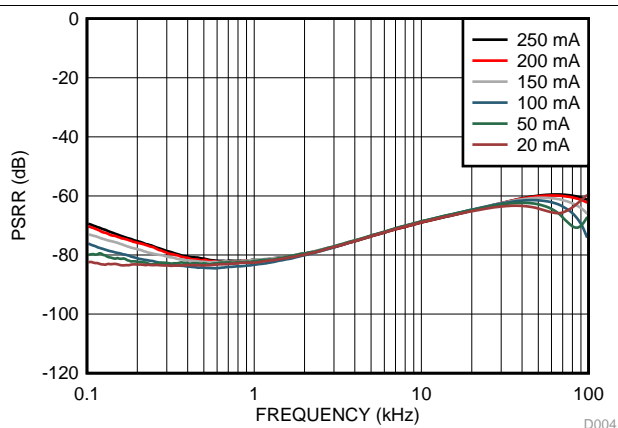


Figure 18. PSRR Loads Averaged 100 Hz To 100 KHz

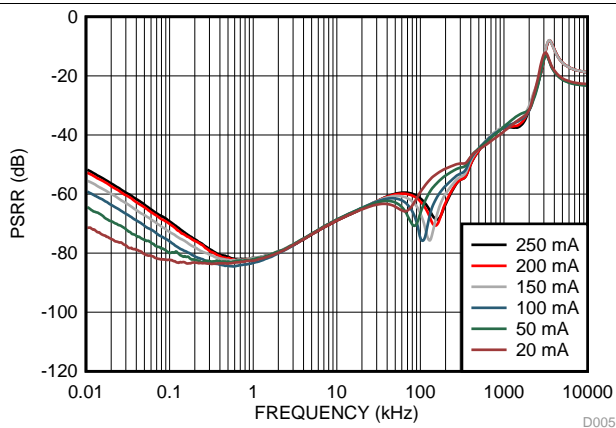


Figure 19. PSRR Loads Averaged 10 Hz To 10 MHz

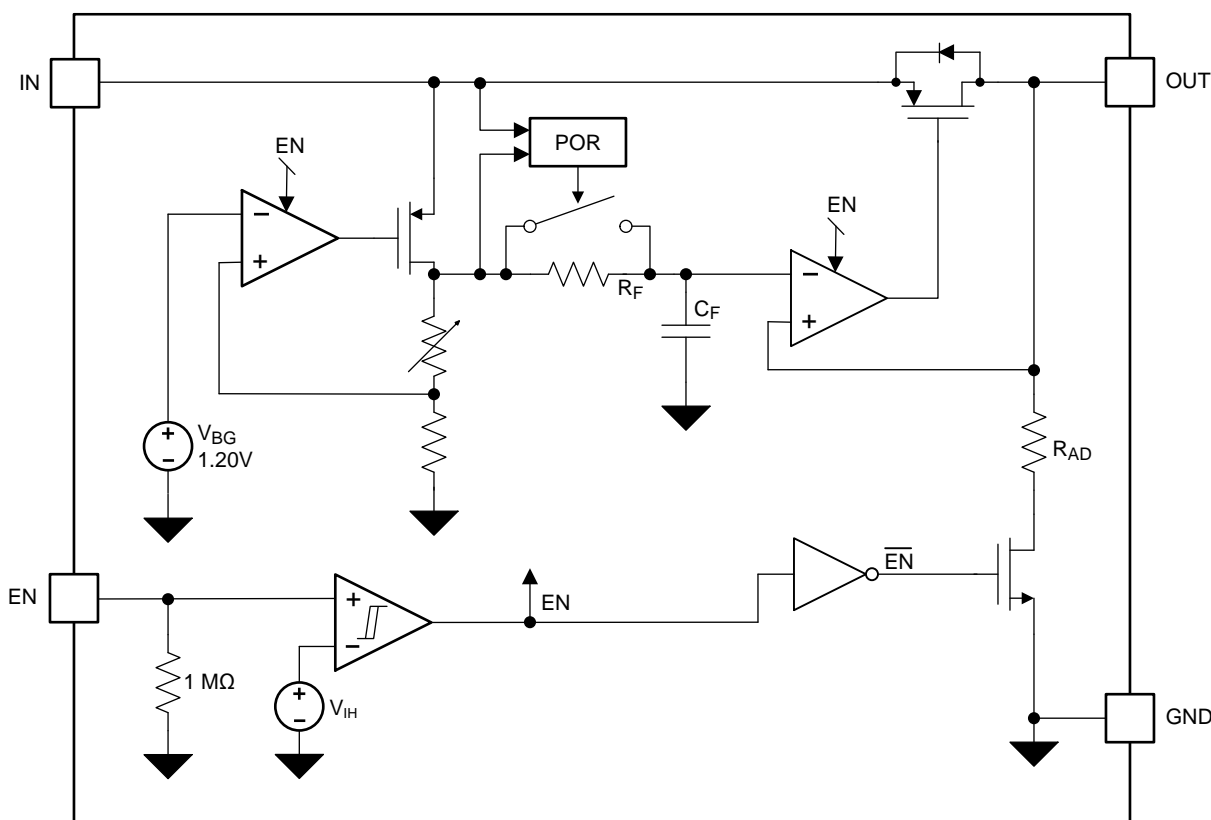
8 Detailed Description

8.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the LP5907-Q1 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using new innovative design techniques, the LP5907-Q1 offers class leading noise performance without the need for a separate noise filter capacitor.

The LP5907-Q1 is designed to perform with a single 1- μF input capacitor and a single 1- μF ceramic output capacitor. With a reasonable PCB layout, the single 1- μF ceramic output capacitor can be placed up to 10 cm away from the LP5907-Q1 package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable (EN)

The LP5907-Q1 EN pin is internally held low by a 1-M Ω resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

8.3.2 Low Output Noise

Any internal noise at the LP5907-Q1 reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. The low-pass RC filter has a -3 dB cut-off frequency of approximately 0.1 Hz.

Feature Description (continued)

8.3.3 Output Automatic Discharge

The LP5907-Q1 output employs an internal 230- Ω (typical) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

8.3.4 Remote Output Capacitor Placement

The LP5907-Q1 requires at least a 1- μ F capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

8.3.5 Thermal Overload Protection (T_{SD})

Thermal Shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The Thermal Shutdown circuitry of the LP5907-Q1 has been designed to protect against temporary thermal overload conditions. The Thermal Shutdown circuitry was not intended to replace proper heat-sinking. Continuously running the LP5907-Q1 device into thermal shutdown may degrade device reliability.

8.4 Device Functional Modes

8.4.1 Enable (EN)

The LP5907-Q1 Enable (EN) pin is internally held low by a 1-M Ω resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuitry is activated. Any charge on the OUT pin is discharged to GND through the internal 230- Ω (typical) pull-down resistance.

8.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5907-Q1 does not include any dedicated UVLO circuitry. The LP5907-Q1 internal circuitry is not fully functional until V_{IN} is at least 2.2 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2 V or ($V_{OUT} + V_{DO}$).

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 20 shows the typical application circuit for the LP5907-Q1. Input and output capacitances may need to be increased above the 1 μF minimum for some applications.

9.2 Typical Application

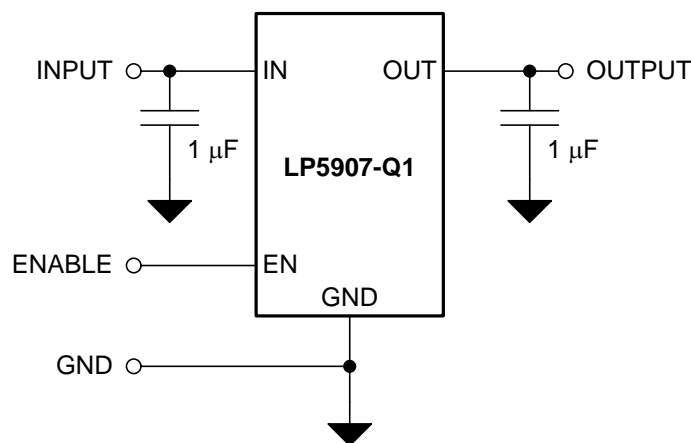


Figure 20. LP5907-Q1 Typical Application

9.2.1 Design Requirements

| DESIGN PARAMETER | EXAMPLE VALUE |
|----------------------------------|-------------------------|
| Input Voltage Range | 2.2 to 5.5 V |
| Output Voltage | 1.8 V |
| Output Current | 200 mA |
| Output Capacitor range | 0.7 to 10 μF |
| Input/Output Capacitor ESR Range | 5 to 500 m Ω |

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Available input voltage range
- Output voltage needed
- Output current needed
- Input and Output capacitors

9.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using [Equation 1](#):

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) may have to be derated. T_{A-MAX} is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by [Equation 3](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (3)$$

Alternately, if T_{A-MAX} can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the ' $V_{IN}-V_{OUT}$ ' term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

9.2.2.2 External Capacitors

Like most low-dropout regulators, the LP5907-Q1 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

9.2.2.3 Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1 μF capacitor has to be connected between the LP5907-Q1 input pin and ground for stable operation over full load current range. Basically, it is ok to have more output capacitance than input, as long as the input is at least 1 μF .

The input capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5907-Q1, then it is recommended to increase the input capacitor to at least 10 μF . Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application. The initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 μF over the entire operating range.

9.2.2.4 Output Capacitor

The LP5907-Q1 is designed specifically to work with a very small ceramic output capacitor, typically 1 μF . A ceramic capacitor (dielectric types X5R or X7R) in the 1 μF to 10 μF range, and with ESR between 5 m Ω to 500 m Ω , is suitable in the LP5907-Q1 application circuit. For this device the output capacitor should be connected between the OUT pin and a good connection back to the GND pin.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT} , but these are not as attractive for reasons of size and cost (see [Capacitor Characteristics](#)).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 m Ω to 500 m Ω for stability. Like the input capacitor, the initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 μF over the entire operating range.

9.2.2.5 Capacitor Characteristics

The LP5907-Q1 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 μF to 10 μF , ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1 μF ceramic capacitor is in the range of 20 m Ω to 40 m Ω , which easily meets the ESR requirement for stability for the LP5907-Q1.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within $\pm 15\%$ over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 μF to 10 μF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

9.2.2.6 Remote Capacitor Operation

The LP5907-Q1 requires at least a 1 μF capacitor at the OUT pin, but there is no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, it is good to keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

9.2.2.7 No-Load Stability

The LP5907-Q1 remains stable, and in regulation, with no external load.

9.2.2.8 Enable Control

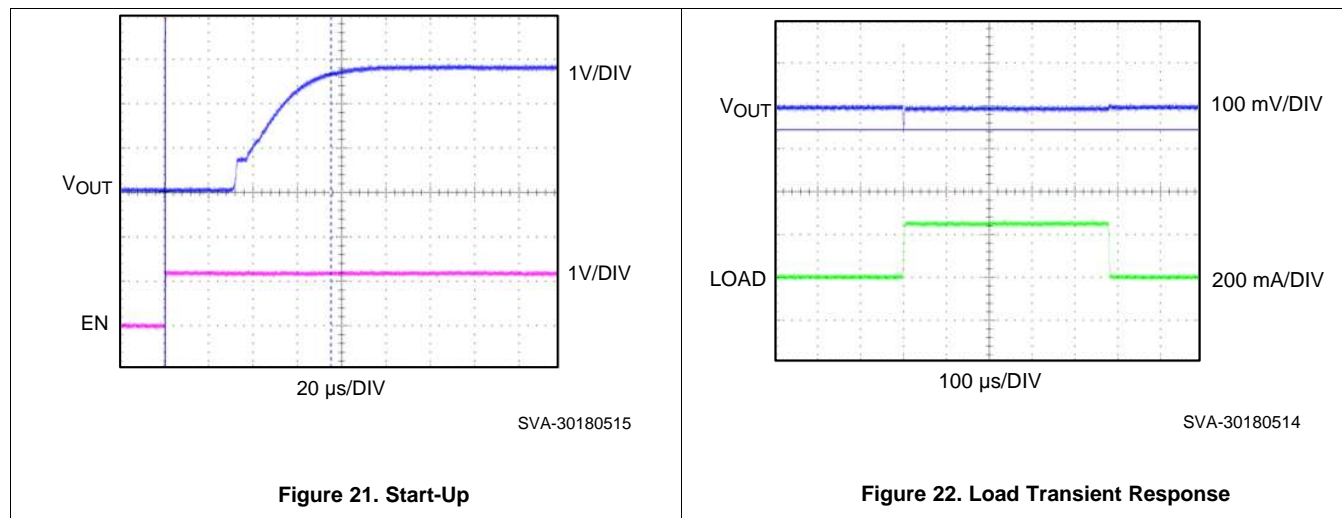
The LP5907-Q1 may be switched ON or OFF by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, while a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 μA . Additionally, an output pull-down circuit is activated which ensures that any charge stored on C_{OUT} is discharged to ground.

If the application does not require the use of the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1-M Ω pull-down resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the [Electrical Characteristics](#) under V_{IL} and V_{IH} .

9.2.3 Application Curves



10 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.2 V to 5.5 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP5907-Q1 output voltage is well regulated and dynamic performance is optimum, the input supply should be at least $V_{OUT} + 1$ V. A minimum capacitor value of 1 μ F is required to be within 1 cm of the IN pin.

11 Layout

11.1 Layout Guidelines

The dynamic performance of the LP5907-Q1 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDO's may degrade the PSRR, noise, or transient performance of the LP5907-Q1.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907-Q1, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LP5907-Q1 ground pin using as wide, and as short, of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions

11.2 Layout Example

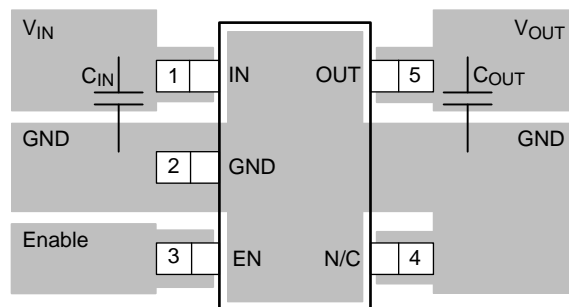


Figure 23. LP5907MF-x.x (SOT-23) Typical Layout

12 器件和文档支持

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12.3 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP5907QMF1-1.2Q1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | RAFQ | Samples |
| LP5907QMF1-1.8Q1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | RAGQ | Samples |
| LP5907QMF1-2.5Q1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | RAJQ | Samples |
| LP5907QMF1-2.8Q1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | RAKQ | Samples |
| LP5907QMF1-3.0Q1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | RALQ | Samples |
| LP5907QMF1-3.3Q1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | RAHQ | Samples |
| LP5907QMF1-3.8Q1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | RAMQ | Samples |
| LP5907QMF1-4.5Q1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | RAIQ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

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TBD: The Pb-Free/Green conversion plan has not been defined.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF LP5907-Q1 :

- Catalog: [LP5907](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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| 放大器和线性器件 | www.ti.com.cn/amplifiers | 计算机及周边 | www.ti.com.cn/computer |
| 数据转换器 | www.ti.com.cn/dataconverters | 消费电子 | www.ti.com.cn/consumer-apps |
| DLP® 产品 | www.dlp.com | 能源 | www.ti.com.cn/energy |
| DSP - 数字信号处理器 | www.ti.com.cn/dsp | 工业应用 | www.ti.com.cn/industrial |
| 时钟和计时器 | www.ti.com.cn/clockandtimers | 医疗电子 | www.ti.com.cn/medical |
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