Micron Parallel NOR Flash Embedded Memory

M29DW256G X16 Multiple Bank, Page, Dual Boot 3V Supply Flash Memory

Features

- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{CCQ} = 1.65–3.6V (I/O buffers)
  - V_{PPH} = 9V for fast program (optional)
- Asynchronous random/page read
  - Page size: 8 words
  - Page access: 25ns, 30ns
  - Random access: 70ns, 80ns
- Fast program commands: 32-word
- Enhanced buffered program commands: 256-word
- Program time
  - 16µs per byte/word TYP
  - Chip program time: 10 s with V_{PPH} and 16s without V_{PPH}
- Memory organization
  - Quadruple bank memory array: 32Mb + 96Mb + 96Mb + 32Mb with parameter blocks at top and bottom
  - Dual operation: program/erase in one bank while reading in any other bank
- Program/erase controller
  - Embedded word program algorithms
- Program/erase suspend and resume capability
  - Read from any block during a PROGRAM SUSPEND operation
  - Read or program another block during an ERASE SUSPEND operation
- Unlock bypass, block erase, chip erase, write to buffer, and enhanced buffer program commands
  - Fast buffered/batch programming
  - Fast block/chip erase
- V_{PP}/WP# pin for fast program and write
  - Protects the four outermost parameter blocks
- Software protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
- Extended memory block
  - Programmed or locked at the factory or by the customer
  - 128 word factory locked and 128 word customer lockable
- Common flash interface
  - 64-bit security code
- Low power consumption: standby and automatic mode
- 100,000 minimum PROGRAM/ERASE cycles per block
- Data retention: 20 years (TYP)
- Fortified BGA, TBGA, and TSOP packages
- Green packages available
  - RoHS-compliant
  - Halogen-free
- Automotive certified parts available
  - Automotive device grade: temperature –40°C to +85°C (automotive grade certified)
- Root part number
  - M29DW256G
- Device code
  - 227Eh + 223Ch + 2202h

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Part Numbering Information

Available with extended memory block prelocked by Micron. Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or high/low protection, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Part Number Information

Part Number Category	Category Details	Notes
Device Type	M29	
Architecture	D = Dual operation	
Operating Voltage	W = VCC = 2.7 to 3.6V	
Device function	256G = 256Mb (x16) page, dual boot	
Speed	70 = 70ns	1, 2
	7A = 70ns	1, 2
Package	NF = 56-pin TSOP, 14mm x 20mm, lead-free, halogen-free, RoHS-compliant	
	ZA = 64-pin TBGA, 10mm x 13mm, lead-free, halogen-free, RoHS-compliant	
	ZS = 64-pin Fortified BGA, 11mm x 13mm, lead-free, halogen-free, RoHS-compliant	
Temperature Range	1 = 0 to 70°C	
	6 = –40°C to +85°C	
Shipping Options	E = RoHS-compliant package, standard packing	
	F = RoHS-compliant package, tape and reel packing	

Notes: 1. 80ns if VCCQ = 1.65V to VCC.
2. Automotive certified –40°C to +85°C, available only with option 6.

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Description

The M29DW256G is a 256Mb (16Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6 V) supply. At power-up the memory defaults to its read mode.

The M29DW256G features an asymmetrical block architecture, with 8 parameter and 126 main blocks, divided into four banks, A, B, C and D, providing multiple bank operations. While programming or erasing in one bank, read operations are possible in any other bank. Four of the parameter blocks are at the top of the memory address space, and four are at the bottom.

Program and erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operations of the memory. They allow simple connection to most microprocessors, often without additional logic.

The device supports asynchronous random read and page read from all blocks of the memory array. The device also features a write to buffer program capability that improves the programming throughput by programming 32 words in one instance. The enhanced buffered program feature is also available to speed up programming throughput, allowing 256 words to be programmed at once. The V_{PP}/WP# signal can be used to enable faster programming of the device.

The M29DW256G has one extra 256-word extended block that can be accessed using a dedicated command: 128-Word factory locked and 128-Word customer lockable. The extended block can be protected and so is useful for storing security information. However the protection is irreversible; once protected the protection cannot be undone.

The device features different levels of hardware and software block protection to avoid unwanted program or erase (modify):

- Hardware protection: V_{PP}/WP# provides hardware protection on four outermost parameter blocks (two at the top and two at the bottom of the address space)
- Software protection: Volatile protection, nonvolatile protection, password protection

The memory is offered in TSOP56 (14mm x 20mm), TBGA64 (10mm x 13mm, 1mm pitch), and FBGA (11mm x 13mm) packages. The memory is delivered with all the bits erased (set to '1').

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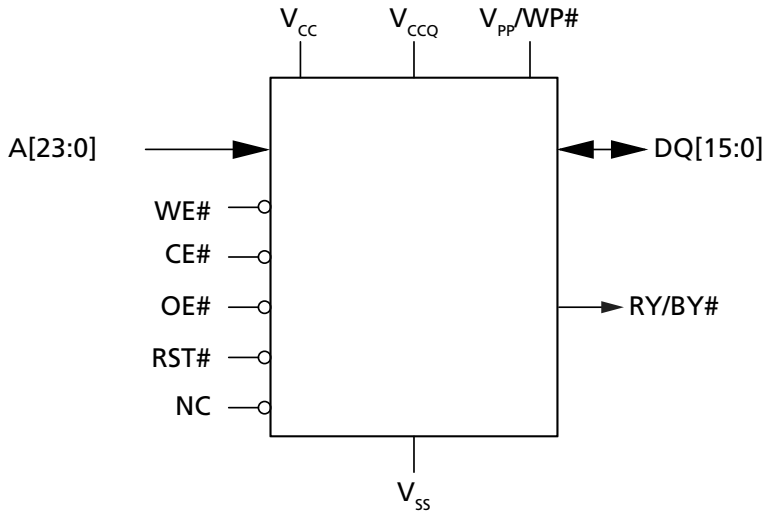
Signals

Table 2: Signal names

Name	Description	Direction
A[23:0]	Address inputs	Inputs
DQ[15:0]	Data inputs/outputs	I/O
CE#	Chip enable	Input
OE#	Output enable	Input
WE#	Write enable	Input
RST#	Reset	Input
RY/BY#	Ready/busy output	Output
V_{CCQ}	Input/output buffer supply voltage	Supply
V_{CC}	Supply voltage	Supply
V_{PP}/WP#	V_{PP}/write protect	Supply/Input
V_{SS}	Ground	–
NC	Not connected	–

Note: 1. [1] V_{PP}/WP# may be left floating as it is internally connected to a pull-up resistor which enables program/erase operations.

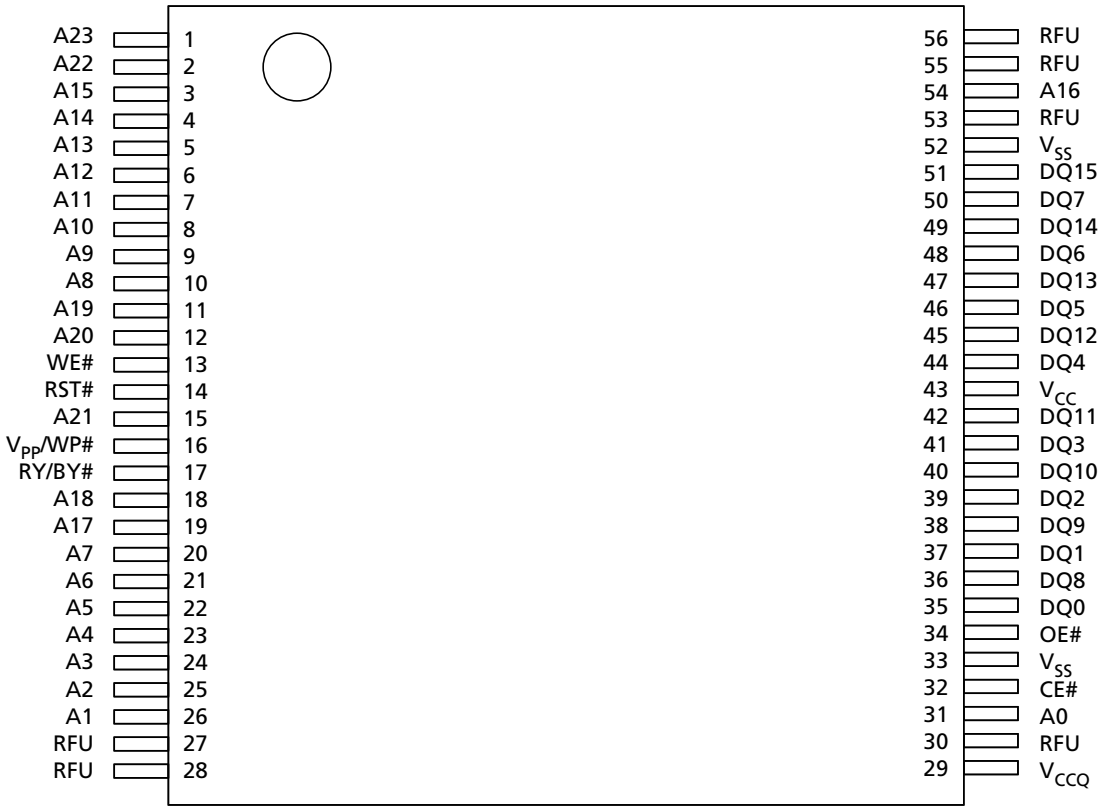
Figure 1: Logic diagram



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Signal Assignments

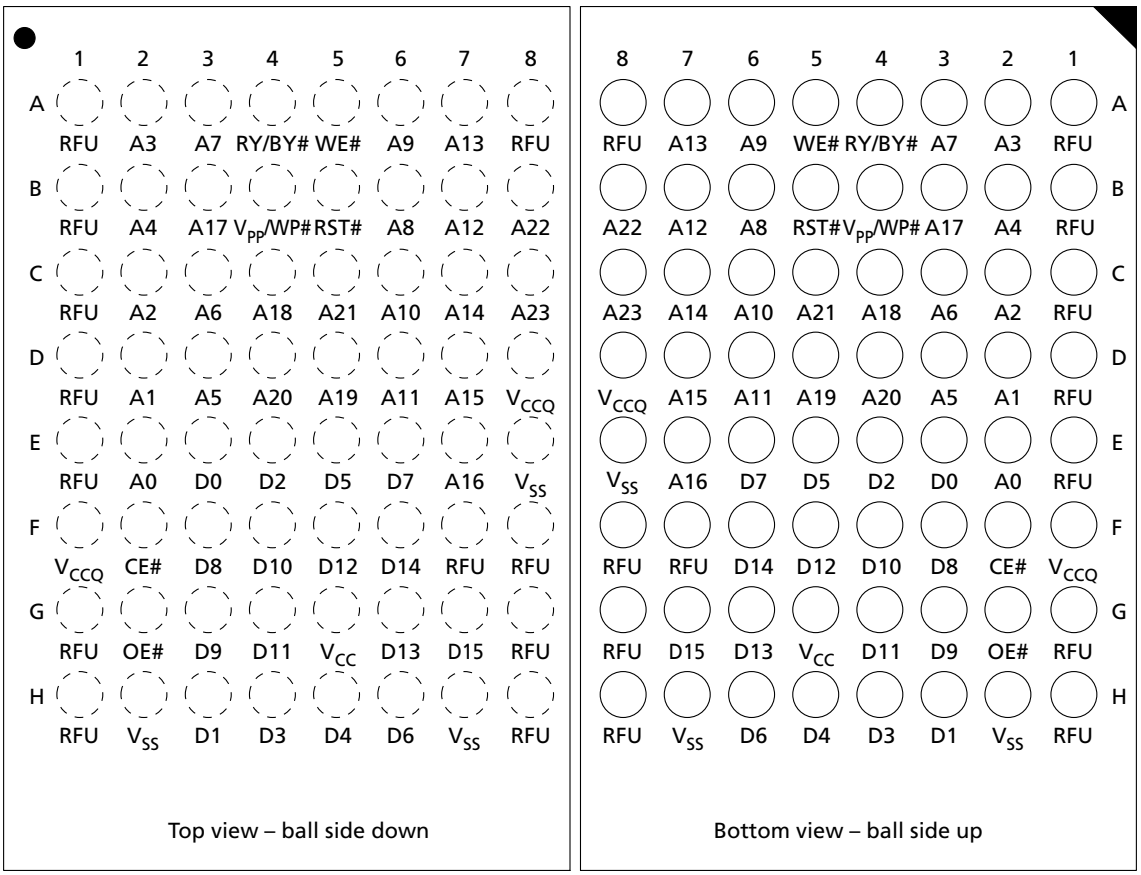
Figure 2: 56-Pin TSOP (Top View)



Note: 1. A[23] = A[MAX].

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Figure 3: 64-Pin Fortified BGA and 64-Pin TBGA



Note: 1. A[23] = A[MAX].

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Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 3: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller.
DQ[15:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine. During WRITE operations, bits DQ[15:8] are not used. When reading the status register, these bits should be ignored.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, the device goes to standby and data outputs are at HIGH-Z.
OE#	Input	**Output enable:** Controls the bus READ operation.
WE#	Input	**Write enable:** Controls the bus WRITE operation of the command interface.
V_{PP}/WP#	Input	**V_{PP}/Write Protect:** Provides two functions. The V_{PPH} function enables the device to bypass unlock cycles and use an external high voltage power supply to reduce time required for PROGRAM operations. Second, When V_{PP}/WP# is LOW, the four outermost blocks of the address space (two 32KW blocks at the top and two 32KW blocks at the bottom) are protected; PROGRAM and ERASE operations are ignored and the blocks remain protected regardless of the block protection status or the RST# pin state. When V_{PP}/WP# is HIGH, the memory reverts to the previous protection status for those blocks (Refer to Hardware Protection and Bypass Operations for details).
RST#	Input	**Reset:** Applies a hardware reset to the device, which is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^{t}PHEL or ^{t}RHEL, whichever occurs last). See RESET AC Specifications for more details.
RY/BY#	Output	**Ready busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z (see RESET AC Specifications for more details). The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V_{CCQ}. A low value will then indicate that one or more of the devices is busy.
V_{CC}	Supply	**Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The command interface is disabled when V_{CC} <= V_{LKO}. This prevents WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid. A 0.1µF capacitor should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations (see DC Characteristics).

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Table 3: Signal Descriptions (Continued)

Name	Type	Description
V_{CCQ}	Supply	**I/O supply voltage:** Provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.
V_{SS}	Supply	**Ground:** All V_{SS} pins must be connected to the system ground.
RFU	–	**Reserved for future use:** RFUs should be not connected.

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Memory Organization

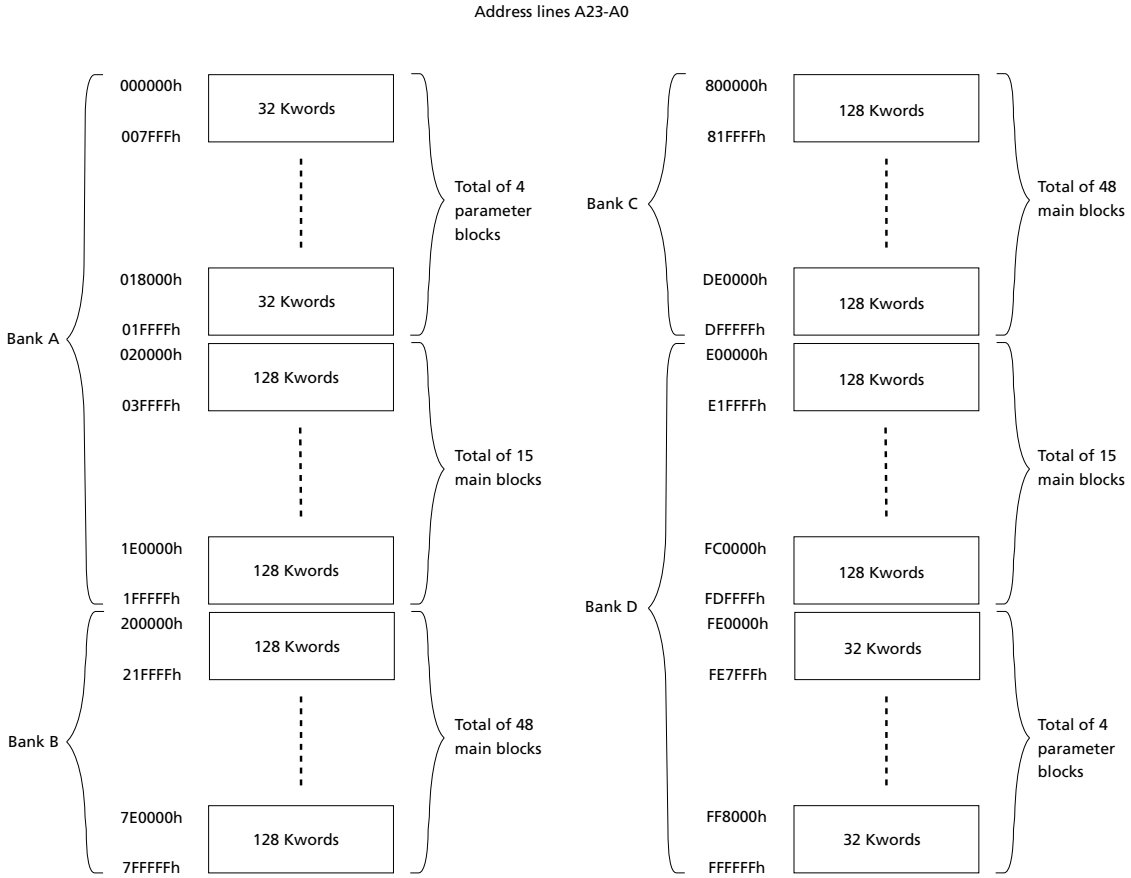
Memory Configuration

The M29DW256G features an asymmetrical block architecture, with 8 parameter and 126 main blocks, divided into four banks providing multiple bank operations. Four parameter blocks are at the top of the memory address space, and four are at the bottom.

Table 4: Bank architecture

Bank	Bank Size	Parameter Blocks		Main Blocks	
		Number of Blocks	Block Size	Number of Blocks	Block Size
A	32Mb	4	32 Kwords	15	128 Kwords
B	96Mb	—	—	48	128 Kwords
C	96Mb	—	—	48	128 Kwords
D	32Mb	4	32 Kwords	15	128 Kwords

Figure 4: Block Addresses



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Block Addresses and Protection Groups

Table 5: Bank A

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
0	Protection Group	32	0000000 - 0007FFF
1	Protection Group	32	0008000 - 000FFFF
2	Protection Group	32	0010000 - 0017FFF
3	Protection Group	32	0018000 - 001FFFF
4	Protection Group	128	0020000 - 003FFFF
5	Protection Group	128	0040000 - 005FFFF
6	Protection Group	128	0060000 - 007FFFF
7	Protection Group	128	0080000 - 009FFFF
8	Protection Group	128	00A0000 - 00BFFFF
9	Protection Group	128	00C0000 - 00DFFFF
10	Protection Group	128	00E0000 - 00FFFFF
11	Protection Group	128	0100000 - 011FFFF
12	Protection Group	128	0120000 - 013FFFF
13	Protection Group	128	0140000 - 015FFFF
14	Protection Group	128	0160000 - 017FFFF
15	Protection Group	128	0180000 - 019FFFF
16	Protection Group	128	01A0000 - 01BFFFF
17	Protection Group	128	01C0000 - 01DFFFF
18	Protection Group	128	01E0000 - 01FFFFF

Table 6: Bank B

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
19	Protection Group	128	0200000 - 021FFFF
20	Protection Group	128	0220000 - 023FFFF
21	Protection Group	128	0240000 - 025FFFF
22	Protection Group	128	0260000 - 027FFFF
23	Protection Group	128	0280000 - 029FFFF
24	Protection Group	128	02A0000 - 02BFFFF
25	Protection Group	128	02C0000 - 02DFFFF
26	Protection Group	128	02E0000 - 02FFFFF
27	Protection Group	128	0300000 - 031FFFF
28	Protection Group	128	0320000 - 033FFFF
29	Protection Group	128	0340000 - 035FFFF
30	Protection Group	128	0360000 - 037FFFF
31	Protection Group	128	0380000 - 039FFFF
32	Protection Group	128	03A0000 - 03BFFFF

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Table 6: Bank B (Continued)

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
33	Protection Group	128	03C0000 - 03DFFFF
34	Protection Group	128	03E0000 - 03FFFFF
35	Protection Group	128	0400000 - 041FFFF
36	Protection Group	128	0420000 - 043FFFF
37	Protection Group	128	0440000 - 045FFFF
38	Protection Group	128	0460000 - 047FFFF
39	Protection Group	128	0480000 - 049FFFF
40	Protection Group	128	04A0000 - 04BFFFF
41	Protection Group	128	04C0000 - 04DFFFF
42	Protection Group	128	04E0000 - 04FFFFF
43	Protection Group	128	0500000 - 051FFFF
44	Protection Group	128	0520000 - 053FFFF
45	Protection Group	128	0540000 - 055FFFF
46	Protection Group	128	0560000 - 057FFFF
47	Protection Group	128	0580000 - 059FFFF
48	Protection Group	128	05A0000 - 05BFFFF
49	Protection Group	128	05C0000 - 05DFFFF
50	Protection Group	128	05E0000 - 05FFFFF
51	Protection Group	128	0600000 - 061FFFF
52	Protection Group	128	0620000 - 063FFFF
53	Protection Group	128	0640000 - 065FFFF
54	Protection Group	128	0660000 - 067FFFF
55	Protection Group	128	0680000 - 06FFFFF
56	Protection Group	128	06A0000 - 06BFFFF
57	Protection Group	128	06C0000 - 06DFFFF
58	Protection Group	128	06E0000 - 06FFFFF
59	Protection Group	128	0700000 - 071FFFF
60	Protection Group	128	0720000 - 073FFFF
61	Protection Group	128	0740000 - 075FFFF
62	Protection Group	128	0760000 - 077FFFF
63	Protection Group	128	0780000 - 079FFFF
64	Protection Group	128	07A0000 - 07BFFFF
65	Protection Group	128	07C0000 - 07DFFFF
66	Protection Group	128	07E0000 - 07FFFFF

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Table 7: Bank C

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
67	Protection Group	128	0800000 - 081FFFF
68	Protection Group	128	0820000 - 083FFFF
69	Protection Group	128	0840000 - 085FFFF
70	Protection Group	128	0860000 - 087FFFF
71	Protection Group	128	0880000 - 089FFFF
72	Protection Group	128	08A0000 - 08BFFFF
73	Protection Group	128	08C0000 - 08DFFFF
74	Protection Group	128	08E0000 - 08FFFFF
75	Protection Group	128	0900000 - 091FFFF
76	Protection Group	128	0920000 - 093FFFF
77	Protection Group	128	0940000 - 095FFFF
78	Protection Group	128	0960000 - 097FFFF
79	Protection Group	128	0980000 - 099FFFF
80	Protection Group	128	09A0000 - 09BFFFF
81	Protection Group	128	09C0000 - 09DFFFF
82	Protection Group	128	09E0000 - 09FFFFF
83	Protection Group	128	0A00000 - 0A1FFFF
84	Protection Group	128	0A20000 - 0A3FFFF
85	Protection Group	128	0A40000 - 0A5FFFF
86	Protection Group	128	0A60000 - 0A7FFFF
87	Protection Group	128	0A80000 - 0A9FFFF
88	Protection Group	128	0AA0000 - 0ABFFFF
89	Protection Group	128	0AC0000 - 0ADFFFF
90	Protection Group	128	0AE0000 - 0AFFFFF
91	Protection Group	128	0B00000 - 0B1FFFF
92	Protection Group	128	0B20000 - 0B3FFFF
93	Protection Group	128	0B40000 - 0B5FFFF
94	Protection Group	128	0B60000 - 0B7FFFF
95	Protection Group	128	0B80000 - 0B9FFFF
96	Protection Group	128	0BA0000 - 0BBFFFF
97	Protection Group	128	0BC0000 - 0BDFFFF
98	Protection Group	128	0BE0000 - 0BFFFFF
99	Protection Group	128	0C00000 - 0C1FFFF
100	Protection Group	128	0C20000 - 0C3FFFF
101	Protection Group	128	0C40000 - 0C5FFFF
102	Protection Group	128	0C60000 - 0C7FFFF
103	Protection Group	128	0C80000 - 0CFFFFF
104	Protection Group	128	0CA0000 - 0CBFFFF

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Table 7: Bank C (Continued)

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
105	Protection Group	128	0CC0000 - 0CDFFFF
106	Protection Group	128	0CE0000 - 0CFFFFF
107	Protection Group	128	0D00000 - 0D1FFFF
108	Protection Group	128	0D20000 - 0D3FFFF
109	Protection Group	128	0D40000 - 0D5FFFF
110	Protection Group	128	0D60000 - 0D7FFFF
111	Protection Group	128	0D80000 - 0D9FFFF
112	Protection Group	128	0DA0000 - 0DBFFFF
113	Protection Group	128	0DC0000 - 0DDFFFF
114	Protection Group	128	0DE0000 - 0DFFFFF

Table 8: Bank D

Block	Protection Group	Block Size (Kwords)	16-bit address range (in hexadecimal)
115	Protection Group	128	E00000h-E1FFFFh
116	Protection Group	128	E20000h-E3FFFFh
117	Protection Group	128	E40000h-E5FFFFh
118	Protection Group	128	E60000h-E7FFFFh
119	Protection Group	128	E80000h-E9FFFFh
120	Protection Group	128	EA0000h-EBFFFFh
121	Protection Group	128	EC0000h-EDFFFFh
122	Protection Group	128	EE0000h-EFFFFFh
123	Protection Group	128	F00000h-F1FFFFh
124	Protection Group	128	F20000h-F3FFFFh
125	Protection Group	128	F40000h-F5FFFFh
126	Protection Group	128	F60000h-F7FFFFh
127	Protection Group	128	F80000h-F9FFFFh
128	Protection Group	128	FA0000h-FBFFFFh
129	Protection Group	128	FC0000h-FDFFFFh
130	Protection Group	32	FE0000h-FE7FFFh
131	Protection Group	32	FE8000h-FEFFFFh
132	Protection Group	32	FF0000h-FF7FFFh
133	Protection Group	32	FF8000h-FFFFFFh

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Bus Operations

Table 9: Bus Operations

Notes 1 through 3 apply to entire table

Operation	CE#	OE#	WE#	RST#	V_{PP}/WP#	Address Inputs A[MAX], A[0]	Data Inputs/ Outputs DQ[15:0]
READ	L	L	H	H	X	Cell address	Data output
WRITE	L	H	L	H	X[4]	Command address	Data input[5]
STANDBY	H	X	X	H	X	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z
RESET	X	X	X	L	X	X	High-Z

Notes:
1. Typical glitches of less than 5ns on CE#, WE#, and RST# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. Dual operations are possible with the device multiple bank architecture. While programming or erasing in one bank, read operations are possible in any of the other banks. Write operations are only allowed in one bank at a time.
4. To write the four outermost parameter blocks (first two and the last two) V_{PP}/WP# must be equal to V_{IH}.
5. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer. Page size is 8 words and is addressed by address inputs A[2:0].

A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. (See AC Characteristics for details about when the output becomes valid.)

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation. (See AC Characteristics for timing requirement details.)

Standby and Automatic Standby

Driving CE# HIGH in read mode causes the device to enter standby, and data I/Os to be High-Z. To reduce the supply current to the standby supply current (I_{CC2}), CE# must be held within V_{CC} ±0.3V. (See DC Characteristics.)

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During PROGRAM or ERASE operations the device will continue to use the program/erase supply current (I_{CC3}) until the operation completes.

Automatic standby allows the memory to achieve low power consumption during read mode. After a READ operation, if CMOS levels (VCC ± 0.3 V) are used to drive the bus and the bus is inactive for tAVQV + 30ns or more, the memory enters automatic standby where the internal supply current is reduced to the standby supply current, ICC2 (see DC characteristics). The data inputs/outputs still output data if a READ operation is in progress. Depending on load circuits connected with data bus, VCCQ, can have a null consumption when the memory enters automatic standby.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and the outputs are High-Z. The device is in reset mode when RST# is LOW. The power consumption is reduced to the standby level, independently from CE#, OE#, or WE# inputs.

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Registers

Status Register

Table 10: Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 3, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase controller during ERASE operations. During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode (see WRITE TO BUFFER PROGRAM command).	

Notes:
1. The status register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.
3. After successful completion of a PROGRAM or ERASE operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.
5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.

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6. When DQ5 is set to 1, a READ/RESET command must be issued before any subsequent command.

Table 11: Operations and Corresponding Bit Settings

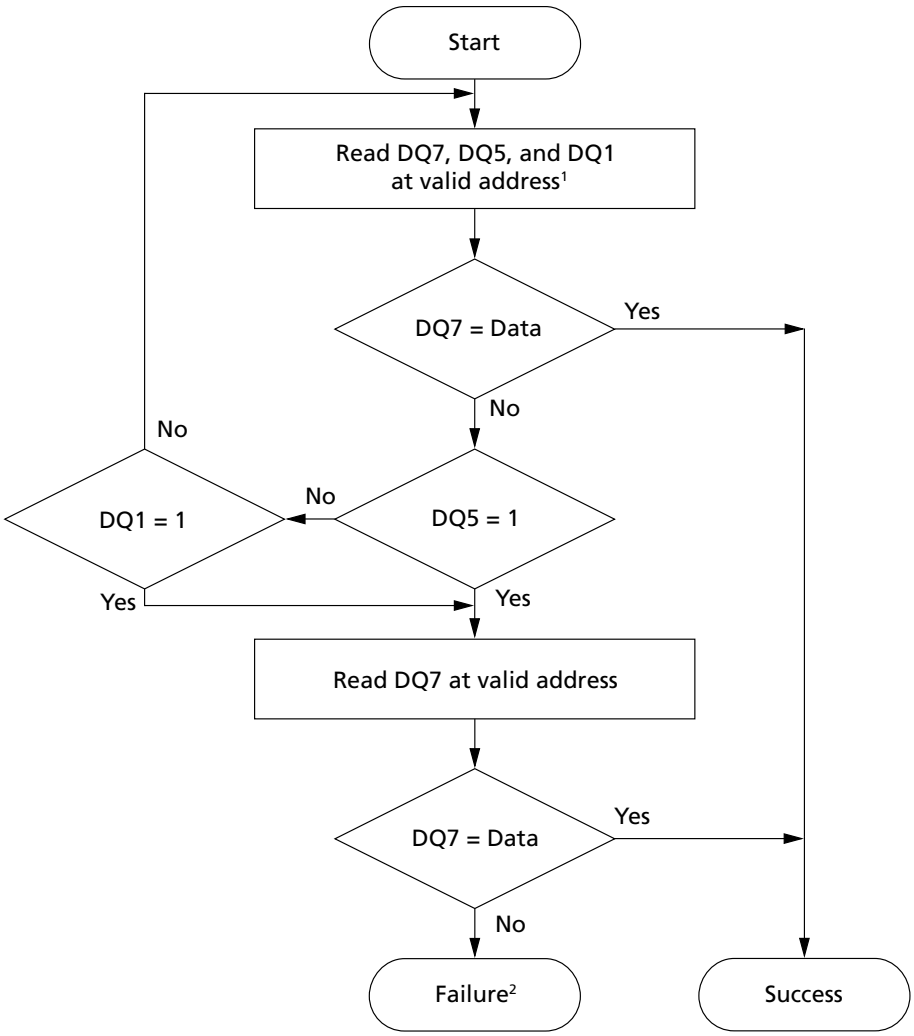
Note 1 applies to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	No toggle	0	0	2
PROGRAM during ERASE SUSPEND	Any address	DQ7#	Toggle	0	–	–	–	0	
ENHANCED BUFFERED PROGRAM Entry	Any address	–	Toggle	0	–	–	–	0	
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	0	2
PROGRAM error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0	
BLOCK ERASE before time-out	Erasing block	0	Toggle	0	0	Toggle	–	0	
	Non-erasing block	0	Toggle	0	0	No toggle	–	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	
ERASE SUSPEND	Erasing block	1	No toggle	0	–	Toggle	–	High-Z	
	Non-erasing block	Outputs memory array data as if in read mode					–	High-Z	
BLOCK ERASE error	Good block address	0	Toggle	1	1	No toggle	–	High-Z	
	Faulty block address	0	Toggle	1	1	Toggle	–	High-Z	

Notes: 1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.

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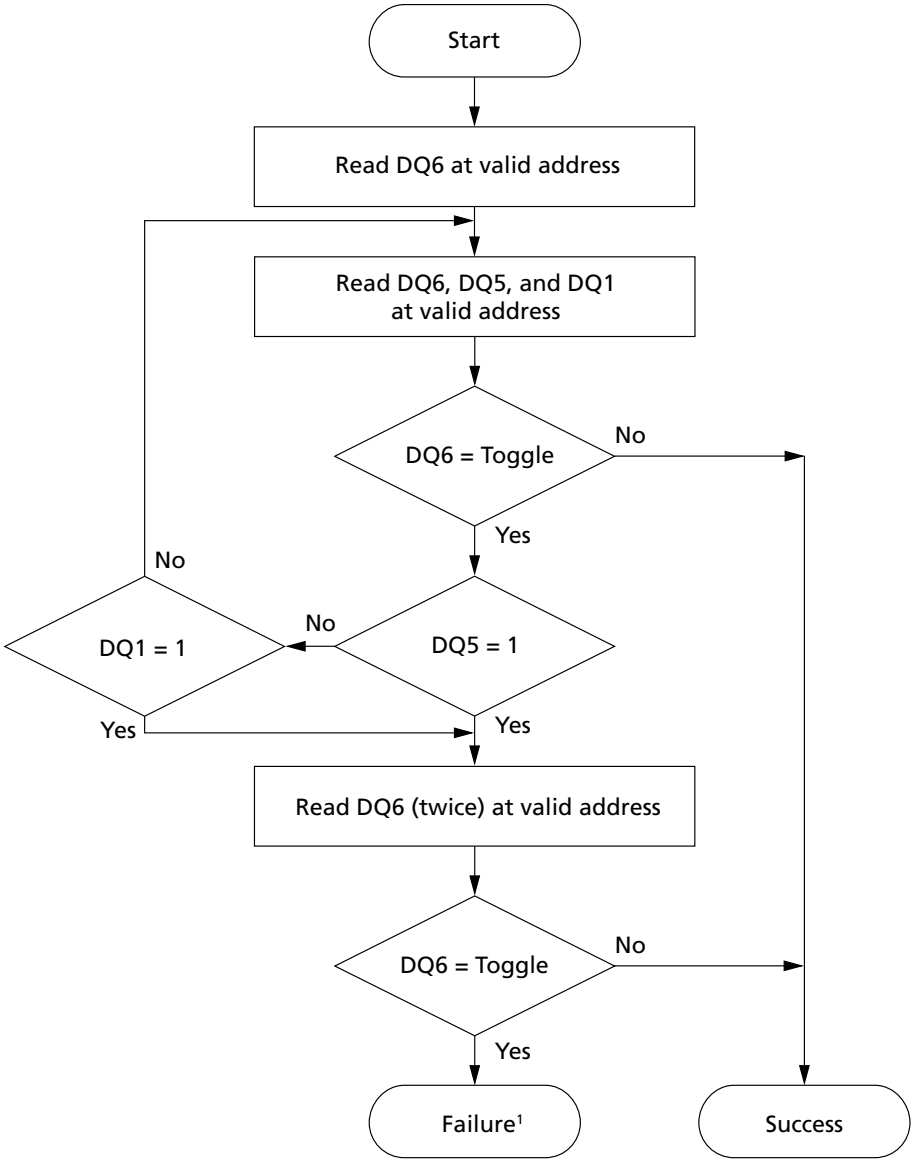
Figure 5: Data Polling Flowchart



Notes:
1. Valid address is the address being programmed or an address within the block being erased.
2. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

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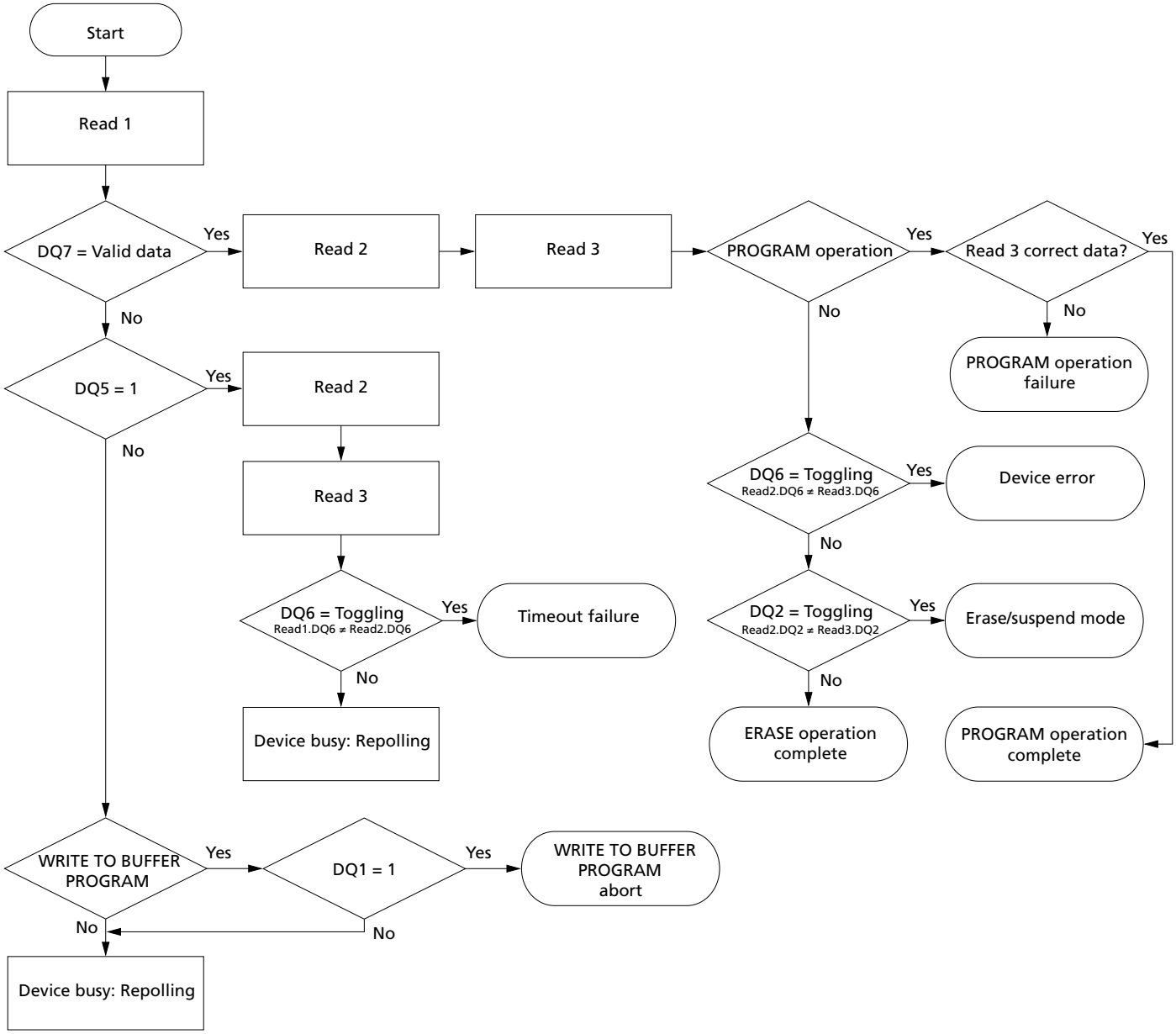
Figure 6: Toggle Bit Flowchart



Note: 1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

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Figure 7: Status Register Polling Flowchart



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Lock Register

Table 12: Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ[15:5]	RFU	–	Reserved for future use	2
DQ4	Volatile lock boot bit	Programmable	Sets default values for volatile block protection; when this bit is programmed, blocks are protected at power-up.	
DQ3	RFU	–	Reserved for future use	2
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (Default)	Places the device permanently in password protection mode.	3
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (Default)	Places the device in nonvolatile protection mode with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	3
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (Default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command. It can also be read by applying V_{ID} to A9.	

Notes:
1. The lock register is a 16-bit, one-time programmable register.
2. DQ[15:5] and DQ[3] are reserved and are set to a default value of 1. During programming, they must be held to 1.
3. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

Table 13: Block Protection Status

Nonvolatile Protection Bit Lock Bit[1]	Nonvolatile Protection Bit[2]	Volatile Protection Bit[3]	Block Protection Status	Block Protection Status
0	0	X	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit unchangeable.
0	1	1	00h	Block unprotected; nonvolatile protection bit unchangeable.
0	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit unchangeable.
1	0	X	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit changeable.
1	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit changeable.

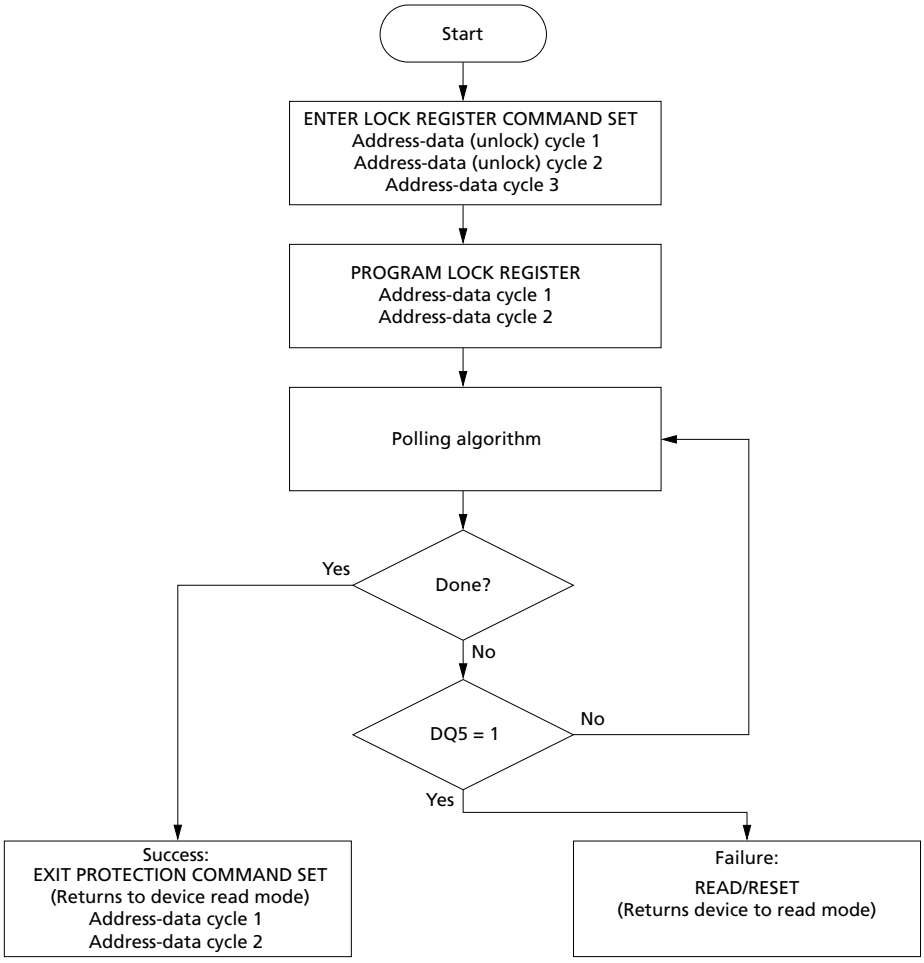
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Table 13: Block Protection Status (Continued)

Nonvolatile Protection Bit Lock Bit[1]	Nonvolatile Protection Bit[2]	Volatile Protection Bit[3]	Block Protection Status	Block Protection Status
1	1	1	00h	Block unprotected; nonvolatile protection bit changeable.

Notes:
1. Nonvolatile protection bit lock bit: when cleared to 1, all nonvolatile protection bits are unlocked; when set to 0, all nonvolatile protection bits are locked.
2. Block nonvolatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.
3. Block volatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.

Figure 8: Lock Register Program Flowchart



Notes:
1. Each lock register bit can be programmed only once.
2. See the Block Protection Command Definitions table for address-data cycle details.

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Standard Command Definitions – Address-Data Cycles

Table 14: Standard Command Definitions – Address-Data Cycles, 16-Bit

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
READ and AUTO SELECT Operations														
READ/RESET (F0h)	x16	X	F0											
		555	AA	2AA	55	X	F0							
READ CFI (98h)	x16	BKA 555	98											
UNLOCK BYPASS READ CFI (98h)	x16	BKA	98											
AUTO SELECT (90h)	x16	555	AA	2AA	55	BKA 555	90	Note 2	Note 2					2, 3, 4
BYPASS Operations														
UNLOCK BYPASS (20h)	x16	555	AA	2AA	55	555	20							
UNLOCK BYPASS RESET (90h/00h)	x16	X	90	X	00									
PROGRAM Operations														
PROGRAM (A0h)	x16	555	AA	2AA	55	555	A0	PA	PD					
UNLOCK BYPASS PROGRAM (A0h)	x16	X	A0	PA	PD									5
WRITE TO BUFFER PROGRAM (25h)	x16	555	AA	2AA	55	BAd	25	BAd	N	PA	PD			6, 7, 8
UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h)	x16	BAd	25	BAd	N	PA	PD							5
WRITE TO BUFFER PROGRAM CONFIRM (29h)	x16	BAd	29											
BUFFERED PROGRAM ABORT and RESET (F0h)	x16	555	AA	2AA	55	555	F0							
ENTER ENHANCED BUFFERED PROGRAM COMMAND SET (38h)	x16	555	AA	2AA	55	555	38							9
ENHANCED BUFFERED PROGRAM (33h)	x16	BAd	33	BAd (00)	Data	BAd (01)	Data							9

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Table 14: Standard Command Definitions – Address-Data Cycles, 16-Bit (Continued)

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
ENHANCED BUFFERED PROGRAM CONFIRM (29h)	x16	BAd (00)	29											
EXIT ENHANCED BUFFERED PROGRAM COMMAND SET (90h)	x16	X	90	X	00									
PROGRAM SUSPEND (B0h)	x16	BKA	B0											
PROGRAM RESUME (30h)	x16	BKA	30											
WRITE TO BUFFER PROGRAM SUSPEND (B0h)	x16	BAd	B0											
WRITE TO BUFFER PROGRAM RESUME (30h)	x16	BAd	30											
ERASE Operations														
CHIP ERASE (80/10h)	x16	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10	
UNLOCK BYPASS CHIP ERASE (80/10h)	x16	X	80	X	10									5
BLOCK ERASE (80/30h)	x16	555	AA	2AA	55	555	80	555	AA	2AA	55	BAd	30	10
UNLOCK BYPASS BLOCK ERASE (80/30h)	x16	X	80	BAd	30									5
ERASE SUSPEND (B0h)	x16	BKA	B0											
ERASE RESUME (30h)	x16	BKA	30											

Notes:
1. A = Address; D = Data; X = "Don't Care;" BKA = Bank address; BAd = Any address in the block; N = Number of bytes to be programmed; PA = Program address; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode.
2. These cells represent READ cycles (versus WRITE cycles for the others).
3. AUTO SELECT enables the device to read the manufacturer code, device code, block protection status, and extended memory block protection indicator.
4. AUTO SELECT addresses and data are specified in the Electronic Signature table and the Extended Memory Block Protection table.
5. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
6. BAd must be the same as the address loaded during the WRITE TO BUFFER PROGRAM 3rd and 4th cycles.
7. WRITE TO BUFFER PROGRAM operation: maximum cycles 36 (x16). UNLOCK BYPASS WRITE TO BUFFER PROGRAM operation: maximum cycles = 34 (x16). WRITE TO BUFFER

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PROGRAM operation: N + 1 = bytes to be programmed; maximum buffer size = 32 words (x16).

8. For x16, A[MAX:5] address pins should remain unchanged while A[4:0] pins are used to select a word within the N + 1 word page.
9. The following is content for address-data cycles 256 through 258: BAd (FE) - Data; BAd (FF) - Data; BAd (00) - 29.
10. BLOCK ERASE address cycles can extend beyond six address-data cycles, depending on the number of blocks to erase.

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READ and AUTO SELECT Operations

READ/RESET Command

The device is in read mode after a reset or power-up. The READ/RESET (F0h) command returns the device to read mode and resets the errors in the status register. One or three bus WRITE operations can be used to issue the READ/RESET command.

To return the device to read mode, this command can be issued between bus WRITE cycles before the start of a PROGRAM or ERASE operation. If the READ/RESET command is issued during the timeout of a BLOCK ERASE operation, the device requires up to 10µs to abort, during which time no valid data can be read.

The READ/RESET command will not abort a PROGRAM operation if executed while the device is in program suspend, or an ERASE operation if executed while the device is in erase suspend.

READ CFI Command

The READ CFI (98h) command puts the device in read CFI mode and is only valid when the device is in read array or auto select mode. One bus WRITE cycle is required to issue the command.

Once in read CFI mode, bus READ operations will output data from the CFI memory area (Refer to the Common Flash Interface for details). A READ/RESET command must be issued to return the device to the previous mode (read array or auto select). A second READ/RESET command is required to put the device in read array mode from auto select mode.

UNLOCK BYPASS READ CFI Command

The UNLOCK BYPASS READ CFI (98h) command enables the device to read the CFI when the device is in the unlock bypass mode.

Once in read CFI mode, bus READ operations will output data from the CFI memory area (Refer to the Common Flash Interface for details). A READ/RESET command must be issued to return the device to the previous mode (read array or auto select). A second READ/RESET command is required to put the device in read array mode from auto select mode.

AUTO SELECT Command

At power-up or after a hardware reset, the device is in read mode. It can then be put in auto select mode by issuing an AUTO SELECT (90h) command. Auto select mode enables the following device information to be read:

- Electronic signature, which includes manufacturer and device code information as shown in the Electronic Signature tables.
- Block protection, which includes the block protection status and extended memory block protection indicator, as shown in the Block Protection tables.

For example, auto select mode can be used by the programming equipment to automatically match a device with the application code to be programmed.

Electronic signature or block protection information is read by executing a READ operation with control signals and addresses set, as shown in the Read Electronic Signature

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tables or the Block Protection tables, respectively. If the block is protected, then 01h is output on data input/outputs DQ0-DQ7, otherwise 00h is output.

Three consecutive bus WRITE operations are required to issue an AUTO SELECT command. The device remains in auto select mode until a READ/RESET or READ CFI command is issued.

The device cannot enter auto select mode when a PROGRAM or ERASE operation is in progress (RY/BY# LOW) unless the respective operation is suspended by a PROGRAM SUSPEND or an ERASE SUSPEND command.

Auto select mode is exited by performing a reset. The device returns to read mode unless it entered auto select mode after an ERASE SUSPEND or PROGRAM SUSPEND command, in which case it returns to erase or program suspend mode.

Table 15: Read Electronic Signature, Auto Select Mode and Programmer Method

Read cycle[1]	E#	G#	W#	Address inputs								Data IO
				A[23:10]	A[9:8]	A[7:5]	A4	A3	A2	A1	A0	DQ[15:0]
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0020h
Device code (cycle 1)							X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Device code (cycle 2)								V_{IH}	V_{IH}	V_{IH}	V_{IL}	223Ch
Device code (cycle 3)								V_{IH}	V_{IH}	V_{IH}	V_{IH}	2202h

Note: 1. X = V_{IL} or V_{IH}.

Table 16: Block protection (16-bit mode)

E#	G#	W#	RST#	V_{PP}/WP#	Address inputs										Data IO	
					A[23:12]	A[11:10]	A9	A8	A7	A6	A[5:4]	A[3:2]	A1	A0	Bits	Value
Operation: Verify extended memory block indicator bit																
V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	BKA	X	X	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	DQ[15:8]	0
															DQ7	1 = factory locked
															DQ6	1 = customer locked, 0 = customer lockable
															DQ5	1 = reserved, 0 = standard
															DQ[4:3]	00 = WP# protects 4 outermost blocks, 11 = No WP# protection (hardware write protection)
															DQ[2:0]	0
Operation: Verify block protection status																
V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	BAd	X	X	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}		0000h (unprotected) 0001h (protected)

Note: 1. X = V_{IL} or V_{IH}. BAd any address in the block, BKA bank address.

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Bypass Operations

UNLOCK BYPASS Command

The UNLOCK BYPASS (20h) command is used to place the device in unlock bypass mode. Three bus WRITE operations are required to issue the UNLOCK BYPASS command.

When the device enters unlock bypass mode, the two initial UNLOCK cycles required for a standard PROGRAM or ERASE operation are not needed, thus enabling faster total program or erase time.

The UNLOCK BYPASS command is used in conjunction with UNLOCK BYPASS PROGRAM or UNLOCK BYPASS ERASE commands to program or erase the device faster than with standard PROGRAM or ERASE commands. When the cycle time to the device is long, considerable time savings can be gained by using these commands. When in unlock bypass mode, only the following commands are valid:

- The UNLOCK BYPASS PROGRAM command can be issued to program addresses within the device.
- The UNLOCK BYPASS BLOCK ERASE command can be issued to erase one or more memory blocks.
- The UNLOCK BYPASS CHIP ERASE command can be issued to erase the whole memory array.
- The UNLOCK BYPASS WRITE TO BUFFER PROGRAM command can be issued to speed up the programming operation.
- The UNLOCK BYPASS CFI command can be issued to read the CFI when the memory is in unlock bypass mode
- The UNLOCK BYPASS RESET command can be issued to return the device to read mode.

In unlock bypass mode, the device can be read as if in read mode.

In addition to the UNLOCK BYPASS command, when V_{PP}/WP# is raised to V_{PPH}, the device automatically enters unlock bypass mode. When V_{PP}/WP# returns to V_{IH} or V_{IL}, the device is no longer in unlock bypass mode and normal operation resumes. The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than $^{t}VHVPP$ (see the Accelerated Program, Data Polling/Toggle AC Characteristics).

Note: Micron recommends the user enter and exit unlock bypass mode using ENTER UNLOCK BYPASS and UNLOCK BYPASS RESET commands rather than raising V_{PP}/WP# to V_{PPH}. V_{PP}/WP# should never be raised to V_{PPH} from any mode except read mode; otherwise, the device may be left in an indeterminate state.

UNLOCK BYPASS RESET Command

The UNLOCK BYPASS RESET (90/00h) command is used to return to read/reset mode from unlock bypass mode. Two bus WRITE operations are required to issue the UNLOCK BYPASS RESET command. The READ/RESET command does not exit from unlock bypass mode.

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Program Operations

PROGRAM Command

The PROGRAM (A0h) command can be used to program a value to one address in the memory array. The command requires four bus WRITE operations, and the final WRITE operation latches the address and data in the internal state machine and starts the program/erase controller.

Programming can be suspended and then resumed by issuing a PROGRAM SUSPEND command and a PROGRAM RESUME command, respectively.

If the address falls in a protected block, the PROGRAM command is ignored, and the data remains unchanged. The status register is not read, and no error condition is given.

After programming has started, bus READ operations output the status register content. A bus READ operation from a bank different from the one whose blocks are being programmed will output the memory array content.

After the PROGRAM operation has completed, the device returns to read mode, unless an error has occurred. When an error occurs, bus READ operations to the device continue to output the status register. A READ/RESET command must be issued to reset the error condition and return the device to read mode.

The PROGRAM command cannot change a bit set to 0 back to 1, and an attempt to do so is masked during a PROGRAM operation. Instead, an ERASE command must be used to set all bits in one memory block or in the entire memory from 0 to 1.

The PROGRAM operation is aborted by performing a reset or by powering-down the device. In this case, data integrity cannot be ensured, and it is recommended that the aborted data be reprogrammed.

UNLOCK BYPASS PROGRAM Command

When the device is in unlock bypass mode, the UNLOCK BYPASS PROGRAM (A0h) command can be used to program one address in the memory array. The command requires two bus WRITE operations instead of four required by a standard PROGRAM command; the final WRITE operation latches the address and data and starts the program/erase controller (The standard PROGRAM command requires four bus WRITE operations). This UNLOCK BYPASS PROGRAM operation behaves identically to the PROGRAM operation. The operation cannot be aborted. A bus READ operation from the memory outputs the status register. A bus READ operation from a bank different from the one whose blocks are being programmed will output the memory array content.

WRITE TO BUFFER PROGRAM Command

The WRITE TO BUFFER PROGRAM (25h) command makes use of the 32-word program buffer to speed up programming. A maximum of 32 words can be loaded into the program buffer; each write buffer has the same A[23:5]. The WRITE TO BUFFER PROGRAM command dramatically reduces system programming time compared to the standard non-buffered PROGRAM command.

When issuing a WRITE TO BUFFER PROGRAM command, V_{PP}/WP# can be either held HIGH or raised to V_{PPH}. Also, it can be held LOW if the block is not one of the four outer-

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most blocks, depending on the part number. The following successive steps are required to issue the WRITE TO BUFFER PROGRAM command:

First, two UNLOCK cycles are issued. Next, a third bus WRITE cycle sets up the WRITE TO BUFFER PROGRAM command. The set-up code can be addressed to any location within the targeted block. Then, a fourth bus WRITE cycle sets up the number of words to be programmed. Value *n* is written to the same block address, where *n + 1* is the number of words to be programmed. Value *n + 1* must not exceed the size of the program buffer, or the operation will abort. A fifth cycle loads the first address and data to be programmed. Last, *n* bus WRITE cycles load the address and data for each word into the program buffer. Addresses must lie within the range from *the start address +1* to *the start address + (n - 1)*.

Optimum programming performance and lower power usage are achieved by aligning the starting address at the beginning of a 32-word boundary; otherwise, programming time doubles. All addresses used in the operation must lie within the same page.

To program the content of the program buffer, this command must be followed by a WRITE TO BUFFER PROGRAM CONFIRM command.

If an address is written several times during a WRITE TO BUFFER PROGRAM operation, the address/data counter will be decremented at each data load operation, and the data will be programmed to the last word loaded into the buffer.

Invalid address combinations or the incorrect sequence of bus WRITE cycles will abort the WRITE TO BUFFER PROGRAM command.

The status register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a WRITE TO BUFFER PROGRAM operation.

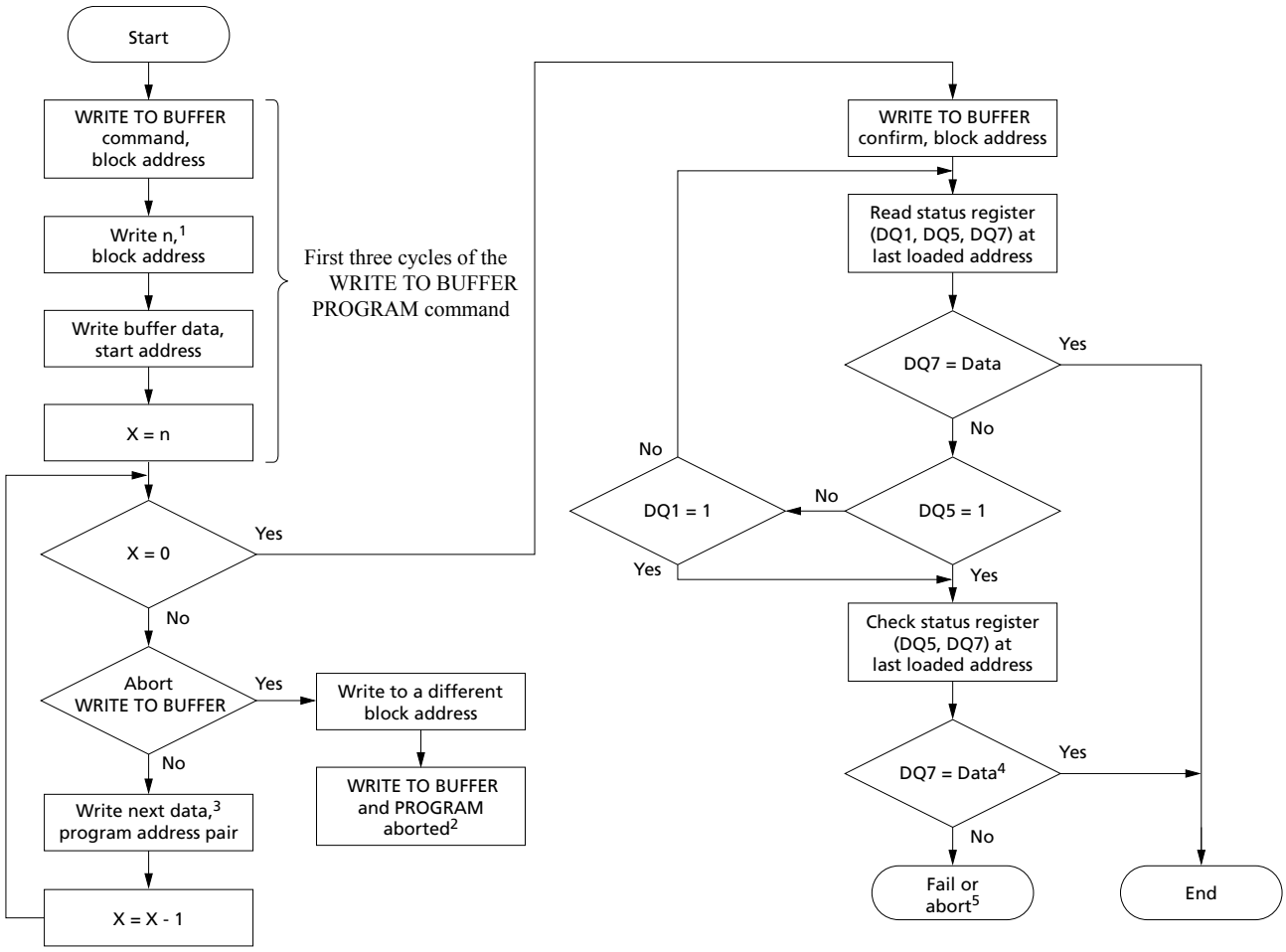
The WRITE TO BUFFER PROGRAM command should not be used to change a bit set to 0 back to 1, and an attempt to do so is masked during the operation. Rather than the WRITE BUFFER PROGRAM command, the ERASE command should be used to set memory bits from 0 to 1.

The WRITE TO BUFFER PROGRAM command can be suspended and then resumed by issuing a PROGRAM SUSPEND command and then a PROGRAM RESUME command, respectively.

After the WRITE TO BUFFER PROGRAM operation has completed, the memory will return to read mode, unless an error has occurred. When an error occurs, a read operation from the bank being programmed will continue to output the status register. A read operation from any bank other than the one being programmed will output the memory array content.

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Figure 9: WRITE TO BUFFER PROGRAM Flowchart



Notes:
1. *n + 1* is the number of addresses to be programmed.
2. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode.
3. When the block address is specified, any address in the selected block address space is acceptable. However, when loading program buffer address with data, all addresses must fall within the selected program buffer page.
4. DQ7 must be checked because DQ5 and DQ7 may change simultaneously.
5. If this flowchart location is reached because DQ5 = 1, then the WRITE TO BUFFER PROGRAM command failed. If this flowchart location is reached because DQ1 = 1, then the WRITE TO BUFFER PROGRAM command aborted. In both cases, the appropriate RESET command must be issued to return the device to read mode: A RESET command if the operation failed; a WRITE TO BUFFER PROGRAM ABORT AND RESET command if the operation aborted.
6. See the Standard Command Definitions – Address-Data Cycles, 16-Bit table for details about the WRITE TO BUFFER PROGRAM command sequence.

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UNLOCK BYPASS WRITE TO BUFFER PROGRAM Command

When the device is in unlock bypass mode, the UNLOCK BYPASS WRITE TO BUFFER (25h) command can be used to program the device in fast program mode. The command requires two bus WRITE operations fewer than the standard WRITE TO BUFFER PROGRAM command.

The UNLOCK BYPASS WRITE TO BUFFER PROGRAM command behaves the same way as the WRITE TO BUFFER PROGRAM command: the operation cannot be aborted, and a bus READ operation from the memory outputs the status register. A bus READ operation from a bank different from the one whose blocks are being programmed will output the memory array content.

The WRITE TO BUFFER PROGRAM CONFIRM command is used to confirm an UNLOCK BYPASS WRITE TO BUFFER PROGRAM command and to program the *n + 1* words loaded in the program buffer by this command.

WRITE TO BUFFER PROGRAM CONFIRM Command

The WRITE TO BUFFER PROGRAM CONFIRM (29h) command is used to confirm a WRITE TO BUFFER PROGRAM command and to program the *n + 1* words loaded in the program buffer by this command.

BUFFERED PROGRAM ABORT AND RESET Command

A BUFFERED PROGRAM ABORT AND RESET (F0h) command must be issued to abort the WRITE TO BUFFER PROGRAM and ENHANCED BUFFERED PROGRAM operations and reset the device in read mode. The buffer programming sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the number of locations to program in the WRITE TO BUFFER PROGRAM command.
- Write to an address in a different block than the one specified during the WRITE BUFFER LOAD command.
- Write an address/data pair to a different write buffer page than the one selected by the starting address during the program buffer data loading stage of the operation.
- Write data other than the CONFIRM command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ6 = toggle, and DQ5 = 0 (all of which are status register bits). A BUFFERED PROGRAM ABORT and RESET command sequence must be written to reset the device for the next operation.

Note: The full three-cycle BUFFERED PROGRAM ABORT and RESET command sequence is required when using buffer programming features in unlock bypass mode.

PROGRAM SUSPEND Command

The PROGRAM SUSPEND (B0h) command can be used to interrupt a program operation so that data can be read from any block. When the PROGRAM SUSPEND command is issued during a program operation, the device suspends the operation within the program suspend latency time and updates the status register bits.

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After the program operation has been suspended, data can be read from any address. However, data is invalid when read from an address where a program operation has been suspended.

The PROGRAM SUSPEND command may also be issued during a PROGRAM operation while an erase is suspended. In this case, data may be read from any address not in erase suspend or program suspend mode. To read from the extended memory block area (one-time programmable area), the ENTER/EXIT EXTENDED MEMORY BLOCK command sequences must be issued.

The system may also issue the AUTO SELECT command sequence when the device is in program suspend mode. The system can read as many auto select codes as required. When the device exits auto select mode, the device reverts to program suspend mode and is ready for another valid operation.

The PROGRAM SUSPEND operation is aborted by performing a device reset or power-down. In this case, data integrity cannot be ensured, and it is recommended that the aborted data be reprogrammed.

PROGRAM RESUME Command

The PROGRAM RESUME (30h) command must be issued to exit a program suspend mode and resume a PROGRAM operation. The controller can use DQ7 or DQ6 status bits to determine the status of the PROGRAM operation. After a PROGRAM RESUME command is issued, subsequent PROGRAM RESUME commands are ignored. Another PROGRAM SUSPEND command can be issued after the device has resumed programming.

WRITE TO BUFFER PROGRAM SUSPEND Command

The WRITE TO BUFFER PROGRAM SUSPEND (B0h) command can be used to interrupt a write to buffer program operation so that data can be read from any block. When this command is issued, the device suspends the operation within the program suspend latency time and updates the status register bits.

After the operation has been suspended, data can be read from any address. However, data is invalid when read from an address where a program operation has been suspended.

This command can also be issued during a WRITE TO BUFFER PROGRAM operation while an erase is also suspended. In this case, data may be read from any address not in erase suspend or program suspend mode. To read from the extended memory block area (one-time programmable area), the ENTER/EXIT EXTENDED MEMORY BLOCK command sequences must be issued.

The system may also issue the AUTO SELECT command sequence when the device is in write to buffer program suspend mode. The system can read as many auto select codes as required. When the device exits auto select mode, the device reverts to write to buffer program suspend mode and is ready for another valid operation.

The PROGRAM SUSPEND operation is aborted by performing a device reset or power-down. In this case, data integrity cannot be ensured, and it is recommended that the aborted data be reprogrammed.

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WRITE TO BUFFER PROGRAM RESUME Command

The WRITE TO BUFFER PROGRAM RESUME (30h) command must be issued to exit a write to buffer program suspend mode and resume a WRITE TO BUFFER PROGRAM operation. The controller can use DQ7 or DQ6 status bits to determine the status of the WRITE TO BUFFER PROGRAM operation. After a WRITE TO BUFFER PROGRAM RESUME command is issued, subsequent WRITE TO BUFFER PROGRAM RESUME commands are ignored. Another WRITE TO BUFFER PROGRAM SUSPEND command can be issued after the device has resumed programming.

ENTER ENHANCED BUFFERED Command

The ENTER ENHANCED BUFFERED command is used to allow execution of the enhanced buffered program commands. The device accepts only these following commands after the ENTER ENHANCED BUFFERED command is issued; any other command is ignored:

- ENHANCED BUFFERED PROGRAM (can be issued multiple times once the ENTER ENHANCED BUFFERED command is executed)
- ENHANCED BUFFERED PROGRAM ABORT/RESET
- EXIT ENHANCED BUFFERED PROGRAM

To ensure the ENTER ENHANCED BUFFERED command has completed successfully and the device is ready to receive one of the commands listed above, it is recommended to monitor toggle bit (DQ6).

ENHANCED BUFFERED PROGRAM Command

The ENHANCED BUFFERED PROGRAM command makes use of a 256-word write buffer to speed up programming. Each write buffer has the same A23-A8 addresses. This command dramatically reduces system programming time compared to both the standard non-buffered PROGRAM command and the WRITE TO BUFFER command.

When issuing the ENHANCED BUFFERED PROGRAM command, the V_{PP}/WP pin can be held HIGH or raised to V_{PPH} (see Program/Erase Characteristics). The following successive steps are required to issue the ENHANCED BUFFERED PROGRAM command:

First, the ENTER ENHANCED BUFFERED PROGRAM command issued. Next, one bus WRITE cycle sets up the ENHANCED BUFFERED PROGRAM command. The set-up code can be addressed to any location within the targeted block. Then, a second bus WRITE cycle loads the first address and data to be programmed. There are a total of 256 address and data loading cycles. When the 256 words are loaded to the buffer, a third WRITE cycle programs the content of the buffer. Last, when the command completes, the EXIT ENHANCED BUFFERED PROGRAM command is issued.

Address/data cycles must be loaded in an increasing address order, from A[7:0] = 00000000 to A[7:0] = 11111111 until all 256 words are loaded. Invalid address combinations or the incorrect sequence of bus WRITE cycles will abort the ENHANCED BUFFERED PROGRAM command.

The status register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during an ENHANCED BUFFERED PROGRAM operation.

An external 12V supply can be used to improve programming efficiency.

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When reprogramming data in a portion of memory already programmed (changing programmed data from '0' to '1') operation failure can be detected by a logical OR between the previous and the current value.

ENHANCED BUFFERED PROGRAM ABORT RESET Command

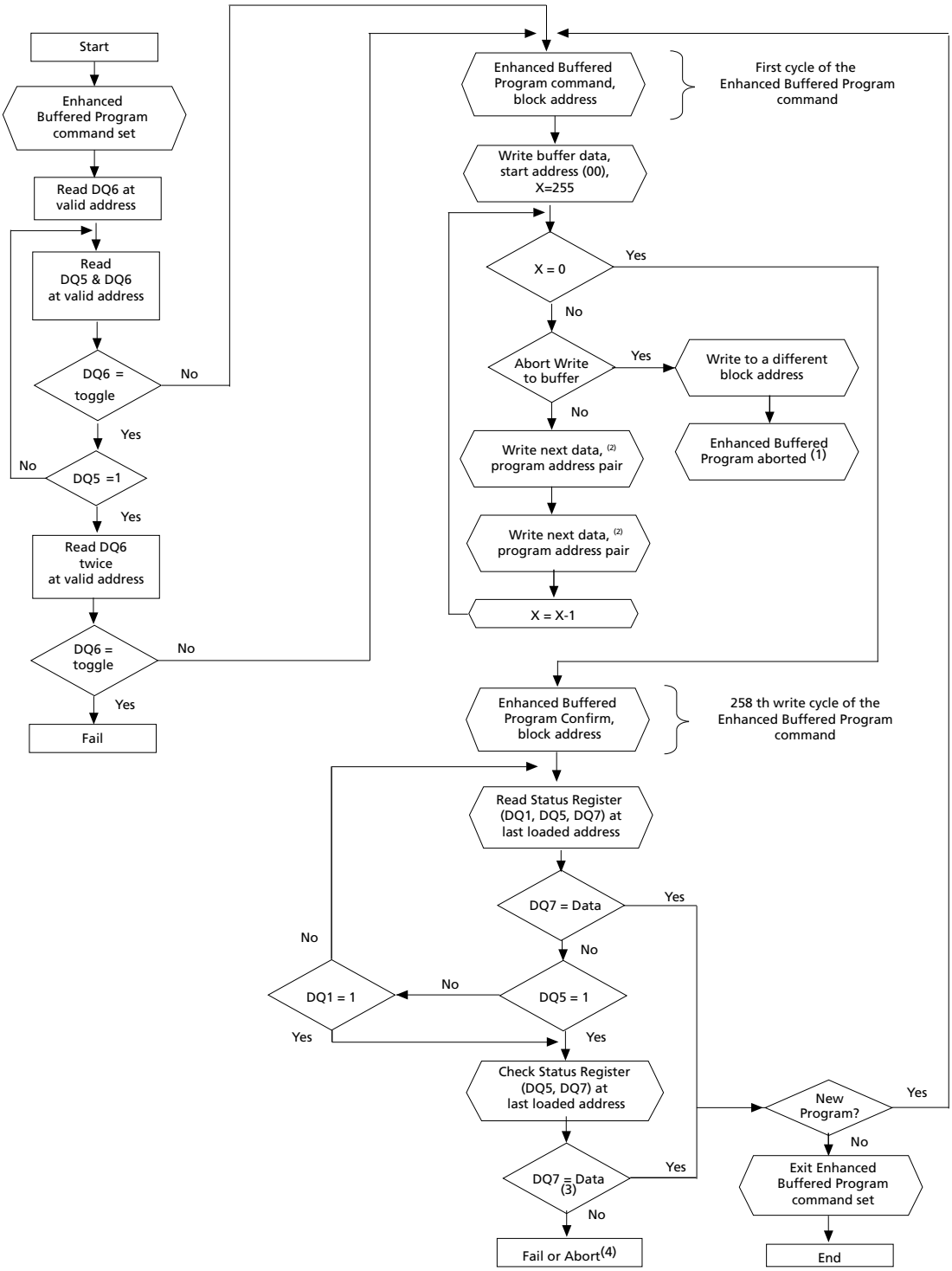
After an ENHANCED BUFFERED PROGRAM command is aborted, the device will accept only an ENHANCED BUFFERED PROGRAM ABORT RESET (F0h) command. This command resets the device following the aborted command and before the next command can be executed. When this command completes and the device is reset, the memory waits for either an ENHANCED BUFFERED PROGRAM command or an EXIT ENHANCED BUFFERED PROGRAM command. The enhanced buffered programming sequence can be aborted in the following ways:

- Write to an address in a different block than the one specified during the ENHANCED BUFFERED PROGRAM LOAD command.
- Write an address/data pair to a different write buffer page than the one selected by the starting address during the program buffer data loading stage of the operation.
- Write data other than the CONFIRM command after the specified number of data load cycles.
- Load address/data pairs in an incorrect sequence during the enhanced buffered program.
- Load a number of data that is less or greater than 256 during the program step.

The abort condition is indicated by DQ1 = 1, DQ6 = toggle, and DQ5 = 0 (all of which are status register bits). A BUFFERED PROGRAM ABORT and RESET command sequence must be written to reset the device for the next operation.

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Figure 10: ENHANCED BUFFERED PROGRAM Flowchart



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Notes:
1. The ENHANCED BUFFERED PROGRAM ABORT RESET command must be issued to return the device to read mode.
2. When the block address is specified, all addresses in the selected block address space must be issued starting from 00h. Furthermore, when loading the write buffer address with data, data program addresses must be consecutive.
3. DQ7 must be checked since DQ5 and DQ7 may change simultaneously.
4. If this flowchart location is reached because DQ5 = 1, then the ENHANCED BUFFERED PROGRAM command failed. If this flowchart location is reached because DQ1 = 1, then the ENHANCED BUFFERED PROGRAM command aborted. In both cases, the appropriate reset command must be issued to return the device to read mode: A RESET command if the operation failed; an ENHANCED BUFFERED PROGRAM ABORT RESET command if the operation aborted.

EXIT ENHANCED BUFFERED PROGRAM Command

The EXIT ENHANCED BUFFERED PROGRAM command requires two bus write cycles and is used to return the device to read mode. Until this command is issued, only the ENHANCED BUFFERED PROGRAM command can be issued, and all other commands are ignored.

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Erase Operations

CHIP ERASE Command

The CHIP ERASE (80/10h) command erases the entire chip. Six bus WRITE operations are required to issue the command and start the program/erase controller.

Protected blocks are not erased. If all blocks are protected, the CHIP ERASE operation appears to start, but will terminate within approximately100µs, leaving the data unchanged. No error is reported when protected blocks are not erased.

During the CHIP ERASE operation, the device ignores all other commands, including ERASE SUSPEND. It is not possible to abort the operation. All bus READ operations during CHIP ERASE output the status register on the data I/Os. See the Status Register section for more details.

After the CHIP ERASE operation completes, the device returns to read mode, unless an error has occurred. If an error occurs, the device will continue to output the status register. A READ/RESET command must be issued to reset the error condition and return to read mode.

The CHIP ERASE command sets all of the bits in unprotected blocks of the device to 1. All previous data is lost.

The operation is aborted by performing a reset or by powering-down the device. In this case, data integrity cannot be ensured, and it is recommended that the entire chip be erased again.

UNLOCK BYPASS CHIP ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS CHIP ERASE (80/10h) command can be used to erase all memory blocks at one time. The command requires only two bus WRITE operations instead of six using the standard CHIP ERASE command. The final bus WRITE operation starts the program/erase controller.

The UNLOCK BYPASS CHIP ERASE command behaves the same way as the CHIP ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the status register.

BLOCK ERASE Command

The BLOCK ERASE (80/30h) command erases a list of one or more blocks. It sets all of the bits in the unprotected selected blocks to 1. All previous data in the selected blocks is lost.

Six bus WRITE operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth bus WRITE operation using the address of the additional block. After the command sequence is written, a block erase timeout occurs. During the timeout period, additional block addresses and BLOCK ERASE commands can be written. After the program/erase controller has started, it is not possible to select any more blocks. Therefore, each additional block must be selected within the timeout period of the last block. The timeout timer restarts when an additional block is selected. After the sixth bus WRITE operation, a bus READ operation outputs the status register. Bus READ operations from banks different from those that include the blocks being erased output the memory array content. See the WE#-Con-

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trolled Program waveforms for details on how to identify if the program/erase controller has started the BLOCK ERASE operation.

After the BLOCK ERASE operation completes, the device returns to read mode, unless an error has occurred. If an error occurs, bus READ operations will continue to output the status register. A READ/RESET command must be issued to reset the error condition and return to read mode.

If any selected blocks are protected, they are ignored, and all the other selected blocks are erased. If all of the selected blocks are protected, the BLOCK ERASE operation appears to start, but will terminate within approximately100µs, leaving the data unchanged. No error condition is given when protected blocks are not erased.

During the BLOCK ERASE operation, the device ignores all commands except the ERASE SUSPEND command and the READ/RESET command, which is accepted only during the timeout period. The operation is aborted by performing a reset or powering-down the device. In this case, data integrity cannot be ensured, and it is recommended that the aborted blocks be erased again.

UNLOCK BYPASS BLOCK ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS BLOCK ERASE (80/30h) command can be used to erase one or more memory blocks at a time. The command requires two bus WRITE operations instead of six using the standard BLOCK ERASE command. The final bus WRITE operation latches the address of the block and starts the program/erase controller.

To erase multiple blocks (after the first two bus WRITE operations have selected the first block in the list), each additional block in the list can be selected by repeating the second bus WRITE operation using the address of the additional block.

The UNLOCK BYPASS BLOCK ERASE command behaves the same way as the BLOCK ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the status register. Bus READ operations from banks different from those that include the blocks being erased output the memory array content. See the BLOCK ERASE Command section for details.

ERASE SUSPEND Command

The ERASE SUSPEND (B0h) command temporarily suspends a BLOCK ERASE operation. One bus WRITE operation with the block address is required to issue the command.

After the command sequence is written, a minimum block erase timeout occurs. During the timeout period, additional block addresses and block erase commands can be written.

The program/erase controller suspends the ERASE operation within the erase suspend latency time of the ERASE SUSPEND command being issued. However, when the ERASE SUSPEND command is written during the block erase timeout, the device immediately terminates the timeout period and suspends the ERASE operation. After the program/erase controller has stopped, the device operates in read mode, and the erase is suspended.

During an ERASE SUSPEND operation, it is possible to read and execute PROGRAM operations or WRITE TO BUFFER PROGRAM operations in blocks that are not suspended.

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Both READ and PROGRAM operations behave normally on these blocks. Reading from blocks that are suspended will output the status register. If any attempt is made to program in a protected block or in the suspended block, the PROGRAM command is ignored, and the data remains unchanged. In this case, the status register is not read, and no error condition is given.

It is also possible to issue the AUTO SELECT command after entering auto select mode. The READ/RESET command must be issued to return the device to read array mode before the ERASE RESUME command will be accepted.

During an ERASE SUSPEND operation and after the ENTER EXTENDED MEMORY BLOCK command is issued, a bus READ operation to the extended memory block will output the extended memory block data. After the device enters extended memory block mode, the EXIT EXTENDED MEMORY BLOCK command must be issued before the ERASE operation can be resumed.

An ERASE SUSPEND command is ignored if it is written during a CHIP ERASE operation.

If the ERASE SUSPEND operation is aborted by performing a device reset or power-down, data integrity cannot be ensured, and it is recommended that the suspended blocks be erased again.

ERASE RESUME Command

The ERASE RESUME (30h) command restarts the program/erase controller after an ERASE SUSPEND operation.

The device must be in read array mode before the ERASE RESUME command will be accepted. An erase can be suspended and resumed more than once.

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Block Protection Command Definitions – Address-Data Cycles

Table 17: Block Protection Command Definitions – Address-Data Cycles, 16-Bit

Notes 1 and 2 apply to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		…	*n*th		
		A	D	A	D	A	D	A	D		A	D	
LOCK REGISTER Commands													
ENTER LOCK REGISTER COMMAND SET (40h)	x16	555	AA	2AA	55	555	40						3
PROGRAM LOCK REGISTER (A0h)	x16	X	A0	X	Data								5
READ LOCK REGISTER	x16	X	Data										4, 5, 6
PASSWORD PROTECTION Commands													
ENTER PASSWORD PROTECTION COMMAND SET (60h)	x16	555	AA	2AA	55	555	60						3
PROGRAM PASSWORD (A0h)	x16	X	A0	PWAn	PWDn								7
READ PASSWORD	x16	00	PWD0	01	PWD1	02	PWD2	03	PWD3				4, 6, 8
UNLOCK PASSWORD (25h/03)	x16	00	25	00	03	00	PWD0	01	PWD1	…	00	29	8
NONVOLATILE PROTECTION Commands													
ENTER NONVOLATILE PROTECTION COMMAND SET (C0h)	x16	555	AA	2AA	55	(BKA) BAd	C0						3
PROGRAM NONVOLATILE PROTECTION BIT (A0h)	x16	X	A0	(BKA) BAd	00								
READ NONVOLATILE PROTECTION BIT STATUS	x16	(BKA) BAd	READ(0)										4, 6, 10
CLEAR ALL NONVOLATILE PROTECTION BITS (80/30h)	x16	X	80	00	30								11
NONVOLATILE PROTECTION BIT LOCK BIT Commands													
ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h)	x16	555	AA	2AA	55	555	50						3
PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h)	x16	X	A0	X	00								10
READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS	x16	(BKA)	READ(0)										4, 6, 10
VOLATILE PROTECTION Commands													

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Table 17: Block Protection Command Definitions – Address-Data Cycles, 16-Bit (Continued)

Notes 1 and 2 apply to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		...	*n*th		
		A	D	A	D	A	D	A	D		A	D	
ENTER VOLATILE PROTECTION COMMAND SET (E0h)	x16	555	AA	2AA	55	(BKA) 555	E0						3
PROGRAM VOLATILE PROTECTION BIT (A0h)	x16	X	A0	(BKA) BAd	00								
READ VOLATILE PROTECTION BIT STATUS	x16	(BKA) BAd	READ(0)										4, 6, 10
CLEAR VOLATILE PROTECTION BIT (A0h)	x16	X	A0	(BKA) BAd	01								
EXTENDED MEMORY BLOCK Commands													
ENTER EXTENDED MEMORY BLOCK (88h)	x16	555	AA	2AA	55	555	88						3
READ EXTENDED MEMORY BLOCK	x16	BAd	RD										
PROGRAM EXTENDED MEMORY BLOCK	x16	X	A0	BAd	PD								
EXIT EXTENDED MEMORY BLOCK (90/00h)	x16	555	AA	2AA	55	555	90	X	00				
EXIT PROTECTION Commands													
EXIT PROTECTION COMMAND SET (90/00h)	x16	X	90	X	00								3

Notes:
1. Key: A = Address and D = Data; X = "Don't Care;" BAd = any address in the block; BKA = Bank address; PWDn = password bytes 0 to 7; PWAn = password address, n = 0 to 7; RD(0) = DQ0 protection indicator bit; If protected, DQ0 = 00h, while if unprotected, DQ0 = 01h. Gray = not applicable. All values in the table are hexadecimal.
2. DQ[15:8] are "Don't Care" during UNLOCK and COMMAND cycles. A[MAX:16] are "Don't Care" during UNLOCK and COMMAND cycles, unless an address is required.
3. The ENTER command sequence must be issued prior to any operation. It disables READ and WRITE operations from and to block 0. READ and WRITE operations from and to any other block are allowed. Also, when an ENTER COMMAND SET command is issued, an EXIT PROTECTION COMMAND SET command must be issued to return the device to READ mode.
4. READ REGISTER/PASSWORD commands have no command code; CE# and OE# are driven LOW and data is read according to a specified address.
5. Data = Lock register content.
6. All address cycles shown for this command are READ cycles.
7. Only one portion of the password can be programmed by each PROGRAM PASSWORD command.
8. Each portion of the password can be entered or read in any order as long as the entire 64-bit password is entered or read.
9. For the x16 UNLOCK PASSWORD command, the *n*th (and final) address cycle equals the 7th address cycle. For the 5th and 6th address cycles, the values for the address and data

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pair continue the pattern shown in the table as follows: address and data = 02 and PWD2; 03 and PWD3.

10. Both nonvolatile and volatile protection bit settings are as follows: Protected state = 00; Unprotected state= 01.
11. The CLEAR ALL NONVOLATILE PROTECTION BITS command programs all nonvolatile protection bits before erasure. This prevents over-erasure of previously cleared nonvolatile protection bits.

Protection Operations

Blocks can be protected individually against accidental PROGRAM and ERASE operations. The block protection scheme is shown in the Software Protection Scheme figure.

Memory block and extended memory block protection is configured through the lock register.

LOCK REGISTER Commands

The ENTER LOCK REGISTER COMMAND SET (40h) requires three bus write cycles. After it has been issued, all bus READ or PROGRAM operations can be issued to the lock register.

The EXIT PROTECTION COMMAND SET (90/00h) command must be used to exit the lock register ane return to read mode.

The PROGRAM LOCK REGISTER (A0h) command allows the lock register to be configured. The programmed data can then be checked with a READ LOCK REGISTER command by driving CE# and OE# LOW with the appropriate address data on the address bus.

PASSWORD PROTECTION Commands

After the ENTER PASSWORD PROTECTION COMMAND SET (60h) command has been issued, only commands related to password protection mode and the EXIT PROTECTION COMMAND SET command can be issued to the device. This command requires three bus write cycles. The EXIT PROTECTION COMMAND SET command must be issued following all password protection commands to return the device to read mode.

The PROGRAM PASSWORD (A0h) command is used to program the 64-bit password used in the password protection mode. To program the 64-bit password, the complete command sequence must be entered four times at four consecutive addresses selected by A[1:0] in 16-bit mode. This command must be used according to all program command timings. Command results can be verified by checking the status register. By default, all password bits are set to 1. The password can be checked by issuing a READ PASSWORD command.

The READ PASSWORD command is used to verify the password used in password protection mode. To verify the 64-bit password, the complete command sequence must be entered four times at four consecutive addresses selected by A[1:0] in 16-bit mode. If the password mode lock bit is programmed and the user attempts to read the password, the device will output FFh onto the I/O data bus.

The UNLOCK PASSWORD (25/03h) command is used to clear the nonvolatile protection bit lock bit, allowing the nonvolatile protection bits to be modified. The UNLOCK PASSWORD command must be issued, along with the correct password, and requires a

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1µs delay between successive UNLOCK PASSWORD commands in order to prevent unauthorized intruders from retrieving the password by trying all possible 64-bit combinations. If this delay does not occur, the latest command will be ignored. Approximately 1µs is required for unlocking the device after the valid 64-bit password has been provided.

NONVOLATILE PROTECTION Commands

After the ENTER NONVOLATILE PROTECTION COMMAND SET (C0h) command has been issued, the commands related to nonvolatile protection mode can be issued to the device. This command requires three bus write cycles.

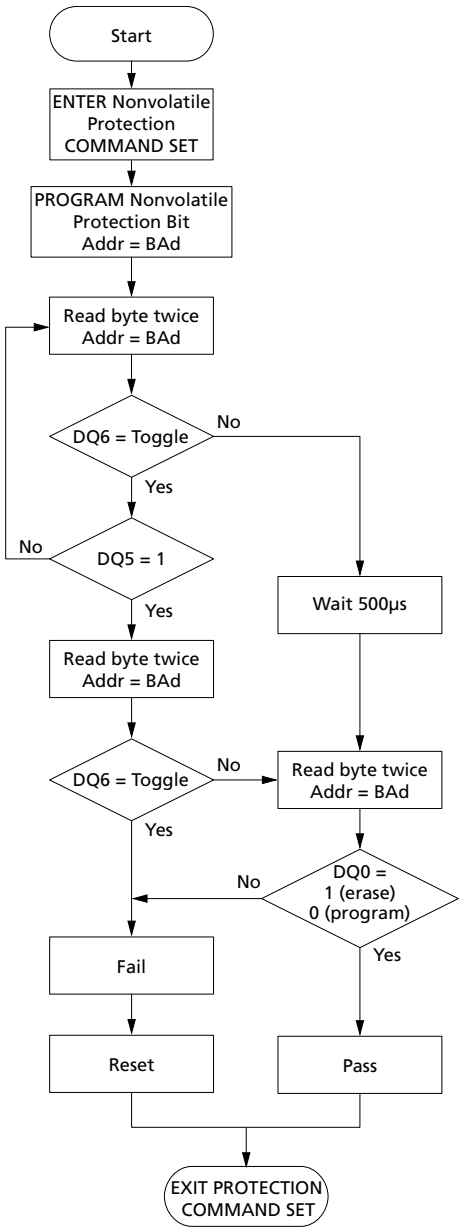
A block can be protected from program or erase by issuing a PROGRAM NONVOLATILE PROTECTION BIT (A0h) command, along with the block address. This command sets the nonvolatile protection bit to 0 for a given block. This command must be used according to all program command timings. Command results can be verified by checking the status register.

The status of a nonvolatile protection bit for a given block or group of blocks can be read by issuing a READ NONVOLATILE MODIFY PROTECTION BIT command, along with the block address.

The nonvolatile protection bits are erased simultaneously by issuing a CLEAR ALL NONVOLATILE PROTECTION BITS (80/30h) command. No specific block address is required. If the nonvolatile protection bit lock bit is set to 0, the command fails.

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Figure 11: Program/Erase Nonvolatile Protection Bit Algorithm



NONVOLATILE PROTECTION BIT LOCK BIT Commands

After the ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h) command has been issued, the commands that allow the nonvolatile protection bit lock bit to be set can be issued to the device. This command requires three bus write cycles.

The PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h) command is used to set the nonvolatile protection bit lock bit to 0, thus locking the nonvolatile protection bits and preventing them from being modified.

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The READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS command is used to read the status of the nonvolatile protection bit lock bit.

VOLATILE PROTECTION Commands

After the ENTER VOLATILE PROTECTION COMMAND SET (E0h) command has been issued, commands related to the volatile protection mode can be issued to the device. This command requires three bus write cycles.

The PROGRAM VOLATILE PROTECTION BIT (A0h) command individually sets a volatile protection bit to 0 for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit. (See the Block Protection Status table.)

The status of a volatile protection bit for a given block can be read by issuing a READ VOLATILE PROTECTION BIT STATUS command along with the block address.

The CLEAR VOLATILE PROTECTION BIT (A0h) command individually clears (sets to 1) the volatile protection bit for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit. (See the Block Protection Status table.)

EXTENDED MEMORY BLOCK Commands

The device has one extra 256-word block (extended memory block) that can only be accessed by the ENTER EXTENDED MEMORY BLOCK command when the device is in extended block mode. The device can be shipped with the extended memory block prelocked permanently by Micron, or with the extended memory block unlocked, enabling customers to permanently program and lock it. (See Lock Register, the AUTO SELECT command, and the Block Protection table.)

The extended memory block is used as a security block (to provide a permanent security identification number) or to store additional information. The extended memory block is divided in two memory areas of 128 words each:

The first area is factory locked and the second one is customer lockable. It is permanently protected from program operations and cannot be unprotected. The random number, electronic serial number (ESN) and security identification number are written in this section in the factory.

The second area is customer lockable. It is up to the customer to protect it from program operations. Its status is indicated by bit DQ6 and DQ7. When DQ7 is set to 1 and DQ6 to 0, it indicates that this second memory area is customer lockable. When DQ7 and DQ6 are both set to 1, it indicates that the second part of the extended memory block is customer locked and protected from program operations. Bits DQ6 and DQ7 are the most significant bits in the extended block protection indicator and a specific procedure must be followed to read it.

Table 18: Extended Memory Block Address and Data

Address	Data	
	Micron prelocked	Customer Lockable
000000h–00007Fh	Secure ID number	Unavailable
000080h-0000FFh	Unavailable	Determined by customer

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Three Bus Write cycles are required to issue the Extended Memory Block command. Once the command has been issued the device enters the extended memory block mode where all bus read or program operations are conducted on the extended memory block. Once the device is in the extended block mode, the extended memory block is addressed by using the addresses occupied by block 0 in the other operating modes (see the Memory Map table).

The device remains in extended memory block mode until the EXIT EXTENDED MEMORY BLOCK command is issued or power is removed from the device. After power-up or hardware reset, the device reverts to read mode where the commands issued to the block 0 address space will properly address block 0.

The extended memory block cannot be erased, and can be treated as one-time programmable (OTP) memory.

In extended block mode, Erase, Chip Erase, Erase Suspend and Erase Resume commands are not allowed.

To exit from the extended memory block mode the EXIT EXTENDED MEMORY BLOCK command must be issued. This command requires four bus write cycles.

The extended memory block can be protected by setting the extended memory block protection bit to 0 (see Lock Register); however once protected the protection cannot be undone.

Note: When the device is in the extended memory block mode, the VPP/WP pin cannot be used for fast programming and the unlock bypass mode is not available (see V_{PP}//WP).

EXIT PROTECTION Command

The EXIT PROTECTION COMMAND SET (90/00h) command is used to exit the lock register, password protection, nonvolatile protection, volatile protection, and nonvolatile protection bit lock bit command set modes and return the device to read mode.

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Device Protection

Hardware Protection

The V_{PP}/WP# function provides a hardware method of protecting the four outermost blocks; that is, the two 32-kword blocks at the top and the two 32-KWord blocks at the bottom of the address space. When V_{PP}/WP# is LOW, PROGRAM and ERASE operations on the four outermost blocks are ignored to provide protection. When V_{PP}/WP# is HIGH, the device reverts to the previous protection status for these four outermost blocks. PROGRAM and ERASE operations can modify the data in these blocks unless the blocks are protected using block protection.

When V_{PP}/WP# is raised to VPPH, the device automatically enters the unlock bypass mode, and command execution time is faster. This must never be done from any mode except read mode; otherwise the device might be left in an indeterminate state.

A 0.1 µF capacitor should be connected between the V_{PP}/WP# pin and the VSS ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during unlock bypass program.

When V_{PP}/WP# returns to HIGH or LOW, normal operation resumes. When operations execute in unlock bypass mode, the device draws IPP from the pin to supply the programming circuits. Transitions from HIGH to VPPH and from VPPH to LOW must be slower than t_{VHVPP}.

Note: Micron highly recommends driving V_{PP}/WP# HIGH or LOW. If a system needs to float the V_{PP}/WP# pin, without a pull-up/pull-down resistor and no capacitor, then an internal pull-up resistor is enabled.

Table 19: V_{PP}/WP# Functions

V_{PP}/WP# Settings	Function
V_{IL}	Four outermost parameter blocks (first two and last two) protected from PROGRAM or ERASE operations.
V_{IH}	Four outermost parameter blocks (first two and last two) unprotected from PROGRAM or ERASE operations, unless a software activated protection is in place.
V_{PPH}	Unlock bypass mode supplies current necessary to speed up PROGRAM execution time.

Software Protection

The following software protection modes are available:

- Volatile protection
- Nonvolatile protection
- Password protection

The device is shipped with all blocks unprotected. On first use, the device defaults to the nonvolatile protection mode but can be activated in either the nonvolatile protection or password protection mode.

The desired protection mode is activated by setting either the nonvolatile protection mode lock bit or the password protection mode lock bit of the lock register (see the Lock Register section). Both bits are one-time-programmable and nonvolatile; therefore, after the protection mode has been activated, it cannot be changed, and the device is set

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permanently to operate in the selected protection mode. It is recommended that the desired software protection mode be activated when first programming the device.

For the four outermost blocks (that is the two blocks at the top and the two at the bottom of the address space), an even higher level of block protection can be achieved by locking the blocks using the non-volatile protection and then by holding V_{PP} /WP# LOW.

Blocks with volatile protection and nonvolatile protection can coexist within the memory array. If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The block protection status can be read by performing a read electronic signature or by issuing an AUTO SELECT command (see the Block Protection table).

Refer to the Block Protection Status table and the Software Protection Scheme figure for details on the block protection scheme. Refer to the Protection Operations section for a description of the command sets.

Volatile Protection Mode

Volatile protection enables the software application to protect blocks against inadvertent change and can be disabled when changes are needed. Volatile protection bits are unique for each block and can be individually modified. Volatile protection bits control the protection scheme only for unprotected blocks whose nonvolatile protection bits are cleared to 1.

Issuing a PROGRAM VOLATILE PROTECTION BIT or CLEAR VOLATILE PROTECTION BIT command sets to 0 or clears to 1 the volatile protection bits and places the associated blocks in the protected (0) or unprotected (1) state, respectively. The volatile protection bit can be set or cleared as often as needed. The default values of the volatile protections are set through the volatile lock boot bit of the lock register (See the Lock Register section).

When the parts are first shipped, or after a power-up or hardware reset, the volatile protection bits can be set or cleared depending upon the ordering option chosen: if the option to clear the volatile protection bits after power-up is selected, then the blocks can be programmed or erased depending on the nonvolatile protection bits state (See the Block Protection Status table); If the option to set the volatile protection bits after power-up is selected, the blocks default to be protected (Refer also to the Protection commands).

Nonvolatile Protection Mode

A nonvolatile protection bit is assigned to each block. Each of these bits can be set for protection individually by issuing a PROGRAM NONVOLATILE PROTECTION BIT command. Also, each device has one global volatile bit called the nonvolatile protection bit lock bit; it can be set to protect all nonvolatile protection bits at once. This global bit must be set to 0 only after all nonvolatile protection bits are configured to the desired settings. When set to 0, the nonvolatile protection bit lock bit prevents changes to the state of the nonvolatile protection bits. When cleared to 1, the nonvolatile protection bits can be set and cleared using the PROGRAM NONVOLATILE PROTECTION BIT and CLEAR ALL NONVOLATILE PROTECTION BITS commands, respectively.

No software command unlocks the nonvolatile protection bit lock bit unless the device is in password protection mode; in nonvolatile protection mode, the nonvolatile protec-

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tion bit lock bit can be cleared only by taking the device through a hardware reset or power-up.

Nonvolatile protection bits cannot be cleared individually; they must be cleared all at once using a CLEAR ALL NONVOLATILE PROTECTION BITS command. They will remain set through a hardware reset or a power-down/power-up sequence.

If one of the nonvolatile protection bits needs to be cleared (unprotected), additional steps are required: First, the nonvolatile protection bit lock bit must be cleared to 1, using either a power-cycle or hardware reset. Then, the nonvolatile protection bits can be changed to reflect the desired settings. Finally, the nonvolatile protection bit lock bit must be set to 0 to lock the nonvolatile protection bits. The device now will operate normally.

To achieve the best protection, the PROGRAM NONVOLATILE PROTECTION LOCK BIT command should be executed early in the boot code, and the boot code should be protected by holding V_{PP}/WP# LOW.

Nonvolatile protection bits and volatile protection bits have the same function when V_{PP}/WP# is HIGH or when V_{PP}/WP# is at the voltage for program acceleration (V_{PPH}).

Password Protection Mode

Password protection mode provides a higher level of security than the nonvolatile protection mode by requiring a 64-bit password to unlock the nonvolatile protection bit lock bit. In addition to this password requirement, the nonvolatile protection bit lock bit is set to 0 after power-up and reset to maintain the device in password protection mode.

Executing the UNLOCK PASSWORD command by entering the correct password clears the nonvolatile protection bit lock bit, enabling the block nonvolatile protection bits to be modified. If the password provided is incorrect, the nonvolatile protection bit lock bit remains locked, and the state of the nonvolatile protection bits cannot be modified.

To place the device in password protection mode, the following two steps are required: First, before activating the password protection mode, a 64-bit password must be set and the setting verified. Password verification is allowed only before the password protection mode is activated. Next, password protection mode is activated by programming the password protection mode lock bit to 0. This operation is irreversible; after the bit is programmed, it cannot be erased. The device remains permanently in password protection mode, and the 64-bit password can be neither retrieved nor reprogrammed. In addition, all commands to the address where the password is stored are disabled.

Note: There is no means to verify the password after password protection mode is enabled. If the password is lost after enabling the password protection mode, there is no way to clear the nonvolatile protection bit lock bit.

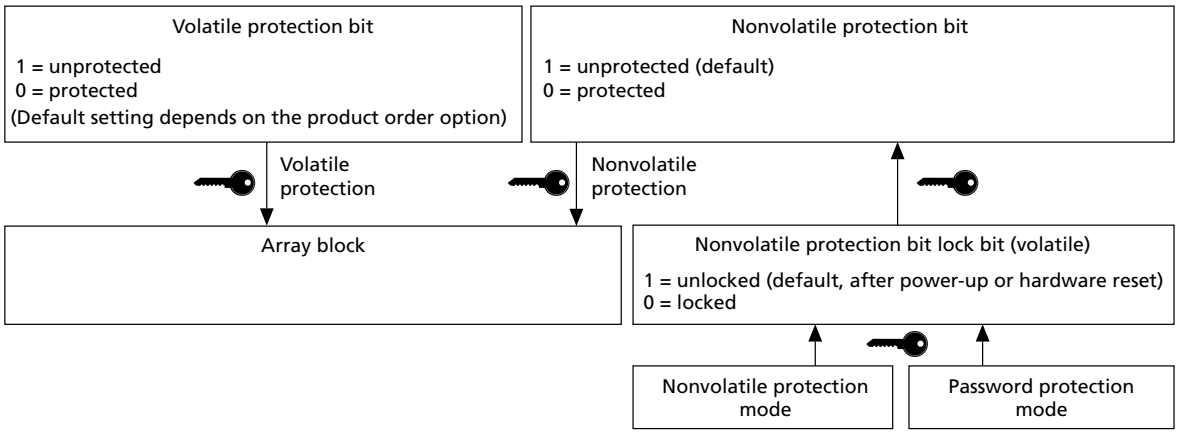
NVPBs default to ‘1’ (block unprotected) after power-up and hardware reset. A block is protected or unprotected when its NVPB is set to ‘0’ and ‘1’, respectively. NVPBs are programmed individually and cleared collectively.

VPB default status depends on ordering option. A block is protected or unprotected when its VPB is set to ‘0’ and ‘1’, respectively. VPBs are programmed and cleared individually. For the volatile protection to be effective, the NVPB lock bit must be set to ‘0’ (NVPB bits unlocked) and the block NVPB must be set to ‘1’ (block unprotected).

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3. The NVPB lock bit is volatile and default to ‘1’ (NVPB bits unlocked) after power-up and hardware reset. NVPB bits are locked by setting the NVPB lock bit to ‘0’. Once programmed to ‘0’, the NVPB lock bit can be reset to ‘1’ only be taking the device through a power-up or hardware reset.

Figure 12: Software Protection Scheme



Notes:
1. Nonvolatile protection bits default to 1 (block unprotected) when the parts are first shipped. A block is protected or unprotected when its nonvolatile protection bit is set to 0 and 1, respectively.
2. Volatile protection bits are programmed and cleared individually. Nonvolatile protection bits are programmed individually and cleared collectively.
3. Volatile protection bit default status depends on ordering option. A block is protected or unprotected when its volatile protection bit is set to 0 and 1, respectively. For the volatile protection to be effective, the block nonvolatile protection bit must be set to 1 (block unprotected).
4. Once programmed to 0, the nonvolatile protection bit lock bit can be reset to 1 only by taking the device through a power-up or hardware reset.

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Dual Operations and Multiple Bank Architecture

The multiple bank architecture gives greater flexibility for software developers to split the code and data spaces within the memory array. The dual operations feature simplifies the software management of the device by allowing code to be executed from one bank while another bank is being programmed or erased.

The dual operations feature means that while programming or erasing in one bank, read operations are possible in another bank with zero latency.

Only one bank at a time is allowed to be in program or erase mode. However, certain commands can cross bank boundaries, which means that during an operation only the banks that are not concerned with the cross bank operation are available for dual operations. For example, if a Block Erase command is issued to erase blocks in both bank A and bank B, then only banks C or D are available for read operations while the erase is being executed.

If a read operation is required in a bank, which is programming or erasing, the program or erase operation can be suspended.

Also if the suspended operation was erase then a program command can be issued to another block, so the device can have one block in erase suspend mode, one programming and other banks in read mode.

By using a combination of these features, read operations are possible at any moment.

The tables below show the dual operations possible in other banks and in the same bank. Note that only the commonly used commands are represented in these tables.

Table 20: Dual Operations Allowed in Other Banks

Status of bank	Commands Allowed in Another Bank							
	Read	Read Status Register[2]	Read CFI Query	Auto Select	Program	Erase	Program/Erase Suspend	Program/Erase Resume
Idle	Yes	Yes[3]	Yes	Yes	Yes	Yes	Yes[3]	Yes[4]
Programming	Yes	No	No	No	–	–	No	No
Erasing	Yes	No	No	No	–	–	No	No
Program suspended	Yes	No	No	Yes	No	No	–	No
Erase suspended	Yes	No	No	Yes	Yes	No	–	Yes[5]

Notes:
1. If several banks are involved in a program or erase operation, then only the banks that are not concerned with the operation are available for dual operations.
2. Read Status Register is not a command. The status register can be read during a block program or erase operation.
3. Only after a program or erase operation in that bank.
4. Only after a Program or Erase Suspend command in that bank.
5. Only an erase resume is allowed if the bank was previously in erase suspend mode.

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Table 21: Dual Operations Allowed in Same Bank

Status of bank	Commands Allowed in Same Bank							
	Read	Read Status Register[1]	Read CFI Query	Auto Select	Program	Erase	Program/Erase Suspend	Program/Erase Resume
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes[2]	Yes[3]
Programming	No	Yes	No	No	–	–	Yes[4]	–
Erasing	No	Yes	No	No	–	No	Yes[5]	–
Program suspended	Yes	No	No	Yes	No	–	–	Yes
Erase suspended	Yes[6]	Yes[7]	No	Yes	Yes[6]	No	–	Yes

Notes:
1. Read status register is not a command. The status register can be read during a block program or erase operation.
2. Only after a program or erase operation in that bank.
3. Only after a Program or Erase Suspend command in that bank.
4. Only a program suspend.
5. Only an erase suspend.
6. Not allowed in the block or word that is being erased or programmed.
7. The status register can be read by addressing the block being erase suspended.

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Common Flash Interface

The common flash interface is a JEDEC approved, standardized data structure that can be read from the flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query command is issued, the memory enters read CFI query mode and read operations output the CFI data. The tables here show the addresses (A0-A7) used to retrieve the data. The CFI data structure also contains a security area where a 64-bit unique security number is written (see Table 40: Security Code Area). This area can be accessed only in read mode by the final user. It is impossible to change the security number after it has been written by Micron.

Table 22: Query Structure Overview

Note applies to the entire table.

Address x16	Sub-section name	Description
10h	CFI query identification string	Command set ID and algorithm data offset
1Bh	System interface information	Device timing & voltage information
27h	Device geometry definition	Flash device layout
40h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)
61h	Security code area	64-bit unique device number

Note: 1. Query data are always presented on the lowest order data outputs.

Table 23: CFI Query Identification String

Note applies to the entire table.

Address x16	Data	Description	Value
10h	0051h		'Q'
11h	0052h	Query unique ASCII string 'QRY'	'R'
12h	0059h		'Y'
13h	0002h	Primary algorithm command set and control interface ID code 16 bit ID code defining a specific algorithm	Spansion compatible
14h	0000h		
15h	0040h	Address for primary algorithm extended query table (see the Primary Algorithm-Specific Extended Query Table)	P = 40h
16h	0000h		
17h	0000h	Alternate vendor command set and control interface ID code second vendor - specified algorithm supported	NA
18h	0000h		
19h	0000h	Address for alternate algorithm extended query table	NA
1Ah	0000h		

Note: 1. Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are '0'.

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Table 24: CFI Query System Interface Information

Note applies to the entire table.

Address x16	Data	Description	Value
1Bh	0027h	V_{CC} logic supply minimum program/erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	2.7 V
1Ch	0036h	V_{CC} logic supply maximum program/erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	3.6 V
1Dh	0085h	V_{PPH} [programming] supply minimum program/erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	8.5 V
1Eh	0095h	V_{PPH} [programming] supply maximum program/erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	9.5 V
1Fh	0004h	Typical timeout for single word program = 2^n µs	16 µs
20h	0004h	Typical timeout for minimum size write buffer program = 2^n µs	16 µs
21h	0009h	Typical timeout for individual block erase = 2^n ms	0.5 s
22h	0011h	Typical timeout for full chip erase = 2^n ms	80 s
23h	0004h	Maximum timeout for word program = 2^n times typical	200 µs
24h	0004h	Maximum timeout for write buffer program = 2^n times typical	200 µs
25h	0003h	Maximum timeout per individual block erase = 2^n times typical	2.3 s
26h	0004h	Maximum timeout for chip erase = 2^n times typical	800 s

Note: 1. The values given in the above table are valid for both packages.

Table 25: Device Geometry Definition

Address x16	Data	Description	Value
27h	0019h	Device size = 2^n in number of bytes	32 Mbytes
28h 29h	0001h 0000h	Flash device interface code description	x16 async.
2Ah 2Bh	0006h 0000h	Maximum number of bytes in multiple-byte program or page= 2^n	64
2Ch	0003h	Number of Erase block regions. It specifies the number of regions containing contiguous Erase blocks of the same size.	3
2Dh 2Eh 2Fh 30h	0003h 0000h 0000h 0001h	Erase block region 1 information 2Dh-2Eh: number of erase blocks of identical size 2Fh-30h: block size (n*256 bytes)	4 blocks, 32-Kwords
31h 32h 33h 34h	007Dh 0000h 0000h 0004h	Erase block region 2 information	126 blocks, 128-Kwords
35h 36h 37h 38h	0003h 0000h 0000h 0001h	Erase block region 3 information	4 blocks, 32-Kwords
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase block region 4 information	NA

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Table 26: Primary Algorithm-Specific Extended Query Table

Address x16	Data	Description	Value
40h	0050h	Primary algorithm extended query table unique ASCII string "PRI"	'P'
41h	0052h		'R'
42h	0049h		'I'
43h	0031h	Major version number, ASCII	'1'
44h	0033h	Minor version number, ASCII	'3'
45h	0010h	Address sensitive unlock (bits 1 to 0) 00 = required, 01= not required Silicon revision number (bits 7 to 2)	Yes 65 nm
46h	0002h	Erase suspend 00 = not supported, 01 = read only, 02 = read and write	2
47h	0001h	Block protection 00 = not supported, x = number of blocks per group	1
48h	0000h	Temporary block unprotect 00 = not supported, 01 = supported	Not supported
49h	0008h	Block protect /unprotect 08 = M29DW256G	8
4Ah	0073h	Simultaneous operations: x= block number (excluding bank A)	115
4Bh	0000h	Burst mode, 00 = not supported, 01 = supported	Not supported
4Ch	0002h	Page mode, 00 = not supported, 02 = 8-word page	02
4Dh	0085h	V_{PPH} supply minimum program/erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	8.5 V
4Eh	0095h	V_{PPH} supply maximum program/erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	9.5 V
4Fh	0001h	01 = Dual Boot	Dual Boot
50h	0001h	Program suspend, 00 = not supported, 01 = supported	Supported
51h	0001h	Unlock bypass: 00 = not supported, 01 = supported	Supported
52h	0008h	Extended memory block size (customer lockable), 2^n bytes	256
57h	0004h	Bank organization, 00 = data at 4Ah is 0, x= bank number	4
58h	0013h	Bank A information, x = number of blocks in bank A	19
59h	0030h	Bank B information, x = number of blocks in bank B	48
5Ah	0030h	Bank C information, x = number of blocks in bank C	48
5Bh	0013h	Bank D information, x = number of blocks in bank D	19

Note: 1. The values given in the above table are valid for both packages.

Table 27: Security Code Area

Address x16	Data	Description
61h	XXXX	64-bit: unique device number
62h	XXXX	
63h	XXXX	
64h	XXXX	

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Power-Up and Reset Characteristics

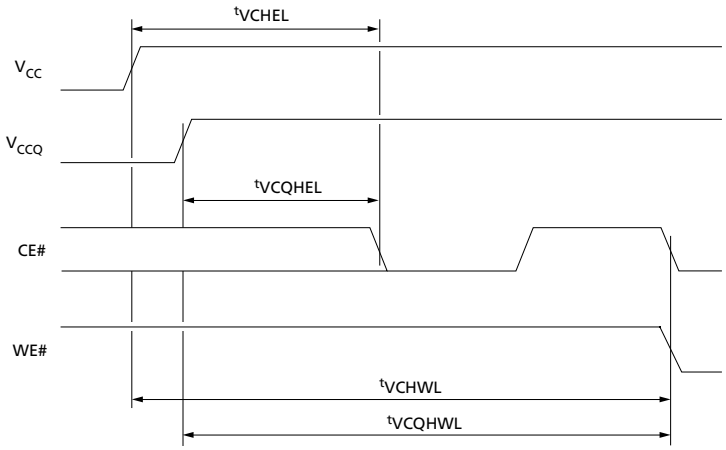
Table 28: Power-Up Wait Timing Specifications

Note 1 applies to the entire table

Parameter	Symbol		Min	Max	Unit	Notes
	Legacy	JEDEC				
V_{CC} HIGH to CE# LOW	^{t}VCH	^{t}VCHEL	55	–	µs	2
V_{CCQ} HIGH to CE# LOW	–	^{t}VCQHEL	55	–	µs	2
V_{CC} HIGH to WE# LOW	–	^{t}VCHWL	500	–	µs	
V_{CCQ} HIGH to WE# LOW	–	^{t}VCQHWL	500	–	µs	

Notes: 1. Specifications apply to 70 and 80ns devices unless otherwise noted.
2. V_{CC} and V_{CCQ} ramps must be synchronized during power-up.

Figure 13: Power-Up Timing



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Table 29: Reset AC Specifications

Note 1 applies to the entire table

Condition/Parameter	Symbol		Min	Max	Unit	Notes
	Legacy	JEDEC				
RST# LOW to read mode during program or erase	tREADY	tPLRH	–	55	µs	2
RST# pulse width	tRP	tPLPH	20	–	µs	
RST# HIGH to CE# LOW, OE# LOW	tRH	tPHEL, tPHGL, tPHWL	55	–	ns	2
RST# LOW to standby mode during read mode	tRPD	–	20	–	µs	
RST# LOW to standby mode during program or erase			55	–	µs	
RY/BY# HIGH to CE# LOW, OE# LOW	tRB	tRHEL, tRHGL, tRHWL	0	–	ns	2

Notes: 1. Specifications apply to 70 and 80ns devices unless otherwise noted.
2. Sampled only; not 100% tested.

Figure 14: Reset AC Timing – No PROGRAM/ERASE Operation in Progress

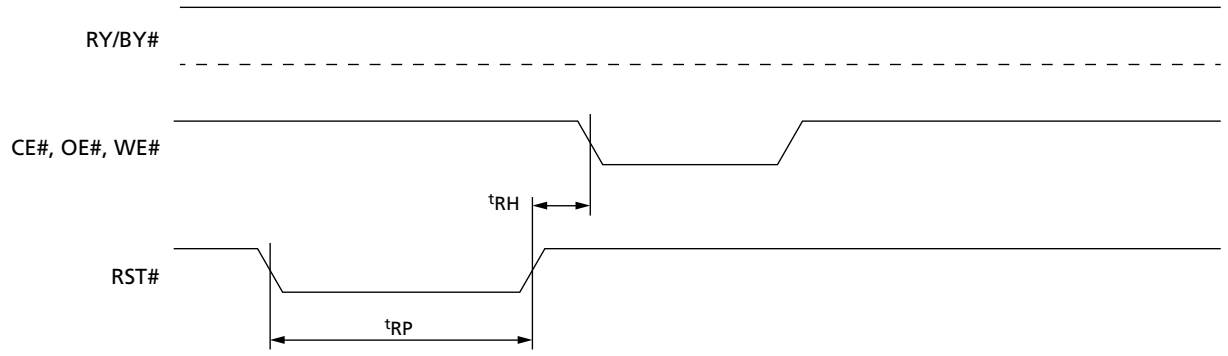
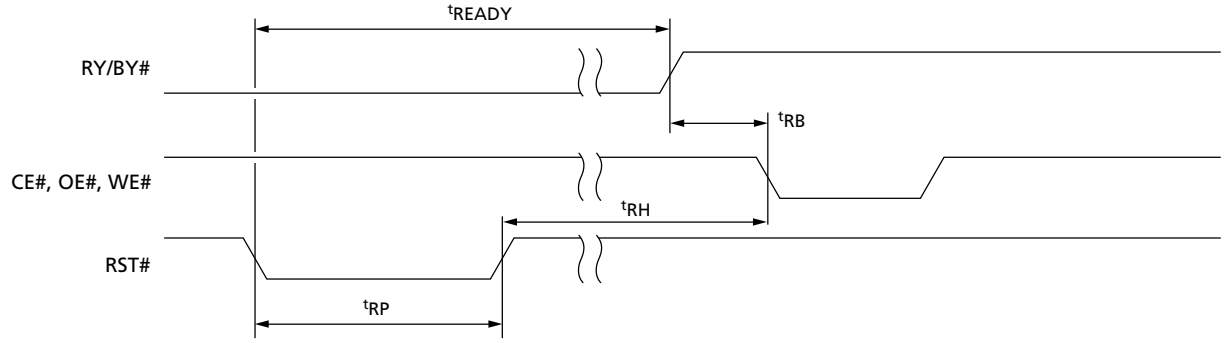


Figure 15: Reset AC Timing During PROGRAM/ERASE Operation



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Absolute Ratings and Operating Conditions

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 30: Absolute Maximum/Minimum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Temperature under bias	T_{BIAS}	–50	125	°C	
Storage temperature	T_{STG}	–65	150	°C	
Input/output voltage	V_{IO}	–0.6	V_{CC} + 0.6	V	1, 2
Supply voltage	V_{CC}	–0.6	4	V	
Input/output supply voltage	V_{CCQ}	–0.6	4	V	
Program voltage	V_{PPH}	–0.6	10.5	V	3

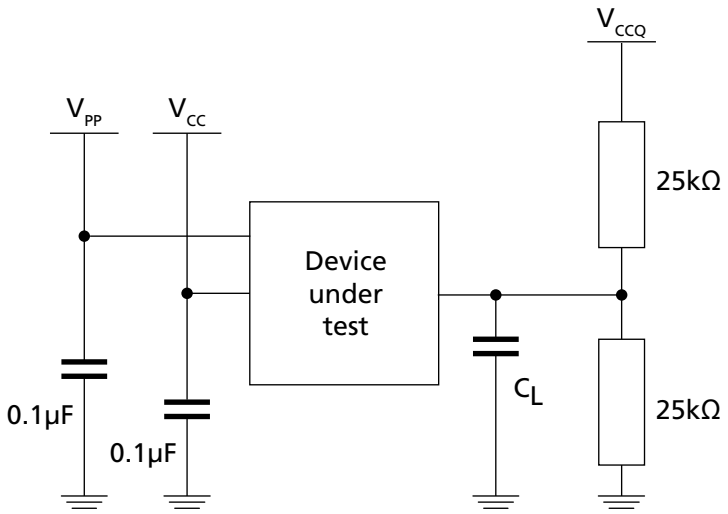
Notes:
1. During signal transitions, minimum voltage may undershoot to –2V for periods less than 20ns.
2. During signal transitions, maximum voltage may overshoot to V_{CC} + 2V for periods less than 20ns.
3. V_{PPH} must not remain at 9V for more than 80 hours cumulative.

Table 31: Operating Conditions

Parameter	Symbol	70ns		80ns		Unit
		Min	Max	Min	Max	
Supply voltage	V_{CC}	2.7	3.6	2.7	3.6	V
Input/output supply voltage ($V_{CCQ} \le V_{CC}$)	V_{CCQ}	2.7	3.6	1.65	3.6	V
Ambient operating temperature (range 1)	T_A	0	70	0	70	°C
Ambient operating temperature (range 6)	T_A	–40	85	–40	85	°C
Load capacitance	C_L	30		30		pF
Input rise and fall times	–	–	10	–	10	ns
Input pulse voltages	–	0 to V_{CCQ}		0 to V_{CCQ}		V
Input and output timing reference voltages	–	$V_{CCQ}/2$		$V_{CCQ}/2$		V

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Figure 16: AC Measurement Load Circuit



Note: 1. C_L includes jig capacitance.

Figure 17: AC Measurement I/O Waveform

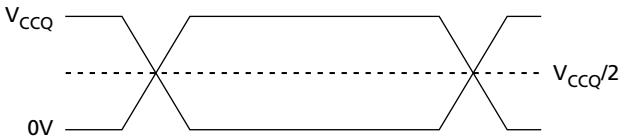


Table 32: Input/Output Capacitance[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	–	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	–	12	pF

Note: 1. Sampled only, not 100% tested.

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DC Characteristics

Table 33: DC Current Characteristics

Parameter		Symbol	Conditions		Min	Typ	Max	Unit	Notes
Input leakage current		I_{LI}	$0V \le V_{IN} \le V_{CC}$		–	–	±1	µA	1
Output leakage current		I_{LO}	$0V \le V_{OUT} \le V_{CC}$		–	–	±1	µA	
VCC read current	Random read	I_{CC1}	CE# = V_{IL}, OE# = V_{IH}, f = 6 MHz		–	–	10	mA	
	Page read		CE# = V_{IL}, OE# = V_{IH}, f = 10 MHz		–	–	1	mA	
VCC standby current		I_{CC2}	CE# = V_{CCQ} ±0.2V, RST# = V_{CCQ} ±0.2V		–	–	100	µA	
VCC program/erase current		I_{CC3}	Program/ erase controller active	V_{PP}/WP# = V_{IL} or V_{IH}	–	–	20	mA	2
				V_{PP}/WP# = V_{PPH}	–	–	15	mA	
V_{PP} current	Read	I_{PP1}	V_{PP}/WP# ≤ V_{CC}		–	1	5	µA	
	Standby				–	1	5	µA	
	Reset	I_{PP2}	RST# = V_{SS} ±0.2V		–	1	5	µA	
	PROGRAM operation ongoing	I_{PP3}	V_{PP}/WP# = 12V ±5%		–	1	10	mA	
			V_{PP}/WP# = V_{CC}		–	1	5	mA	
	ERASE operation ongoing	I_{PP4}	V_{PP}/WP# = 12V ±5%		–	3	10	mA	
			V_{PP}/WP# = V_{CC}		–	1	5	mA	

Notes: 1. The maximum input leakage current is ±5µA on the V_{PP}/WP# pin.
2. Sampled only; not 100% tested.

Table 34: DC Voltage Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Notes
Input LOW voltage	V_{IL}	$V_{CC} \ge 2.7V$	–0.5	–	$0.3V_{CCQ}$	V	
Input HIGH voltage	V_{IH}	$V_{CC} \ge 2.7V$	$0.7V_{CCQ}$	–	V_{CCQ} + 0.4	V	
Output LOW voltage	V_{OL}	I_{OL} = 100µA, V_{CC} = $V_{CC,min}$, V_{CCQ} = $V_{CCQ,min}$	–	–	$0.15V_{CCQ}$	V	
Output HIGH voltage	V_{OH}	I_{OH} = 100µA, V_{CC} = $V_{CC,min}$, V_{CCQ} = $V_{CCQ,min}$	$0.85V_{CCQ}$	–	–	V	
Voltage for V_{PP}/WP# program acceleration	V_{PPH}	–	–	8.5	9.5	V	
Program/erase lockout supply voltage	V_{LKO}	–	1.8	–	2.5	V	1

Note: 1. Sampled only; not 100% tested.

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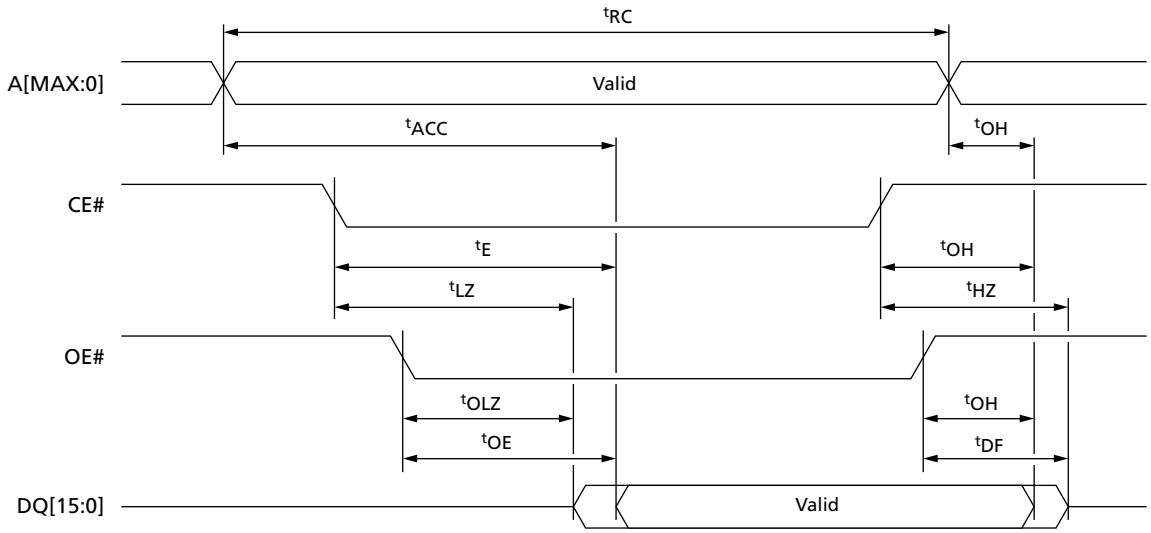
Read AC Characteristics

Table 35: Read AC Characteristics

Parameter	Symbol		Condition	70ns $V_{CCQ} = V_{CC}$		80ns V_{CCQ} = 1.65V to V_{CC}		Unit	Notes
	Legacy	JEDEC		Min	Max	Min	Max		
Address valid to next address valid	^{t}RC	^{t}AVAV	CE# = V_{IL}, OE# = V_{IL}	70	–	80	–	ns	
Address valid to output valid	^{t}ACC	^{t}AVQV	CE# = V_{IL}, OE# = V_{IL}	–	70	–	80	ns	
Address valid to output valid (page)	^{t}PAGE	^{t}AVQV1	CE# = V_{IL}, OE# = V_{IL}	–	25	–	30	ns	
CE# LOW to output transition	^{t}LZ	^{t}ELQX	OE# = V_{IL}	0	–	0	–	ns	1
CE# LOW to output valid	^{t}E	^{t}ELQV	OE# = V_{IL}	–	70	–	80	ns	
OE# LOW to output transition	^{t}OLZ	^{t}GLQX	CE# = V_{IL}	0	–	0	–	ns	1
OE# LOW to output valid	^{t}OE	^{t}GLQV	CE# = V_{IL}	–	25	–	30	ns	
CE# HIGH to output High-Z	^{t}HZ	^{t}EHQZ	OE# = V_{IL}	–	25	–	30	ns	1
OE# HIGH to output High-Z	^{t}DF	^{t}GHQZ	CE# = V_{IL}	–	25	–	30	ns	1
CE#, OE#, or address transition to output transition	^{t}OH	^{t}EHQX, ^{t}GHQX, ^{t}AXQX	–	0	–	0	–	ns	

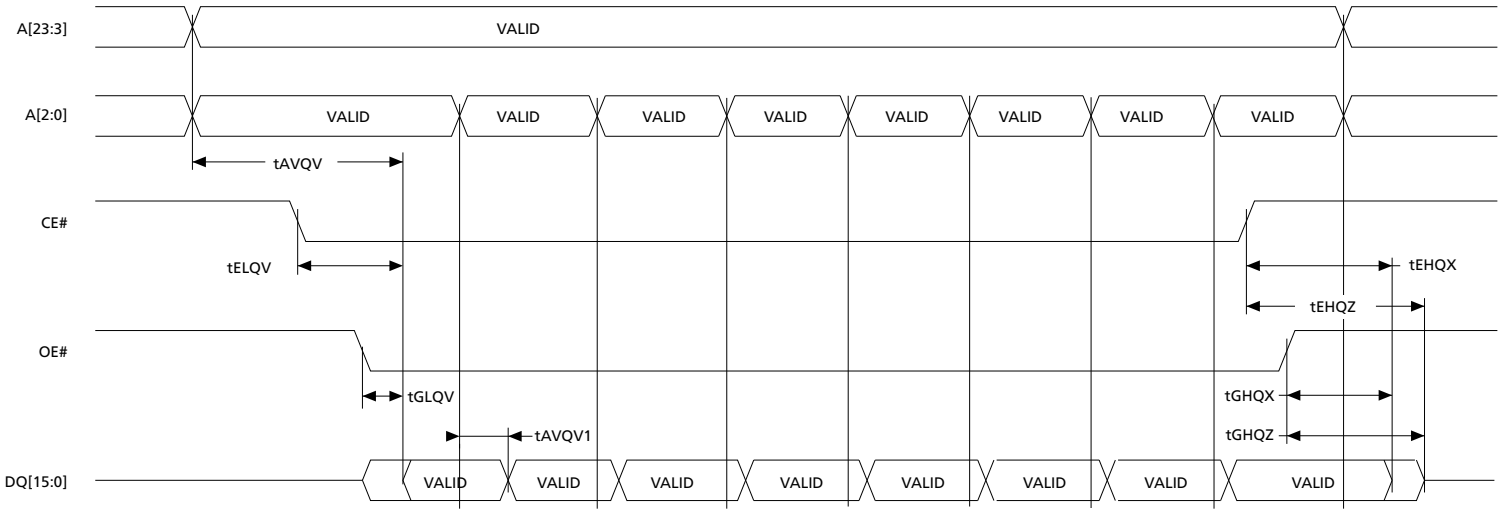
Note: 1. Sampled only; not 100% tested.

Figure 18: Random Read AC Timing



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Figure 19: Page Read AC Timing



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Write AC Characteristics

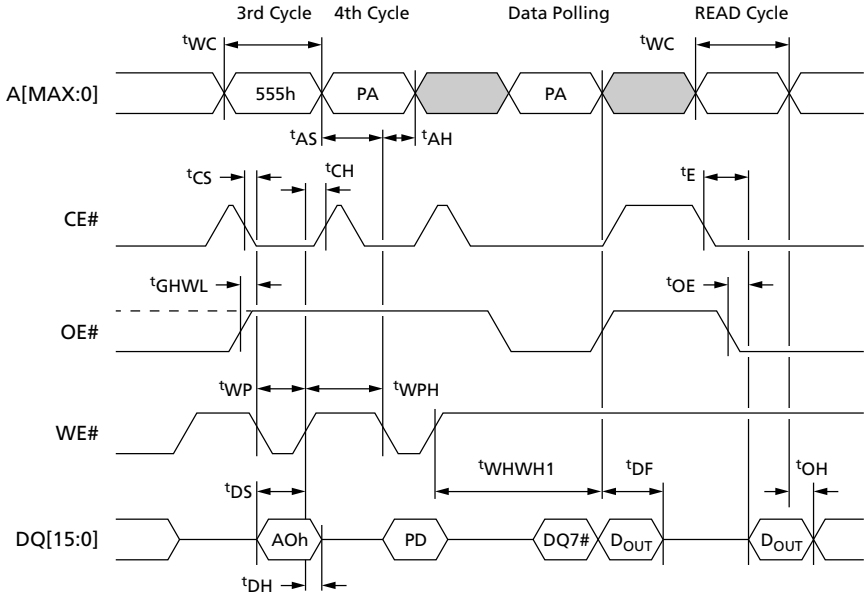
Table 36: WE#-Controlled Write AC Characteristics

Parameter	Symbol		70ns $V_{CCQ} = V_{CC}$		80ns V_{CCQ} = 1.65V to V_{CC}		Unit	Notes
	Legacy	JEDEC	Min	Max	Min	Max		
Address valid to next address valid	^{t}WC	^{t}AVAV	70	–	80	–	ns	
CE# LOW to WE# LOW	^{t}CS	^{t}ELWL	0	–	0	–	ns	
WE# LOW to WE# HIGH	^{t}WP	^{t}WLWH	35	–	35	–	ns	
Input valid to WE# HIGH	^{t}DS	^{t}DVWH	45	–	45	–	ns	
WE# HIGH to input transition	^{t}DH	^{t}WHDX	0	–	0	–	ns	
WE# HIGH to CE# HIGH	^{t}CH	^{t}WHEH	0	–	0	–	ns	
WE# HIGH to WE# LOW	^{t}WPH	^{t}WHWL	30	–	30	–	ns	
Address valid to WE# LOW	^{t}AS	^{t}AVWL	0	–	0	–	ns	
WE# LOW to address transition	^{t}AH	^{t}WLAX	45	–	45	–	ns	
OE# HIGH to WE# LOW	–	^{t}GHWL	0	–	0	–	ns	
WE# HIGH to OE# LOW	^{t}OEH	^{t}WHGL	0	–	0	–	ns	
Program/erase valid to RY/BY# LOW	^{t}BUSY	^{t}WHRL	–	30	–	30	ns	1
V_{CC} HIGH to CE# LOW	^{t}VCS	^{t}VCHEL	50	–	50	–	µs	

Note: 1. Sampled only; not 100% tested.

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Figure 20: WE#-Controlled Program AC Timing



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit and by a READ operation that outputs the data (D_{OUT}) programmed by the previous PROGRAM command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (See Data Polling Bit [DQ7]).
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

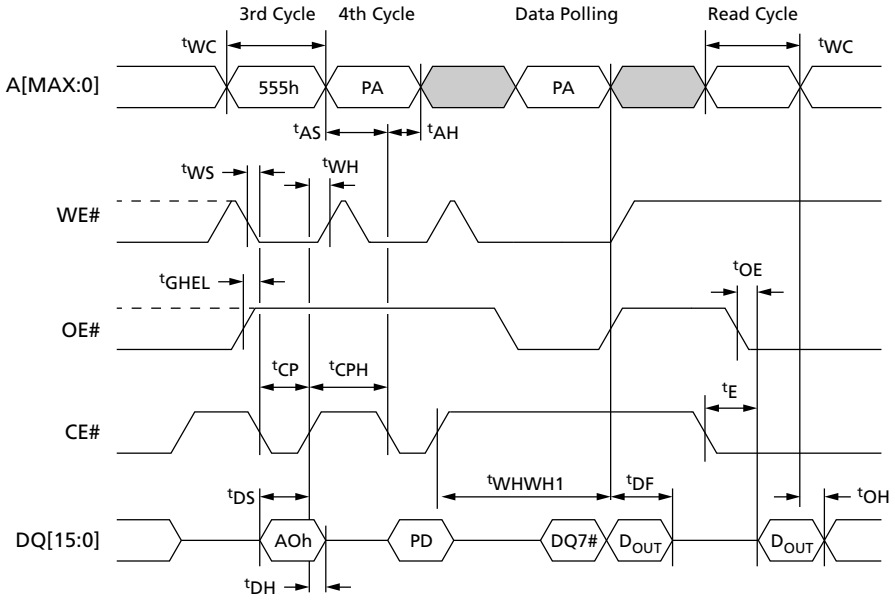
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Table 37: CE#-Controlled Write AC Characteristics

Parameter	Symbol		70ns $V_{CCQ} = V_{CC}$		80ns V_{CCQ} = 1.65V to V_{CC}		Unit
	Legacy	JEDEC	Min	Max	Min	Max	
Address valid to next address valid	^{t}WC	^{t}AVAV	75	–	85	–	ns
WE# LOW to CE# LOW	^{t}WS	^{t}WLEL	0	–	0	–	ns
CE# LOW to CE# HIGH	^{t}CP	^{t}ELEH	35	–	35	–	ns
Input valid to CE# HIGH	^{t}DS	^{t}DVEH	45	–	45	–	ns
CE# HIGH to input transition	^{t}DH	^{t}EHDX	0	–	0	–	ns
CE# HIGH to WE# HIGH	^{t}WH	^{t}EHWH	0	–	0	–	ns
CE# HIGH to CE# LOW	^{t}CPH	^{t}EHEL	30	–	30	–	ns
Address valid to CE# LOW	^{t}AS	^{t}AVEL	0	–	0	–	ns
CE# LOW to address transition	^{t}AH	^{t}ELAX	45	–	45	–	ns
OE# HIGH to CE# LOW	–	^{t}GHEL	0	–	0	–	ns

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Figure 21: CE#-Controlled Program AC Timing



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (See Data Polling Bit [DQ7]).
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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Accelerated Program, Data Polling/Toggle AC Characteristics

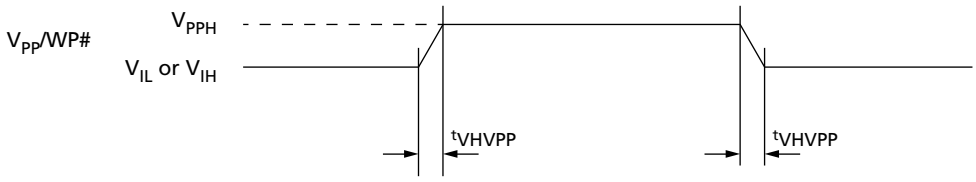
Table 38: Accelerated Program and Data Polling/Data Toggle AC Characteristics

Note 1 applies to the entire table.

Parameter	Symbol		Min	Max	Unit
	Legacy	JEDEC			
V_{PP}/WP# rising or falling time	–	^{t}VHVPP	250	–	ns
Address setup time to OE# LOW during toggle bit polling	^{t}ASO	^{t}AXGL	10	–	ns
Address hold time from OE# during toggle bit polling	^{t}AHT	^{t}GHAX, ^{t}EHAX	10	–	ns
CE# HIGH during toggle bit polling	^{t}EPH	^{t}EHEL2	10	–	ns
Output hold time during data and toggle bit polling	^{t}OEH	^{t}WHGL2, ^{t}GHGL2	20	–	ns
Program/erase valid to RY/BY# LOW	^{t}BUSY	^{t}WHRL	–	30	ns

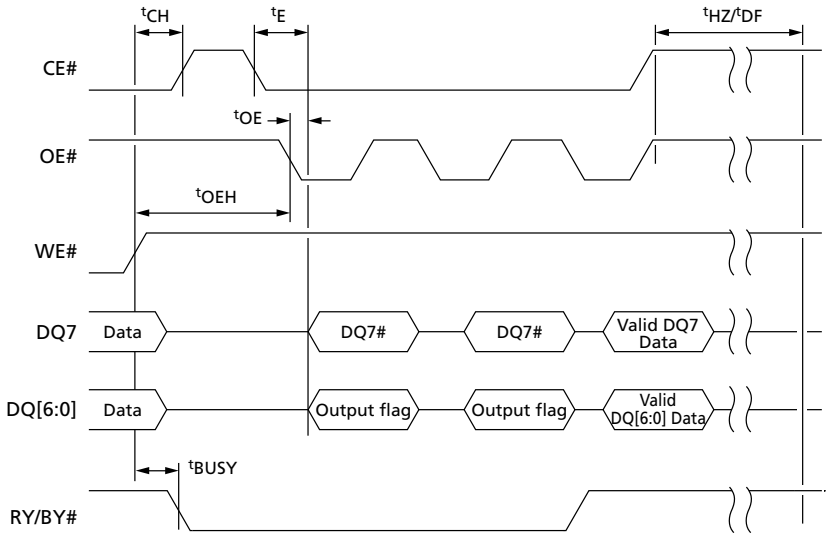
Note: 1. Specifications apply to 70, and 80ns devices unless otherwise noted.

Figure 22: Accelerated Program AC Timing



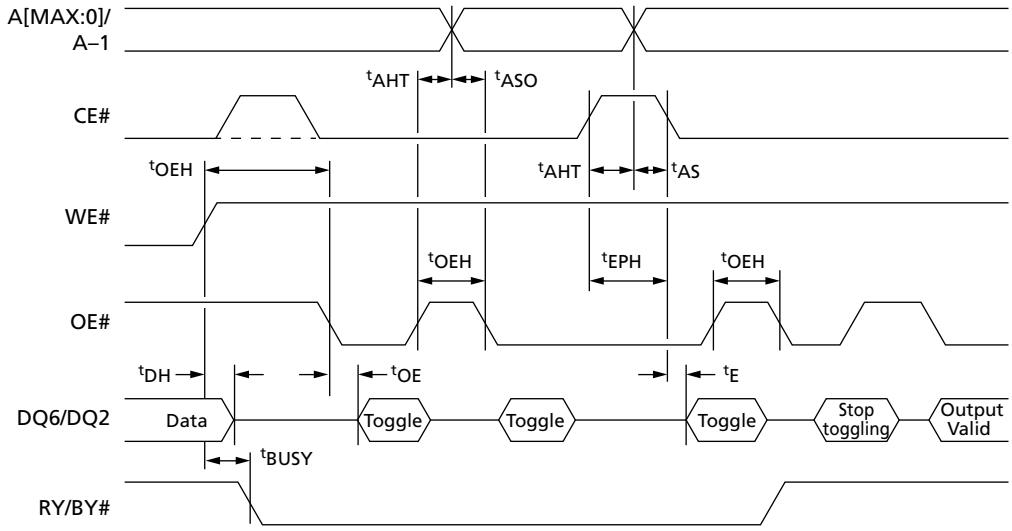
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Figure 23: Data Polling AC Timing



Notes:
1. DQ7 returns a valid data bit when the PROGRAM or ERASE command has completed.
2. See the following tables for timing details: Read AC Characteristics, Accelerated Program and Data Polling/Data Toggle AC Characteristics.

Figure 24: Toggle/Alternative Toggle Bit Polling AC Timing



Notes:
1. DQ6 stops toggling when the PROGRAM or ERASE command has completed. DQ2 stops toggling when the CHIP ERASE or BLOCK ERASE command has completed.
2. See the following tables for timing details: Read AC Characteristics, Accelerated Program and Data Polling/Data Toggle AC Characteristics.

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Program/Erase Characteristics

Table 39: Program/Erase Characteristics

Notes 1 and 2 apply to the entire table

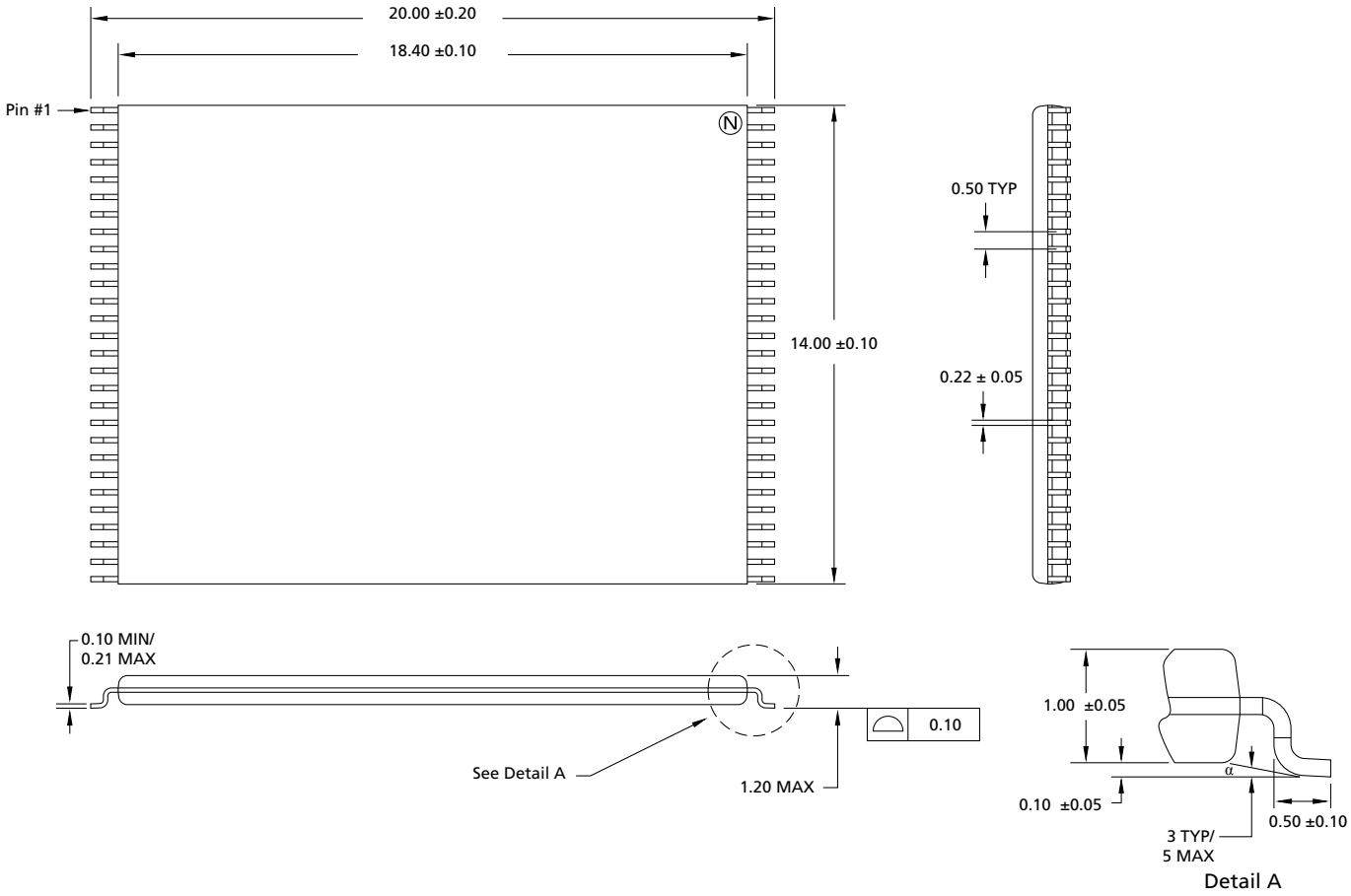
Parameter			Min	Typ	Max	Unit	Notes
Chip erase			–	145	400	s	3
Chip erase		V_{PP}/WP# = V_{PPH}	–	125	400	s	3
Block erase (128 Kword)			–	1	4	s	3, 4
Block erase (32 Kword)			–	0.37	1.5	s	
Erase suspend latency time			–	25	45	µs	
Block erase timeout			50	–	–	µs	
Word program	Single-word program		–	16	200	µs	3
	Write to buffer program (32 words at-a-time)	V_{PP}/WP# = V_{PPH}	–	50	200	µs	3
		V_{PP}/WP# = V_{IH}	–	70	200	µs	3
Chip program (word by word)			–	270	400	s	3
Chip program (write to buffer program)			–	25	200	s	3, 6
Chip program (write to buffer program with V_{PP}/WP# = V_{PPH})			–	13	50	s	3, 5
Chip program (enhanced buffered program)			–	15	60	s	5
Chip program (enhanced buffered program with V_{PP}/WP# = V_{PP})			–	10	40	s	5
Program suspend latency time			–	5	15	µs	
PROGRAM/ERASE cycles (per block)			100,000	–	–	cycles	
Data retention			20	–	–	years	

Notes:
1. Typical values measured at room temperature and nominal voltages and for not cycled devices.
2. Typical and maximum values are sampled, but not 100% tested.
3. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,000 PROGRAM/ERASE cycles.
4. Block erase polling cycle time (see Data polling AC waveforms figure).
5. Intrinsic program timing, that means without the time required to execute the bus cycles to load the PROGRAM commands.

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Package Dimensions

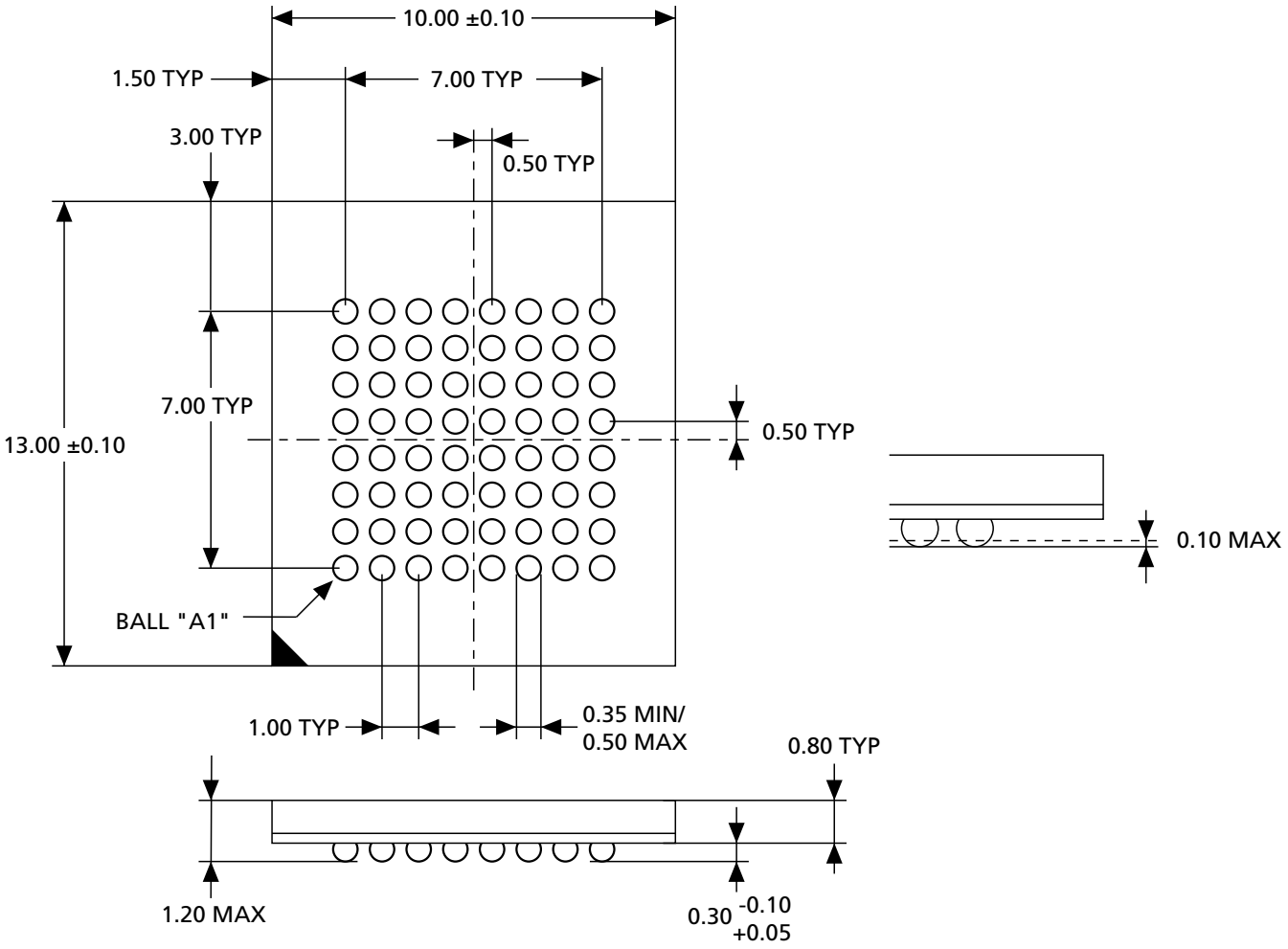
Figure 25: 56-Pin TSOP – 14mm x 20mm



Notes:
1. All dimensions are in millimeters.
2. For the lead width value of 0.22 ±0.05, there is also a legacy value of 0.15 ±0.05.

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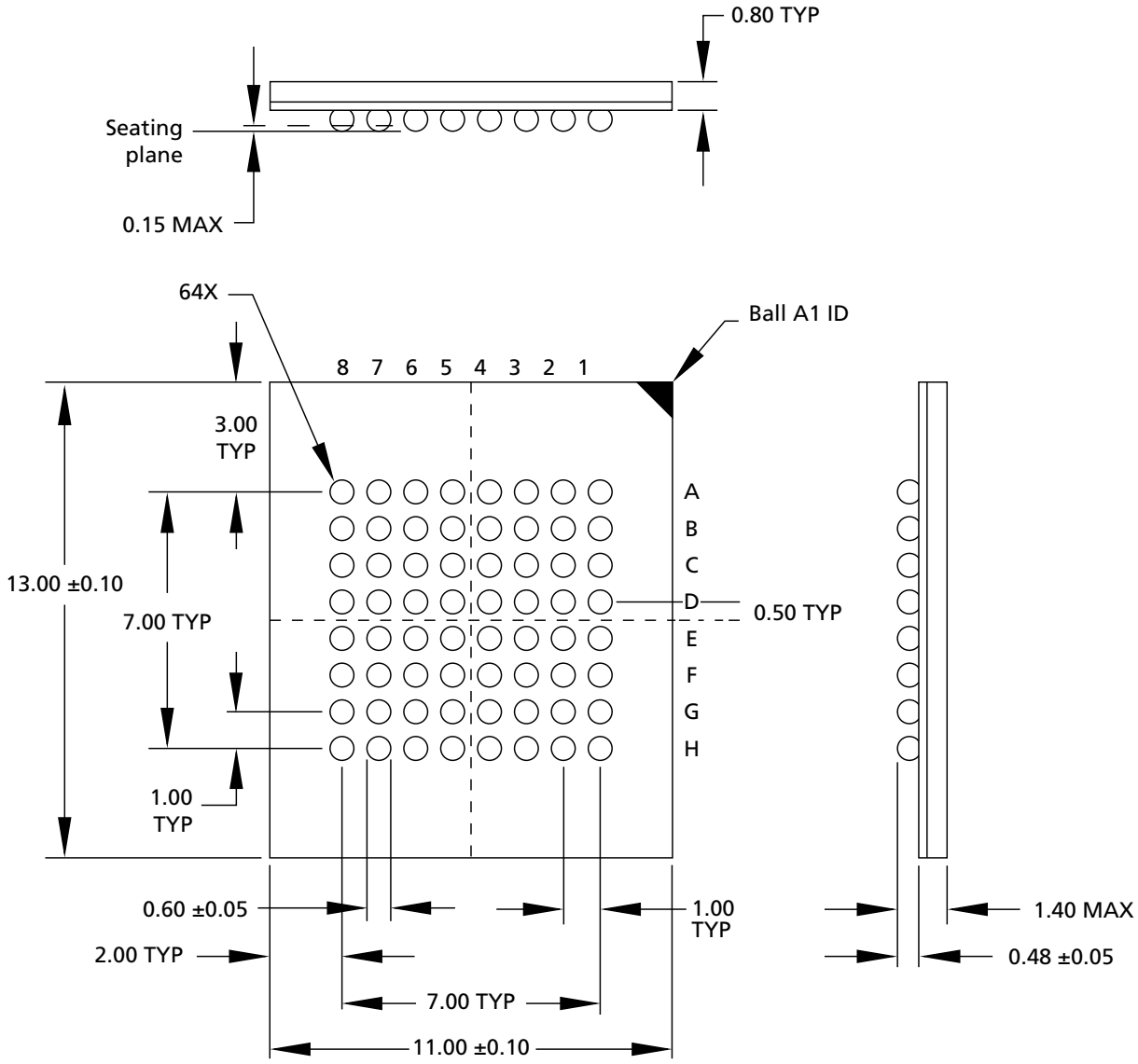
Figure 26: 64-Pin TBGA – 10mm x 13mm



Note: 1. All dimensions are in millimeters.

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Figure 27: 64-Ball Fortified BGA – 11mm x 13mm



Note: 1. All dimensions are in millimeters.

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Revision History

Rev. A – 10/12

- Initial Micron brand release

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