TPA2012D2 2.1-W/Channel Stereo Filter-Free Class-D Audio Power Amplifier

1 Features

- Output Power By Package:
  - WQFN:
    - 2.1 W/Ch Into 4 Ω at 5 V
    - 1.4 W/Ch Into 8 Ω at 5 V
    - 720 mW/Ch Into 8 Ω at 3.6 V
  - DSBGA:
    - 1.2 W/Ch Into 4 Ω at 5 V (Thermally Limited)
    - 1.3 W/Ch Into 8 Ω at 5 V
    - 720 mW/Ch Into 8 Ω at 3.6 V
- Only Two External Components Required
- Power Supply Range: 2.5 V to 5.5 V
- Independent Shutdown Control for Each Channel
- Selectable Gain of 6, 12, 18, and 24 dB
- Internal Pulldown Resistor on Shutdown Pins
- High PSRR: 77 dB at 217 Hz
- Fast Start-Up Time (3.5 ms)
- Low Supply Current
- Low Shutdown Current
- Short-Circuit and Thermal Protection
- Space-Saving Packages
  - 2.01-mm × 2.01-mm NanoFree™ DSBGA (YZH)
  - 4-mm × 4-mm Thin WQFN (RTJ) With PowerPAD™

2 Applications

- Wireless or Cellular Handsets and PDAs
- Portable DVD Players
- Notebook PCs
- Portable Radios
- Portable Gaming
- Educational Toys
- USB Speakers

3 Description

The TPA2012D2 is a stereo, filter-free, Class-D audio amplifier (Class-D amp) available in a DSBGA or WQFN package. The TPA2012D2 only requires two external components for operation.

The TPA2012D2 features independent shutdown controls for each channel. The gain can be selected to 6, 12, 18, or 24 dB using the G0 and G1 gain select pins. High PSRR and differential architecture provide increased immunity to noise and RF rectification. In addition to these features, a fast start-up time and small package size make the TPA2012D2 class-D amp an ideal choice for both cellular handsets and PDAs.

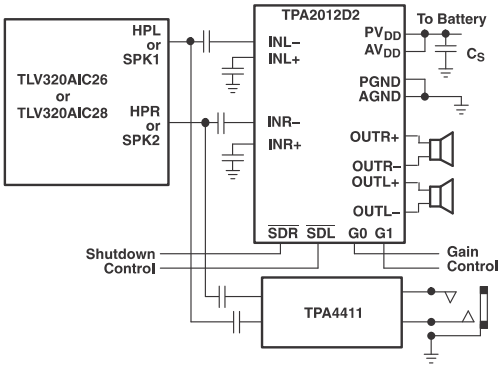
The TPA2012D2 is capable of driving 1.4 W/Ch at 5 V or 720 mW/Ch at 3.6 V into 8 Ω. The TPA2012D2 is also capable of driving 4 Ω. The TPA2012D2 is thermally limited in DSBGA and may not achieve 2.1 W/Ch for 4 Ω. The maximum output power in the DSBGA is determined by the ability of the circuit board to remove heat. Figure 33 shows thermally limited region of the DSBGA in relation to the WQFN package. The TPA2012D2 provides thermal and short-circuit protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA2012D2	DSBGA (16)	2.01 mm × 2.01 mm
	WQFN (20)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2016) to Revision F	Page
• Switched the BODY SIZE values in the *Device Information* table: DSBGA From: 4.00 mm × 4.00 mm To: 2.01 mm × 2.01 mm and WQFN From: 2.01 mm × 2.01 mm To: 4.00 mm × 4.00 mm	1

Changes from Revision D (June 2008) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted Available-Options table; see POA at the end of the data sheet	1
• Deleted previous application schematics: Typical Application Circuit (previously Figure 33), TPA2012D2 Application Schematic With Differential Input and Input Capacitors (previously Figure 34), and TPA2012D2 Application Schematic With Single-Ended Input (previously Figure 35)	16

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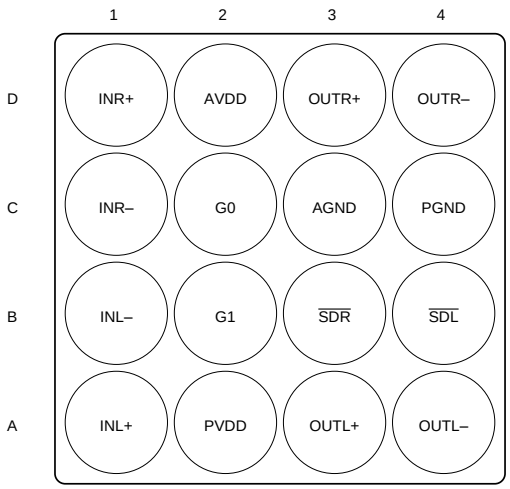
5 Device Comparison Table

DEVICE NO.	SPEAKER AMP TYPE	SPECIAL FEATURE	OUTPUT POWER (M)	PSRR (dB)
TPA2012D2	Class D	—	2.1	71
TPA2016D2	Class D	AGC/DRC	2.8	80
TPA2026D2	Class D	AGC/DRC	3.2	80

6 Pin Configuration and Functions

YZH Package
16-Pin DSBGA
Top View



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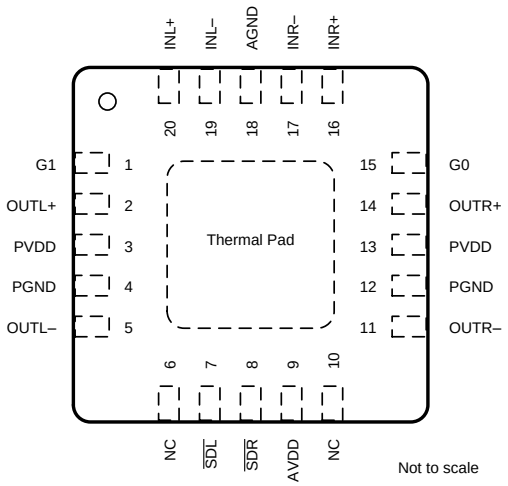
RTJ Package
20-Pin WQFN
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	DSBGA	WQFN		
AGND	C3	18	I	Analog ground
AVDD	D2	9	I	Analog supply (must be same voltage as PVDD)
G0	C2	15	I	Gain select (LSB)
G1	B2	1	I	Gain select (MSB)
INL–	B1	19	I	Left channel negative input
INL+	A1	20	I	Left channel positive input
INR–	C1	17	I	Right channel negative input
INR+	D1	16	I	Right channel positive input
NC	—	6, 10	—	No internal connection
OUTL–	A4	5	O	Left channel negative differential output
OUTL+	A3	2	O	Left channel positive differential output
OUTR–	D4	11	O	Right channel negative differential output
OUTR+	D3	14	O	Right channel positive differential output
PGND	C4	4, 12	I	Power ground
PVDD	A2	3, 13	I	Power supply (must be same voltage as AVDD)
$\overline{\text{SDL}}$	B4	7	I	Left channel shutdown terminal (active low)
$\overline{\text{SDR}}$	B3	8	I	Right channel shutdown terminal (active low)
Thermal Pad	—	—	—	Connect the thermal pad of WQFN package to PCB GND

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_{SS} (AVDD, PVDD)	Active mode	–0.3	6	V
	Shutdown mode	–0.3	7	
Input voltage, V_I		–0.3	V_{DD} + 0.3	V
Continuous total power dissipation		See *Dissipation Rating Table*		
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{SS}	Supply voltage, AVDD, PVDD	2.5	5.5	V
V_{IH}	High-level input voltage, $\overline{SDL}$, $\overline{SDR}$, G0, G1	1.3		V
V_{IL}	Low-level input voltage, $\overline{SDL}$, $\overline{SDR}$, G0, G1		0.35	V
T_A	Operating free-air temperature	–40	85	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPA2012D2		UNIT
		YZH (DSBGA)	RTJ (WQFN)	
		16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.4	34.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.3	11.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	Inputs ac grounded, A_V = 6 dB, V_{DD} = 2.5 to 5.5 V			5	25	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 to 5.5 V			–75	–55	dB
V_{icm}	Common-mode input voltage			0.5		V_{DD} – 0.8	V
CMRR	Common-mode rejection ration	Inputs shorted together, V_{DD} = 2.5 to 5.5 V			–69	–50	dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, V_I = V_{DD}				50	µA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V				5	µA
I_{DD}	Supply current	V_{DD} = 5.5 V, no load or output filter			6	9	mA
		V_{DD} = 3.6 V, no load or output filter			5	7.5	
		V_{DD} = 2.5 V, no load or output filter			4	6	
		Shutdown mode				1.5	µA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{DD} = 5.5 V			500		mΩ
		V_{DD} = 3.6 V			570		
		V_{DD} = 2.5 V			700		
	Output impedance in shutdown mode	$V_{(\overline{SDR}, \overline{SDL})}$= 0.35 V			2		kΩ
$f_{(sw)}$	Switching frequency	V_{DD} = 2.5 V to 5.5 V		250	300	350	kHz
	Closed-loop voltage gain	G0, G1 = 0.35 V		5.5	6	6.5	dB
		G0 = V_{DD}, G1 = 0.35 V		11.5	12	12.5	
		G0 = 0.35 V, G1 = V_{DD}		17.5	18	18.5	
		G0, G1 = V_{DD}		23.5	24	24.5	
OPERATING CHARACTERISTICS, R_L = 8 Ω							
P_O	Output power (per channel)	R_L = 8 Ω	V_{DD} = 5 V, f = 1 kHz, THD = 10%		1.4		W
			V_{DD} = 3.6 V, f = 1 kHz, THD = 10%		0.72		
		R_L = 4 Ω	V_{DD} = 5 V, f = 1 kHz, THD = 10%		2.1		
THD+N	Total harmonic distortion plus noise	P_O = 1 W, V_{DD} = 5 V, A_V = 6 dB, f = 1 kHz			0.14%		
		P_O = 0.5 W, V_{DD} = 5 V, A_V = 6 dB, f = 1 kHz			0.11%		
	Channel crosstalk	f = 1 kHz			–85		dB
k_{SVR}	Supply ripple rejection ratio	V_{DD} = 5 V, A_V = 6 dB, f = 217 Hz			–77		dB
		V_{DD} = 3.6 V, A_V = 6 dB, f = 217 Hz			–73		
CMRR	Common mode rejection ratio	V_{DD} = 3.6 V, V_{IC} = 1 V_{pp}, f = 217 Hz			–69		dB
	Input impedance	Av = 6 dB			28.1		kΩ
		Av = 12 dB			17.3		
		Av = 18 dB			9.8		
		Av = 24 dB			5.2		
	Start-up time from shutdown	V_{DD} = 3.6 V			3.5		ms
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 to 20 kHz, inputs are ac grounded, A_V = 6 dB	No weighting		35		µV
			A weighting		27		

7.6 Dissipation Rating Table

PACKAGE	T_A = 25°C POWER RATING (1)	DERATING FACTOR	T_A = 75°C POWER RATING	T_A = 85°C POWER RATING
RTJ	5.2 W	41.6 mW/°C	3.12 W	2.7 W
YZH	1.2 W	9.12 mW/°C	690 mW	600 mW

(1) This data was taken using 2-oz trace and copper pad that is soldered directly to a JEDEC standard 4-layer 3 in × 3 in PCB.

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7.7 Typical Characteristics

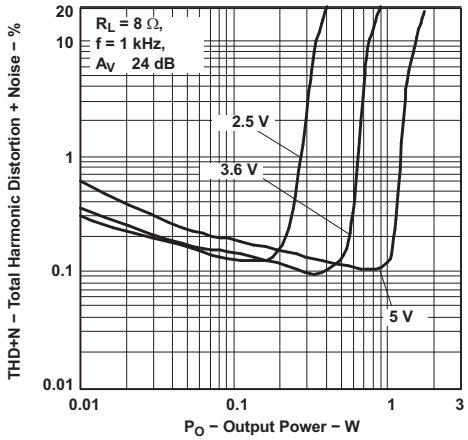

Figure 1. Total Harmonic Distortion vs Output Power

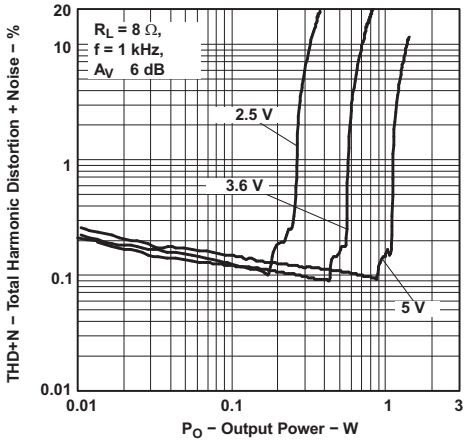

Figure 2. Total Harmonic Distortion vs Output Power

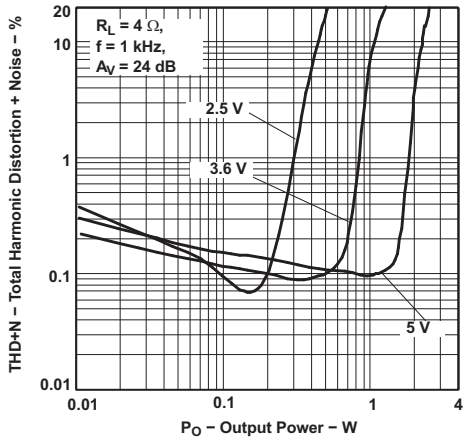

Figure 3. Total Harmonic Distortion vs Output Power

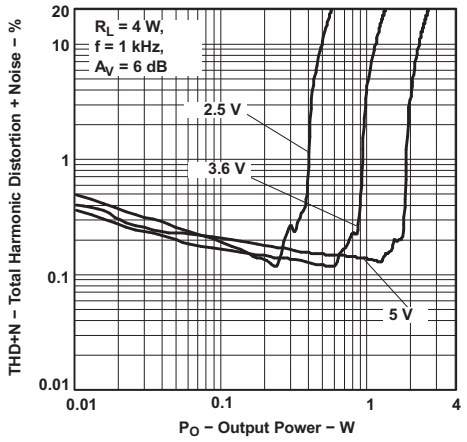

Figure 4. Total Harmonic Distortion vs Output Power

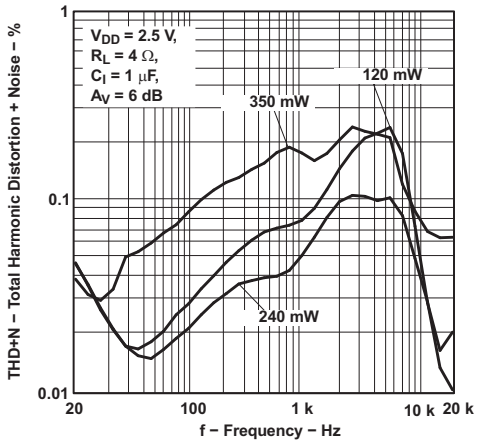

Figure 5. Total Harmonic Distortion vs Frequency

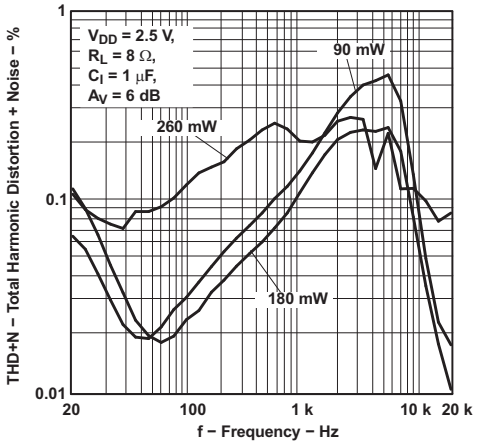

Figure 6. Total Harmonic Distortion vs Frequency

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Typical Characteristics (continued)

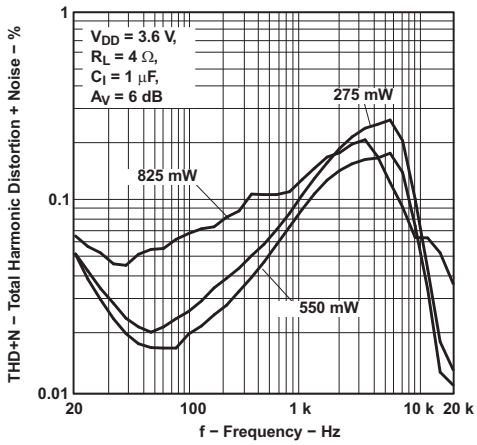

Figure 7. Total Harmonic Distortion vs Frequency

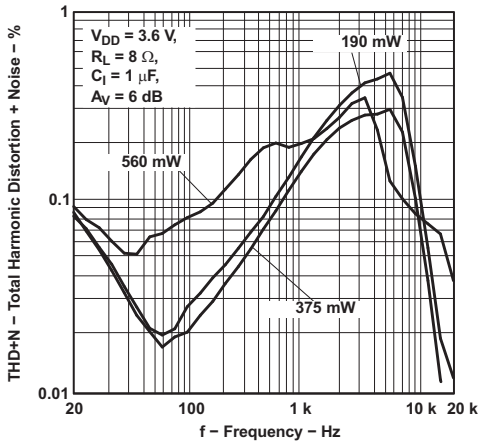

Figure 8. Total Harmonic Distortion vs Frequency

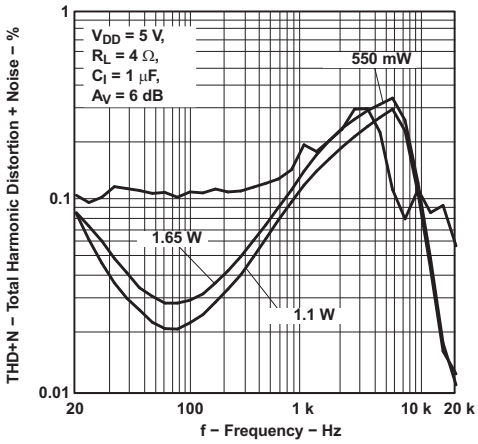

Figure 9. Total Harmonic Distortion vs Frequency

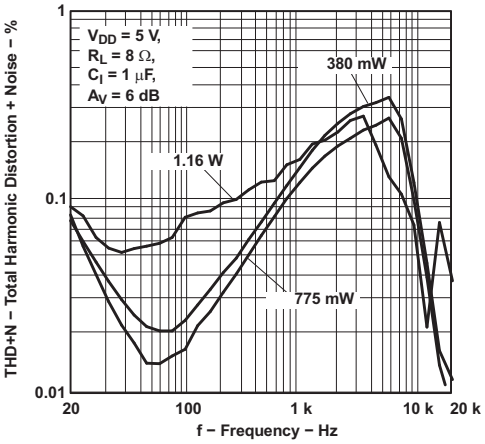

Figure 10. Total Harmonic Distortion vs Frequency

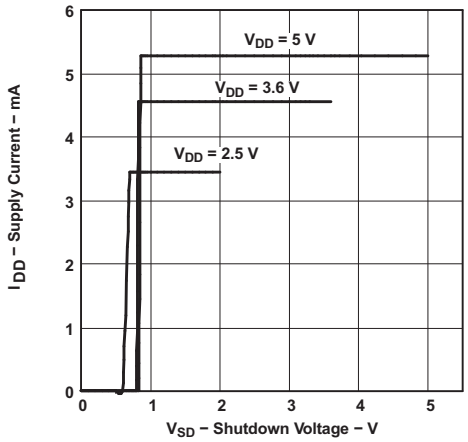

Figure 11. Supply Current vs Shutdown Voltage

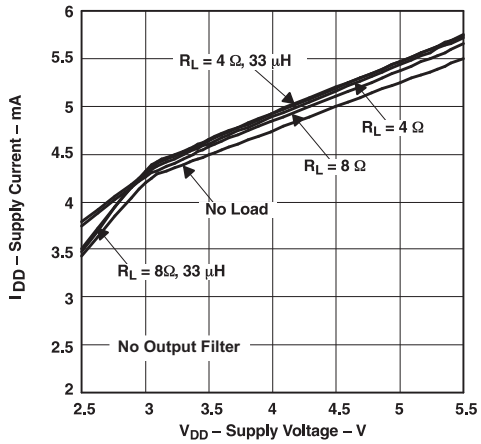

Figure 12. Supply Current vs Supply Voltage

Typical Characteristics (continued)

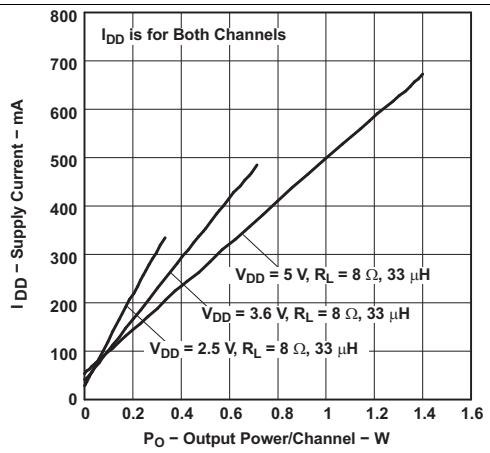

Figure 13. Supply Current vs Output Power

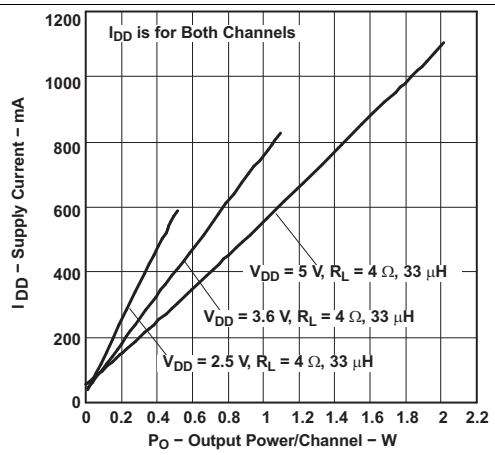

Figure 14. Supply Current vs Output Power

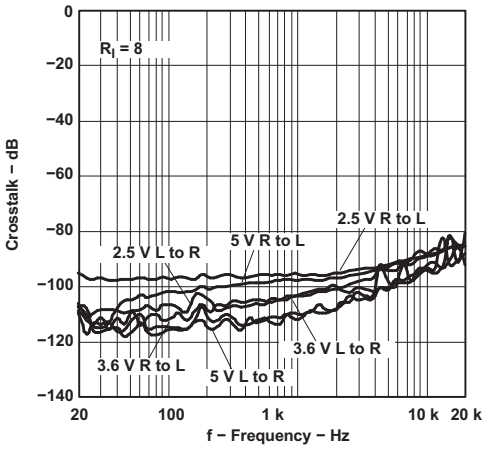

Figure 15. Crosstalk vs Frequency

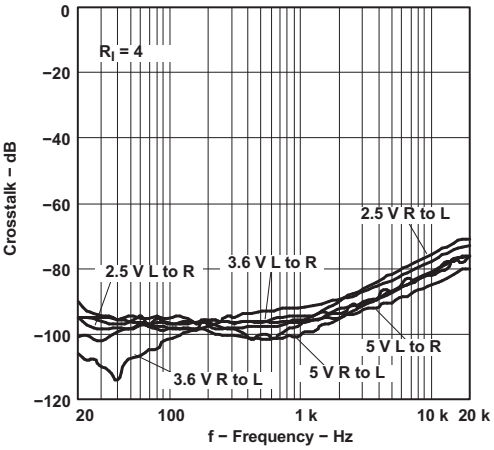

Figure 16. Crosstalk vs Frequency

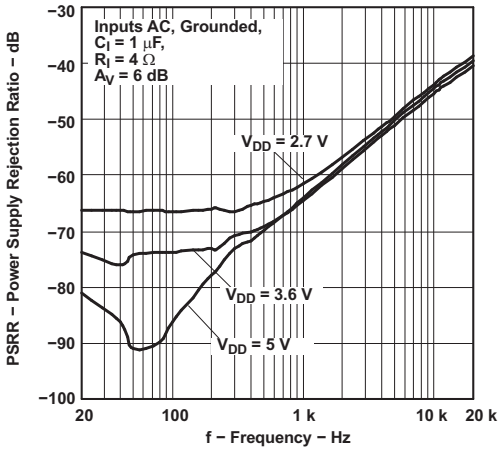

Figure 17. Power Supply Rejection Ratio vs Frequency

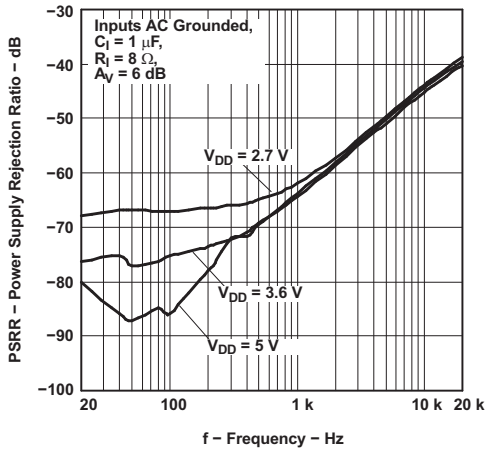

Figure 18. Power Supply Rejection Ratio vs Frequency

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Typical Characteristics (continued)

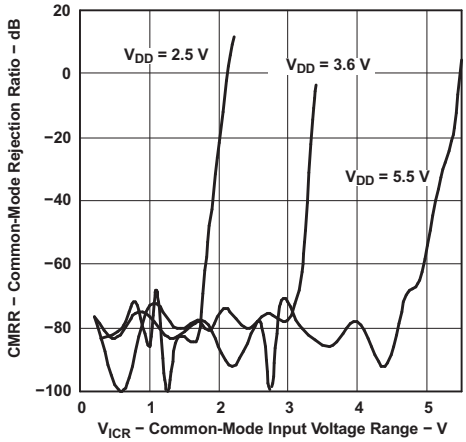

Figure 19. Common-Mode Rejection Ratio vs Common-Mode Input Voltage

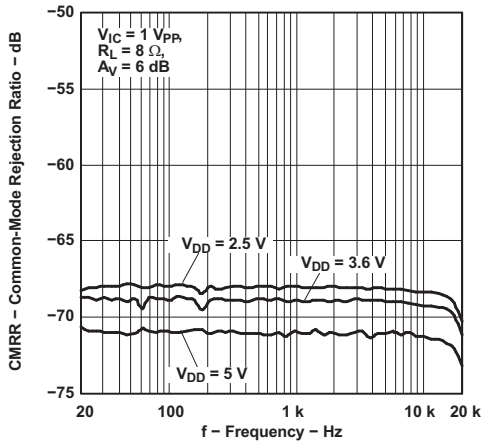

Figure 20. Common-Mode Rejection Ratio vs Frequency

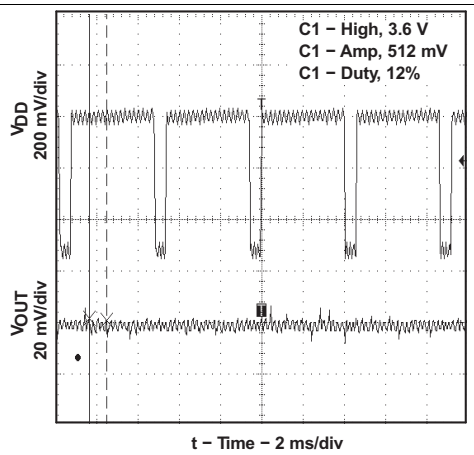

Figure 21. GSM Power Supply Rejection vs Time

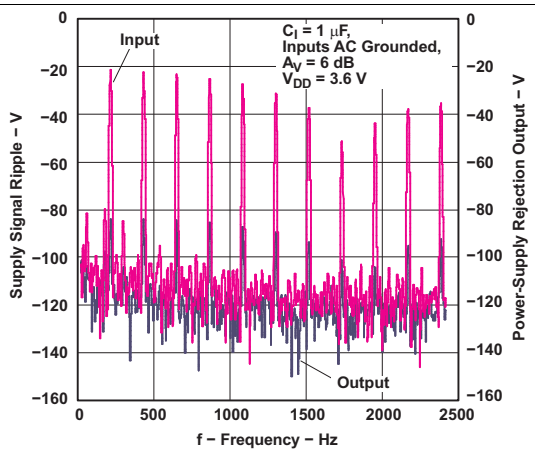

Figure 22. Power Supply Rejection vs Frequency

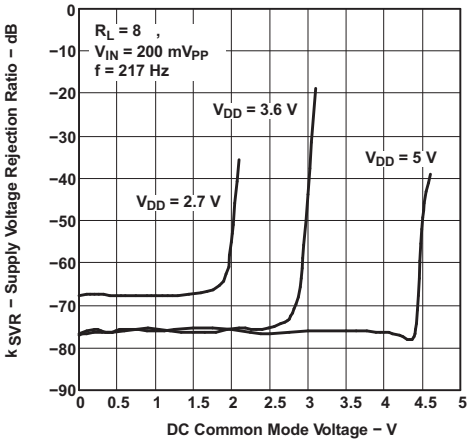

Figure 23. Supply Voltage Rejection Ratio vs DC Common-Mode Voltage

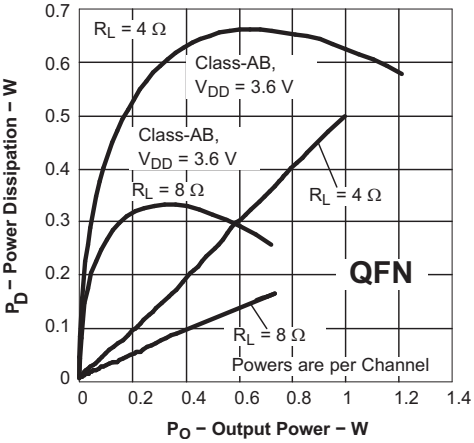

Figure 24. Power Dissipation vs Output Power

Typical Characteristics (continued)

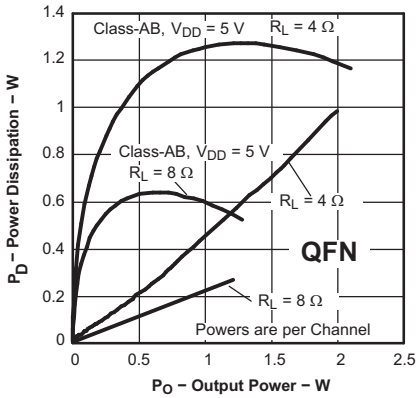

Figure 25. Power Dissipation vs Output Power

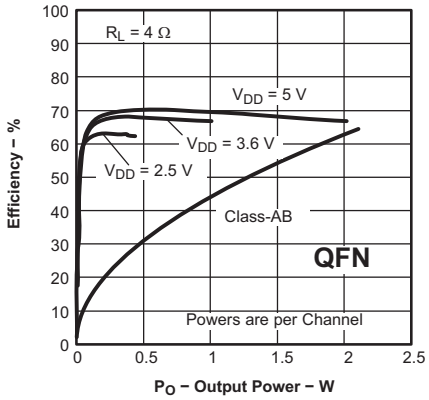

Figure 26. Efficiency vs Output Power

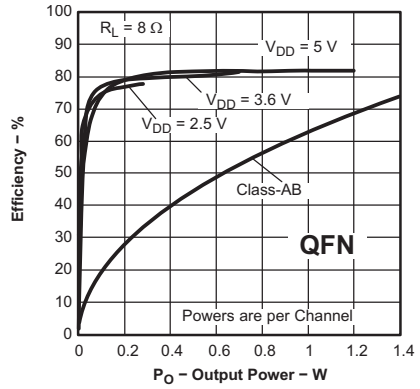

Figure 27. Efficiency vs Output Power

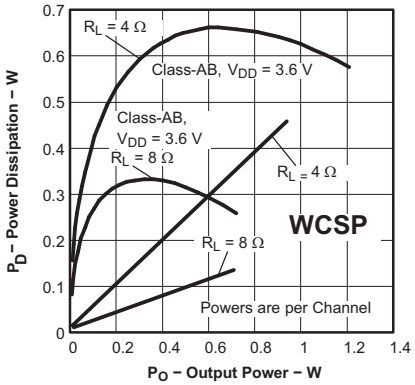

Figure 28. Power Dissipation vs Output Power

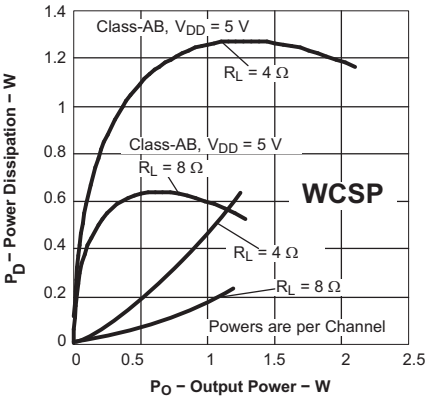

Figure 29. Power Dissipation vs Output Power

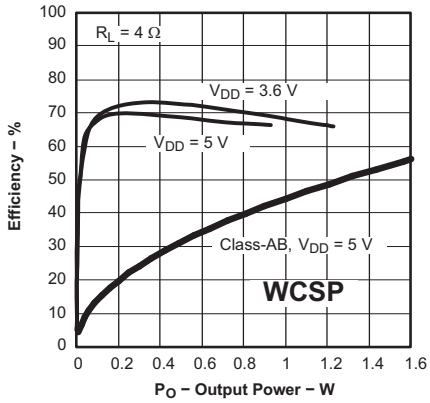

Figure 30. Efficiency vs Output Power

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Typical Characteristics (continued)

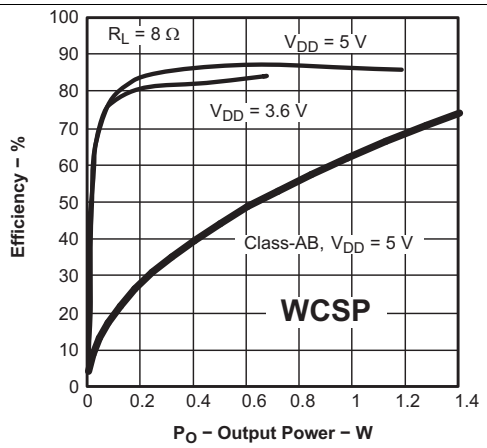


Figure 31. Efficiency vs Output Power

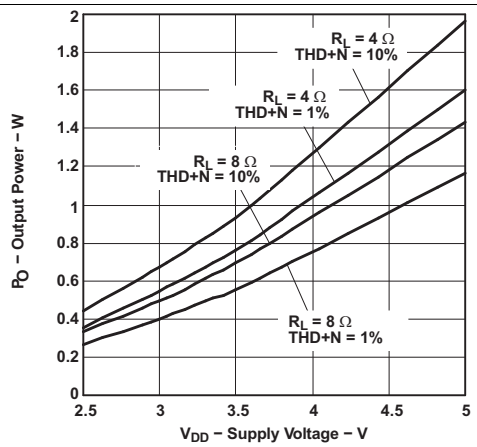


Figure 32. Output Power vs Supply Voltage

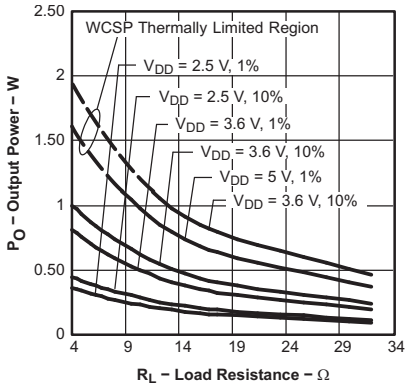
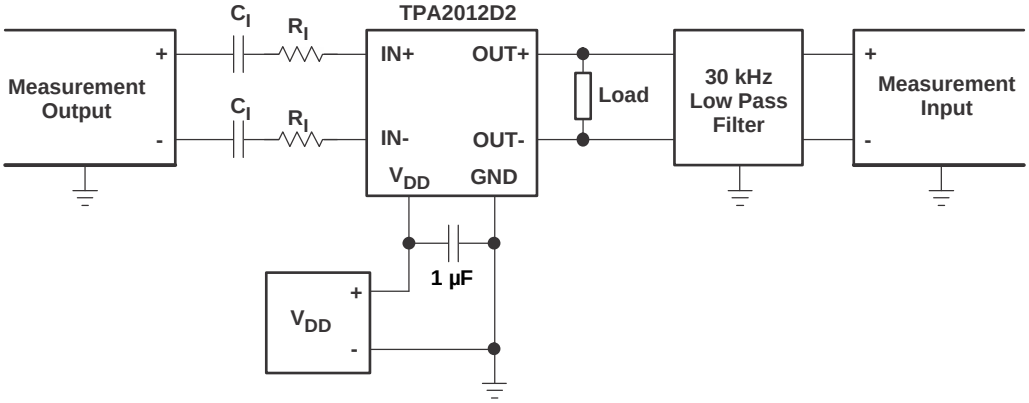


Figure 33. Output Power vs Load Resistance

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications*. Figure 34 shows the setup used for the typical characteristics of the test device.



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(1) C_I was shorted for any common-mode input voltage measurement.

(2) A 33-µH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

(3) The 30-kHz low-pass filter is required even if the analyzer has an internal low-pass filter. An RC low-pass filter (100 Ω, 47 nF) is used on each output for the data sheet graphs.

Figure 34. Test Setup For Graphs (Per Channel)

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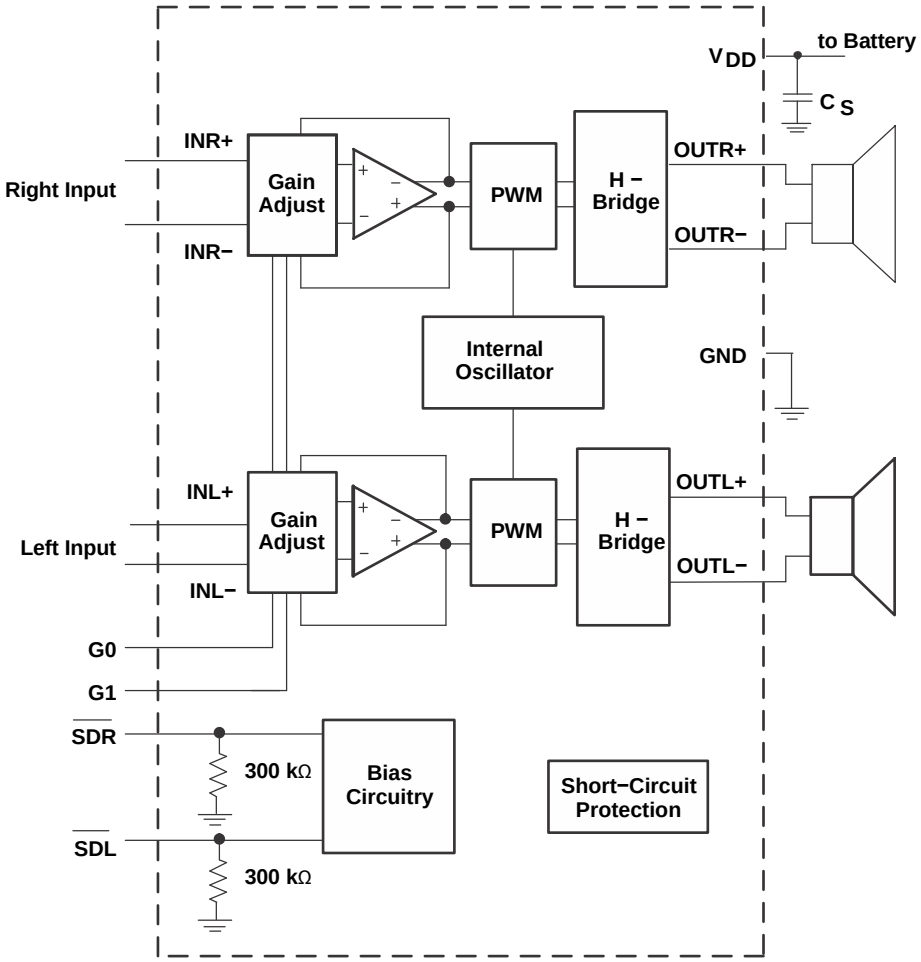
9 Detailed Description

9.1 Overview

The TPA2012D2 is capable of driving 1.4 W/Ch at 5-V or 720 mW/Ch at 3.6-V into 8 Ω. The TPA2012D2 is also capable of driving a load of 4 Ω.

The TPA2012D2 feature independent shutdown controls for each channel. High PSRR and differential architecture provide increased immunity to noise and RF rectification. The TPA2012D2 provides thermal and short-circuit protection.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Fixed Gain Setting

The TPA2012D2 has 4 selectable fixed gains: 6 dB, 12 dB, 18 dB, and 24 dB. Connect the G0 and G1 pins as shown in Table 1.

Table 1. Gain Setting

G1	G0	GAIN (V/V)	GAIN (dB)	INPUT IMPEDANCE (R_I, kΩ)
0	0	2	6	28.1
0	1	4	12	17.3
1	0	8	18	9.8
1	1	16	24	5.2

9.3.2 Short-Circuit Protection

TPA2012D2 goes to low duty cycle mode when a short-circuit event happens. To return to normal duty cycle mode, the device must be reset. The shutdown mode can be set through the SDL and SDR pins, or the device can be turned off and turned on to return to normal duty cycle mode. This feature protects the device without affecting long-term reliability.

9.3.3 Operation With DACs and CODECs

In using Class-D amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when mixing of the output frequencies of the CODEC and DAC mix with the switching frequencies of the audio amplifier input stage. The noise increase can be solved by placing a low-pass filter between the CODEC, DAC, and audio amplifier. This filters off the high frequencies that cause the problem and allow proper performance. The recommended resistor value is 100 Ω and the capacitor value of 47 nF. Figure 35 shows the typical input filter.

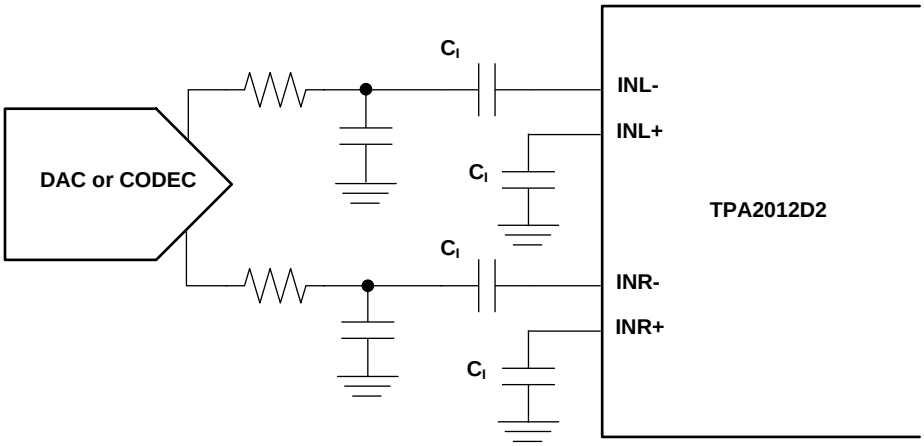

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Figure 35. Reducing Out-of-Band DAC Noise With External Input Filter

9.3.4 Filter-Free Operation and Ferrite Bead Filters

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and very low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 36 shows typical ferrite bead and LC output filters.

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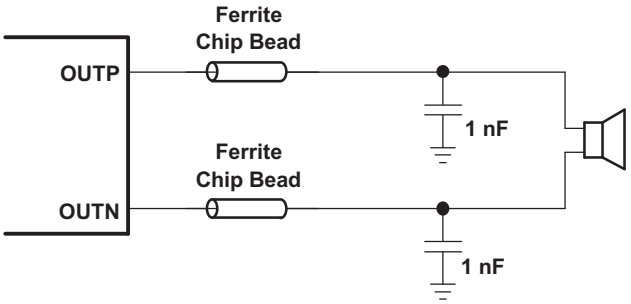

Figure 36. Typical Ferrite Chip Bead Filter (Chip Bead Example: TDK – MPZ1608S221A)

9.4 Device Functional Modes

9.4.1 Shutdown Mode

The TPA2012D2 amplifier can be put in shutdown mode when asserting SDR and SDL pins to a logic LOW. While in shutdown mode, the device output stage is turned off and the current consumption is very low.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device. Each of these configurations can be realized using the evaluation modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.2 Typical Applications

10.2.1 TPA2012D2 With Differential Input Signal

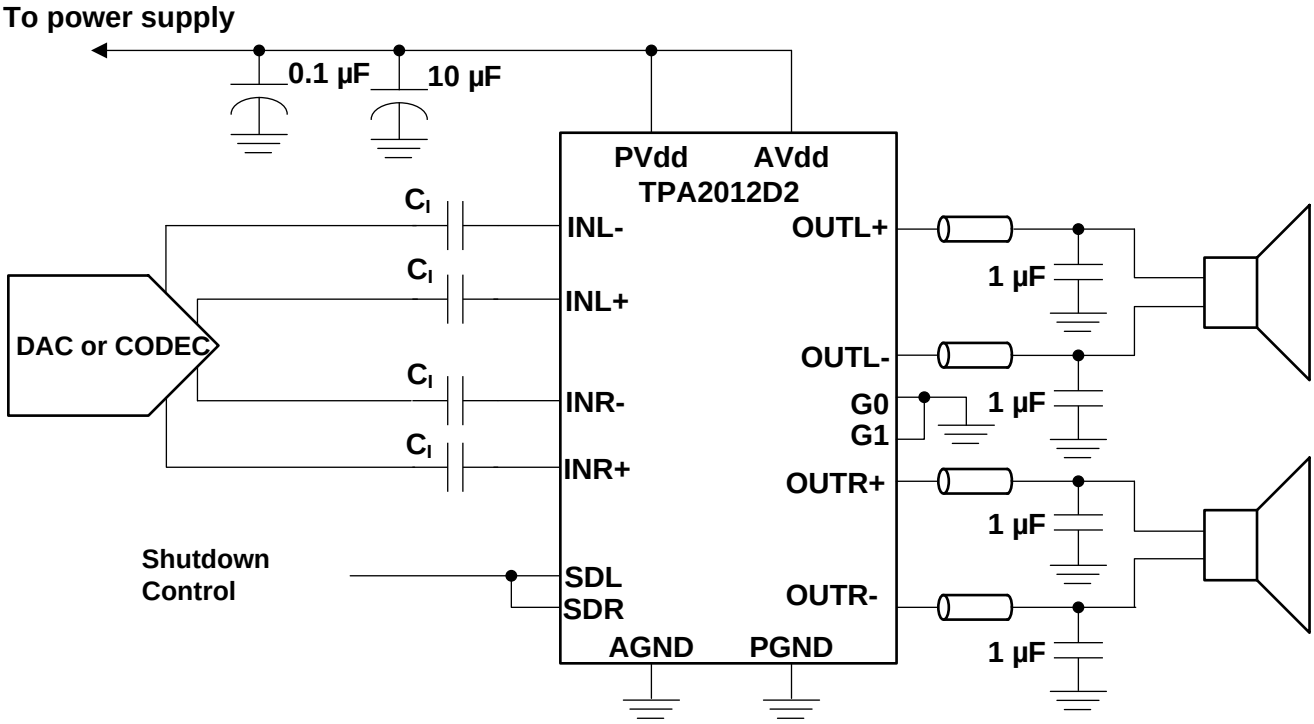

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Figure 37. Typical Application Schematic With Differential Input Signals

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Typical Applications (continued)

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
Power supply	5 V
Enable inputs	High > 1.3 V
	Low < 0.35 V
Speaker	8 Ω

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Surface Mount Capacitors

Temperature and applied DC voltage influence the actual capacitance of high-K materials. Table 3 shows the relationship between the different types of high-K materials and their associated tolerances, temperature coefficients, and temperature ranges. Notice that a capacitor made with X5R material can lose up to 15% of its capacitance within its working temperature range.

In an application, the working capacitance of components made with high-K materials is generally much lower than nominal capacitance. A worst-case result with a typical X5R material might be –10% tolerance, –15% temperature effect, and –45% DC voltage effect at 50% of the rated voltage. This particular case would result in a working capacitance of 42% (0.9 × 0.85 × 0.55) of the nominal value.

Select high-K ceramic capacitors according to the following rules:

1. Use capacitors made of materials with temperature coefficients of X5R, X7R, or better.
2. Use capacitors with DC voltage ratings of at least twice the application voltage. Use minimum 10-V capacitors for the TPA2012D2.
3. Choose a capacitance value at least twice the nominal value calculated for the application. Multiply the nominal value by a factor of 2 for safety. If a 10-µF capacitor is required, use 20 µF.

The preceding rules and recommendations apply to capacitors used in connection with the TPA2012D2. The TPA2012D2 cannot meet its performance specifications if the rules and recommendations are not followed.

Table 3. Typical Tolerance and Temperature Coefficient of Capacitance by Material

MATERIAL	COG/NPO	X7R	X5R
Typical tolerance	±5%	±10%	80% to –20%
Temperature	±30 ppm	±15%	22% to –82%
Temperature range (°C)	–55°C to 125°C	–55°C to 125°C	–30°C to 85°C

10.2.1.2.2 Decoupling Capacitor (C_S)

The TPA2012D2 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device PV_{DD} lead works best. Placing this decoupling capacitor close to the TPA2012D2 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 4.7 µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

10.2.1.2.3 Input Capacitors (C_I)

The TPA2012D2 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V_{DD} – 0.8 V. If the input signal is not biased within the recommended common-mode input range, if high-pass filtering is needed (see Figure 37), or if using a single-ended source (see Figure 38), input coupling capacitors are required.

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c, determined in Equation 1.

$$f_C = \frac{1}{(2\pi R_I C_I)} \tag{1}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset.

Equation 2 is used to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi R_I f_C)} \tag{2}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

10.2.1.3 Application Curves

For application curves, see the figures listed in Table 4.

Table 4. Table of Graphs

DESCRIPTION	FIGURE NO.(1)
THD+N vs Output power	Figure 1
THD+N vs Frequency	Figure 5
Power dissipation vs Output power	Figure 24
Output power vs Supply voltage	Figure 32

(1) All figure numbers have a hyperlink to a figure in the *Typical Characteristics*.

10.2.2 TPA2012D2 With Single-Ended Input Signal

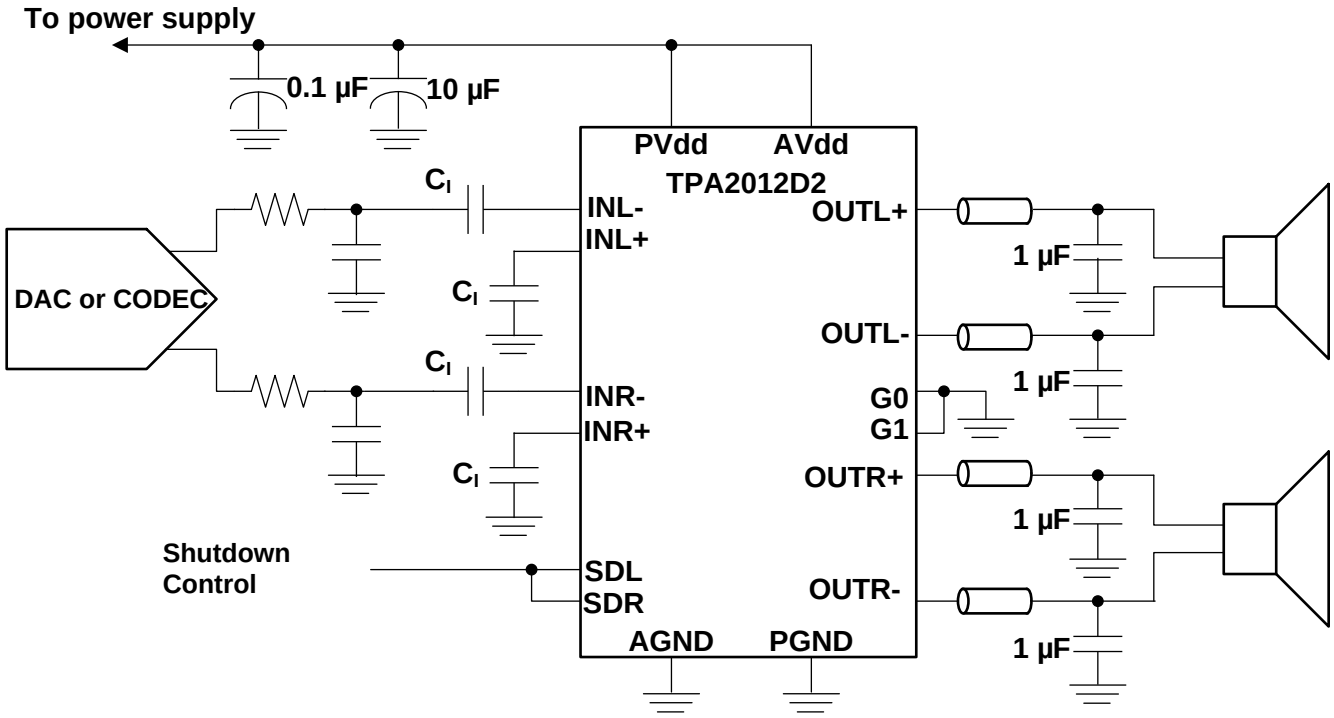

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Figure 38. Typical Application Schematic With Single-Ended Input Signal

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10.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

10.2.2.2 Detailed Design Procedure

For the design procedure, see *Detailed Design Procedure* from the previous example.

10.2.2.3 Application Curves

For application curves, see the figures listed in Table 4.

11 Power Supply Recommendations

The TPA2012D2 is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Therefore, the output voltage range of the power supply must be within this range. The current capability of upper power must not exceed the maximum current limit of the power switch.

11.1 Power Supply Decoupling Capacitor

The TPA2012D2 requires adequate power supply decoupling to ensure a high efficiency operation with low total harmonic distortion (THD). Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1-µF, within 2 mm of the PVDD/AVDD pins. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. In addition to the 0.1-µF ceramic capacitor, TI recommends placing a 2.2-µF to 10-µF capacitor on the PVDD/AVDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

12 Layout

12.1 Layout Guidelines

12.1.1 Pad Side

In making the pad size for the DSBGA balls, TI recommends that the layout use non-solder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 39 and Table 5 shows the appropriate diameters for a DSBGA layout. The TPA2012D2 evaluation module (EVM) layout is shown in the next section as a layout example.

Table 5. Land Pattern Dimensions (1) (2) (3) (4)

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) (7) OPENING	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	275 µm (+0.0, –25 µm)	375 µm (+0.0, –25 µm)	1 oz max (32 µm)	275 µm × 275 µm (square) (rounded corners)	125 µm

(1) Circuit traces from NSMD defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern
(6) Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
(7) Trace routing away from DSBGA device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

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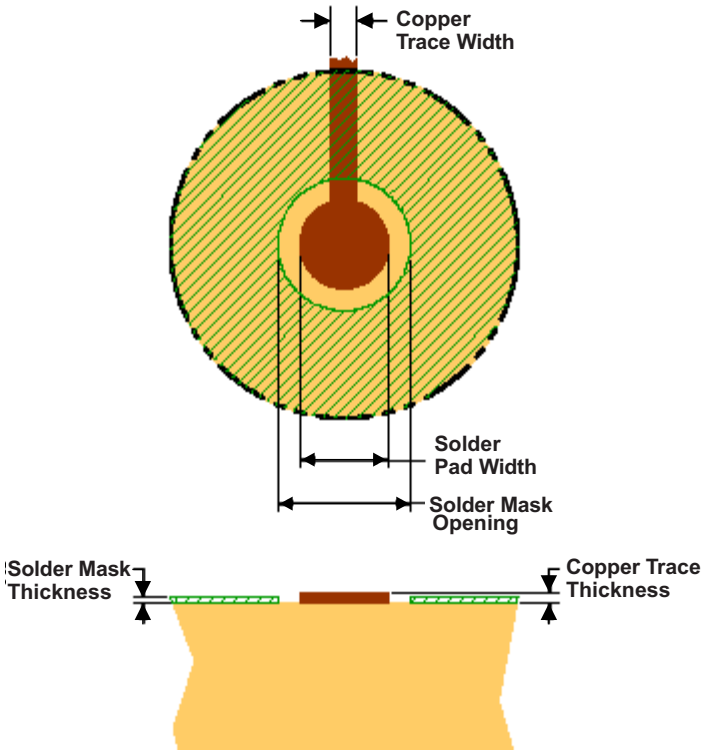

Figure 39. Land Pattern Dimensions

12.1.2 Component Location

Place all the external components very close to the TPA2012D2. Placing the decoupling capacitor, C_S, close to the TPA2012D2 is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

12.1.3 Trace Width

Recommended trace width at the solder balls is 75 µm to 100 µm to prevent solder wicking onto wider PCB traces.

For high current pins (PV_{DD}, PGND, and audio output pins) of the TPA2012D2, use 100-µm trace widths at the solder balls and at least 500-µm PCB traces to ensure proper performance and output power for the device.

For the remaining signals of the TPA2012D2, use 75-µm to 100-µm trace widths at the solder balls. The audio input pins (INR± and INL±) must run side-by-side to maximize common-mode noise cancellation.

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12.2 Layout Examples

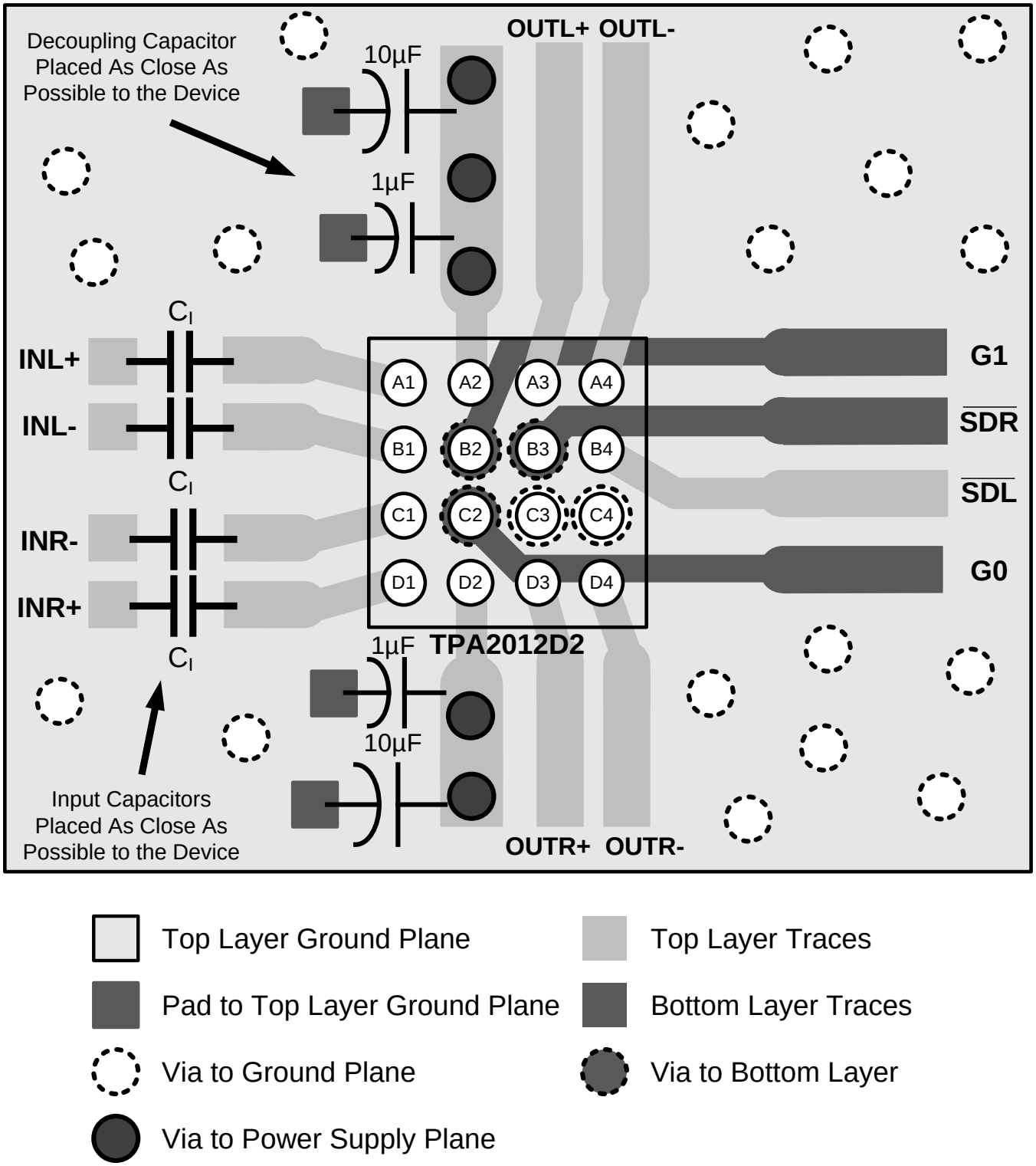
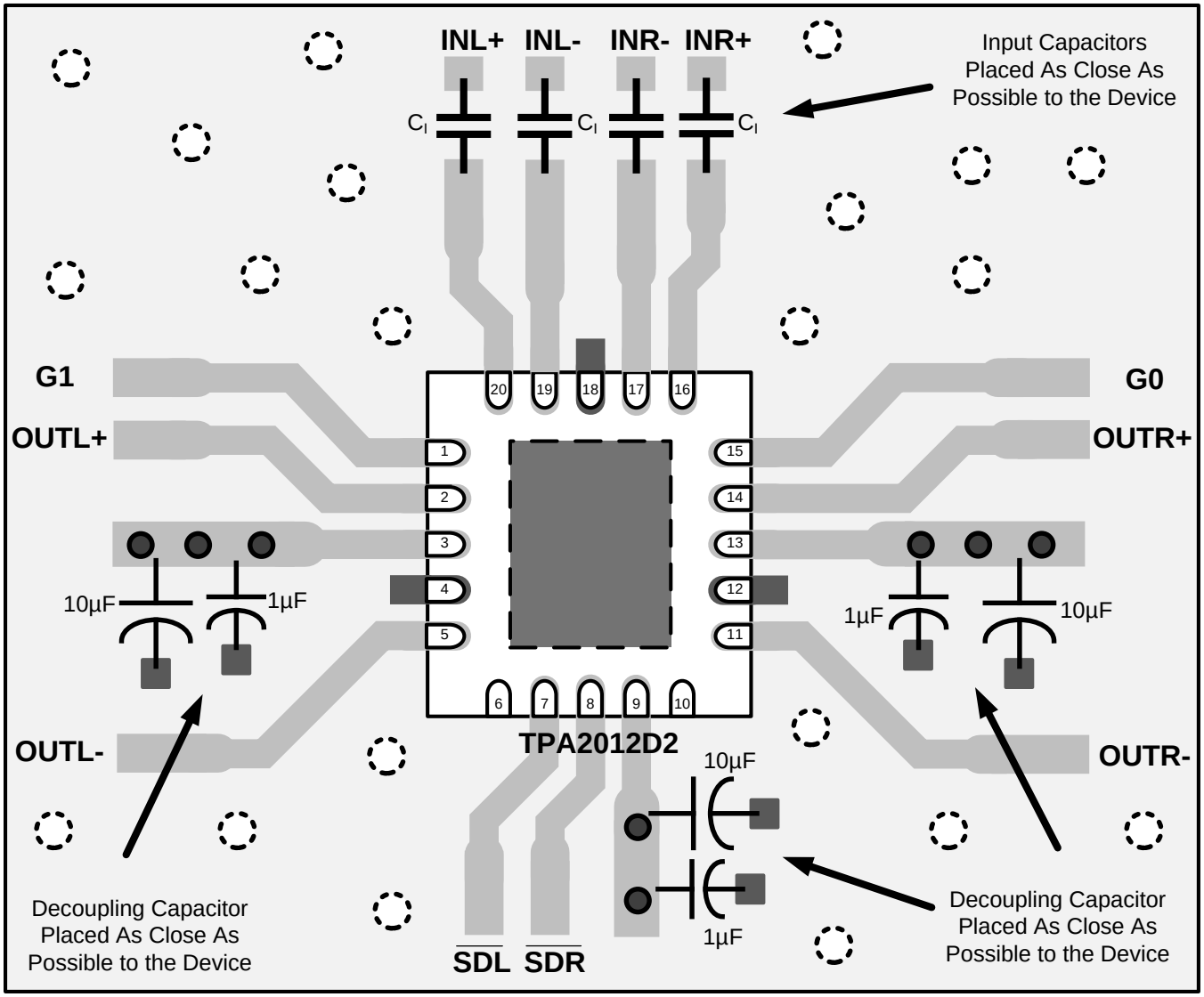


Figure 40. TPA2012D2 DSBGA Layout Example

Layout Examples (continued)



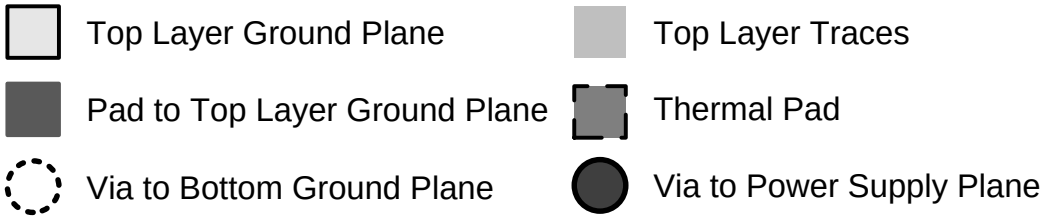


Figure 41. TPA2012D2 WQFN Layout Example

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12.3 Efficiency and Thermal Considerations

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the packages are shown in the dissipation rating table. Converting this to θ_{JA} for the WQFN package with Equation 3.

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.041} = 24°\text{C / W} \tag{3}$$

Given θ_{JA} of 24°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 1.5 W (0.75 W per channel) for 2.1 W per channel, 4-Ω load, 5-V supply, from Figure 25, the maximum ambient temperature can be calculated with Equation 4.

$$T_A\text{Max} = T_J\text{Max} - \theta_{JA}P_{D\,max} = 150 - 24(1.5) = 114°\text{C} \tag{4}$$

Equation 4 shows that the calculated maximum ambient temperature is 114°C at maximum power dissipation with a 5-V supply and a 4-Ω load. The TPA2012D2 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 4-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

NanoFree, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA01081RTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AKS	Samples
TPA2012D2RTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AKS	Samples
TPA2012D2RTJRG4	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AKS	Samples
TPA2012D2RTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AKS	Samples
TPA2012D2RTJTG4	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AKS	Samples
TPA2012D2YZHR	ACTIVE	DSBGA	YZH	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKR	Samples
TPA2012D2YZHT	ACTIVE	DSBGA	YZH	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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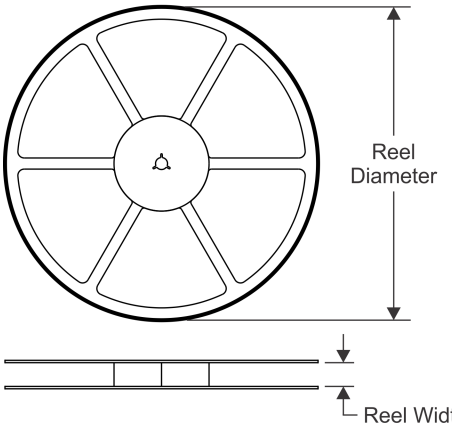
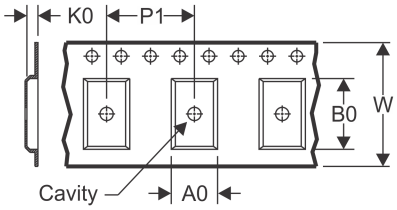
TAPE AND REEL INFORMATION

REEL DIMENSIONS

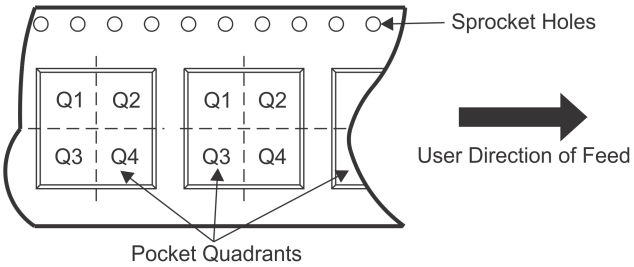


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

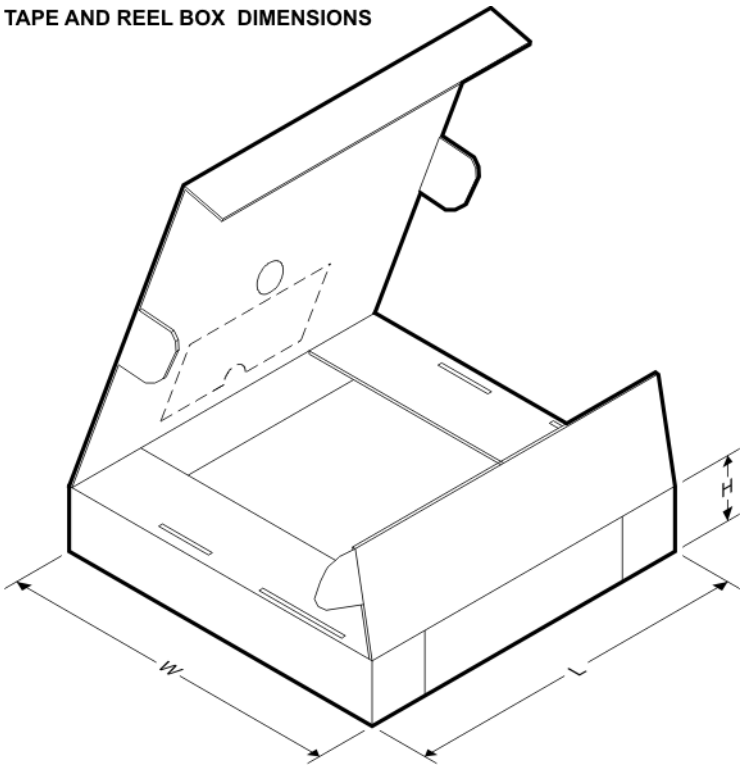
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2012D2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2012D2RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2012D2YZHR	DSBGA	YZH	16	3000	180.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1
TPA2012D2YZHT	DSBGA	YZH	16	250	180.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1

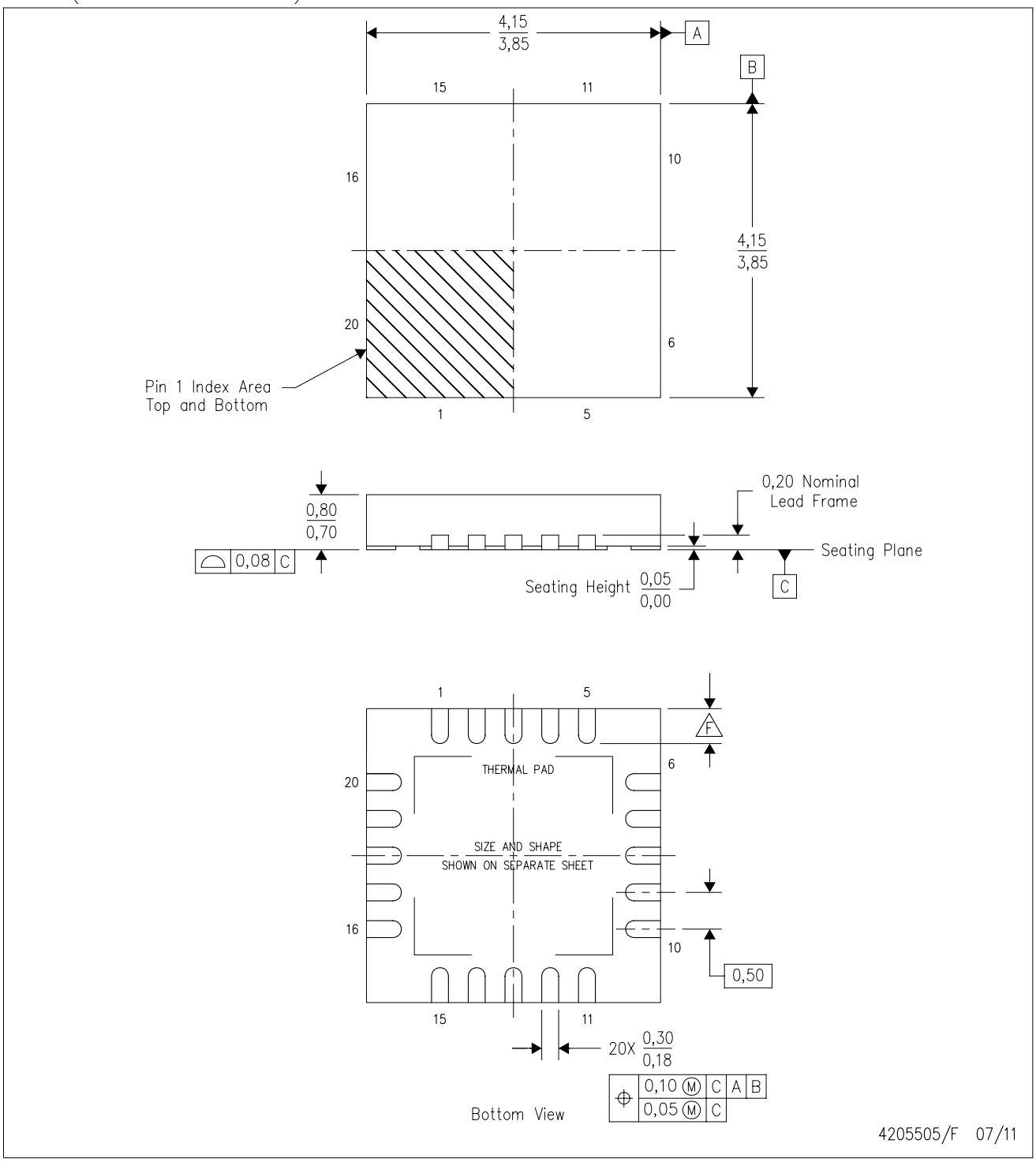
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2012D2RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TPA2012D2RTJT	QFN	RTJ	20	250	210.0	185.0	35.0
TPA2012D2YZHR	DSBGA	YZH	16	3000	182.0	182.0	20.0
TPA2012D2YZHT	DSBGA	YZH	16	250	182.0	182.0	20.0

RTJ (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

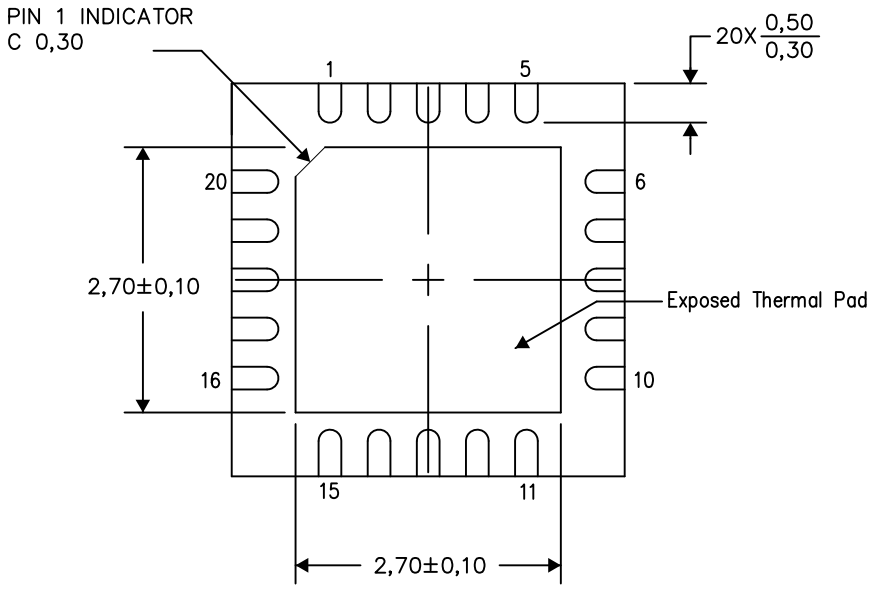
RTJ (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



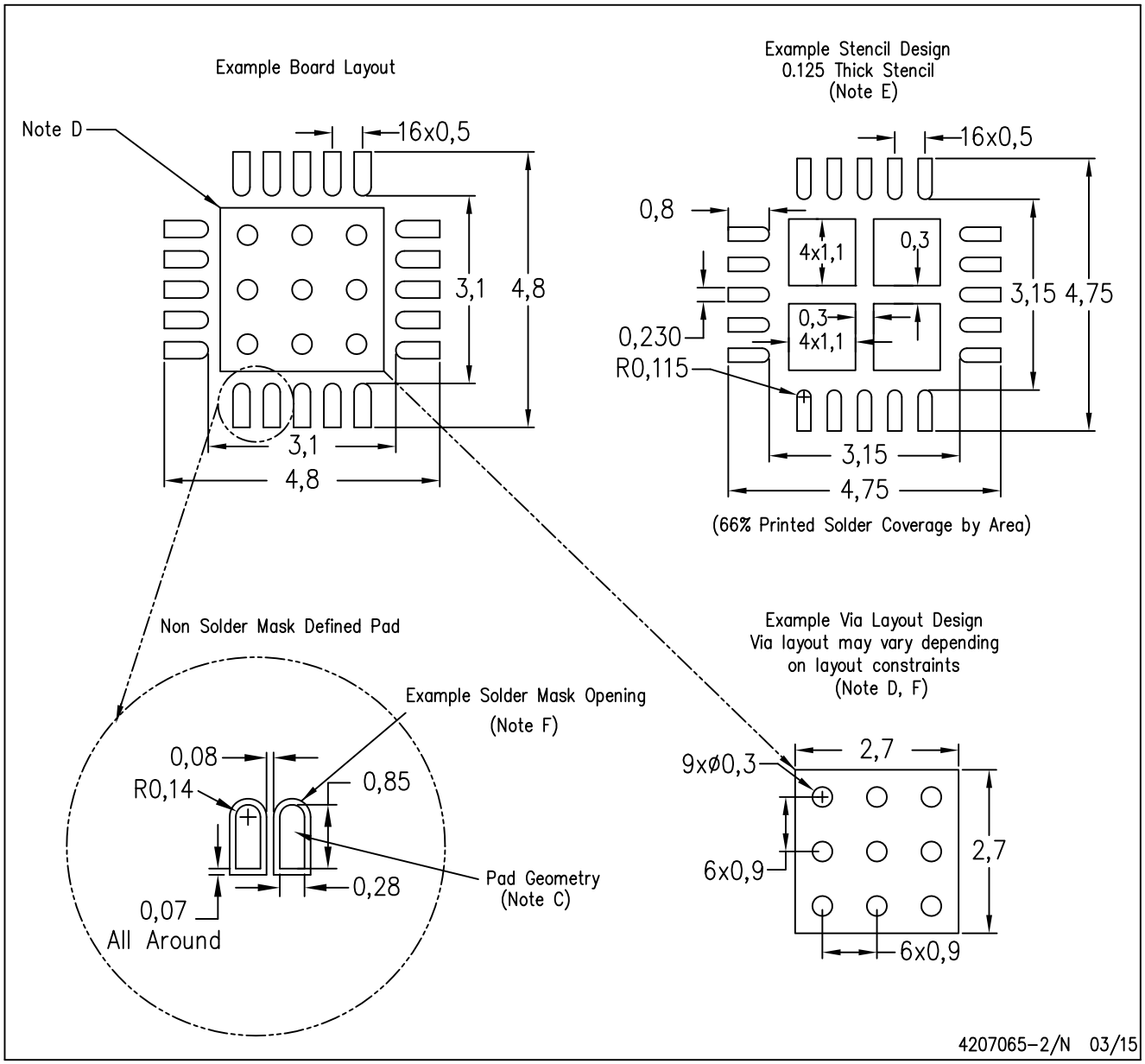
Bottom View

Exposed Thermal Pad Dimensions

4206256-2/V 05/15

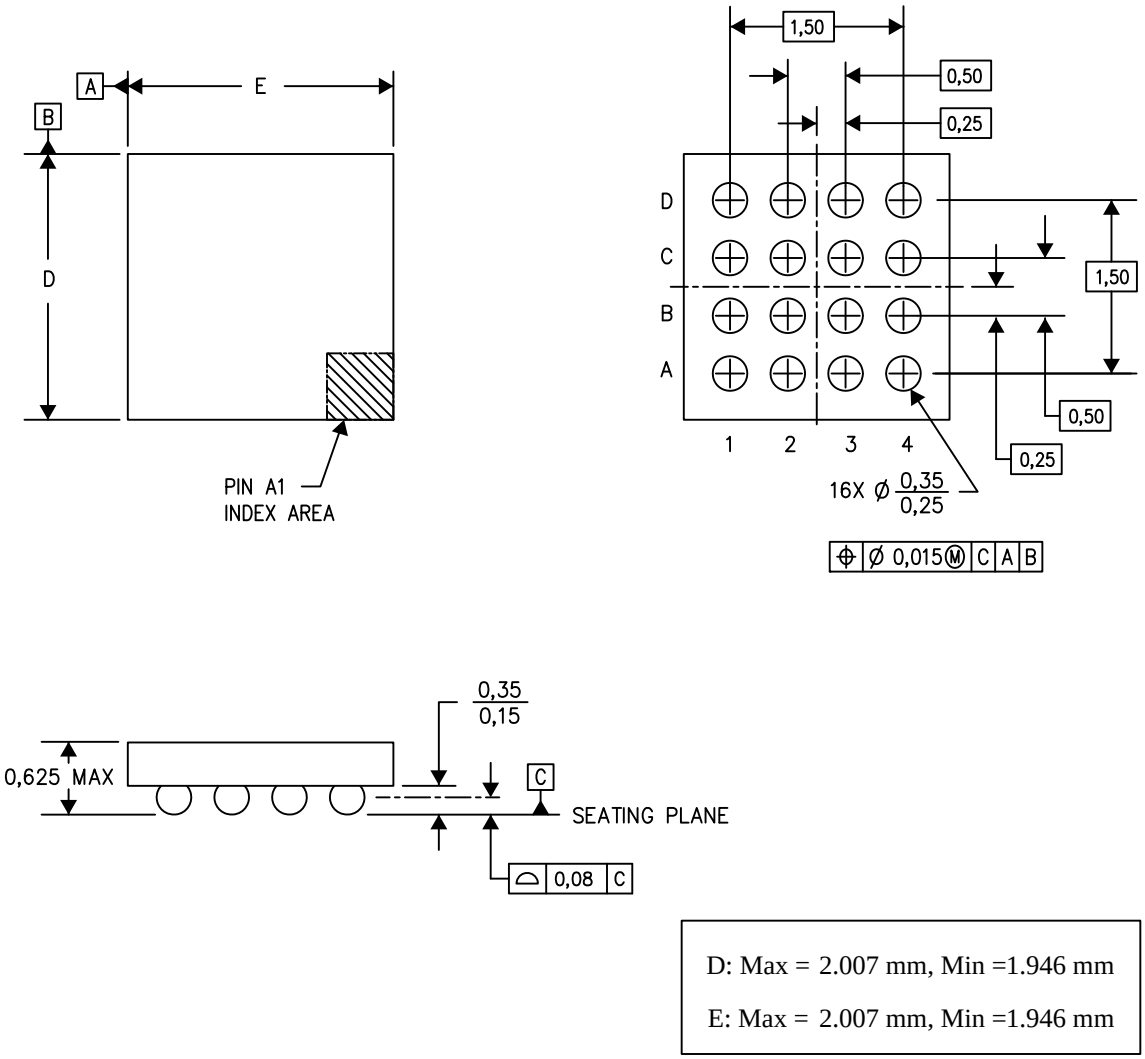
NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YZH (S–XBGA–N16) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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