# VERSATILE BUFFERED REFERENCE IC

## 1. Introduction

In the analog arena, there are some ICs that are extremely versatile, with a number of tools built into one package. The 555 timer comes to mind because it can be configured to perform an amazing range of tasks. As a result, it has found its way into a great variety of end products. As of 2004, one billion were being manufactured every year, making it probably the best-selling IC ever. The LM10 is another good example, as the idea of gain-block plus reference in one package is definitely versatile.

To work with analog signals at super-low supply voltages, something other than a 555 or LM10 is necessary, as these ICs either die out below 4.5 V or draw too much battery current (270 µA for the LM10). Silicon Labs' TS12011 is used in the following circuits to generate some unusual reference voltages for applications where battery current draw is critical. Like an LM10, it contains an op amp plus a reference and, additionally, a comparator (unused in the circuits below).

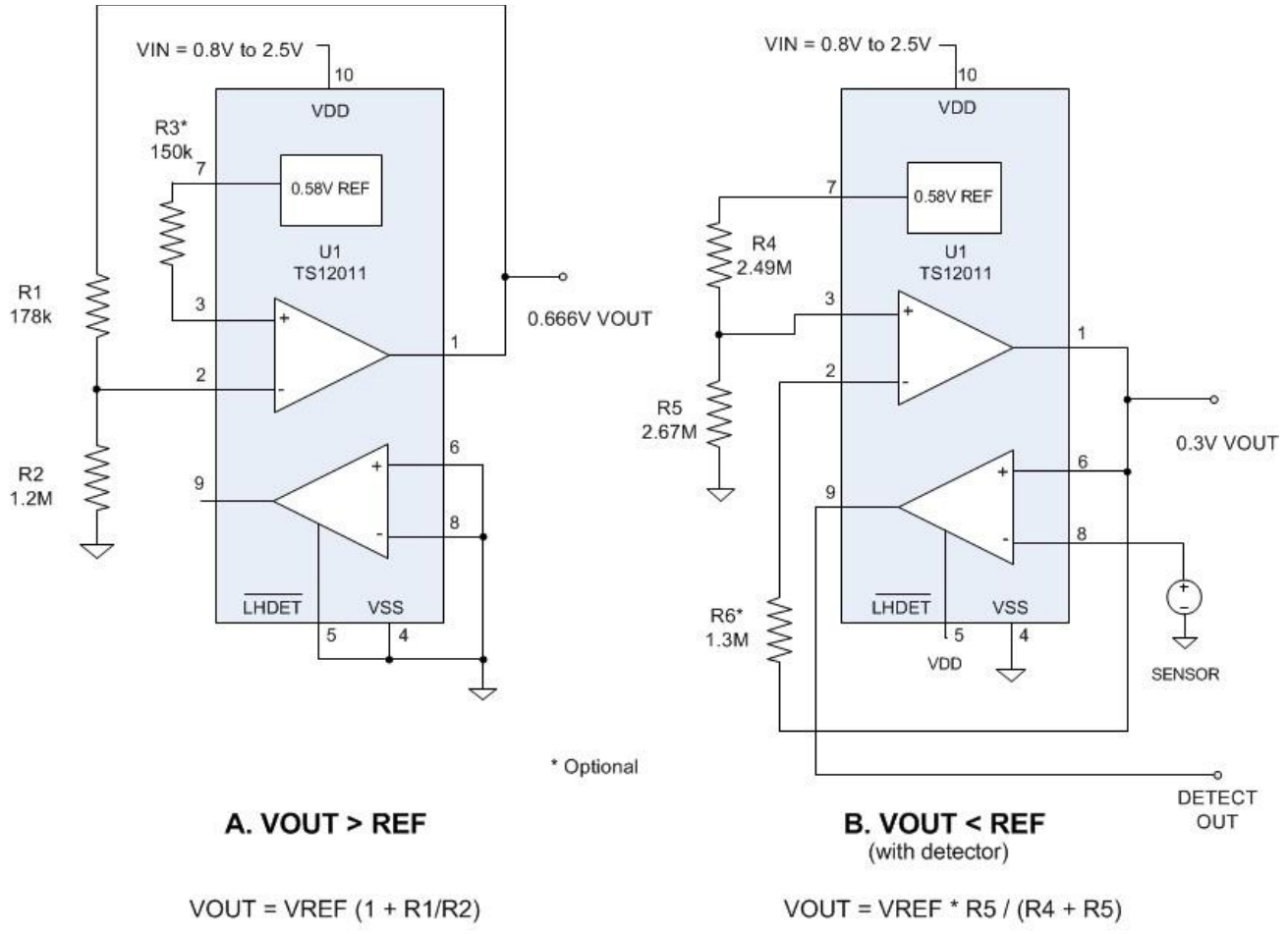



**Figure 1. Buffered Reference Generators**


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The nano-power reference in the TS12011 is unbuffered, a design trade-off taken to absolutely minimize the supply current drain at all costs. You can only draw 100 nA from it, according to the data sheet specification. That is acceptable if the reference is being used to set a comparator threshold or op-amp virtual ground level, but, if more drive is needed, buffering is required. When dividing the reference output with resistors, lower values are generally better from a noise and leakage standpoint, but care should be taken not to overload it. In Figure 1B, the total divider series resistance must be 5.8 MΩ or greater (0.58 V/100 nA). The TS12011 op amp has tighter offset current specs than input bias current specs, so it usually makes sense to add a series resistor at the other input to compensate for the high values used in the divider.

These basic reference circuits are a good starting point for all sorts of designs. Accuracy for Figure 1A is ±4.8% including temp drift, VOS, IOS, and 1% resistor tolerances, which is good enough for building a wake-up detector, timer, or power converter. The relatively high open-loop gain of the op amp keeps the load regulation characteristic flat up to 1 mA. Supply current for either circuit is less than 2 µA. The extra latching comparator is a bonus, shown employed as a voltage detector with 0.3 V trip threshold in Figure 1B.

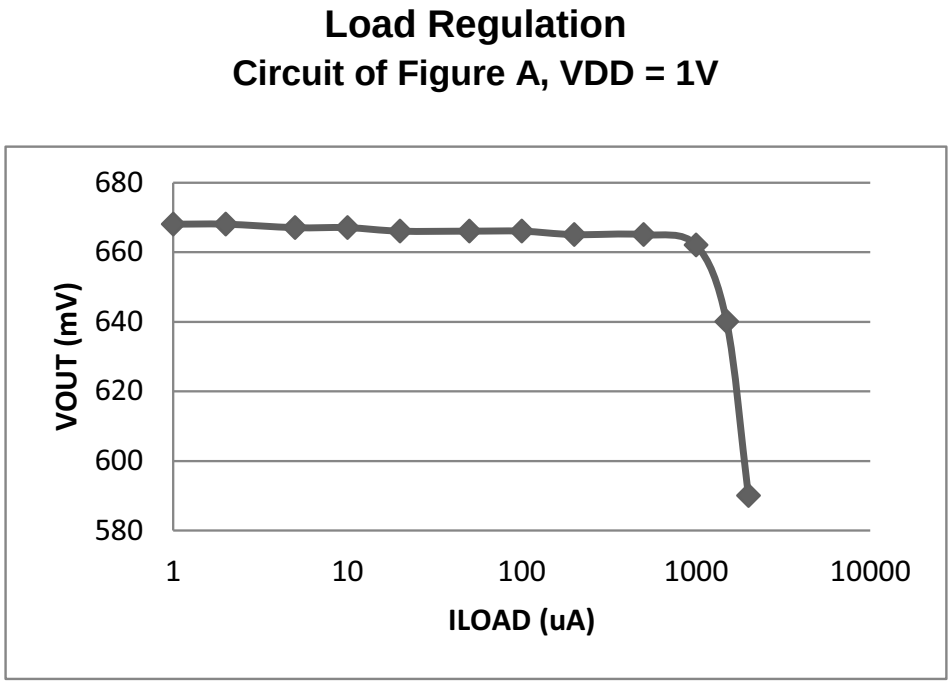
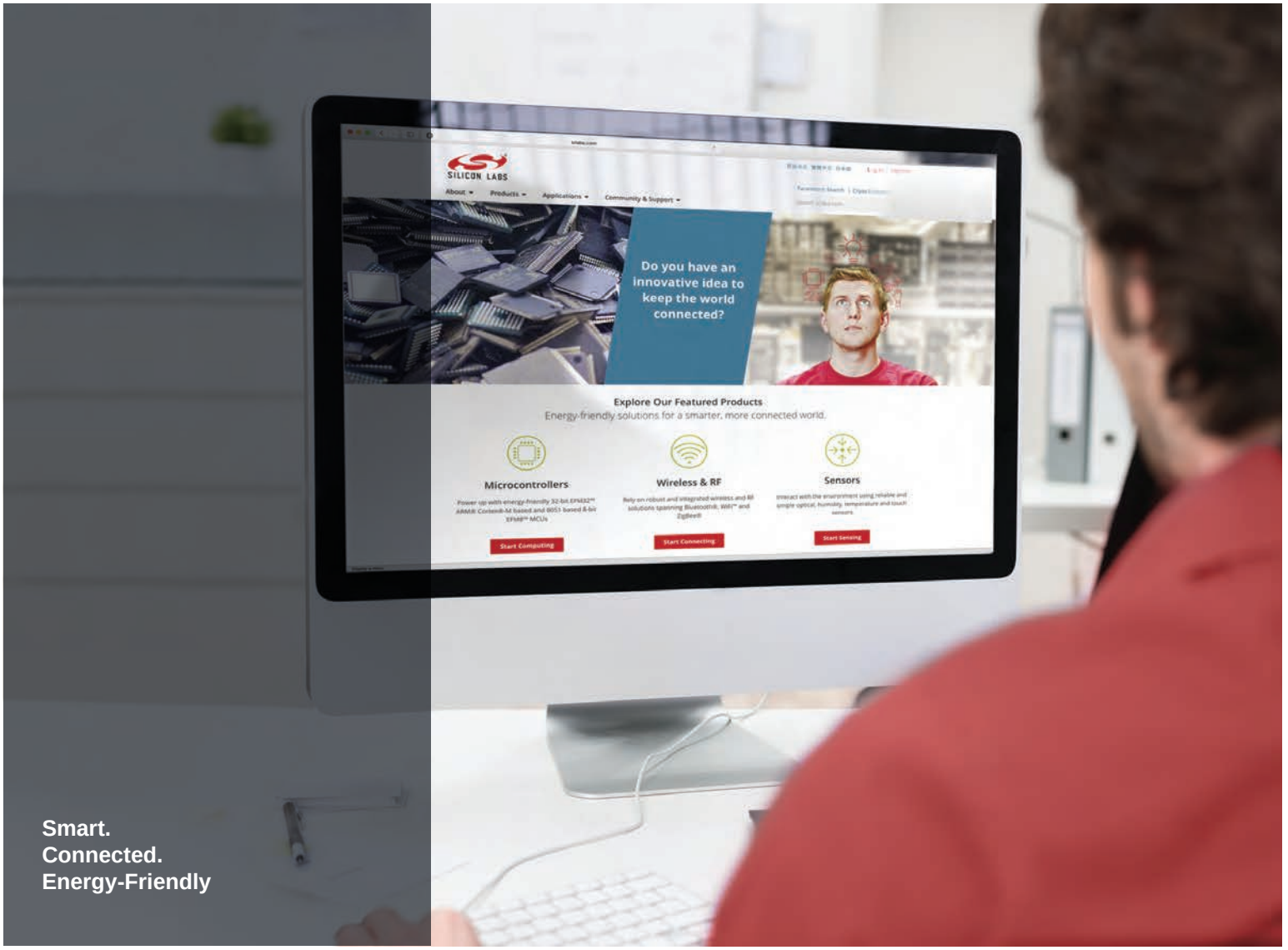



**Figure 2. 0.666 V VREF Load Regulation**

For additional information, please see the TS12011 data sheet.




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**Silicon Laboratories Inc.**
**400 West Cesar Chavez**
**Austin, TX 78701**
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