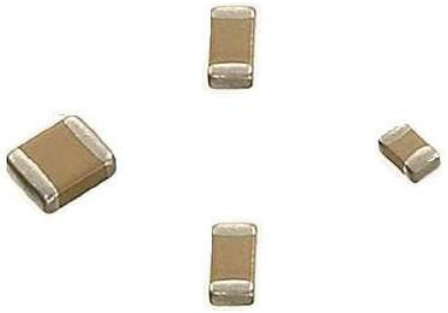
Website: www.kingtronics.com Email: info@kingtronics.com Tel: (852) 8106 7033 Fax: (852) 8106 7099



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Low Voltage Multilayer Chip Ceramic Capacitor

■ Capacitance and Capacitance Tolerance

Different circuit needs different capacitance and capacitance tolerance. So the selection of capacitance is depended on the need of customers.

■ Dielectric Material Type of Capacitor

-NPO : The capacitor of this kind dielectric material is considered as Class Ⅰ capacitor, including general capacitor and high frequency NPO capacitor. The electrical properties of NPO capacitor are the most stable one and have little change with temperature, voltage and time. They are suited for applications where low-losses and high-stability are required, such as filters, oscillators, and timing circuits.

- X7R, X5R : X7R, X5R material is a kind of material has high dielectric constant. The capacitor made of this kind material is considered as Class Ⅱ capacitor whose capacitance is higher than that of class Ⅰ. These capacitors are classified as having a semi-stable temperature characteristic and used over a wide temperature range, such in these kinds of circuits, DC-blocking, decoupling, bypassing, frequency discriminating etc.

-Y5V : The capacitor made of this kind of material is the highest dielectric constant of all ceramic capacitors. They are used over a moderate temperature range in application where high capacitance is required because of its unstable temperature coefficient, but where moderate losses and capacitance changes can be tolerated. Its capacitance and dissipation factors are sensible to measuring conditions, such as temperature and voltage, etc.

■ Temperature Range

NPO/ X7R: -55~125℃
X5R: -55~85℃
Y5V: -30~85℃

■ Voltage

16, 25, 50, 63 VDC.

■ Capacitance

0.5pF ~ 10uF

■ Terminations

Tin / Nickel

■ Tolerance

±0.1pF , +80 ~ -20%

■ Packing

Tape and Reel (0402, 0603, 0805, 1206, 1210, 1812, 2220)

■ Dielectric & Values

NPO X7R Y5V Z5U consult product pages of catalog for cap ranges and voltage rating

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Low Voltage Multilayer Chip Ceramic Capacitor

■ How To Order

LKT	0805	N	102	J	500	R
|	|	|	|	|	|	|
Series	1.	2.	3.	4.	5.	6

NOTE:

1. Dimensions

Size Code	0402	0603	0805	1206
LxW (inch)	0.04x0.02	0.06x0.03	0.08x0.05	0.12x0.06

2. Dielectric Style

Dielectric Code	N	B	X	F
Dielectric material	NPO	X7R	X5R	Y5V

3. Nominal Capacitance Unit : pF

102	$10X10^2$	Note : First two digits are significant; third digit denotes number of zeros; R = decimal.
0R5	0.5	
1R0	1.0	
224	$22X10^4$	
…	…	

4. Capacitance Tolerance

Code	C	D	J	K	M	Z
Tolerance	±0.25pF	±0.5pF	±5.0%	±10%	±20%	+80% -20%

5. Rated Voltage

Express Method	160	250	500
Actual Value	$16V^0$	$25V^0$	$50V^0$

6. Pb

Code	R
Pb	RoHS

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■ Specification and Test Condition:

1. Appearance

Dielectrics	Specification	Testing Condition
NPO/X7R/X5R/Y5V	No defects or abnormalities	Visual inspection

2. Dimensions

Dielectrics	Specification	Testing Condition
NPO/X7R/X5R/Y5V	Within the specified dimensions	Using calipers on micrometer

3. Capacitance

Dielectrics	Specification	Testing Condition
NPO	Within the specified tolerance B:±0.1pF;C:±0.25pF;D:±0.5pF;J: ±5%	1.0±0.2Vrms, 1MHz±10% (C>1000 pF, 1.0±0.2Vrms, 1KHz±10%，) 25℃
X7R/X5R	Within the specified tolerance J: ±5%；K: ±10%； M: ±20%	1.0±0.2Vrms, 1KHz±10% （Cp＞10uF,0.5±0.1Vrms,120±24Hz） at 25℃,48hrs after annealing
Y5V	Within the specified tolerance M: ±20%; Z: +80% ~ -20%	1.0±0.2Vrms, 1KHz±10% （Cp＞10uF,0.5±0.1Vrms,120±24Hz） at 25℃, 48hrs after annealing

4. Dissipation Factor

Dielectrics	Specification	Testing Condition
NPO	Cp<30pF, Q≥400+20Cp; Cp≥30pF, Q≥1000	1.0±0.2Vrms,1MHz±10% ,25℃ (Cp>1000pF,1.0±0.2Vrms,1KHz±10%)
X7R/X5R	V_R≥25V, DF ≤2.5% V_R =16V, DF ≤3.5% V_R ≤10V, DF ≤5.0%	1.0±0.2Vrms, 1KHz±10%, (Cp＞10uF,0.5±0.1Vrms,120±24Hz) at 25℃,48hrs after annealing
Y5V	V_R≥25V, DF ≤7.0% (C<1.0μF) DF ≤9.0% (C≥1.0μF) V_R =16V, DF ≤9.0% V_R ≤10V, DF ≤12.5%	1.0±0.2Vrms, 1KHz±10%, (Cp＞10uF,0.5±0.1Vrms,120±24Hz) at 25℃,48hrs after annealing

5. Insulation Resistance

Dielectrics	Specification	Testing Condition
NPO/X7R/ X5R/Y5V	More than 10 GΩ or 500Ω·F, whichever is smaller.	Rated voltage for 60±5sec, at 25℃

6. Dielectric Strength

Dielectrics	Specification	Testing Condition
NPO /X7R/X5R/Y5V	No defects or abnormalities.	No failure shall be observed when 300% (NPO);250% (X7R/ X5R/Y5V)of the rated voltage is applied between terminations for 1 to 5 seconds, provided the charge /discharge current is less than 500mA

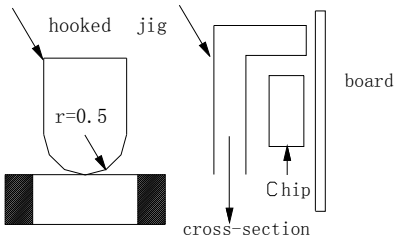
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7. Temperature Coefficient of Capacitance

Dielectrics	Specification	Testing Condition			
NPO	Temperature coefficient within ±30ppm/℃ Cp drift within ±0.2% or ±0.05pF	Measure capacitance under follow table list temperature:			
		STEP	NPO, X7R	X5R	Y5V
		1	25 ±2	25 ±2	25 ±2
		2	-55±3	-55±3	-30±3
X7R/X5R	Capacitance change within ±15%	3 4 5	25 ±2 125±3 25 ±2	25 ±2 85±3 25 ±2	25 ±2 85±3 25 ±2
Y5V	Capacitance change within +22%, -82%	1) NPO The capacitance drift is calculated by dividing the differences between the maximum and minimum measured values in the step 1,3 and 5. The temperature coefficient is determined using the Capacitance measured in step 3 as a reference. 2) X7R ,X5R and Y5V The ranges of capacitance change compared within the above 25℃ value over the temperature ranges shall be within the specified ranges.			

8. Adhesion

Dielectrics	Specification	Testing Condition
NPO X7R/X5R Y5V	No removal of the terminations or other defect shall occur.	The pressurizing force shall be 10N (=1000g*f) and the duration of application shall be 10±1sec. 

9. Solderability of Termination

Dielectrics	Specification	Testing Condition
NPO X7R/X5R Y5V	95% min. coverage of both terminal electrodes and less than 5% have pin holes or rough spots.	Solder temperature: 230±5℃ Dipping time: 2±1 seconds. Completely soak both terminal electrodes in solder

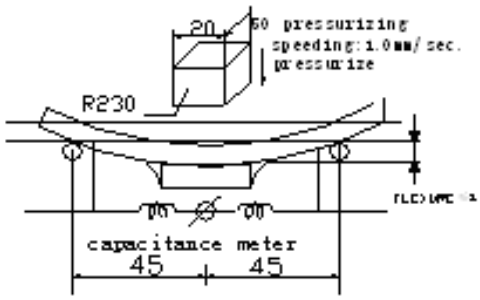
10. Resistance to leaching

Dielectrics	Specification	Testing Condition
NPO X7R/X5R Y5V	95% min. coverage of both terminal electrodes and less than 5% have pin holes or rough spots. No remarkable visual damage.	Solder temperature: 270±5℃ Dipping time: 10±1 seconds. Completely soak both terminal electrodes in solder

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Low Voltage Multilayer Chip Ceramic Capacitor

11. Bending

Dielectrics	Specification	Testing Condition
NPO	No remarkable visual damage Cp change ≤ ±5% or ≤ 0.5 pF	Solder the capacitor on testing substrate and put it on testing stand. The middle part of substrate shall successively be pressurized by pressuring rod at a rated of about 1.0mm/sec. Until the deflection become means of the 1.0mm. 
X7R/X5R	No remarkable visual damage Cp change ≤ ±12.5%	
Y5V	No remarkable visual damage Cp change ≤ ±30%	

12. Resistance to Soldering Heat

Dielectrics	Specification	Testing Condition
NPO	No remarkable visual damage Cp change within ±2.5% or ±0.25pF, whichever is larger. DF meets initial standard value. IR meets initial standard value.	Soldering temperature: 270±5℃ Preheating: 120~150℃ 60sec. Dipping time: 10±1 seconds. Measurement to be made after being kept at room temperature for 24±2 (COG) or 48±4(X7R ,X5R, Y5V) hours. Recovery for the following period under the standard condition after test. *Initial measurement for high dielectric constant type Perform a heat treatment at 140~150℃ for 1hr and let sit for 48±4hrs at room temperature. Perform the initial measurement.
X7R/X5R	No remarkable visual damage Cp change within ±5% DF meets initial standard value. IR meets initial standard value.	
Y5V	No remarkable visual damage Cp change within ±20% DF meets initial standard value. IR meets initial standard value.	

13. Temperature Cycle

Dielectrics	Specification	Testing Condition		
NPO	No remarkable visual damage Cp change within ±2.5% or ±0.25pF, whichever is larger.	To perform 5 cycles of the stated environment:		
		Step	Temperature	Time
		1	Min. operating Temp.+0/-3℃	30min
		2	25℃	2~3 min
		3	Max. operating Temp.+0/-3℃	30 min
X7R/X5R	No remarkable visual damage Cp change within ±7.5%	4	25℃	2~3 min
		Measurement to be made after being kept at room temperature for 24±2hrs (COG) or 48±4hrs (X7R, X5R, Y5V) at room temperature, then measure. *Initial measurement for high dielectric constant type Perform a heat treatment at 140~150℃ for 1hr and let sit for 48±4hrs at room temperature. Perform the initial measurement.		

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14. Moisture Resistance ,steady state

Dielectrics	Specification	Testing Condition
NPO	No remarkable visual damage Cp change within ±5% or ±0.5pF, whichever is larger. Cp<10pF, Q≥200+10Cp; IO≤Cp<30pF, Q≥275+2.5Cp Cp≥30pF, Q≥350 R*C≥1000MΩ or 50Ω·F, whichever is smaller	Test temperature: 40±2℃ Humidity: 90~95% RH Testing time: 500 ±12hrs Measurement to be made after being kept at room temperature for 24±2hrs (COG) or 48±4hrs (X7R, X5R, Y5V) *Initial measurement for high dielectric constant type Perform a heat treatment at 140~150℃ for 1hr and let sit for 48±4hrs at room temperature. Perform the initial measurement.
X7R/X5R	Cp change within ±12.5% DF: Not more than 2 times of initial value R*C≥1000MΩ or 50Ω·F, whichever is smaller	
Y5V	No remarkable visual damage Cp change within ±30% DF: Not more than 1.5 times of initial value R*C≥1000MΩ or 50Ω·F, whichever is smaller	

15. Damp heat with load

Dielectrics	Specification	Testing Condition
NPO	No remarkable visual damage Cp change≤±7.5% or ±0.75pF, whichever is larger. Cp<30pF, Q≥100+10/3*Cp Cp≥30pF, Q≥200 R*C≥500MΩ or 25Ω·F, whichever is smaller	Test temperature: 40±2℃ Humidity: 90~95% RH Voltage: 100% of the rated voltage Testing time: 500 ±12hrs Measurement to be made after being kept at room temperature for 24±2hrs (COG) or 48±4hrs (X7R, X5R, Y5V) *Apply the rated DC voltage for 1 hour at 40±2℃. Remove and let sit for 48±4hrs at room temperature. Perform the initial measurement.
X7R/X5R	No remarkable visual damage Cp change≤±12.5% DF: Not more than 2 times of initial value R*C≥500MΩ or 25Ω·F, whichever is smaller	
Y5V	No remarkable visual damage Cp change≤±30% DF: Not more than 1.5 times of initial value R*C≥500MΩ or 25Ω·F , whichever is smaller	

16. Life Test

Dielectrics	Specification	Testing Condition
NPO	No remarkable visual damage Cp change≤±3% or ±0.3pF, whichever is larger. Q≥350 (Cp≥30 PF) Q≥275+(2.5* Cp) (10 pF≤Cp<30 PF) Q≥200+10*Cp (Cp<10 PF) R*C≥1000MΩ or 50Ω·F, whichever is smaller	Test temperature: Max. Operating Temp. ±3℃ Voltage: 200% of the rated voltage Testing time: 1000 hrs Measurement to be made after being kept at room temperature for 24±2hrs (COG) or 48±4hrs (X7R, X5R,Y5V) *Initial measurement for high dielectric constant type Apply 200% of the rated DC voltage for one hour at the maximum operating temperature ±3℃. Remove and let sit for 48±4hrs at room temperature. Perform the initial measurement
X7R/X5R	No remarkable visual damage Cp change≤±12.5% DF:Not more than 2 times of initial value R*C≥1000MΩ or 50Ω·F, whichever is smaller	
Y5V	No remarkable visual damage Cp change≤±30% DF:Not more than 1.5 times of initial value R*C≥1000MΩ or 50Ω·F, whichever is smaller	

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Low Voltage Multilayer Chip Ceramic Capacitor

Packing

1. Tape Packing

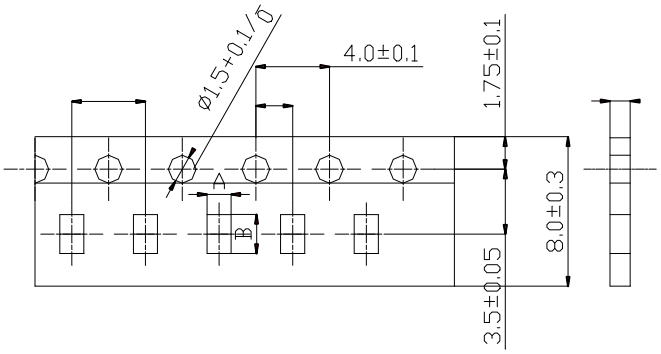
Paper Tape: Standard taping (8mm paper width) suitable to 0603,0805,4Kpcs/reel

To 0402, 10Kpcs/reel.

Plastic Tape: Suitable 0805, 1206 sizes, for chip thickness over 0.95 mm, 4Kpcs/reel

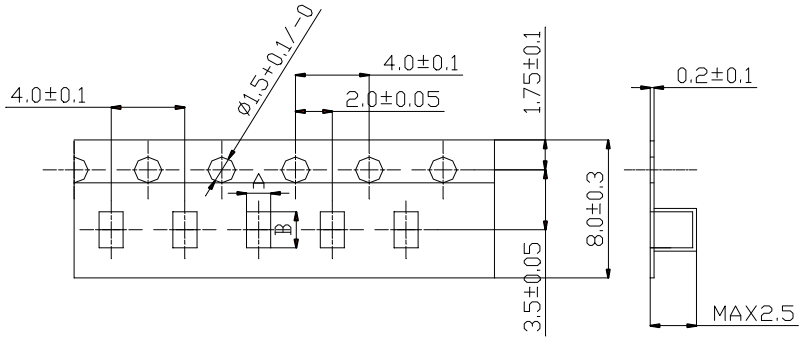
or 3Kpcs/reel are available.

2. Dimensions of Packing Paper：



Type	A	B	C	D	T
0402	0.65±0.10	1.15±0.10	2.0±0.05	2.0±0.05	0.8max
0603	1.05±0.10	1.85±0.10	4.0±0.10	2.0±0.10	1.1max
0805	1.55±0.15	2.3±0.15	4.0±0.10	2.0±0.10	1.1max
1206	1.95±0.15	3.5±0.15	4.0±0.10	2.0±0.10	1.1max

3. Dimensions of Embossed Packing



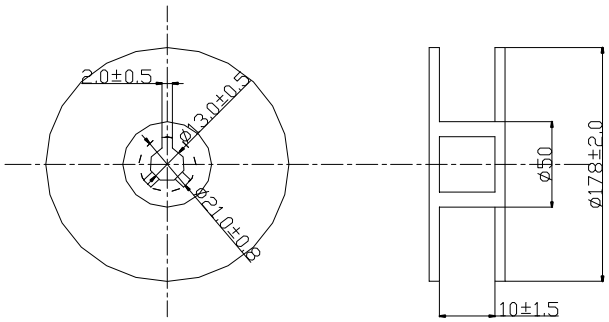
A：1.45±0.20 B：2.25±0.20 （0805）
A：1.95±0.20 B：3.50±0.20 （1206）

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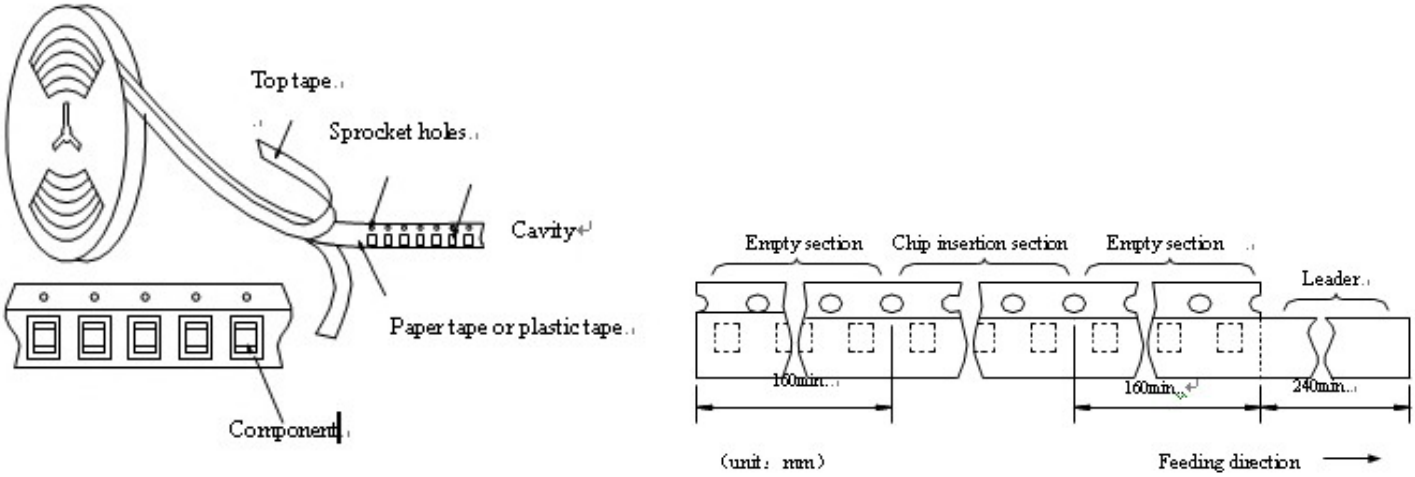
Low Voltage Multilayer Chip Ceramic Capacitor

4. Dimensions of Reel:

φ 180mmReel

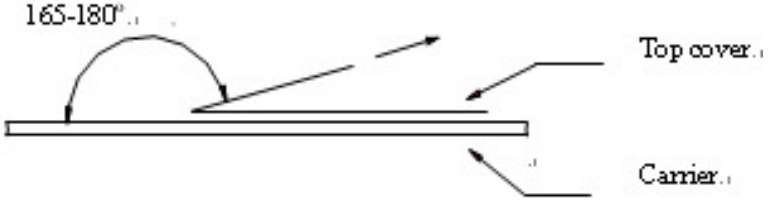


5. Taping Figure



6. Taping Method

①Tapes for capacitors are wound clockwise. The sprocket holes are to the right as the tape is pulled toward the user.
② The top tape and base tape are not attached at the end of the tape for a minimum of 5 pitches.
③ Part of the leader and part of the empty tape shall be attached to the end of the tape as follows.
④Missing capacitors number within 0.1% of the number per reel or 1pc, whichever is greater, and are not continuous.
⑤The top tape and bottom tape shall not protrude beyond the edges of the tape and shall not cover sprocket holes.
⑥Cumulative tolerance of sprocket holes, 10 pitches: ±0.3mm.
⑦Peeling off force: 0.1 to 0.6N in the direction shown down.



Note: Specifications are subject to change without notice.