60V Current Mode Synchronous Switching Regulator Controller

FEATURES

- **High Voltage Operation: Up to 60V**
- **Large 1Ω Gate Drivers**
- **No Current Sense Resistor Required**
- **Dual N-Channel MOSFET Synchronous Drive**
- Extremely Fast Transient Response
- ±0.5% 0.8V Voltage Reference
- Programmable Soft-Start
- Generates 5.5V Driver Supply
- Selectable Pulse-Skipping Mode Operation
- Power Good Output Voltage Monitor
- Adjustable On-Time/Frequency: $t_{ON(MIN)}$ < 100ns
- Adjustable Cycle-by-Cycle Current Limit
- Undervoltage Lockout On Driver Supply
- Output Overvoltage Protection
- Thermally Enhanced 16-Pin TSSOP Package

APPLICATIONS

- 48V Telecom and Base Station Power Supplies
- Networking Equipment, Servers
- Automotive and Industrial Control Systems

DESCRIPTION

The LTC3812-5 is a synchronous step-down switching regulator controller that can directly step down voltages from up to 60V input, making it ideal for telecom and automotive applications. The LTC3812-5 uses a constant on-time valley current control architecture to deliver very low duty cycles with accurate cycle-by-cycle current limit without requiring a sense resistor.

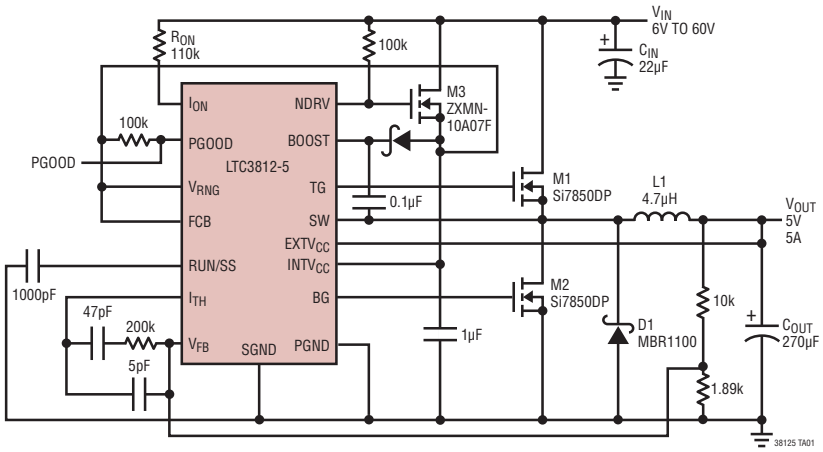
A precise internal reference provides 0.5% DC accuracy. A high bandwidth (25MHz) error amplifier provides very fast line and load transient response. Large 1Ω gate drivers allow the LTC3812-5 to drive large power MOSFETs for higher current applications. The operating frequency is selected by an external resistor and is compensated for variations in V_{IN}. A shutdown pin allows the LTC3812-5 to be turned off reducing the supply current to <230µA.

Integrated bias control generates gate drive power from the input supply during start-up and when an output short-circuit occurs, with the addition of a small external SOT23 MOSFET. When in regulation, power is derived from the output for higher efficiency.

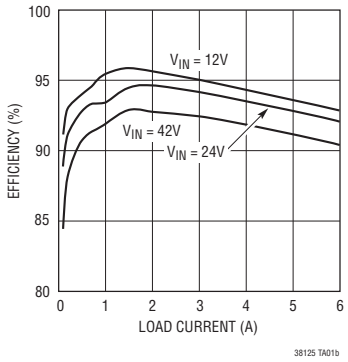
LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents including 5481178, 5847554, 6304066, 6476589, 6580258, 6677210, 6774611.

TYPICAL APPLICATION

High Efficiency High Voltage Step-Down Converter



Efficiency vs Load Current



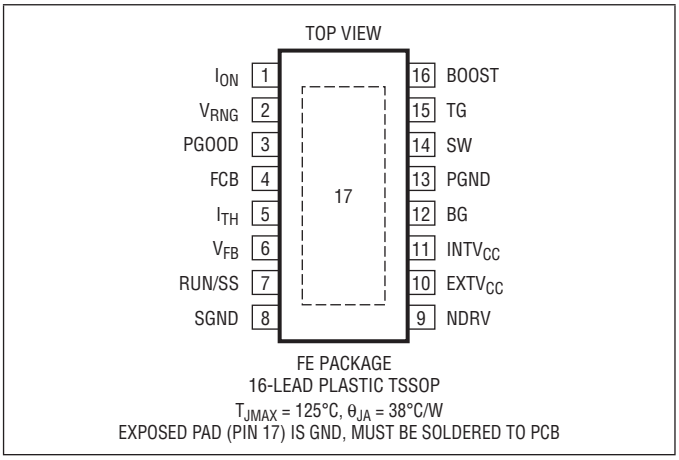
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- $INTV_{CC}$ ..... –0.3V to 14V
- ($INTV_{CC}$ – PGND), (BOOST – SW) ..... –0.3V to 14V
- BOOST (Continuous) ..... –0.3V to 85V
- BOOST (≤400ms) ..... –0.3V to 95V
- $EXTV_{CC}$ ..... –0.3V to 15V
- ($EXTV_{CC}$ – $INTV_{CC}$)..... –12V to 12V

($NDRV – INTV_{CC}$) Voltage..... –0.3V to 10V
SW Voltage (Continuous)..... –1V to 70V
SW Voltage (400ms)..... –1V to 80V
I_{ON} Voltage (Continuous) ..... –0.3V to 70V
I_{ON} Voltage (400ms) ..... –0.3V to 80V
RUN/SS Voltage..... –0.3V to 5V
PGOOD Voltage..... –0.3V to 7V
V_{RNG}, FCB Voltages..... –0.3V to 14V
FB Voltage..... –0.3V to 2.7V
TG, BG, $INTV_{CC}$, $EXTV_{CC}$ RMS Currents.....50mA
Operating Junction Temperature Range
(Notes 2, 3, 7).....–40°C to 125°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....300°C

PIN CONFIGURATION



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3812EFE-5#PBF	LTC3812EFE-5#TRPBF	3812EFE-5	16-Lead Plastic TSSOP	–40°C to 125°C
LTC3812IFE-5#PBF	LTC3812IFE-5#TRPBF	3812IFE-5	16-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), $INTV_{CC}$ = V_{BOOST} = V_{RNG} = V_{EXTVCC} = V_{NDRV} = 5V, V_{FCB} = V_{SW} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
$INTV_{CC}$	$INTV_{CC}$ Supply Voltage		●	4.35		14	V
I_Q	$INTV_{CC}$ Supply Current $INTV_{CC}$ Shutdown Current	RUN/SS > 1.5V (Notes 4, 5) RUN/SS = 0V			3 224	6 600	mA µA
I_{BOOST}	BOOST Supply Current	RUN/SS > 1.5V (Note 5) RUN/SS = 0V			240 0	400 5	µA µA
V_{FB}	Feedback Voltage	(Note 4) 0°C to 85°C –40°C to 85°C –40°C to 125°C	 ● ● ●	0.796 0.794 0.792 0.792	0.800 0.800 0.800 0.800	0.804 0.806 0.806 0.808	V V V V
$\Delta V_{FB,LINE}$	Feedback Voltage Line Regulation	5V < $INTV_{CC}$ < 14V (Note 4)	●		0.002	0.02	%/V
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{RNG} = 2V, V_{FB} = 0.76V V_{RNG} = 0V, V_{FB} = 0.76V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.76V		256 70 170	320 95 215	384 120 260	mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold	V_{RNG} = 2V, V_{FB} = 0.84V V_{RNG} = 0V, V_{FB} = 0.84V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.84V			–300 –85 –200		mV mV mV
I_{VFB}	Feedback Current	V_{FB} = 0.8V			20	150	nA
A_{VOL}(EA)	Error Amplifier DC Open-Loop Gain			65	100		dB
f_U	Error Amp Unity Gain Crossover Frequency	(Note 6)			25		MHz
V_{FCB}	FCB Threshold	V_{FCB} Rising		0.75	0.8	0.85	V
I_{FCB}	FCB Current	FCB = 5V			0	1	µA
$V_{RUN/SS}$	Shutdown Threshold			1.2	1.5	2	V
$I_{RUN/SS}$	RUN/SS Source Current	RUN/SS = 0V		0.7	1.4	2.5	µA
V_{VCCUV}	$INTV_{CC}$ Undervoltage Lockout Linear Regulator Mode External Supply Mode Trickle-Charge Mode	 $INTV_{CC}$ Rising, I_{NDRV} = 100µA $INTV_{CC}$ Rising, NDRV = $INTV_{CC}$ = $EXTV_{CC}$ $INTV_{CC}$ Rising, NDRV = $INTV_{CC}$, $EXTV_{CC}$ = 0 $INTV_{CC}$ Falling	 ● ● ●	 4.05 4.05 8.70	 4.2 4.2 9.0 3.7	 4.35 4.35 9.30	 V V V V
Oscillator							
t_{ON}	On-Time	I_{ON} = 100µA I_{ON} = 300µA		1.55 515	1.85 605	2.15 695	µs ns
$t_{ON(MIN)}$	Minimum On-Time	I_{ON} = 2500µA				100	ns
$t_{OFF(MIN)}$	Minimum Off-Time				250	350	ns
Driver							
$I_{BG,PEAK}$	BG Driver Peak Source Current	V_{BG} = 0V		0.7	1		A
$R_{BG,SINK}$	BG Driver Pull-Down $R_{DS(ON)}$				1	1.5	Ω
$I_{TG,PEAK}$	TG Driver Peak Source Current	V_{TG} – V_{SW} = 0V		0.7	1		A
$R_{TG,SINK}$	TG Driver Pull-Down $R_{DS(ON)}$				1	1.5	Ω
PGOOD Output							
ΔV_{FBOV}	PGOOD Upper Threshold PGOOD Lower Threshold	V_{FB} Rising V_{FB} Falling		7.5 –7.5	10 –10	12.5 –12.5	% %
$\Delta V_{FB,HYST}$	PGOOD Hysterisis	V_{FB} Returning			1.5	3	%
V_{PGOOD}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.3	0.6	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), $INTV_{CC}$ = V_{BOOST} = V_{RNG} = V_{EXTVCC} = V_{NDRV} = 5V, V_{FCB} = V_{SW} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V			0	2	µA
PG Delay	PGOOD Delay	V_{FB} Falling			120		µs
V_{CC} Regulators							
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage $EXTV_{CC}$ Rising $EXTV_{CC}$ Hysterisis		●	4.5 0.1	4.7 0.25	 0.4	V V
$V_{INTVCC,1}$	$INTV_{CC}$ Voltage from $EXTV_{CC}$	6V < V_{EXTVCC} < 15V		5.2	5.5	5.8	V
$\Delta V_{EXTVCC,1}$	V_{EXTVCC} - V_{INTVCC} at Dropout	I_{CC} = 20mA, V_{EXTVCC} = 5V			75	150	mV
$\Delta V_{LOADREG,1}$	$INTV_{CC}$ Load Regulation from $EXTV_{CC}$	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 10V			0.01		%
$V_{INTVCC,2}$	$INTV_{CC}$ Voltage from NDRV Regulator	Linear Regulator in Operation		5.2	5.5	5.8	V
$\Delta V_{LOADREG,2}$	$INTV_{CC}$ Load Regulation from NDRV	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 0			0.01		%
I_{NDRV}	Current into NDRV Pin	V_{NDRV} – V_{INTVCC} = 3V		20	40	60	µA
I_{NDRVTO}	Linear Regulator Timeout Enable Threshold			210	270	350	µA
V_{CCSR}	Maximum Supply Voltage	Trickle Charger Shunt Regulator			15		V
I_{CCSR}	Maximum Current into NDRV/$INTV_{CC}$	Trickle Charger Shunt Regulator, $INTV_{CC}$ ≤ 16.7V (Note 8)		10			mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3812-5 is tested under pulsed load conditions such that $T_J \approx T_A$.The LTC3812E-5 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3812I-5 is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3812-5: $T_J = T_A + (P_D \bullet 38°C/W)$

Note 4: The LTC3812-5 is tested in a feedback loop that servos V_{FB} to the reference voltage with the I_{TH} pin forced to a voltage between 1V and 2V.

Note 5: The dynamic input supply current is higher due to the power MOSFET gate charging being delivered at the switching frequency ($Q_G \bullet f_{OSC}$).

Note 6: Guaranteed by design. Not subject to test.

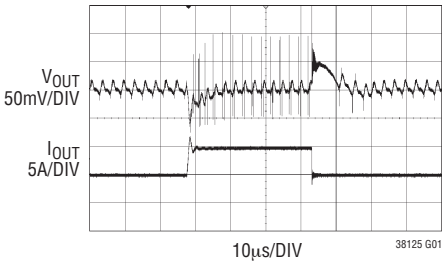
Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 8: I_{CC} is the sum of current into NDRV and $INTV_{CC}$.

PARAMETER	LTC3810	LTC3810-5	LTC3812-5
Maximum V_{IN}	100V	60V	60V
MOSFET Gate Drive	6.35V to 14V	4.5V to 14V	4.5V to 14V
$INTV_{CC}$ UV^+	6.2V	4.2V	4.2V
$INTV_{CC}$ UV^-	6V	4V	4V

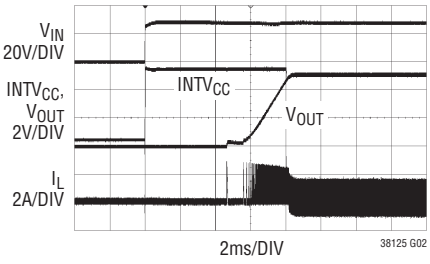
TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response



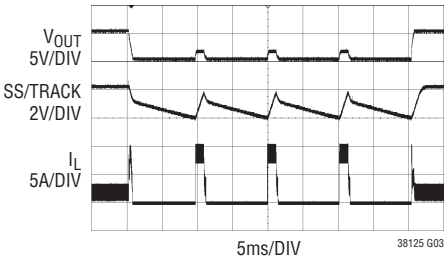
FRONT PAGE CIRCUIT
V_{IN} = 25V
0A TO 5A LOAD STEP

Start-Up



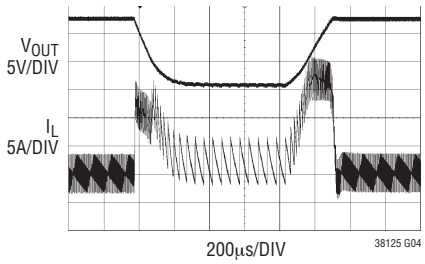
FRONT PAGE CIRCUIT
V_{IN} = 30V
I_{LOAD} = 0.5A
FCB = 0V

Short-Circuit/Fault Timeout Operation



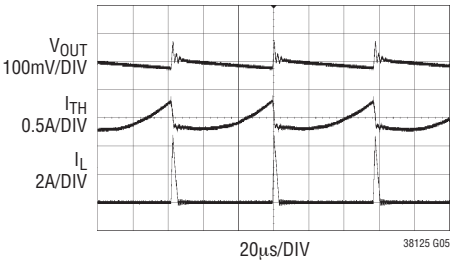
FRONT PAGE CIRCUIT
V_{IN} = 25V
R_{SHORT} = 0.1Ω

Short-Circuit/Foldback Operation



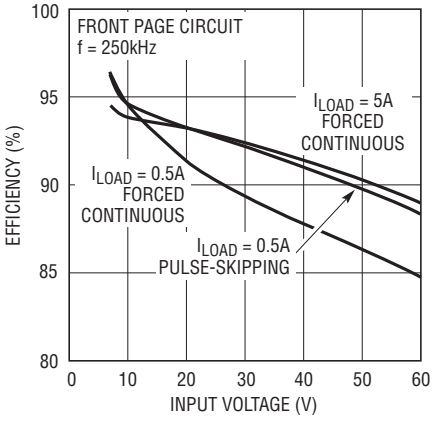
FRONT PAGE CIRCUIT
V_{IN} = 25V

Pulse-Skipping Mode Operation

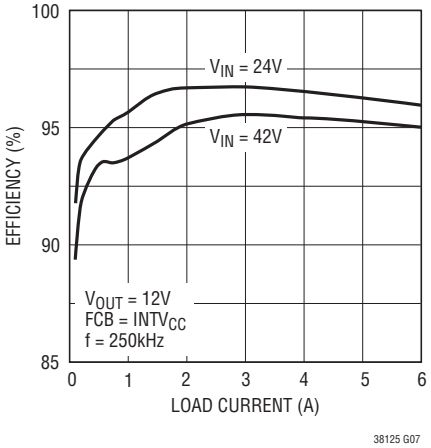


FRONT PAGE CIRCUIT
V_{IN} = 25V
I_{OUT} = 100mA
FCB = $INTV_{CC}$

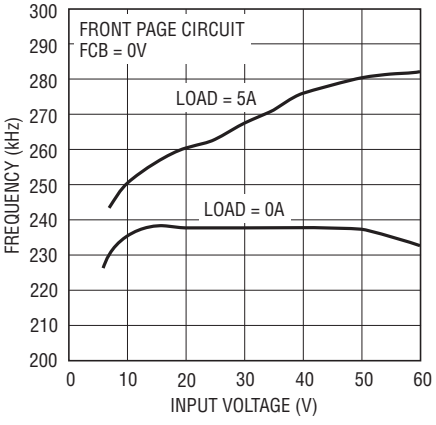
Efficiency vs Input Voltage



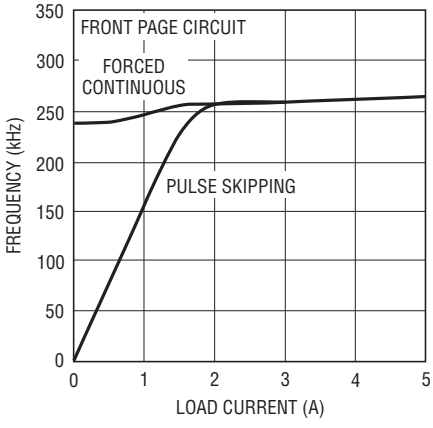
Efficiency vs Load Current



Frequency vs Input Voltage

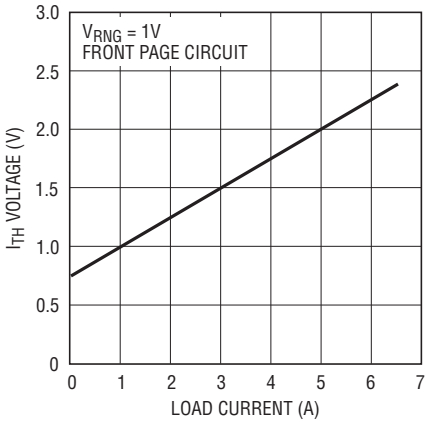


Frequency vs Load Current



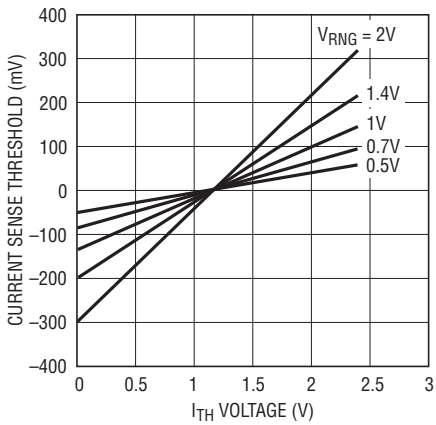
TYPICAL PERFORMANCE CHARACTERISTICS

I_{TH} Voltage vs Load Current



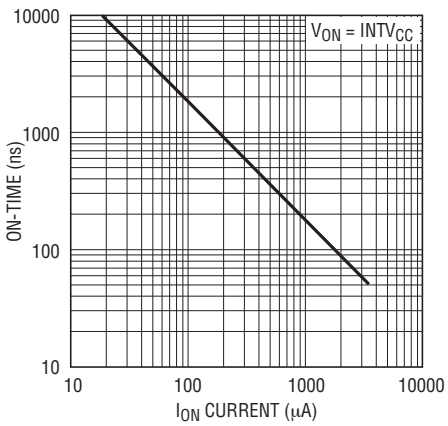
38125 G10

Current Sense Threshold vs I_{TH} Voltage



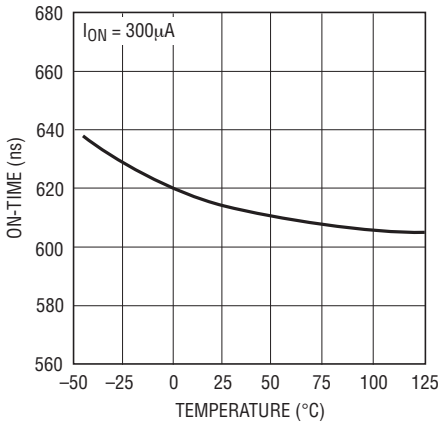
38125 G11

On-Time vs I_{ON} Current



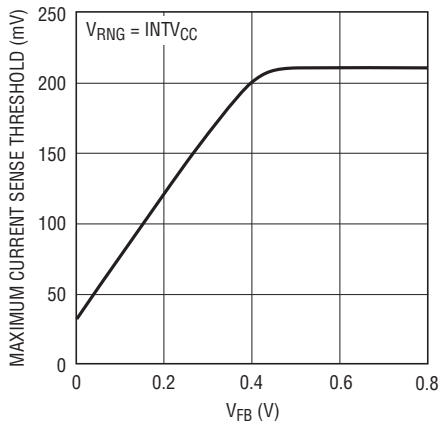
38125 G12

On-Time vs Temperature



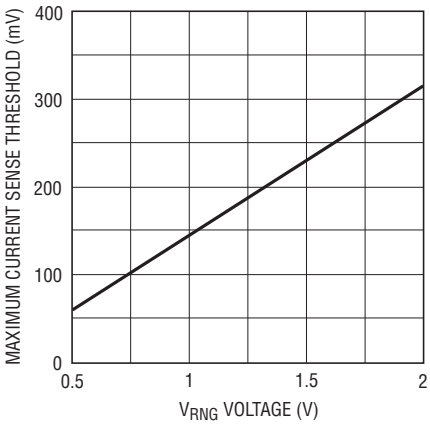
38125 G13

Current Limit Foldback



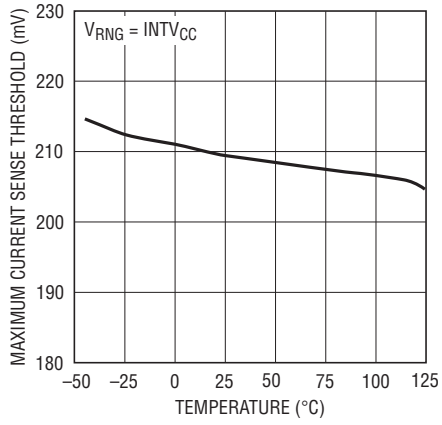
38125 G14

Maximum Current Sense Threshold vs V_{RNG} Voltage



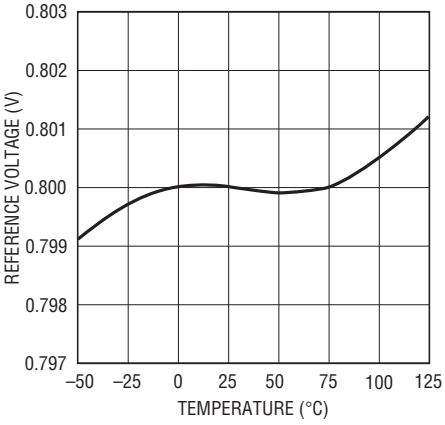
38125 G15

Maximum Current Sense Threshold vs Temperature



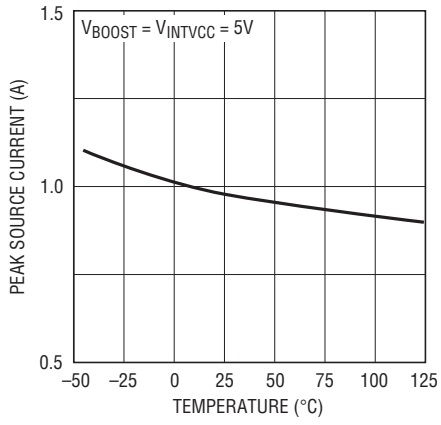
38125 G16

Reference Voltage vs Temperature



38125 G17

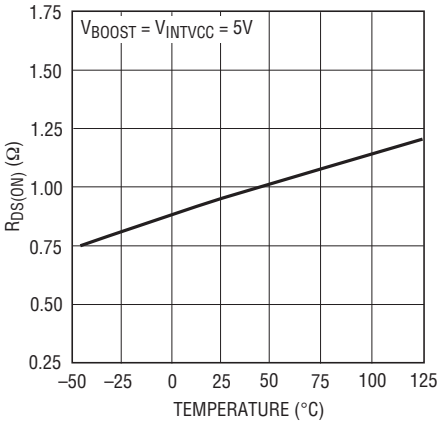
Driver Peak Source Current vs Temperature



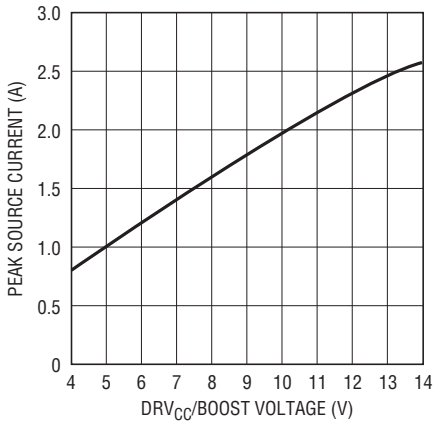
38125 G18

TYPICAL PERFORMANCE CHARACTERISTICS

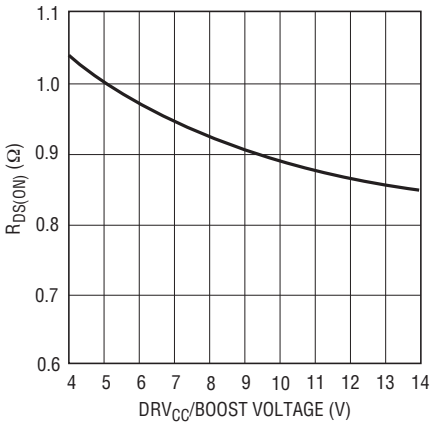
Driver Pull-Down $R_{DS(ON)}$ vs Temperature



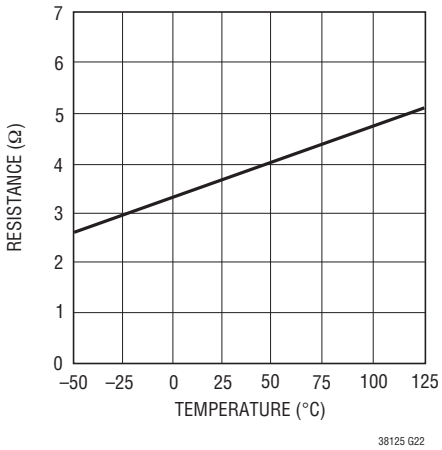
Driver Peak Source Current vs Supply Voltage



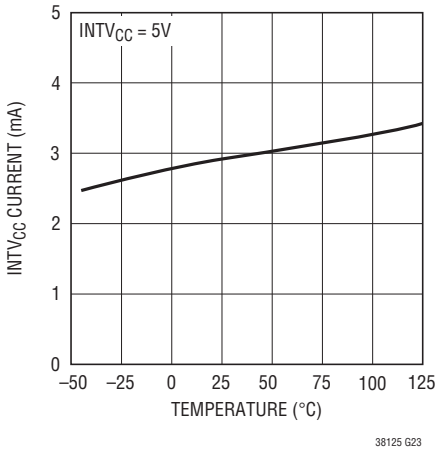
Driver Pull-Down $R_{DS(ON)}$ vs Supply Voltage



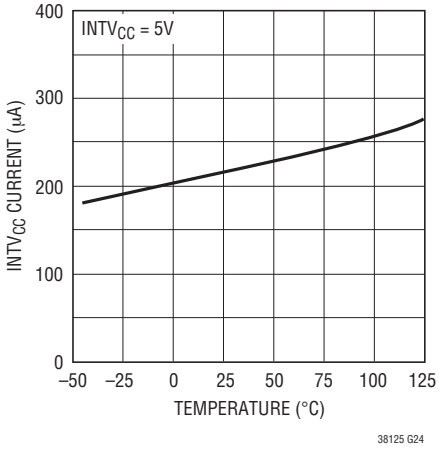
$EXTV_{CC}$ Switch Resistance vs Temperature



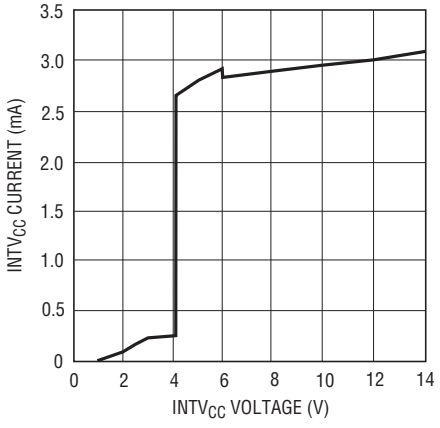
$INTV_{CC}$ Current vs Temperature



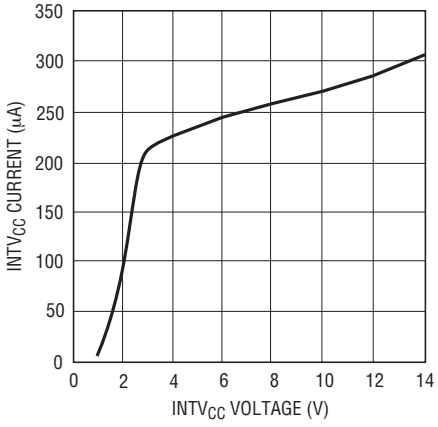
$INTV_{CC}$ Shutdown Current vs Temperature



$INTV_{CC}$ Current vs $INTV_{CC}$ Voltage

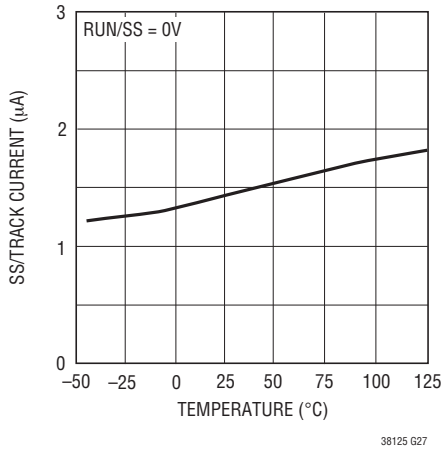


$INTV_{CC}$ Shutdown Current vs $INTV_{CC}$ Voltage

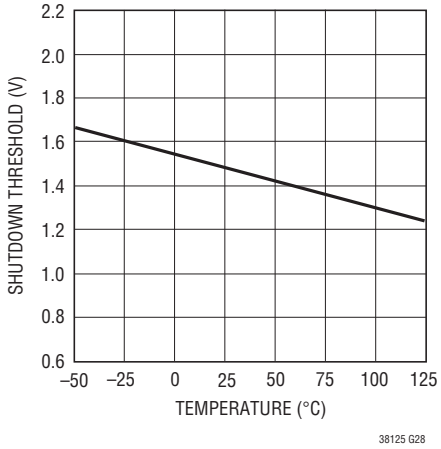


TYPICAL PERFORMANCE CHARACTERISTICS

RUN/SS Pull-Up Current vs Temperature



Shutdown Threshold vs Temperature



PIN FUNCTIONS

I_{ON} (Pin 1): On-Time Current Input. Tie a resistor from V_{IN} to this pin to set the one-shot timer current and thereby set the switching frequency.

V_{RNG} (Pin 2): Sense Voltage Limit Set. The voltage at this pin sets the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from $INTV_{CC}$. The nominal sense voltage defaults to 95mV when this pin is tied to ground, and 215mV when tied to $INTV_{CC}$.

PGOOD (Pin 3): Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not between ±10% of the regulation point. The output voltage must be out of regulation for at least 120µs before the power good output is pulled to ground.

FCB (Pin 4): Pulse-Skipping Mode Enable Pin. This pin provides pulse-skipping mode enable/disable control. Pulling this pin below 0.8V disables pulse-skipping mode operation and forces continuous operation. Pulling this pin above 0.8V enables pulse-skipping mode operation. This pin can also be connected to a feedback resistor divider from a secondary winding on the inductor to regulate a second output voltage.

I_{TH} (Pin 5): Error Amplifier Compensation Point and Current Control Threshold. The current comparator threshold increases with control voltage. The voltage ranges from 0V to 2.6V with 1.2V corresponding to zero sense voltage (zero current).

V_{FB} (Pin 6): Feedback Input. Connect V_{FB} through a resistor divider network to V_{OUT} to set the output voltage.

RUN/SS (Pin 7): RUN/Soft-Start Input. For soft-start, a capacitor to ground at this pin sets the ramp rate of the output voltage (approximately 0.6s/µF). Pulling this pin below 1.5V will shut down the LTC3812-5, turn off both of the external MOSFET switches and reduce the quiescent supply current to 224µA.

SGND (Pin 8): Signal Ground. All small-signal components should connect to this ground and eventually connect to PGND at one point.

NDRV (Pin 9): Drive Output for External Pass Device of the Linear Regulator for $INTV_{CC}$. Connect to the gate of an external NMOS pass device and a pull-up resistor to the input voltage V_{IN}.

PIN FUNCTIONS

$EXTV_{CC}$ (Pin 10): External Driver Supply Voltage. When this voltage exceeds 4.2V, an internal switch connects this pin to $INTV_{CC}$ through an LDO and turns off the external MOSFET connected to NDRV, so that controller and gate drive are drawn from $EXTV_{CC}$.

$INTV_{CC}$ (Pin 11): Main Supply and Driver Supply Pin. All internal circuits and bottom gate output driver are powered from this pin. $INTV_{CC}$ should be bypassed to SGND and PGND with a low ESR (X5R or better) 1µF capacitor in close proximity to the LTC3812-5.

BG (Pin 12): Bottom Gate Drive. The BG pin drives the gate of the bottom N-channel synchronous switch MOSFET. This pin swings from PGND to $INTV_{CC}$.

PGND (Pin 13): Bottom Gate Return. This pin connects to the source of the pull-down MOSFET in the BG driver and is normally connected to ground.

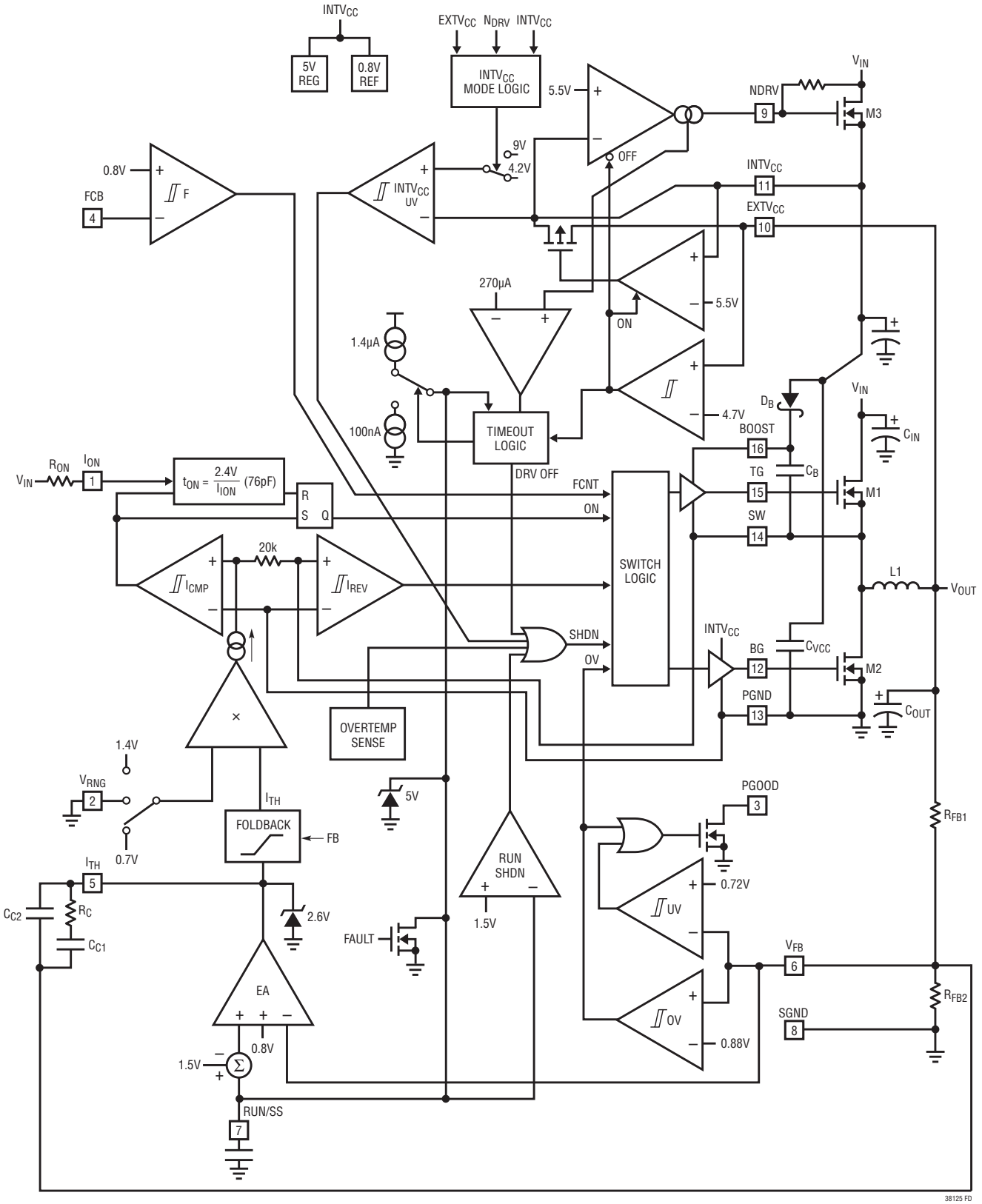
SW (Pin 14): Switch Node Connection to Inductor and Bootstrap Capacitor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{IN}.

TG (Pin 15): Top Gate Drive. The TG pin drives the gate of the top N-channel synchronous switch MOSFET. The TG driver draws power from the BOOST pin and returns to the SW pin, providing true floating drive to the top MOSFET.

BOOST (Pin 16): Top Gate Driver Supply. The BOOST pin supplies power to the floating TG driver. BOOST should be bypassed to SW with a low ESR (X5R or better) 0.1µF capacitor. An additional fast recovery Schottky diode from $INTV_{CC}$ to the BOOST pin will create a complete floating charge-pumped supply at BOOST.

GND (Exposed Pad Pin 17): Ground. The Exposed Pad must be soldered to PCB ground.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3812-5 is a current mode controller for DC/DC step-down converters. In normal operation, the top MOSFET is turned on for a fixed interval determined by a one-shot timer (OST). When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator I_{CMP} trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage between the PGND and SW pins using the bottom MOSFET on-resistance. The voltage on the I_{TH} pin sets the comparator threshold corresponding to the inductor valley current. The fast 25MHz error amplifier EA adjusts this voltage by comparing the feedback signal V_{FB} to the internal 0.8V reference voltage. If the load current increases, it causes a drop in the feedback voltage relative to the reference. The I_{TH} voltage then rises until the average inductor current again matches the load current.

The operating frequency is determined implicitly by the top MOSFET on-time and the duty cycle required to maintain regulation. The one-shot timer generates an on time that is proportional to the ideal duty cycle, thus holding frequency approximately constant with changes in V_{IN}. The nominal frequency can be adjusted with an external resistor R_{ON}.

Pulling the RUN/SS pin low forces the controller into its shutdown state, turning off both M1 and M2. Forcing a voltage above 1.5V will turn on the device.

Pulse-Skipping Mode

The LTC3812-5 can operate in one of two modes selectable with the FCB pin—pulse-skipping mode or forced continuous mode (see Figure 1). Pulse-skipping mode is selected when increased efficiency at light loads is desired (see Figure 2). In this mode, the bottom MOSFET is turned off when inductor current reverses to minimize efficiency loss due to reverse current flow and gate charge switching. At low load currents, I_{TH} will drop below the zero current level (1.2V) shutting off both switches. Both switches will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current

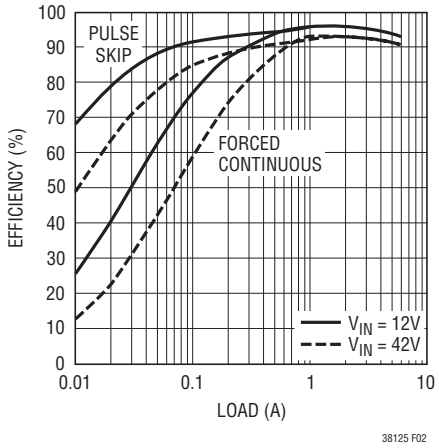


Figure 2. Efficiency in Pulse-Skipping/Forced Continuous Modes

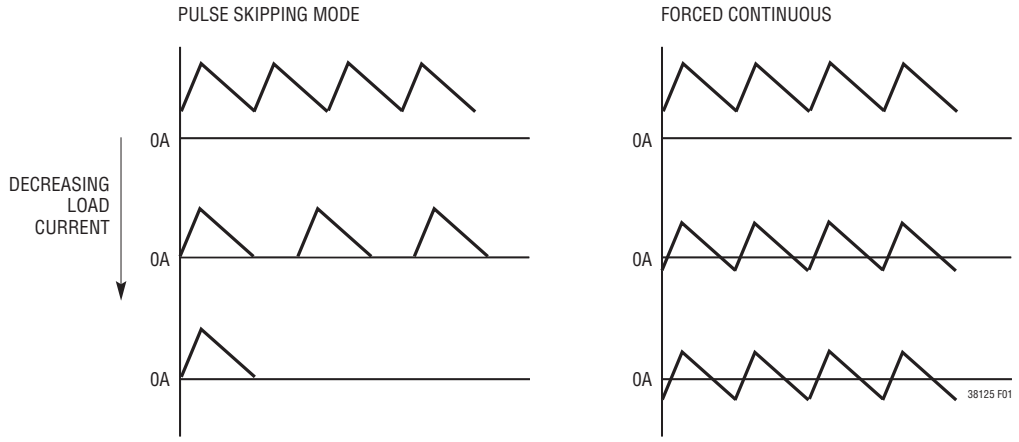


Figure 1. Comparison of Inductor Current Waveforms for Pulse-Skipping Mode and Forced Continuous Operation

OPERATION

level to initiate another cycle. In this mode, frequency is proportional to load current at light loads.

Pulse-skipping mode operation is disabled by comparator F when the FCB pin is brought below 0.8V, forcing continuous synchronous operation. Forced continuous mode is less efficient due to resistive losses, but has the advantage of better transient response at low currents, approximately constant frequency operation, and the ability to maintain regulation when sinking current.

Fault Monitoring/Protection

Constant on-time current mode architecture provides accurate cycle-by-cycle current limit protection—a feature that is very important for protecting the high voltage power supply from output short-circuits. The cycle-by-cycle current monitor guarantees that the inductor current will never exceed the value programmed on the V_{RNG} pin.

Foldback current limiting provides further protection if the output is shorted to ground. As V_{FB} drops, the buffered current threshold voltage I_{THB} is pulled down and clamped to 1V. This reduces the inductor valley current level to one-sixth of its maximum value as V_{FB} approaches 0V. Foldback current limiting is disabled at start-up.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point after the internal 120µs power bad mask timer expires. Furthermore, in an overvoltage condition, M1 is turned off and M2 is turned on immediately and held on until the overvoltage condition clears.

The LTC3812-5 provides an undervoltage lockout comparator for the $INTV_{CC}$ supply. The $INTV_{CC}$ UV threshold is 4.2V to guarantee that the MOSFETs have sufficient gate drive voltage before turning on. If $INTV_{CC}$ is under the UV threshold, the LTC3812-5 is shut down and the drivers are turned off.

Strong Gate Drivers

The LTC3812-5 contains very low impedance drivers capable of supplying amps of current to slew large MOSFET gates quickly. This minimizes transition losses and allows paralleling MOSFETs for higher current applications. A 60V floating high side driver drives the topside MOSFET and a low side driver drives the bottom side MOSFET (see Figure 3). The bottom side driver is supplied directly from the $INTV_{CC}$ pin. The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle through an external diode from $INTV_{CC}$ when the top MOSFET turns off. In pulse-skipping mode operation, where it is possible that the bottom MOSFET will be off for an extended period of time, an internal timeout guarantees that the bottom MOSFET is turned on at least once every 25µs for one on-time period to refresh the bootstrap capacitor.

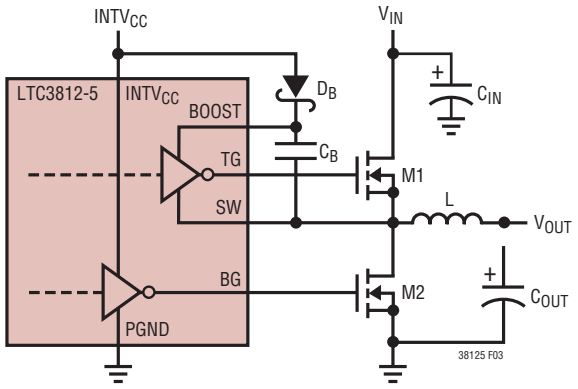


Figure 3. Floating TG Driver Supply and Negative BG Return

IC/Driver Supply Power

The LTC3812-5's internal control circuitry and top and bottom MOSFET drivers operate from a supply voltage ($INTV_{CC}$ pin) in the range of 4.2V to 14V. The LTC3812-5 has two integrated linear regulator controllers to easily generate this IC/driver supply from either the high voltage input or from the output voltage. For best efficiency the supply is derived from the input voltage during start-up and then derived from the lower voltage output as soon as the output is higher than 4.7V. Alternatively, the supply can be derived from the input continuously if the output is < 4.7V or an external supply in the appropriate range can be used. The LTC3812-5 will automatically detect which mode is being used and operate properly.

OPERATION

The four possible operating modes for generating this supply are summarized as follows (see Figure 4):

1. LTC3812-5 generates a 5.5V start-up supply from a small external SOT-23 NMOS acting as linear regulator with drain connected to V_{IN} and gate controlled by the LTC3812-5's internal linear regulator controller through the NDRV pin. As soon as the output voltage reaches 4.7V, the 5.5V IC/driver supply is derived from the output through an internal low dropout regulator to optimize efficiency. If the output is lost due to a short, the LTC3812-5 goes through repeated low duty cycle soft-start cycles (with the drivers shut off in between) to attempt to bring up the output without burning up the SOT-23 NMOS. This scheme eliminates the long start-up times associated with a conventional trickle charger by using an external NMOS to quickly charge the IC/driver supply capacitor (C_{INTVCC}).
2. Similar to (1) except that the external NMOS is used for continuous IC/driver power instead of just for start-up. The NMOS is sized for proper dissipation and the driver shutdown/restart for V_{OUT} < 4.7V is disabled. This scheme is less efficient but may be necessary if V_{OUT} < 4.7V and a boost network is not desired.
3. Trickle charge mode provides an even simpler approach by eliminating the external NMOS. The IC/driver supply capacitors are charged through a single high valued resistor connected to the input supply. When the $INTV_{CC}$ voltage reaches the turn-on threshold of 9V (automatically raised from 4.2V to provide extra headroom for start-up), the drivers turn on and begin charging up the output capacitor. When the output reaches 4.7V, IC/driver power is derived from the output. In trickle-charge mode, the supply capacitors must have sufficient capacitance such that they are not discharged below the 4V $INTV_{CC}$ UV threshold before the output is high enough to take over or else the power supply will not start.
4. Low voltage supply available. The simplest approach is if a low voltage supply (between 4.2V and 14V) is available and connected directly to the IC/driver supply pins.

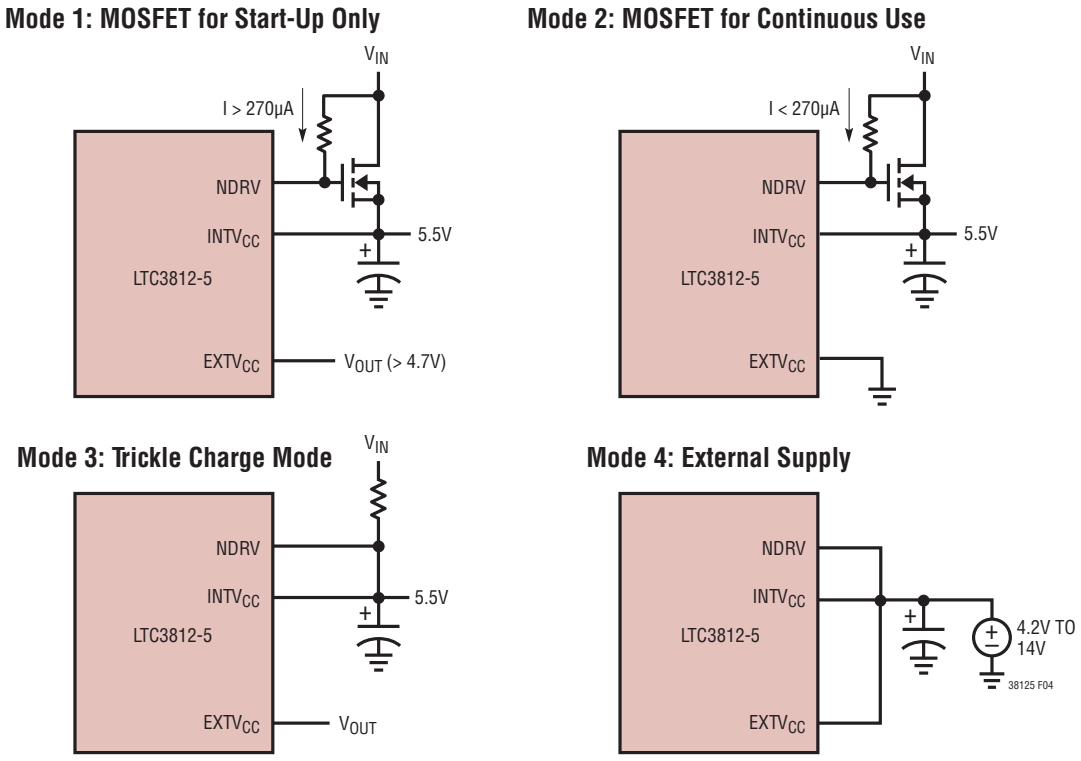


Figure 4. Operating Modes for IC/Driver Supply

APPLICATIONS INFORMATION

The basic LTC3812-5 application circuit is shown on the first page of this data sheet. External component selection is primarily determined by the maximum input voltage and load current and begins with the selection of the power MOSFET switches. The LTC3812-5 uses the on-resistance of the synchronous power MOSFET for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Next, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification. Finally, loop compensation components are selected to meet the required transient/phase margin specifications.

MAXIMUM SENSE VOLTAGE AND V_{RNG} PIN

Inductor current is determined by measuring the voltage across a sense resistance (the on-resistance of the bottom MOSFET) that appears between the PGND and SW pins. The maximum sense voltage is set by the voltage applied to the V_{RNG} pin and is equal to approximately:

$$V_{SENSE(MAX)} = 0.173V_{RNG} – 0.026$$

The current mode control loop will not allow the inductor current valleys to exceed $V_{SENSE(MAX)}/R_{SENSE}$. In practice, one should allow some margin for variations in the LTC3812-5 and external component values and a good guide for selecting the sense resistance is:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{1.3 \bullet I_{OUT(MAX)}}$$

An external resistive divider from $INTV_{CC}$ can be used to set the voltage of the V_{RNG} pin between 0.5V and 2V resulting in nominal sense voltages of 60mV to 320mV. Additionally, the V_{RNG} pin can be tied to SGND or $INTV_{CC}$ in which case the nominal sense voltage defaults to 95mV or 215mV, respectively.

POWER MOSFET SELECTION

The LTC3812-5 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage BV_{DSS}, threshold voltage $V_{(GS)TH}$, on-resistance $R_{DS(ON)}$, input capacitance and maximum current $I_{DS(MAX)}$.

Since the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho_T}$$

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature (see Figure 5) and typically varies from 0.4%/°C to 1.0%/°C depending on the particular MOSFET used.

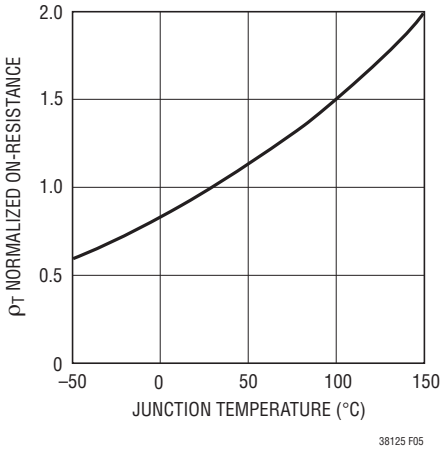


Figure 5. $R_{DS(ON)}$ vs Temperature

APPLICATIONS INFORMATION

The most important parameter in high voltage applications is breakdown voltage BV_{DSS}. Both the top and bottom MOSFETs will see full input voltage plus any additional ringing on the switch node across its drain-to-source during its off-time and must be chosen with the appropriate breakdown specification. The LTC3812-5 is designed to be used with a 4.5V to 14V gate drive supply ($INTV_{CC}$ pin) for driving logic-level MOSFETs ($V_{GS(MIN)} \geq 4.5V$).

For maximum efficiency, on-resistance $R_{DS(ON)}$ and input capacitance should be minimized. Low $R_{DS(ON)}$ minimizes conduction losses and low input capacitance minimizes transition losses. MOSFET input capacitance is a combination of several components but can be taken from the typical "gate charge" curve included on most data sheets (Figure 6).

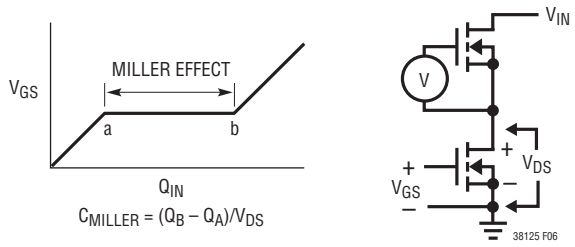


Figure 6. Gate Charge Characteristic

The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturers data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{TOP} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(\rho_T)R_{DS(ON)} + V_{IN}^2\frac{I_{MAX}}{2}(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{CC} - V_{TH(IL)}} + \frac{1}{V_{TH(IL)}}\right](f)$$

$$P_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(\rho_T)R_{DS(ON)}$$

where ρ_T is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential and the change in drain potential in the particular application. $V_{TH(IL)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified

APPLICATIONS INFORMATION

drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the topside N-channel equation incudes an additional term for transition losses, which peak at the highest input voltage. For high input voltage low duty cycle applications that are typical for the LTC3812-5, transition losses are the dominate loss term and therefore using higher $R_{DS(ON)}$ device with lower C_{MILLER} usually provides the highest efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period. Since there is no transition loss term in the synchronous MOSFET, optimal efficiency is obtained by minimizing $R_{DS(ON)}$ —by using larger MOSFETs or paralleling multiple MOSFETS.

Multiple MOSFETs can be used in parallel to lower $R_{DS(ON)}$ and meet the current and thermal requirements if desired. The LTC3812-5 contains large low impedance drivers capable of driving large gate capacitances without significantly slowing transition times. In fact, when driving MOSFETs with very low gate charge, it is sometimes helpful to slow down the drivers by adding small gate resistors (10Ω or less) to reduce noise and EMI caused by the fast transitions.

OPERATING FREQUENCY

The choice of operating frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance in order to maintain low output ripple voltage.

The operating frequency of LTC3812-5 applications is determined implicitly by the one-shot timer that controls the on-time t_{ON} of the top MOSFET switch. The on-time is set by the current out of the I_{ON} pin and the voltage at the V_{ON} pin according to:

$$t_{ON} = \frac{2.4V}{I_{ION}}(76pF)$$

Tying a resistor R_{ON} from V_{IN} to the I_{ON} pin yields an on-time inversely proportional to V_{IN}. For a step-down converter, this results in approximately constant frequency operation as the input supply varies:

$$f = \frac{V_{OUT}}{2.4V \bullet R_{ON}(76pF)}\ [\ Hz]$$

Figure 7 shows how R_{ON} relates to switching frequency for several common output voltages.

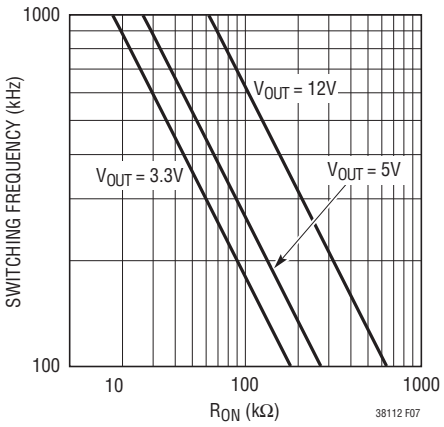


Figure 7. Switching Frequency vs R_{ON}

APPLICATIONS INFORMATION

MINIMUM OFF-TIME AND DROPOUT OPERATION

The minimum off-time $t_{OFF(MIN)}$ is the smallest amount of time that the LTC3812-5 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 250ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

A plot of maximum duty cycle vs frequency is shown in Figure 8.

INDUCTOR SELECTION

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f\,L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f\,\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

SCHOTTKY DIODE D1 SELECTION

The Schottky diode D1 shown in the front page schematic conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half to one fifth of the full load current since

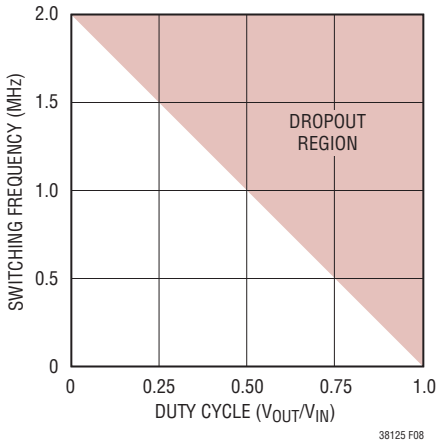


Figure 8. Maximum Switching Frequency vs Duty Cycle

APPLICATIONS INFORMATION

it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently. The diode can be omitted if the efficiency loss is tolerable.

INPUT CAPACITOR SELECTION

In continuous mode, the drain current of the top MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN} which must be supplied by the input capacitor. To prevent large input transients, a low ESR input capacitor sized for the maximum RMS current is given by:

$$I_{CIN(RMS)} \cong I_{O(MAX)} \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{O(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Because tantalum and OS-CON capacitors are not available in voltages above 30V, ceramics or aluminum electrolytics must be used for regulators with input supplies above 30V. Ceramic capacitors have the advantage of very low ESR and can handle high RMS current, but ceramics with high voltage ratings (> 50V) are not available with more than a few microfarads of capacitance. Furthermore, ceramics have high voltage coefficients which means that the capacitance values decrease even more when used at the rated voltage. X5R and X7R type ceramics are recommended for their lower voltage and temperature coefficients. Another consideration when using ceramics is their high Q which, if not properly damped, may result in excessive voltage stress on the power MOSFETs. Aluminum electrolytics have much higher bulk capacitance, but they have higher ESR and lower RMS current ratings.

A good approach is to use a combination of aluminum electrolytics for bulk capacitance and ceramics for low ESR and RMS current. If the RMS current cannot be handled by the aluminum capacitors alone, when used together, the percentage of RMS current that will be supplied by the aluminum capacitor is reduced to approximately:

$$\%\, I_{RMS,ALUM} \approx \frac{1}{\sqrt{1+(8fCR_{ESR})^2}} \bullet 100\%$$

where R_{ESR} is the ESR of the aluminum capacitor and C is the overall capacitance of the ceramic capacitors. Using an aluminum electrolytic with a ceramic also helps damp the high Q of the ceramic, minimizing ringing.

OUTPUT CAPACITOR SELECTION

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple. The output ripple (ΔV_{OUT}) is approximately equal to:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. ESR also has a significant effect on the load transient response. Fast load transitions at the output will appear as voltage across the ESR of C_{OUT} until the feedback loop in the LTC3812-5 can change the inductor current to match the new load current value. Typically, once the ESR requirement is satisfied the capacitance is adequate for filtering and has the required RMS current rating.

Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance throughhole capacitors. The OS-CON (organic semiconductor dielectric) capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the effect of their lead inductance.

In surface mount applications, multiple capacitors placed in parallel may be required to meet the ESR, RMS current

APPLICATIONS INFORMATION

handling and load step requirements. Dry tantalum, special polymer and aluminum electrolytic capacitors are available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Several excellent surge-tested choices are the AVX TPS and TPSV or the KEMET T510 series. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-driven applications providing that consideration is given to ripple current ratings and long term reliability. Other capacitor types include Panasonic SP and Sanyo POSCAPs.

OUTPUT VOLTAGE

The LTC3812-5 output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = 0.8V\left(1+\frac{R_{FB1}}{R_{FB2}}\right)$$

The external resistor divider is connected to the output as shown in the Functional Diagram, allowing remote voltage sensing. The resultant feedback signal is compared with the internal precision 800mV voltage reference by the error amplifier. The internal reference has a guaranteed tolerance of less than ±1%. Tolerance of the feedback resistors will add additional error to the output voltage. 0.1% to 1% resistors are recommended.

TOP MOSFET DRIVER SUPPLY (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from $INTV_{CC}$ when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately $V_{IN} + INTV_{CC}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

The reverse breakdown of the external diode, D_B, must be greater than $V_{IN(MAX)}$. Another important consideration for the external diode is the reverse recovery and reverse leakage, either of which may cause excessive reverse current to flow at full reverse voltage. If the reverse current times reverse voltage exceeds the maximum allowable power dissipation, the diode may be damaged. For best results, use an ultrafast recovery diode such as the MMDL770T1.

IC/MOSFET DRIVER SUPPLY ($INTV_{CC}$)

The LTC3812-5 drivers are supplied from the $INTV_{CC}$ and BOOST pins (see Figure 3), which have an absolute maximum voltage of 14V. Since the main supply voltage, V_{IN} is typically much higher than 14V a separate supply for the IC and driver power ($INTV_{CC}$) must be used. The LTC3812-5 has integrated bias supply control circuitry that allows the IC/driver supply to be easily generated from V_{IN} and/or V_{OUT} with minimal external components. There are four ways to do this as shown in the simplified schematics of Figure 4 and explained in the following sections.

Using the Linear Regulator for $INTV_{CC}$ Supply

In Mode 1, a small external SOT-23 MOSFET, controlled by the NDRV pin, is used to generate a 5.5V start-up supply from V_{IN}. The small SOT-23 package can be used because the NMOS is on continuously only during the brief start-up period. As soon as the output voltage reaches 4.7V, the LTC3812-5 turns off the external NMOS and the LTC3812-5 regulates the 5.5V supply from the $EXTV_{CC}$ pin (connected to V_{OUT} or a V_{OUT} derived boost network) through an internal low dropout regulator. For this mode to work properly, $EXTV_{CC}$ must be in the range $4.7V < EXTV_{CC} < 15V$. If $V_{OUT} < 4.7V$, a charge pump or extra winding can be used to raise $EXTV_{CC}$ to the proper voltage, or alternatively, Mode 2 should be used as explained later in this section. If V_{OUT} is shorted or otherwise goes below the minimum 4.5V threshold, the MOSFET connected to V_{IN} is turned back on to maintain the 5.5V supply. However if the output cannot be brought up within a timeout period,

APPLICATIONS INFORMATION

the drivers are turned off to prevent the SOT-23 MOSFET from overheating. Soft-start cycles are then attempted at low duty cycle intervals to try to bring the output back up (see Figure 9). This fault timeout operation is enabled by choosing the choosing R_{NDRV} such that the resistor current I_{NDRV} is greater than 270µA by using the following formulas:

$$R_{NDRV} \leq \frac{P_{MOSFET(MAX)}/I_{CC} - V_T}{270\mu A}$$

where

$$I_{CC} = (f)(Q_{G(TOP)} + Q_{G(BOTTOM)}) + 3mA$$

and V_T is the threshold voltage of the MOSFET.

The value of R_{NDRV} also affects the $V_{IN(MIN)}$ as follows:

$$V_{IN(MIN)} = V_{INTVCC(MIN)} + (40\mu A)\ R_{NDRV} + V_T \qquad (1)$$

where $V_{INTVCC(MIN)}$ is normally 4.5V for driving logic level MOSFETs. If minimum V_{IN} is not low enough, consider reducing R_{NDRV} and/or using a darlington NPN instead of an NMOS to reduce V_T to ~1.4V.

When using R_{NDRV} equal to the computed value, the LTC3812-5 will enable the low duty cycle soft-start retries only when the desired maximum power dissipation, $P_{MOSFET(MAX)}$, in the MOSFET is exceeded and leave the drivers on continuously otherwise. The shutoff/restart times are a function of the RUN/SS capacitor value.

The external NMOS for the linear regulator should be a standard 3V threshold type (i.e., not a logic level threshold). The rate of charge of V_{CC} from 0V to 5.5V is controlled by the LTC3812-5 to be approximately 75µs regardless of the size of the capacitor connected to the $INTV_{CC}$ pin. The charging current for this capacitor is approximately:

$$I_C = \left(\frac{5.5V}{75\mu s}\right) C_{INTVCC}$$

The safe operating area (SOA) for the external NMOS should be chosen so that capacitor charging does not damage the NMOS. Excessive values of capacitor are unnecessary and should be avoided. Typically values in the 1µF to 10µF work well.

One more design requirement for this mode is the minimum soft-start capacitor value. The fault timeout is enabled when RUN/SS voltage is greater than 4V. This gives the power supply time to bring the output up before it starts the timeout sequence. To prevent timeout sequence from starting prematurely during start-up, a minimum C_{SS} value is necessary to ensure that $V_{RUN/SS} < 4V$ until $V_{EXTVCC} > 4.7V$. To ensure this, choose:

$$C_{SS} > C_{OUT} \bullet (2.3 \bullet 10^{-6})/I_{OUT(MAX)}$$

Mode 2 should be used if V_{OUT} is outside of the $4.7V < EXTV_{CC} < 15V$ operating range and the extra complexity of a charge pump or extra inductor winding is not wanted

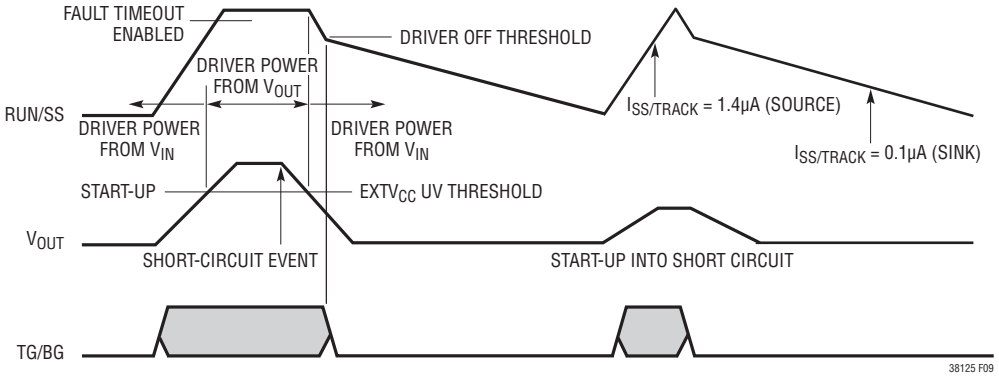


Figure 9. Fault Timeout Operation

APPLICATIONS INFORMATION

to boost this voltage above 4.7V. In this mode, $EXTV_{CC}$ is grounded and the NMOS is chosen to handle the worst-case power dissipation:

$$P_{MOSFET} = (V_{IN(MAX)})[(f)(Q_{G(TOP)} + Q_{G(BOTTOM)} + 3mA]$$

To operate properly, the fault timeout operation must be disabled by choosing

$$R_{NDRV} > (V_{IN(MAX)} – 5.5V – V_T)/270\mu A$$

If the required R_{NDRV} value results in an unacceptable value for $V_{IN(MIN)}$ (see Equation 1), fault timeout operation can also be disabled by connecting a 500k to 1M resistor from RUN/SS to $INTV_{CC}$.

Using Trickle Charge Mode

Trickle charge mode is selected by shorting NDRV and $INTV_{CC}$ and connecting $EXTV_{CC}$ to V_{OUT}. Trickle charge mode has the advantage of not requiring an external MOSFET but takes longer to start up due to slow charge up of C_{INTVCC} through R_{PULLUP} ($t_{DELAY} = 0.77 • R_{PULLUP} • C_{INTVCC}$) and usually requires a larger $INTV_{CC}$ capacitor value to hold up the supply voltage during start-up. Once the $INTV_{CC}$ voltage reaches the trickle charge UV threshold of 9V, the drivers will turn on and start discharging C_{INTVCC} at a rate determined by the driver current I_G. In order to ensure proper start-up, C_{INTVCC} must be chosen large enough so that the $EXTV_{CC}$ voltage reaches the switchover threshold of 4.7V before C_{INTVCC} discharges below the falling UV threshold of 4V. This is ensured if:

$$C_{INTVCC} > I_G • \left(\text{Larger of } \frac{C_{OUT}}{I_{MAX}} \text{ or } \frac{5.5 • 10^5 • C_{SS}}{V_{OUT(REG)}} \right)$$

where I_G is the gate drive current = $(f)(Q_{G(TOP)} + Q_{G(BOTTOM)})$ and I_{MAX} is the maximum inductor current selected by V_{RNG}.

For R_{PULLUP}, the value should fall in the following range to ensure proper start-up:

$$\text{Min } R_{PULLUP} > (V_{IN(MAX)} – 14V)/I_{CCSR}$$

$$\text{Max } R_{PULLUP} < (V_{IN(MIN)} – 9V)/I_{Q,SHUTDOWN}$$

Using an External Supply Connected to the $INTV_{CC}$

If an external supply is available between 4.2V and 14V, the supply can be connected directly to the $INTV_{CC}$ pins. In this mode, $INTV_{CC}$, $EXTV_{CC}$ and NDRV must be shorted together.

$INTV_{CC}$ Supply and the $EXTV_{CC}$ Connection

The LTC3812-5 contains an internal low dropout regulator to produce the 5.5V $INTV_{CC}$ supply from the $EXTV_{CC}$ pin voltage. This regulator turns on when the $EXTV_{CC}$ pin is above 4.7V and remains on until $EXTV_{CC}$ drops below 4.45V. This allows the IC/MOSFET power to be derived from the output or an output derived boost network during normal operation and from the external NMOS from V_{IN} during start-up or short-circuit. Using the $EXTV_{CC}$ pin in this way results in significant efficiency gains compared to what would be possible when deriving this power continuously from the typically much higher V_{IN} voltage. The $EXTV_{CC}$ connection also allows the power supply to be configured in trickle charge mode in which it starts up with a high-valued “bleed” resistor connected from V_{IN} to $INTV_{CC}$ to charge up the $INTV_{CC}$ capacitor. As soon as the output rises above 4.7V the internal $EXTV_{CC}$ regulator takes over before the $INTV_{CC}$ capacitor discharges below the UV threshold. When the $EXTV_{CC}$ regulator is active, the $EXTV_{CC}$ pin can supply up to 50mA RMS. Do not apply more than 15V to the $EXTV_{CC}$ pin. The following list summarizes the possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This connection will require $INTV_{CC}$ to be powered continuously from an external NMOS from V_{IN} resulting in an efficiency penalty as high as 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for 4.7V < V_{OUT} < 15V and provides the highest efficiency. The power supply will start up using an external NMOS or a bleed resistor until the output supply is available.
3. $EXTV_{CC}$ connected to an output-derived boost network. If V_{OUT} < 4.7V. The low voltage output can be boosted using a charge pump or flyback winding to greater than 4.7V.
4. $EXTV_{CC}$ connected to $INTV_{CC}$. This is the required connection for $EXTV_{CC}$ if $INTV_{CC}$ is connected to an external supply where the external supply is 4.2V < V_{EXT} < 14V.

APPLICATIONS INFORMATION

Applications using large MOSFETs with a high input voltage and high frequency of operation may result in a large $EXTV_{CC}$ pin current. Due to the LTC3812-5 thermally enhanced package, maximum junction temperature will rarely be exceeded, however, it is good design practice to verify that the maximum junction temperature rating and RMS current rating are within the maximum limits. Typically, most of the $EXTV_{CC}$ current consists of the MOSFET gates current. In continuous mode operation, this $EXTV_{CC}$ current is:

$$I_{EXTVCC} = f(Q_{G(TOP)} + Q_{G(BOTTOM)}) + 3mA < 50mA$$

The junction temperature can be estimated from the equations given in Note 2 of the Electrical Characteristics as follows:

$$T_J = T_A + I_{EXTVCC} \bullet (V_{EXTVCC} - V_{INTVCC})(38°C/W) < 125°C$$

If absolute maximum ratings are exceeded, consider using an external supply connected directly to the $INTV_{CC}$ pin.

FEEDBACK LOOP/COMPENSATION

Feedback Loop Types

In a typical LTC3812-5 circuit, the feedback loop consists of the modulator, the output filter and load, and the feedback amplifier with its compensation network. All of these components affect loop behavior and must be accounted for in the loop compensation. The modulator and output filter consists of the internal current comparator, the output MOSFET drivers and the external MOSFETs, inductor and output capacitor. Current mode control eliminates the effect of the inductor by moving it to the inner loop, reducing it to a first order system. From a feedback loop point of view, it looks like a linear voltage controlled current source from I_{TH} to V_{OUT} and has a gain equal to $(I_{MAX}R_{OUT})/1.2V$. It has fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency. The external output capacitor and load cause a first order roll off at the output at the $R_{OUT}C_{OUT}$ pole frequency, with the attendant 90° phase shift. This roll off is what filters the PWM waveform, resulting in the desired DC output voltage. The output capacitor also contributes a zero at the $C_{OUT}R_{ESR}$ frequency which adds back the 90° phase and cancels the first order roll off.

So far, the AC response of the loop is pretty well out of the user's control. The modulator is a fundamental piece of the LTC3812-5 design and the external output capacitor is usually chosen based on the regulation and load current requirements without considering the AC loop response. The feedback amplifier, on the other hand, gives us a handle with which to adjust the AC response. The goal is to have 180° phase shift at DC (so the loop regulates), and something less than 360° phase shift (preferably about 300°) at the point that the loop gain falls to 0dB, i.e., the crossover frequency, with as much gain as possible at frequencies below the crossover frequency. Since the modulator/output filter is a first order system with maximum of 90° phase shift (at frequencies below $f_{SW}/4$) and the feedback amplifier adds another 90° of phase shift, some phase boost is required at the crossover frequency to achieve good phase margin. If the ESR zero is below the crossover frequency, this zero may provide enough phase boost to achieve the desired phase margin and the only requirement of the compensation will be to guarantee that the gain is below zero at frequencies above $f_{SW}/4$. If the ESR zero is above the crossover frequency, the feedback amplifier will probably be required to provide phase boost. For most LTC3810 applications, Type 2 compensation will provide enough phase boost; however some applications where high bandwidth is required with low ESR ceramics and lots of bulk capacitance, Type 3 compensation may be necessary to provide additional phase boost.

The two types of compensation networks, "Type 2" and "Type 3" are shown in Figures 10 and 11. When component values are chosen properly, these networks provide

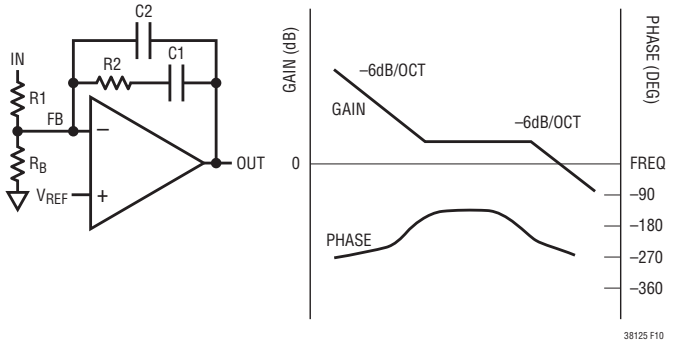


Figure 10. Type 2 Schematic and Transfer Function

APPLICATIONS INFORMATION

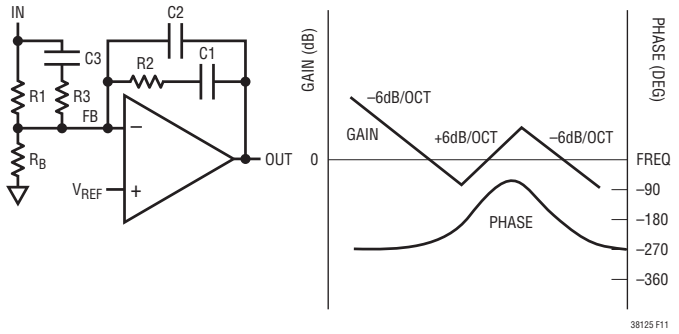


Figure 11. Type 3 Schematic and Transfer Function

a "phase bump" at the crossover frequency. Type 2 uses a single pole-zero pair to provide up to about 60° of phase boost while Type 3 uses two poles and two zeros to provide up to 150° of phase boost.

Feedback Component Selection

Selecting the R and C values for a typical Type 2 or Type 3 loop is a nontrivial task. The applications shown in this data sheet show typical values, optimized for the power components shown. They should give acceptable performance with similar power components, but can be way off if even one major power component is changed significantly. Applications that require optimized transient response will require recalculation of the compensation values specifically for the circuit in question. The underlying mathematics are complex, but the component values can be calculated in a straightforward manner if we know the gain and phase of the modulator at the crossover frequency.

Modulator gain and phase can be obtained in one of three ways: measured directly from a breadboard, or if the appropriate parasitic values are known, simulated or generated from the modulator transfer function. Measurement will give more accurate results, but simulation or transfer function can often get close enough to give a working system. To measure the modulator gain and phase directly, wire up a breadboard with an LTC3812-5 and the actual MOSFETs, inductor and input and output capacitors that the final design will use. This breadboard should use appropriate construction techniques for high speed analog circuitry: bypass capacitors located close to the LTC3812-5, no long wires connecting components, appropriately sized ground returns, etc. Wire the feedback amplifier with a 0.1µF feedback capacitor from I_{TH} to FB and a 10k to 100k resistor from V_{OUT} to FB. Choose the bias resistor (R_B) as required to set the desired output voltage. Disconnect R_B from ground and connect it to a signal generator or to the source output of a network analyzer to inject a test signal into the loop. Measure the gain and phase from the I_{TH} pin to the output node at the positive terminal of the output capacitor. Make sure the analyzer's input is AC-coupled so that the DC voltages present at both the I_{TH} and V_{OUT} nodes don't corrupt the measurements or damage the analyzer.

If breadboard measurement is not practical, a SPICE simulation can be used to generate approximate gain/phase curves. Plug the expected capacitor, inductor and MOSFET values into the following SPICE deck and generate an AC plot of V_{OUT}/V_{ITH} with gain in dB and phase in degrees. Refer to your SPICE manual for details of how to generate this plot.

```
*3810 modulator gain/phase
*2006 Linear Technology
*this file simulates a simplified model of
*the LTC3810 for generating a v(out)/v(ith)
*bode plot

.param rdson=.0135 ;MOSFET rdson
.param Vrng=2      ;use 1.4 for INTVCC and
                    0.7 for ground
.param vsnsmax={0.173*Vrng-0.026}
.param Imax={vsnsmax/rdson}
.param DL=4        ;inductor ripple current

*inductor current
gl out 0 value={(v(ith)-1.2)*Imax/1.2+DL/2}

*output cap
cout out out2 270u ;capacitor value
resr out2 0 0.018 ;capacitor ESR

*load
Rout out 0 2 ; load resistor

vstim ith 0 0 ac 1 ;ac stimulus
.ac dec 100 100 10meg
.probe
.end
```

APPLICATIONS INFORMATION

Mathematical software such as MATHCAD or MATLAB can also be used to generate plots using the following transfer function of the modulator:

$$H(s) = \left(\frac{V_{SENSE(MAX)}}{1.2 \bullet R_{DS(ON)}}\right) \bullet \left(\frac{1 + s \bullet R_{ESR} \bullet C_{OUT}}{1 + s \bullet R_L \bullet C_{OUT}}\right) \bullet R_L \quad (2)$$

$$s = j2\pi f$$

With the gain/phase plot in hand, a loop crossover frequency can be chosen. Usually the curves look something like Figure 12. Choose the crossover frequency about 25% of the switching frequency for maximum bandwidth. Although it may be tempting to go beyond $f_{SW}/4$, remember that significant phase shift occurs at half the switching frequency that isn't modeled in the above H(s) equation and PSPICE code. Note the gain (GAIN, in dB) and phase (PHASE, in degrees) at this point. The desired feedback amplifier gain will be –GAIN to make the loop gain at 0dB at this frequency. Now calculate the needed phase boost, assuming 60° as a target phase margin:

BOOST = – (PHASE + 30°)

If the required BOOST is less than 60°, a Type 2 loop can be used successfully, saving two external components. BOOST values greater than 60° usually require Type 3 loops for satisfactory performance.

Finally, choose a convenient resistor value for R1 (10k is usually a good value). Now calculate the remaining values:

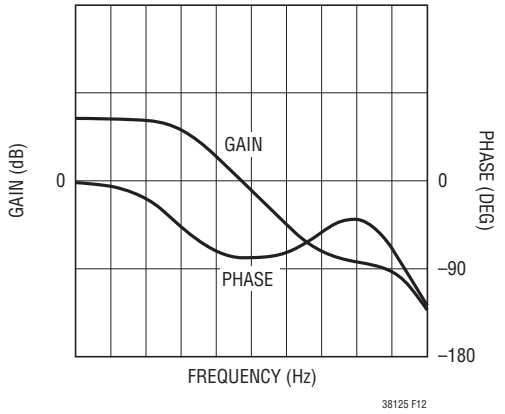


Figure 12. Transfer Function of Buck Modulator

(K is a constant used in the calculations)

f = chosen crossover frequency

G = $10^{(GAIN/20)}$ (this converts GAIN in dB to G in absolute gain)

TYPE 2 Loop:

$$K = \tan\left(\frac{BOOST}{2} + 45°\right)$$

$$C2 = \frac{1}{2\pi \bullet f \bullet G \bullet K \bullet R1}$$

$$C1 = C2\left(K^2 - 1\right)$$

$$R2 = \frac{K}{2\pi \bullet f \bullet C1}$$

$$R_B = \frac{V_{REF}(R1)}{V_{OUT} - V_{REF}}$$

TYPE 3 Loop:

$$K = \tan^2\left(\frac{BOOST}{4} + 45°\right)$$

$$C2 = \frac{1}{2\pi \bullet f \bullet G \bullet R1}$$

$$C1 = C2(K - 1)$$

$$R2 = \frac{\sqrt{K}}{2\pi \bullet f \bullet C1}$$

$$R3 = \frac{R1}{K - 1}$$

$$C3 = \frac{1}{2\pi f \sqrt{K} \bullet R3}$$

$$R_B = \frac{V_{REF}(R1)}{V_{OUT} - V_{REF}}$$

SPICE or mathematical software can be used to generate the gain/phase plots for the compensated power supply to do a sanity check on the component values before trying them out on the actual hardware. For software, use the following transfer function:

T(s) = A(s)H(s)

APPLICATIONS INFORMATION

where H(s) was given in equation 2 and A(s) depends on compensation circuit used:

Type 2:

$$A(s)=\frac{1+s\bullet R2\bullet C1}{s\bullet R1\bullet(C1+C2)\bullet\left(1+s\bullet R2\bullet\frac{C1\bullet C2}{C1+C2}\right)}$$

Type 3:

$$A(s)=\frac{1}{s\bullet R1\bullet(C1+C2)}\bullet\frac{(1+s\bullet(R1+R3)\bullet C3)\bullet(1+s\bullet R2\bullet C1)}{(1+s\bullet R3\bullet C3)\bullet\left(1+s\bullet R2\bullet\frac{C1\bullet C2}{C1+C2}\right)}$$

For SPICE, replace VSTIM line in the previous PSPICE code with following code and generate a gain/phase plot of V(out)/V(outin):

```
rfb1 outin vfb 52.5k
rfb2 vfb 0 10k
eithx ithx 0 laplace {0.8-v(vfb)} =
      {1/(1+s/1000)}
eith ith 0 value={limit(1e6*v(ithx),0,2.4)}
cc1 ith vfb 4p
cc2 ith x1 8p
rc x1 vfb 210k
rf outin x2 11k ;delete this line for Type 2
cf x2 vfb 120p ;delete this line for Type 2
vstim out outin dc=0 ac=1m
```

PULSE-SKIPPING MODE OPERATION AND FCB PIN

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 0.8V threshold enables pulse-skipping mode operation where the bottom MOSFET turns off when inductor current reverses. The load current at which current reverses and discontinuous operation begins depends on the amplitude of the inductor ripple current and will vary with changes in V_{IN}. Tying the FCB pin below the 0.8V threshold forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation. To prevent forcing current back into the main power supply, potentially boosting the input supply to a dangerous voltage level, forced continuous mode of operation is disabled when the RUN/SS voltage is below 2.5V during soft-start or tracking. During these two periods, the PGOOD signal is forced low.

In addition to providing a logic input to force continuous operation, the FCB pin provides a mean to maintain a flyback winding output when the primary is operating in pulse-skipping mode. The secondary output V_{OUT2} is normally set as shown in Figure 13 by the turns ratio N of the transformer. However, if the controller goes into pulse-skipping mode and halts switching due to a light primary load current, then V_{OUT2} will droop. An external resistor divider from V_{OUT2} to the FCB pin sets a minimum voltage $V_{OUT2(MIN)}$ below which continuous operation is forced until V_{OUT2} has risen above its minimum.

$$V_{OUT2(MIN)}=0.8V\left(1+\frac{R4}{R3}\right)$$

Table 1

FCB PIN	CONDITION
DC Voltage: 0V to 0.75V	Forced Continuous Current Reversal Enabled
DC Voltage: ≥0.85V	Pulse-Skipping Mode Operation No Current Reversal
Feedback Resistors	Regulating a Secondary Winding

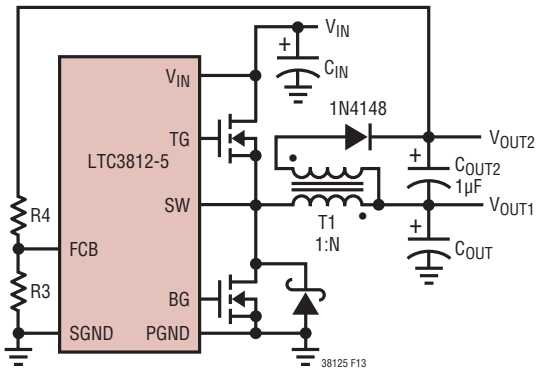


Figure 13. Secondary Output Loop

APPLICATIONS INFORMATION

FAULT CONDITIONS: CURRENT LIMIT AND FOLDBACK

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3812-5, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SNS(MAX)}}{R_{DS(ON)}\ \rho_T} + \frac{1}{2}\Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of I_{LIMIT} which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same percentage below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

To further limit current in the event of a short-circuit to ground, the LTC3812-5 includes foldback current limiting. If the output falls by more than 60%, then the maximum sense voltage is progressively lowered to about one tenth of its full value.

Be aware also that when the fault timeout is enabled for the external NMOS regulator, an over current limit may cause the output to fall below the minimum 4.5V UV threshold. This condition will cause a linear regulator timeout/restart sequence as described in the Linear Regulator Timeout section if this condition persists.

RUN/SOFT-START FUNCTION

The RUN/SS pin is a multipurpose pin that provides a soft-start function and a means to shut down the LTC3812-5. Soft-start reduces the input supply's surge current by controlling the ramp rate of the output voltage, eliminates output overshoot and can also be used for power supply sequencing.

Pulling RUN/SS below 1.5V puts the LTC3812-5 into a low quiescent current shutdown (I_Q = 224µA). This pin can be driven directly from logic as shown in Figure 14. Releasing the RUN/SS pin allows an internal 1.4µA current source to charge up the soft-start capacitor, C_{SS}. When the voltage on RUN/SS reaches 1.5V, the LTC3812-5 turns on and begins regulating the output to $V_{FB} = V_{SS} – 1.5V$. As the RUN/SS voltage increases from 1.5V to 2.3V, the output voltage is raised from 0% to 100% of its regulated value. Current foldback, forced continuous mode and fault timeout are disabled during this soft-start phase and PGOOD signal is forced low. The RUN/SS voltage continues to charge until it reaches its internally clamped value of 4V.

If RUN/SS starts at 0V, the delay before starting is approximately:

$$t_{DELAY,START} = \frac{1.5V}{1.4\mu A} C_{SS} = (1.1s/\mu F) C_{SS}$$

plus an additional delay, before the output will reach its regulated value of:

$$t_{DELAY,REG} \geq \frac{0.8V}{1.4\mu A} C_{SS} = (0.6s/\mu F) C_{SS}$$

The start delay can be reduced by using diode D1 in Figure 14.

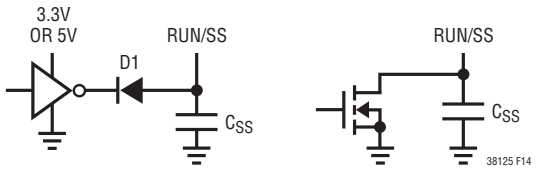


Figure 14. RUN/SS Pin Interfacing

APPLICATIONS INFORMATION

EFFICIENCY CONSIDERATIONS

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3812-5 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)} = 0.01\Omega$ and $R_L = 0.005\Omega$, the loss will range from 15mW to 1.5W as the output current varies from 1A to 10A.
2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from the second term of the P_{MAIN} equation found in the Power MOSFET Selection section. When transition losses are significant, efficiency can be improved by lowering the frequency and/or using a top MOSFET(s) with lower C_{RSS} at the expense of higher $R_{DS(ON)}$.
3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents. Control current is typically about 3mA and driver current can be calculated by: $I_{GATE} = f(Q_{G(TOP)} + Q_{G(BOT)})$, where $Q_{G(TOP)}$ and $Q_{G(BOT)}$ are the gate charges of the top and bottom MOSFETs. This loss is proportional to the supply voltage that $INTV_{CC}$ is derived from, i.e., V_{IN} for the external NMOS linear regulator, V_{OUT} for the internal $EXTV_{CC}$ regulator, or V_{EXT} when an external supply is connected to $INTV_{CC}$.
4. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including C_{OUT} ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss. When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

CHECKING TRANSIENT RESPONSE

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

DESIGN EXAMPLE

As a design example, take a supply with the following specifications: $V_{IN} = 12V$ to 60V, $V_{OUT} = 5V \pm 5\%$, $I_{OUT(MAX)} = 6A$, f = 250kHz. First, calculate the timing resistor:

$$R_{ON} = \frac{5V}{2.4V \bullet 250kHz \bullet 76pF} = 110k$$

and choose the inductor for about 40% ripple current at the maximum V_{IN}:

$$L = \frac{5V}{250kHz \bullet 0.4 \bullet 6A}\left(1 - \frac{5V}{60V}\right) = 7.6\mu H$$

With a 7.7µH inductor, ripple current will vary from 1.5A to 2.4A (25% to 40%) over the input supply range.

Next, choose the bottom MOSFET switch. Since the drain of the MOSFET will see the full supply voltage 60V

APPLICATIONS INFORMATION

(max) plus any ringing, choose an 60V MOSFET. The Si7850DP has:

BV_{DSS} = 60V
$R_{DS(ON)}$ = 25mΩ (max)/31mΩ (nom),
δ= 0.007/°C,
C_{MILLER} = (8.3nC – 2.8nC)/30V = 183pF,
$V_{GS(MILLER)}$ = 3.8V,
θ_{JA}= 22°C/W.

This yields a nominal sense voltage of:

$$V_{SNS(NOM)} = 6A \bullet 1.3 \bullet 0.025\Omega = 195mV$$

To guarantee proper current limit at worst-case conditions, increase nominal V_{SNS} by at least 50% to 320mV (by tying V_{RNG} to 2V). To check if the current limit is acceptable at V_{SNS} = 320mV, assume a junction temperature of about 55°C above a 70°C ambient ($\rho_{125°C}$ = 1.7):

$$I_{LIMIT} \geq \frac{320mV}{1.7 \bullet 0.031\Omega} + \frac{1}{2} \bullet 2.4A = 7.3A$$

and double-check the assumed T_J in the MOSFET:

$$P_{BOT} = \frac{60V - 5V}{60V} \bullet 7.3A^2 \bullet 1.7 \bullet 0.031\Omega = 2.6W$$

T_J = 70°C + 2.6W • 22°C/W = 127°C

Verify that the Si7850DP is also a good choice for the top MOSFET by checking its power dissipation at current limit and maximum input voltage, assuming a junction temperature of 30°C above a 70°C ambient ($\rho_{100°C}$ = 1.5):

$$P_{MAIN} = \frac{5V}{60V} \bullet 7.3A^2 (1.5 \bullet 0.031\Omega)$$
$$+ 60V^2 \bullet \frac{7.3A}{2} \bullet 2\Omega \bullet 183pF \bullet \left(\frac{1}{5V - 3.8V} + \frac{1}{3.8V} \right) \bullet 250kHz$$
$$= 0.206W + 1.32W = 1.53W$$

T_J = 70°C + 1.53W • 22°C/W = 104°C

The junction temperature will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking on the board will be necessary in this circuit.

Since V_{OUT} > 4.7V, the $INTV_{CC}$ voltage can be generated from V_{OUT} with the internal LDO by connecting V_{OUT} to the $EXTV_{CC}$ pin. A small SOT23 MOSFET such as the ZXMN10A07F can be used for the pass device if fault timeout is enabled. Choose R_{NDRV} to guarantee that fault timeout is enabled when power dissipation of M3 exceeds 0.4W (max for 70°C ambient):

$$I_{CC} = 250kHz \bullet 2 \bullet 18nC + 3mA = 12mA$$

$$R_{NDRV} \leq \frac{0.4W / 0.012A - 3V}{270\mu A} = 112k$$

So, choose R_{NDRV} = 100k.

C_{IN} is chosen for an RMS current rating of about 3A at 85°C. The output capacitors are chosen for a low ESR of 0.018Ω to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$$\Delta V_{OUT(RIPPLE)} = \Delta I_{L(MAX)} \bullet ESR = 2.4A \bullet 0.018\Omega = 43mV$$

However, a 0A to 6A load step will cause an output change of up to:

$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD} \bullet ESR = 6A \bullet 0.018\Omega = 108mV$$

An optional 10µF ceramic output capacitor is included to minimize the effect of ESL in the output ripple. The complete circuit is shown in Figure 15.

PC Board Layout Checklist

When laying out a PC board follow one of two suggested approaches. The simple PC board layout requires a dedicated ground plane layer. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, C_{OUT}, MOSFETs, D1 and inductor all in one compact area. It may help to have some components on the bottom side of the board.
- Use an immediate via to connect the components to ground plane including SGND and PGND of LTC3812-5. Use several bigger vias for power components.

APPLICATIONS INFORMATION

- Use compact plane for switch node (SW) to improve cooling of the MOSFETs and to keep EMI down.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND or to any other DC rail in your system).

When laying out a printed circuit board, without a ground plane, use the following checklist to ensure proper operation of the controller.

- Segregate the signal and power grounds. All small signal components should return to the SGND pin at one point which is then tied to the PGND pin close to the source of M2.
- Place M2 as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Connect the input capacitor(s) C_{IN} close to the power MOSFETs. This capacitor carries the MOSFET AC current.
- Keep the high dV/dt SW, BOOST and TG nodes away from sensitive small-signal nodes.
- Connect the $INTV_{CC}$ decoupling capacitor C_{VCC} closely to the $INTV_{CC}$ and SGND pins.
- Connect the top driver boost capacitor C_B closely to the BOOST and SW pins.
- Connect the bottom driver decoupling capacitor C_{INTVCC} closely to the $INTV_{CC}$ and PGND pins.

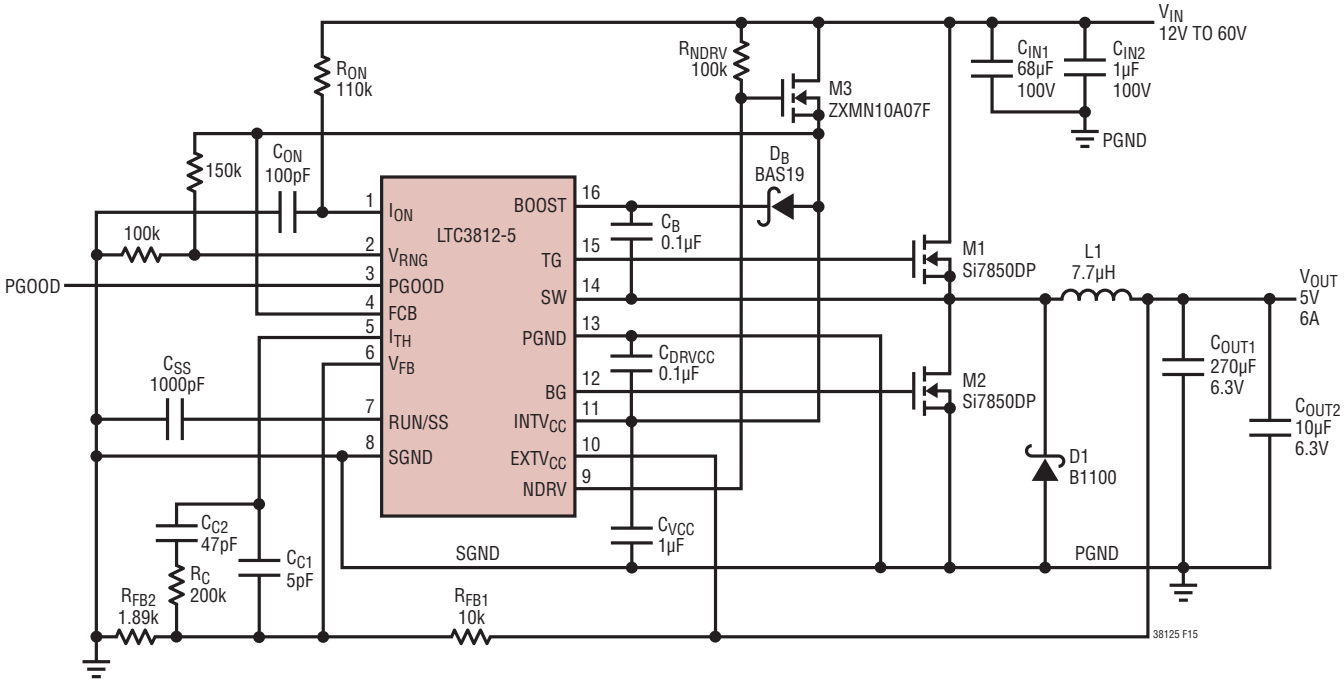
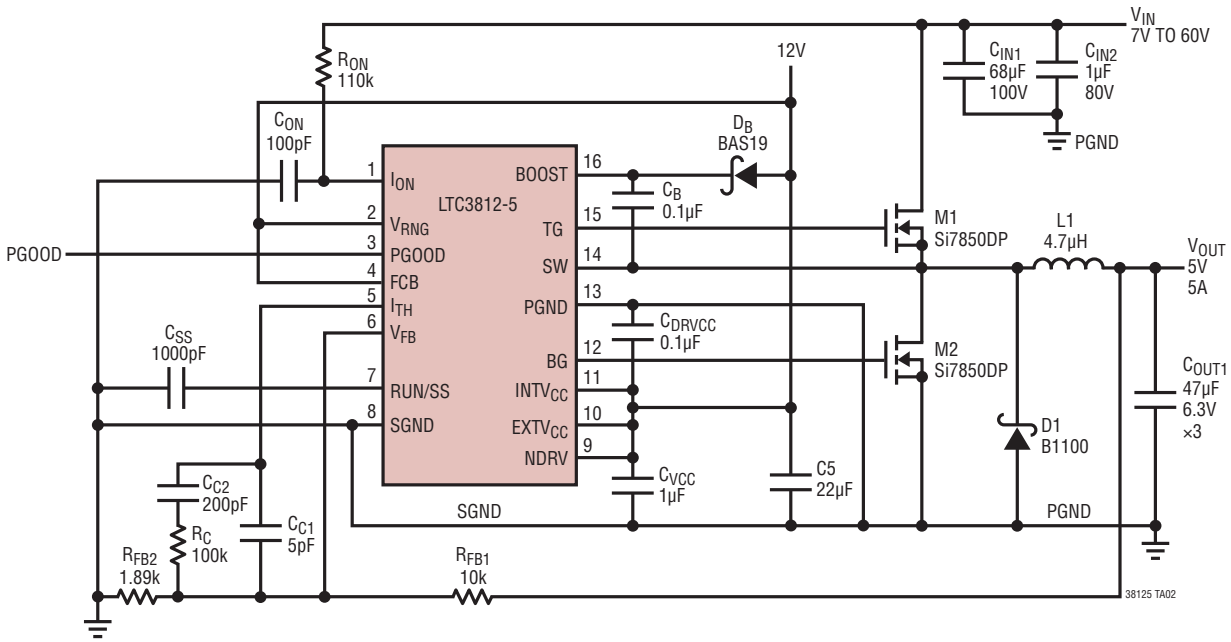


Figure 15. 12V to 60V Input Voltage to 5V/6A

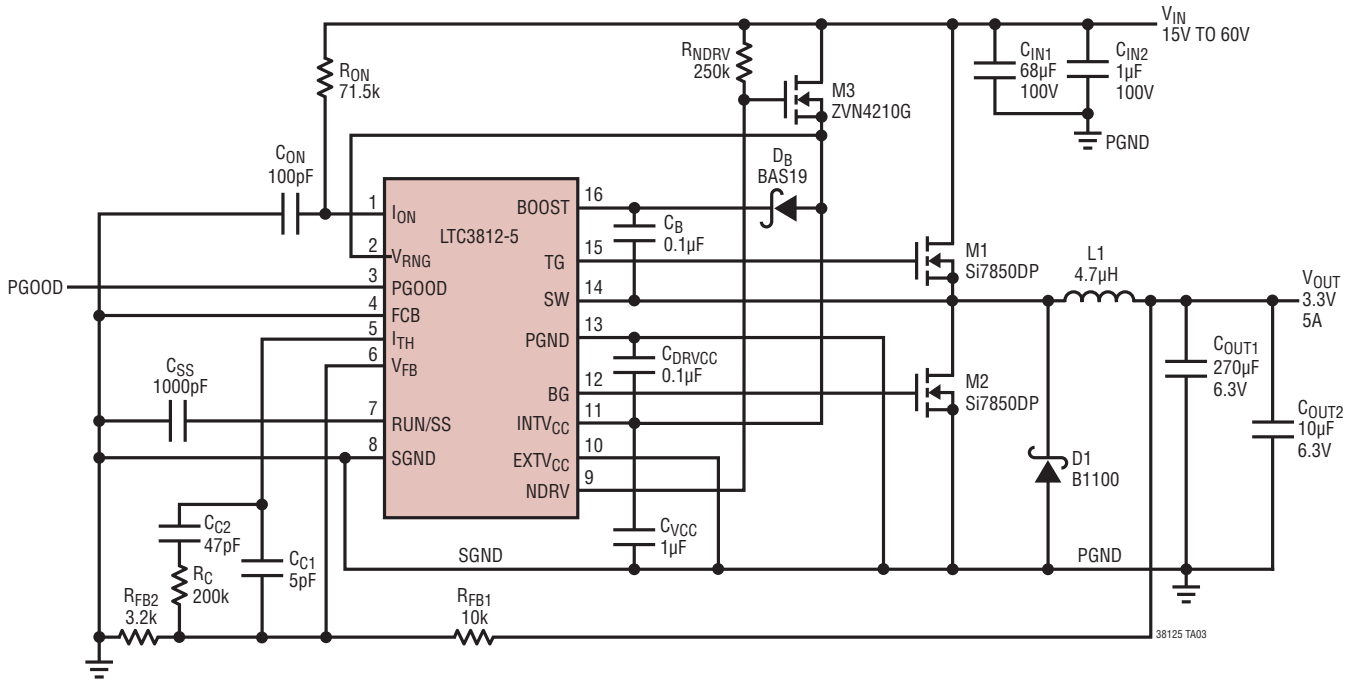
TYPICAL APPLICATIONS

7V to 60V Input Voltage to 5V/5A with IC Power from 12V Supply and All Ceramic Output Capacitors



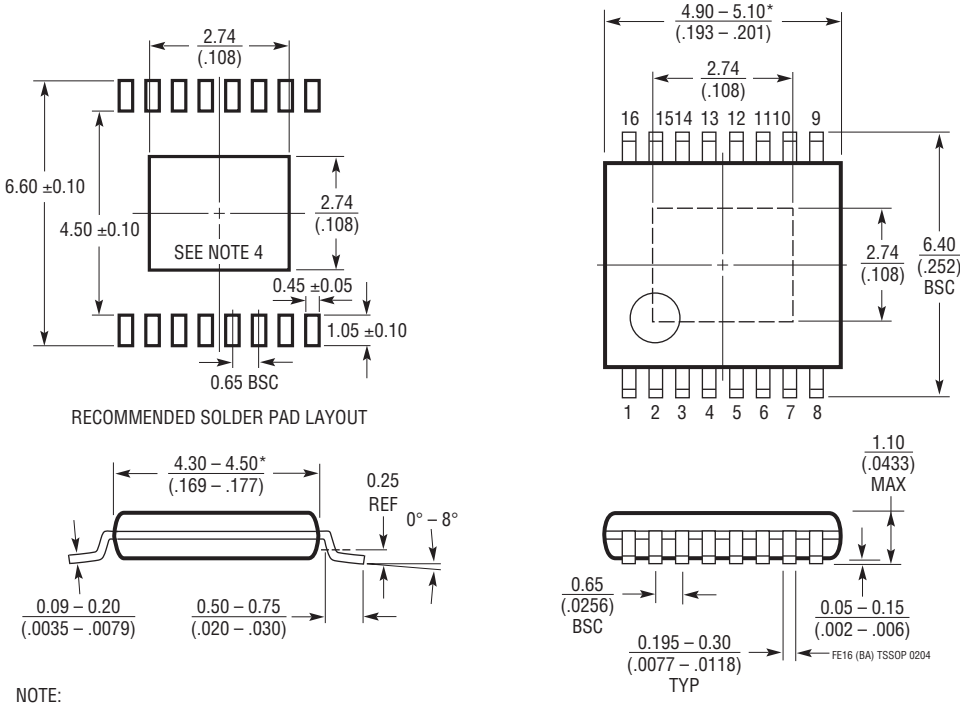
TYPICAL APPLICATIONS

15V to 60V Input Voltage to 3.3V/5A with Fault Timeout and Pulse-Skipping Disabled



PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

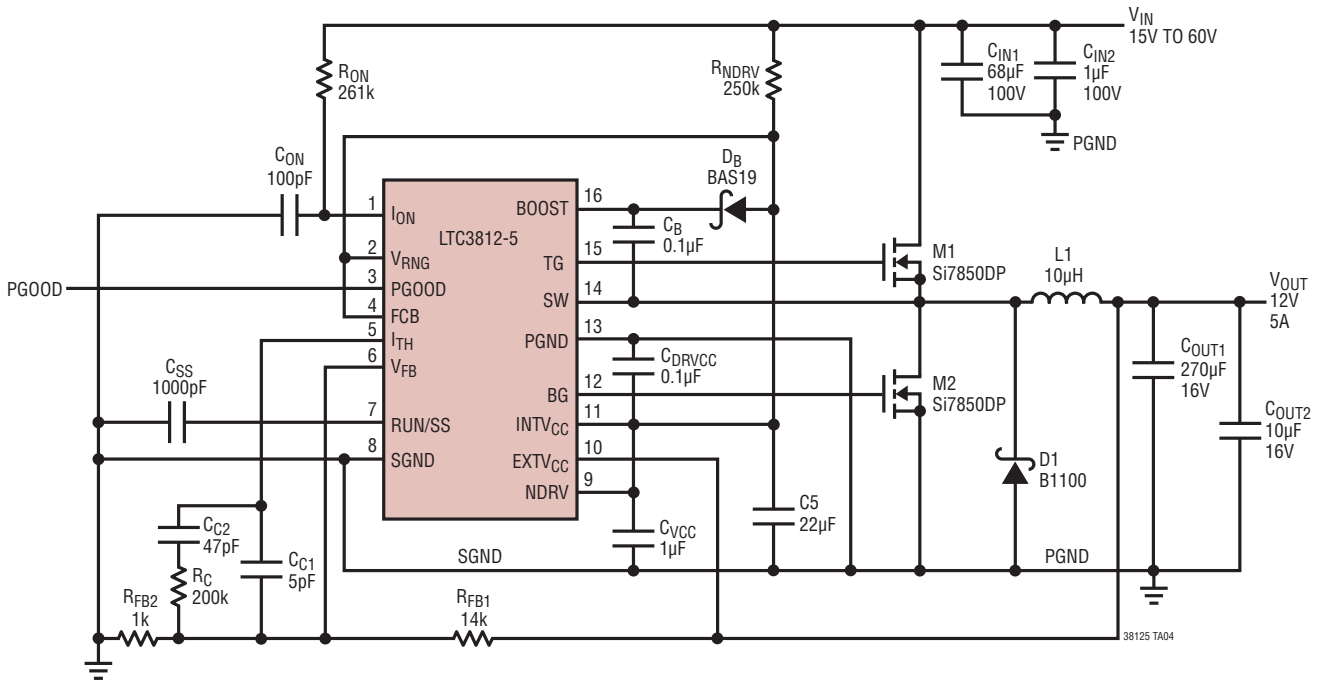
REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	01/11	Changed Operating Junction Temperature Range in Absolute Maximum Ratings and Order Information sections	2
		Remove Lead Based Part Numbers from Order Information	2
		Updated Equations	25
		Updated Related Parts	34

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

15V to 60V Input Voltage to 12V/5A with Trickle Charger Start-Up



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 50kHz to 900kHz $4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 24V$, TSSOP-20E, 3×4 QFN-20
LTC3890	60V, Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 50kHz to 900kHz $4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 24V$, 5×5 QFN-32
LTC3810	100V Synchronous Step-Down DC/DC Controller	Constant On-time Valley Current Mode $4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 0.93V_{IN}$, SSOP-28
LTC3810-5	60V Synchronous Step-Down DC/DC Controller	Constant On-time Valley Current Mode $4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 0.93V_{IN}$, 5×5 QFN-32
LTC3703	100V Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 100kHz to 600kHz $4V \le V_{IN} \le 100V$, $0.8V \le V_{OUT} \le 0.93V_{IN}$, SSOP-16, SSOP-28
LT3845A	60V, Low I_Q, Single Output Synchronous Step-Down DC/DC Controller	Adjustable Fixed Frequency 100kHz to 500kHz, $4V \le V_{IN} \le 60V$, $1.23V \le V_{OUT} \le 36V$, TSSOP-16E
LTC3824	60V, Low I_Q, Step-Down DC/DC Controller, 100% Duty Cycle	Selectable Fixed Frequency 200kHz to 600kHz $4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le V_{IN}$, $I_Q = 40\mu A$, MSOP-10E

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0111 REV C • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2007