V29C31004T/V29C31004B
4 MEGABIT (524,288 x 8 BIT)
3.3 VOLT CMOS FLASH MEMORY

PRELIMINARY

Features

- 512Kx8-bit Organization
- Address Access Time: 90, 120 ns
- Single 3.3V ± 0.3 Power Supply
- Sector Erase Mode Operation
- 16KB Boot Block (lockable)
- 1K bytes per Sector, 512 Sectors
  - Sector-Erase Cycle Time: 10ms (Max)
  - Byte-Write Cycle Time: 60µs (Max)
- Minimum 10,000 Erase-Program Cycles
- Low power dissipation
  - Active Read Current: 16mA (Typ)
  - Active Program Current: 30mA (Typ)
  - Standby Current: 50µA (Max)
- Hardware Data Protection
- Low V_{CC} Program Inhibit Below 2.5V
- Self-timed write/erase operations with end-of-cycle detection
  - $\overline{\text{DATA}}$ Polling
  - Toggle Bit
- CMOS and TTL Interface
- Available in two versions
  - V29C31004T (Top Boot Block)
  - V29C31004B (Bottom Boot Block)
- Packages:
  - 32-pin TSOP-I
  - 32-pin PLCC

Description

The V29C31004T/V29C31004B is a high speed 524,288 x 8 bit CMOS flash memory. Writing or erasing the device is done with a single 3.3 Volt power supply. The device has separate chip enable $\overline{\text{CE}}$, write enable $\overline{\text{WE}}$, and output enable $\overline{\text{OE}}$ controls to eliminate bus contention.

The V29C31004T/V29C31004B offers a combination of: Boot Block with Sector Erase/Write Mode. The end of write/erase cycle is detected by $\overline{\text{DATA}}$ Polling of I/O_7 or by the Toggle Bit I/O_6.

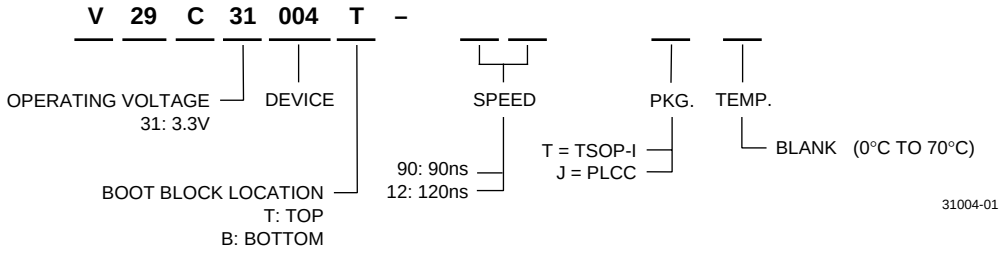
The V29C31004T/V29C31004B features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. The device also supports full chip erase.

Boot block architecture enables the device to boot from a protected sector located either at the top (V29C31004T) or the bottom (V29C31004B). All inputs and outputs are CMOS and TTL compatible.

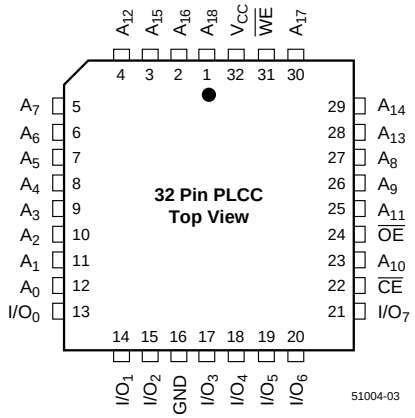
The V29C31004T/V29C31004B is ideal for applications that require updatable code and data storage.

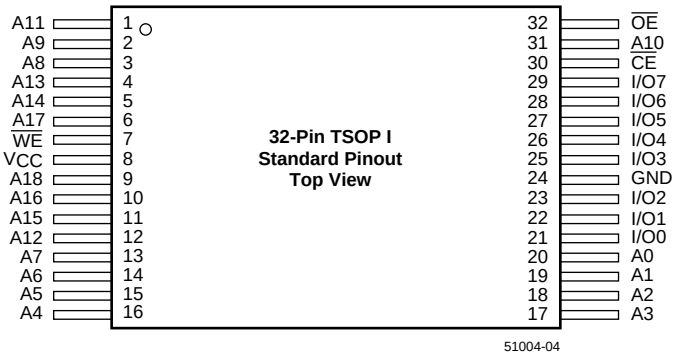
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Temperature Mark
	T	J	90	120	
0°C to 70°C	•	•	•	•	Blank



Pin Configurations

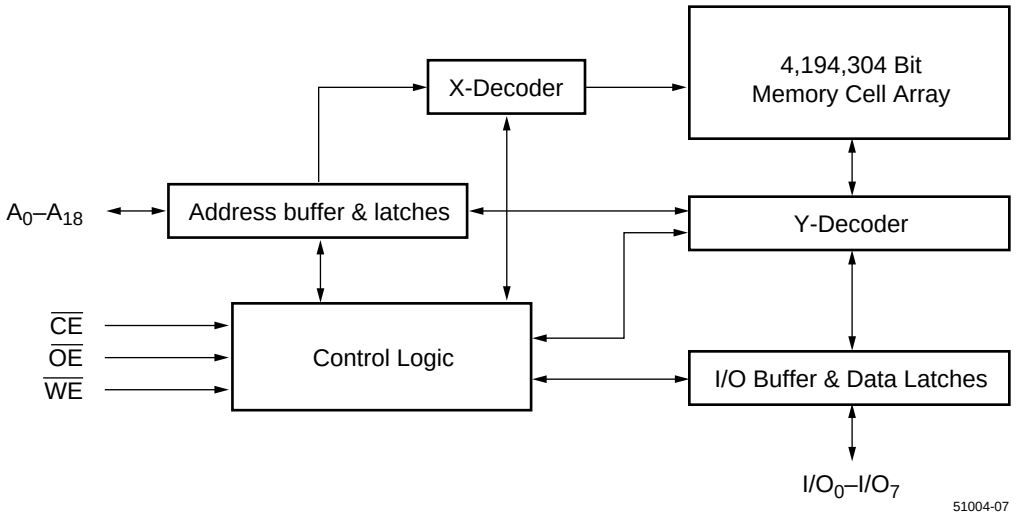




Pin Names

A_0–A_{18}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V ± 10% Power Supply
GND	Ground
NC	No Connect

Functional Block Diagram



Capacitance (1,2)

Symbol	Parameter	Test Setup	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	10	pF

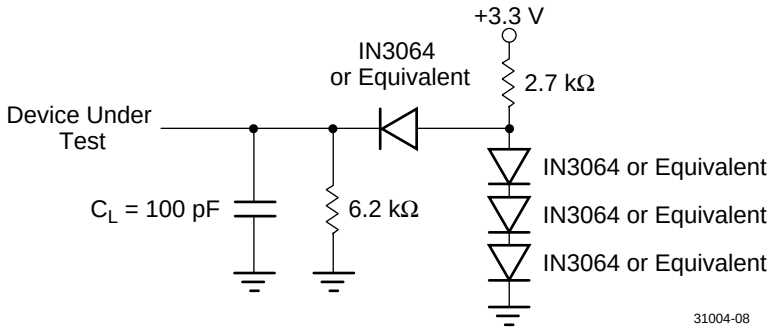
NOTE:
1. Capacitance is sampled and not 100% tested.
2. T_A = 25°C, V_{CC} = 5V ± 10%, f = 1 MHz.

Latch Up Characteristics(1)

Parameter	Min.	Max.	Unit
Input Voltage with Respect to GND on A_9, $\overline{OE}$	-1	+13	V
Input Voltage with Respect to GND on I/O, address or control pins	-1	V_{CC} + 1	V
V_{CC} Current	-100	+100	mA

NOTE:
1. Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.3V, one pin at a time.

AC Test Load



Absolute Maximum Ratings(1)

Symbol	Parameter	Commercial	Unit
V_{IN}	Input Voltage (input or I/O pins)	-0.5 to V_{CC}+0.5	V
V_{IN}	Input Voltage (A_9 pin, $\overline{OE}$)	-0.5 to +13	V
V_{CC}	Power Supply Voltage	-0.5 to +5.5	V
T_{STG}	Storage Temerpature (Plastic)	-65 to +125	°C
T_{OPR}	Operating Temperature	0 to +70	°C
I_{OUT}	Short Circuit Current(2)	200 (Max.)	mA

NOTE:
1. Stress greater than those listed unders “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. No more than one output maybe shorted at a time and not exceeding one second long.

DC Electrical Characteristics

(over the commercial operating range)

Parameter Name	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	$V_{CC} = V_{CC}$ Min.	—	0.8	V
V_{IH}	Input HIGH Voltage	$V_{CC} = V_{CC}$ Max.	2	—	V
I_{IL}	Input Leakage Current	V_{IN} = GND to V_{CC}, $V_{CC} = V_{CC}$ Max.	—	±1	µA
I_{OL}	Output Leakage Current	V_{OUT} = GND to V_{CC}, $V_{CC} = V_{CC}$ Max.	—	±1	µA
V_{OL}	Output LOW Voltage	$V_{CC} = V_{CC}$ Min., I_{OL} = 2.1mA	—	0.4	V
V_{OH}	Output HIGH Voltage	$V_{CC} = V_{CC}$ Min, I_{OH} = -400µA	2.4	—	V
I_{CC1}	Read Current	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/Os open, Address input = V_{IL}/V_{IH}, at f = $1/t_{RC}$ Min., $V_{CC} = V_{CC}$ Max.	—	16	mA
I_{CC2}	Write Current	$\overline{CE} = \overline{WE}$ = VIL, $\overline{OE} = V_{IH}$, $V_{CC} = V_{CC}$ Max.	—	30	mA
I_{SB}	TTL Standby Current	$\overline{CE} = \overline{OE} = \overline{WE} = V_{IH}$, $V_{CC} = V_{CC}$ Max.	—	1	mA
I_{SB1}	CMOS Standby Current	$\overline{CE} = \overline{OE} = \overline{WE} = V_{CC} - 0.3V$, $V_{CC} = V_{CC}$ Max.	—	50	µA
V_H	Device ID Voltage for A_9	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$	11.5	12.5	V
I_H	Device ID Current for A_9	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, A9 = V_H Max.	—	50	µA

AC Electrical Characteristics

(over all temperature ranges)

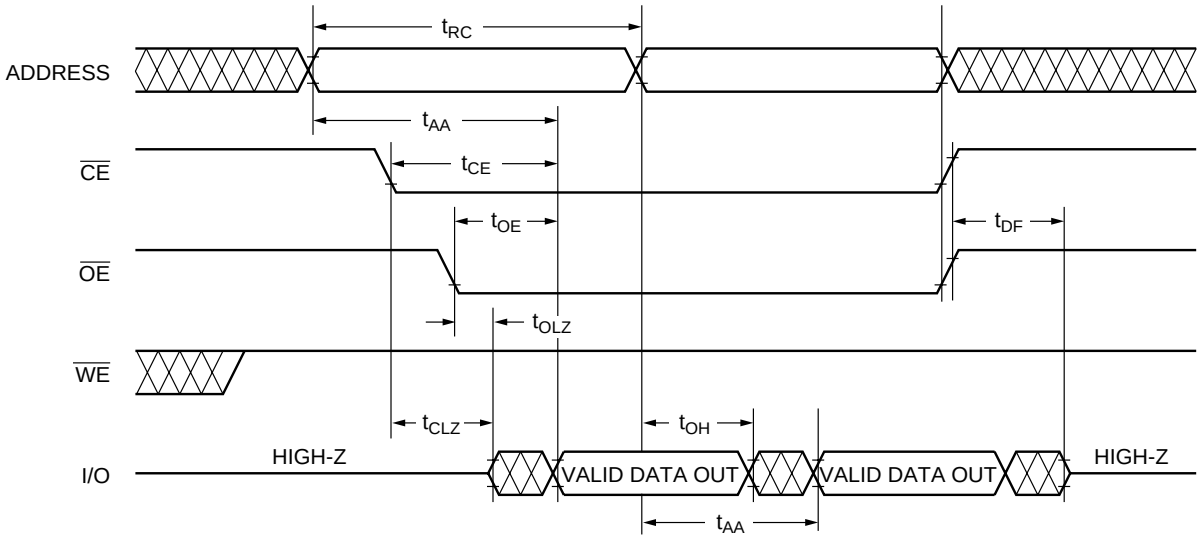
Read Cycle

Parameter Name	Parameter	-90		-12		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	90	—	120	—	ns
t_{AA}	Address Access Time	—	90	—	120	ns
t_{ACS}	Chip Enable Access Time	—	90	—	120	ns
t_{OE}	Output Enable Access Time	—	45	—	60	ns
t_{CLZ}	$\overline{CE}$ Low to Output Active	0	—	0	—	ns
t_{OLZ}	$\overline{OE}$ Low to Output Active	0	—	0	—	ns
t_{DF}	$\overline{OE}$ or $\overline{CE}$ High to Output in High Z	0	40	0	50	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	ns

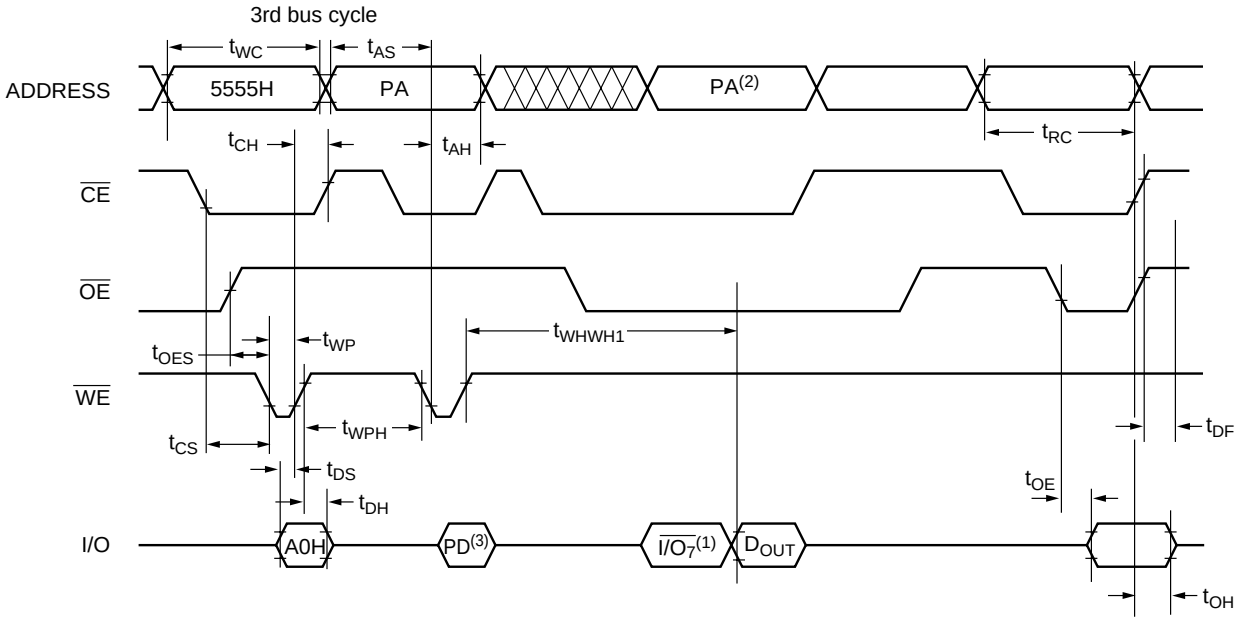
Program (Erase/Program) Cycle

Parameter Name	Parameter	-90			-12			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{WC}	Write Cycle Time	90	—	—	120	—	—	ns
t_{AS}	Address Setup Time	0	—	—	0	—	—	ns
t_{AH}	Address Hold Time	45	—	—	50	—	—	ns
t_{CS}	$\overline{CE}$ Setup Time	0	—	—	0	—	—	ns
t_{CH}	$\overline{CE}$ Hold Time	0	—	—	0	—	—	ns
t_{OES}	$\overline{OE}$ Setup Time	0	—	—	0	—	—	ns
t_{OEH}	$\overline{OE}$ High Hold Time	0	—	—	0	—	—	ns
t_{WP}	$\overline{WE}$ Pulse Width	45	—	—	50	—	—	ns
t_{WPH}	$\overline{WE}$ Pulse Width High	30	—	—	35	—	—	ns
t_{DS}	Data Setup Time	30	—	—	30	—	—	ns
t_{DH}	Data Hold Time	0	—	—	0	—	—	ns
t_{WHWH1}	Programming Cycle	—	—	60	—	—	60	µs
t_{WHWH2}	Sector Erase Cycle	—	—	10	—	—	10	ms
t_{WHWH3}	Chip Erase Cycle	—	3	—	—	3	—	sec

Waveforms of Read Cycle



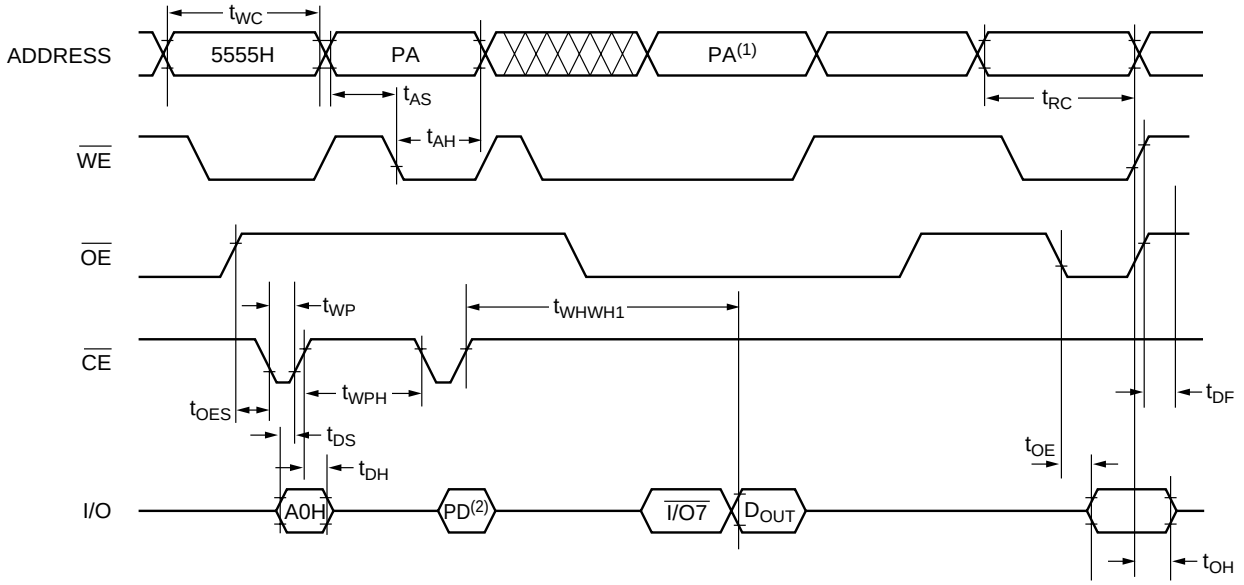
Waveforms of $\overline{WE}$ Controlled-Program Cycle



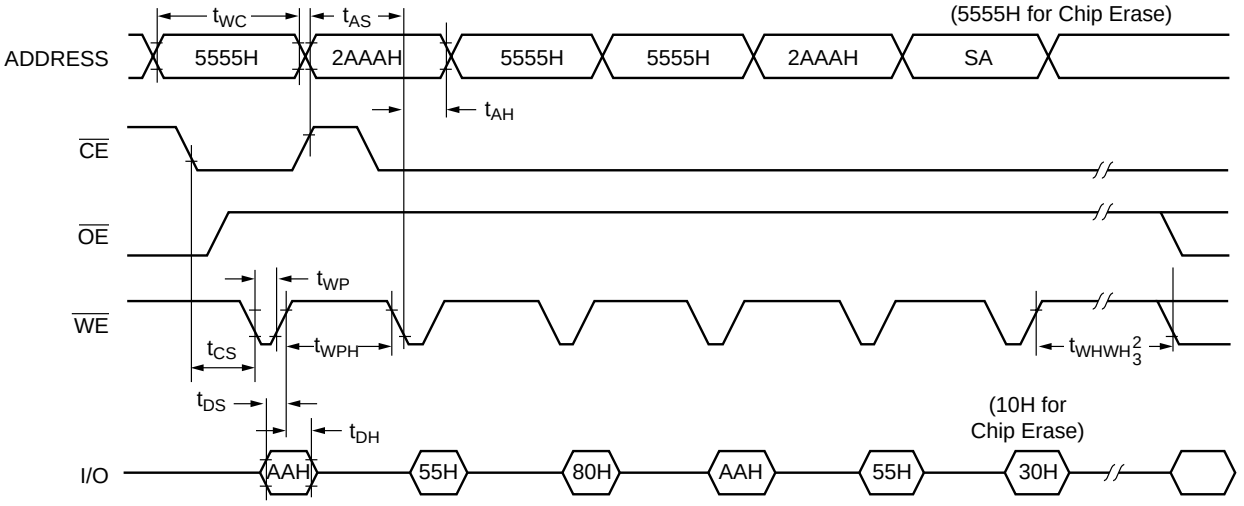
NOTES:

1. I/O_7: The output is the complement of the data written to the device.
2. PA: The address of the memory location to be programmed.
3. PD: The data at the byte address to be programmed.

Waveforms of CE Controlled-Program Cycle



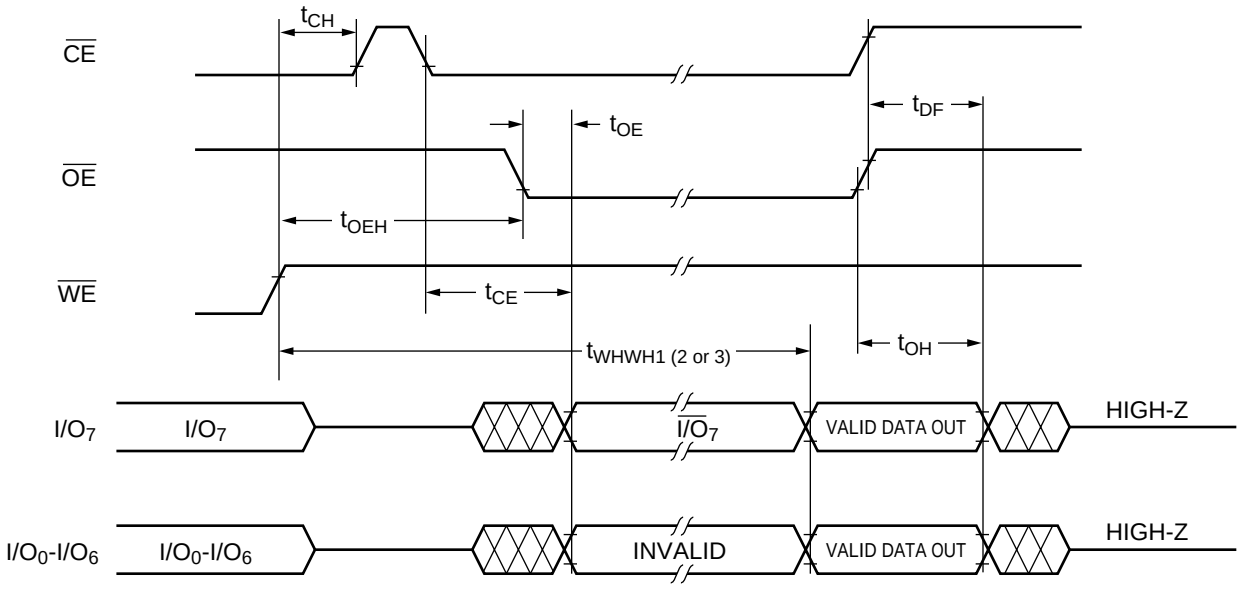
Waveforms of Erase Cycle(1)



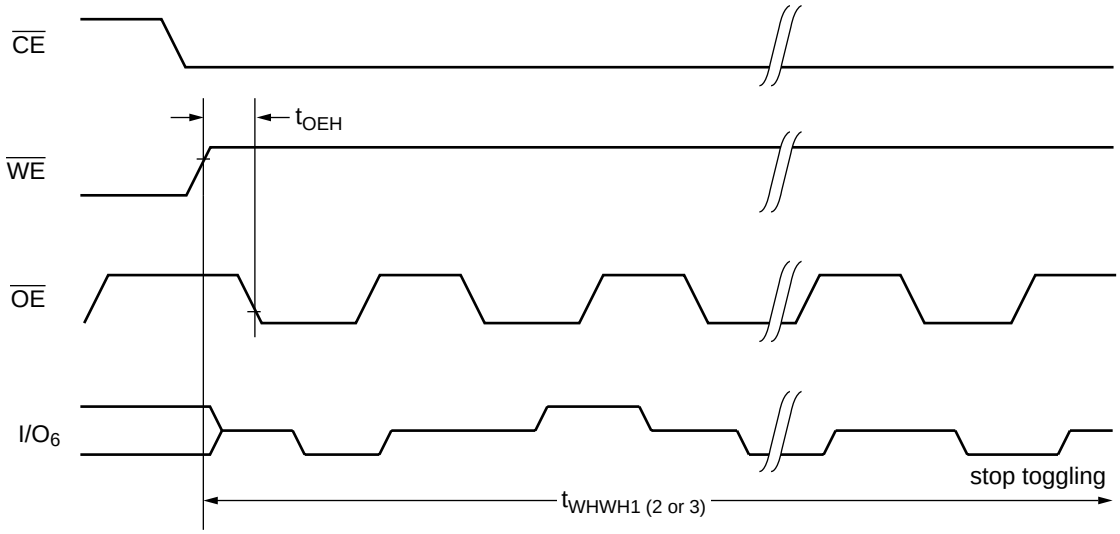
NOTES:

1. PA: The address of the memory location to be programmed.
2. PD: The data at the byte address to be programmed.
3. SA: The sector address for Sector Erase.

Waveforms of $\overline{DATA}$ Polling Cycle



Waveforms of Toggle Bit Cycle



Functional Description

The V29C31004T/V29C31004B consists of 512 equally-sized sectors of 1K bytes each. The 16 KB lockable Boot Block is intended for storage of the system BIOS boot code. The boot code is the first piece of code executed each time the system is powered on or rebooted.

The V29C31004 is available in two versions: the V29C31004T with the Boot Block address starting from 7C000H to 7FFFFH, and the V29C31004B with the Boot Block address starting from 00000H to 3FFFFH.

Read Cycle

A read cycle is performed by holding both $\overline{CE}$ and $\overline{OE}$ signals LOW. Data Out becomes valid only when these conditions are met. During a read cycle $\overline{WE}$ must be HIGH prior to $\overline{CE}$ and $\overline{OE}$ going LOW. $\overline{WE}$ must remain HIGH during the read operation for the read to complete (see Table 1).

Output Disable

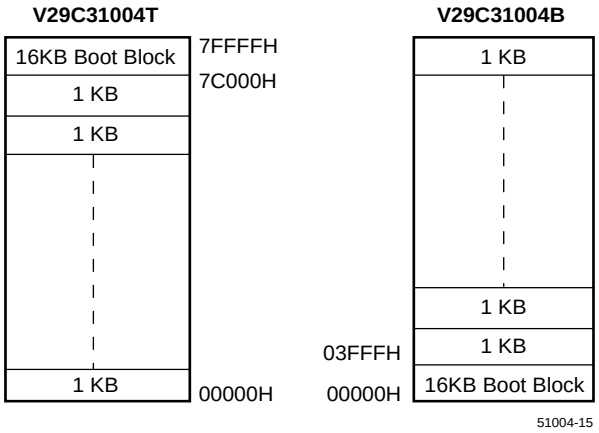
Returning $\overline{OE}$ or $\overline{CE}$ HIGH, whichever occurs first will terminate the read operation and place the I/O pins in the HIGH-Z state.

Standby

The device will enter standby mode when the $\overline{CE}$ signal is HIGH. The I/O pins are placed in the HIGH-Z, independent of the $\overline{OE}$ input state.

Command Sequence

The V29C31004T/V29C31004B does not provide the “reset” feature to return the chip to its normal state when an incomplete command sequence or an interruption has happened. In this case, normal operation (Read Mode) can be restored by issuing a “non-existent” command sequence, for example Address: 5555H, Data FFH.



16KB Boot Block = 16 Sectors

Byte Write Cycle

The V29C31004T/V29C31004B is programmed on a byte-by-byte basis. The byte write operation is initiated by using a specific four-bus-cycle sequence: two unlock program cycles, a program setup command and program data program cycles (see Table 2).

During the byte write cycle, addresses are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever is last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first. The byte write cycle can be $\overline{CE}$ controlled or $\overline{WE}$ controlled.

Sector Erase Cycle

The V29C31004T/V29C31004B features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. Sector erase operation is initiated by using a specific six-bus-cycle sequence: Two unlock program cycles, a setup command, two additional unlock program cycles, and the sector erase command (see Table 2). A sector must be first erased before it can be re-

Table 1. Operation Modes Decoding

Decoding Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_9	I/O
Read	V_{IL}	V_{IL}	V_{IH}	A_0	A_1	A_9	READ
Byte Write	V_{IL}	V_{IH}	V_{IL}	A_0	A_1	A_9	PD
Standby	V_{IH}	X	X	X	X	X	HIGH-Z
Autoselect Device ID	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_H	CODE
Autoselect Manufacture ID	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_H	CODE
Enabling Boot Block Protection Lock	V_{IL}	V_H	V_{IL}	X	X	V_H	X
Disabling Boot Block Protection Lock	V_H	V_H	V_{IL}	X	X	V_H	X
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	HIGH-Z

NOTES:

1. X = Don’t Care, V_{IH} = HIGH, V_{IL} = LOW, V_H = 12.5V Max.
2. PD: The data at the byte address to be programmed.

Table 2. Command Codes

Command Sequence	First Bus Program Cycle		Second Bus Program Cycle		Third Bus Program Cycle		Fourth Bus Program Cycle		Fifth Bus Program Cycle		Six Bus Program Cycle	
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read	XXXXH	F0H										
Read	5555H	AAH	2AAAH	55H	5555H	F0H	RA(1)	RD(2)				
Autoselect Mode	5555H	AAH	2AAAH	55H	5555H	90H	See table 3 for detail.					
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD(4)				
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA(5)	30H

NOTES:
1. RA: Read Address
2. RD: Read Data
3. PA: The address of the memory location to be programmed.
4. PD: The data at the byte address to be programmed.

written. While in the internal erase mode, the device ignores any program attempt into the device. The internal erase completion can be determined via DATA polling or toggle bit status.

The V29C31004T/V29C31004B is shipped fully erased (all bits = 1).

Chip Erase Cycle

The V29C31004T/V29C31004B features a chip-erase operation. The chip erase operation is initiated by using a specific six-bus-cycle sequence: two unlock program cycles, a setup command, two additional unlock program cycles, and the chip erase command (see Table 2).

The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$ pulse in the command sequence and terminates when the data on DQ7 is “1”.

Program Cycle Status Detection

There are two methods for determining the state of the V29C31004T/V29C31004B during a program (erase/write) cycle: $\overline{DATA}$ Polling (I/O_7) and Toggle Bit (I/O_6).

$\overline{DATA}$ Polling (I/O_7)

The V29C31004T/V29C31004B features $\overline{DATA}$ polling to indicate the end of a program cycle. When the device is in the program cycle, any attempt to read the device will received the complement of the loaded data on I/O_7. Once the program cycle is completed, I/O_7 will show true data, and the device is then ready for the next cycle.

Toggle Bit (I/O_6)

The V29C31004T/V29C31004B also features another method for determining the end of a program cycle. When the device is in the program cycle, any attempt to read the device will result in I/O_6 toggling between 1 and 0. Once the program is completed, the toggling will stop. The device is then ready for the next operation. Examining the toggle bit may begin at any time during a program cycle.

Boot Block Protection Enabling/Disabling

The V29C31004T/V29C31004B features hardware Boot Block Protection. The boot block sector protection is enabled when high voltage (12.5V) is applied to $\overline{OE}$ and A9 pins with $\overline{CE}$ pin LOW and $\overline{WE}$ pin LOW. The sector protection is disabled when high voltage is applied to $\overline{OE}$, $\overline{CE}$ and A9 pins with $\overline{WE}$ pin LOW. Other pins can be HIGH or LOW. This is shown in table 1.

Autoselect Mode

The V29C31004T/V29C31004B features an Autoselect mode to identify boot block locking status, device ID and manufacturer ID.

Entering Autoselect mode is accomplished by applying a high voltage (VH) to the A9 Pin, or through a sequence of commands (as shown in table 2). Device will exit this mode once high voltage on A9 is removed or another command is loaded into the device.

Boot Block Protection Status

In Autoselect mode, performing a read at address location 3CXX2H (V29C31004T) or 0CXX2H (V29C31004B) will indicate boot block protection status. If the data is 01H, the boot block is protected. If the data is 00H, the boot block is unprotected. This is also shown is table 3.

Device ID

In Autoselect mode, performing a read at address XXX1H will determine whether the device is a Top Boot Block device or a Bottom Boot Block device. If the data is 63H, the device is a Top Boot Block. If the data is 73H, the device is a Bottom Boot Block device (see Table 3).

Manufacturer ID

In Autoselect mode, performing a read at address XXXX0H will determine the manufacturer ID. 40H is the manufacturer code for Mosel Vitelic Flash.

Hardware Data Protection

V_{CC} Detection: the program operation is inhibited when VCC is less than 2.5V.

Noise Protection: a CE or WE pulse of less than 5ns will not initiate a program cycle.

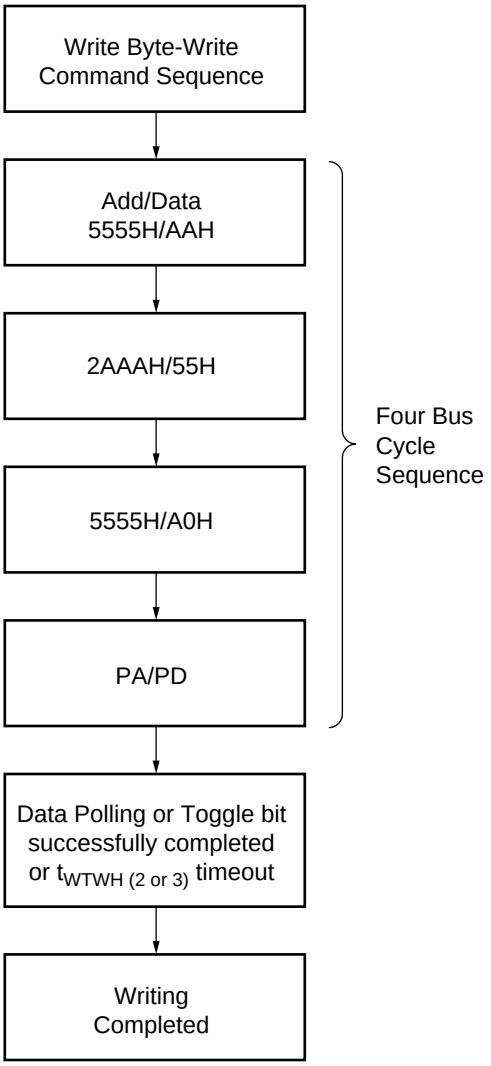
Program Inhibit: holding any one of $\overline{OE}$ LOW, $\overline{CE}$ HIGH or $\overline{WE}$ HIGH inhibits a program cycle.

Table 3. Autoselect Decoding

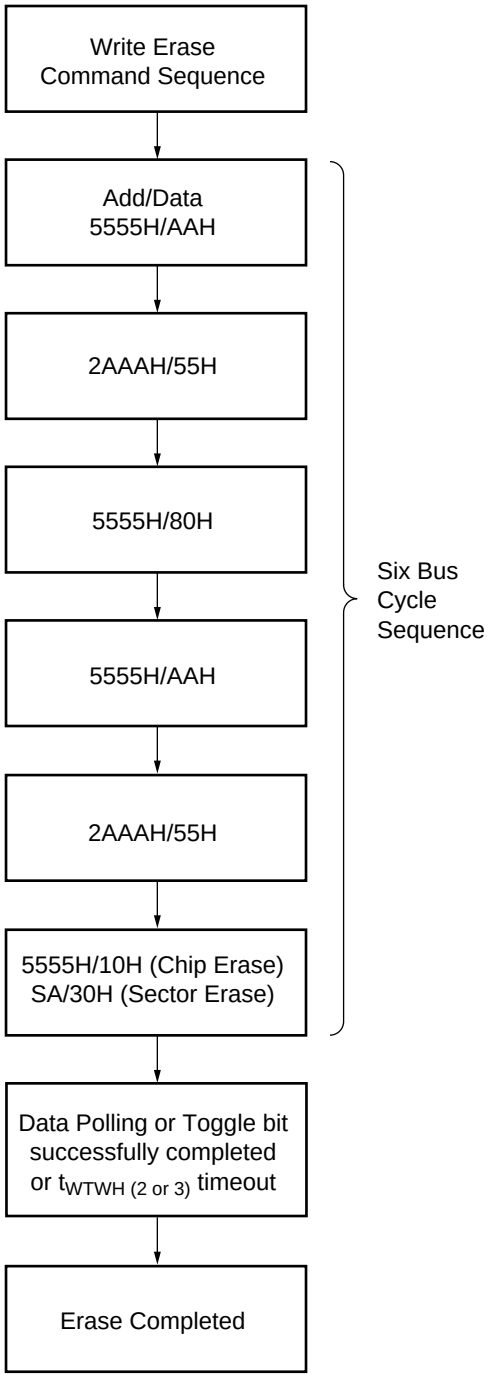
Decoding Mode	Boot Block	Address				Data I/O_0–I/O_7
		A_0	A_1	A_2–A_{13}	A_{14}–A_{17}	
Boot Block Protection	Top	V_{IL}	V_{IH}	X	V_{IH}	01H: protected
	Bottom	V_{IL}	V_{IH}	X	V_{IL}	00H: unprotected
Device ID	Top	V_{IH}	V_{IL}	X	X	63H
	Bottom					73H
Manufacture ID		V_{IL}	V_{IL}	X	X	40H

NOTE:
1. X = Don't Care, V_{IH} = HIGH, V_{IL} = LOW.

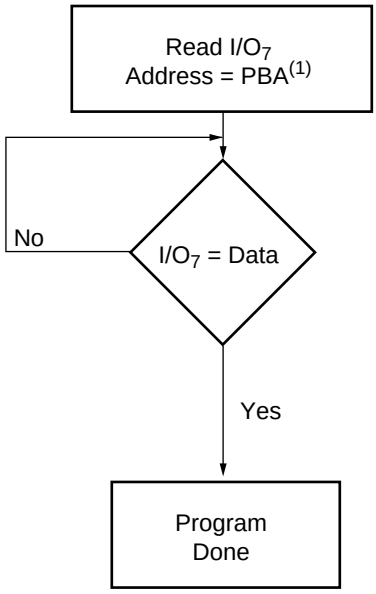
Byte Program Algorithm



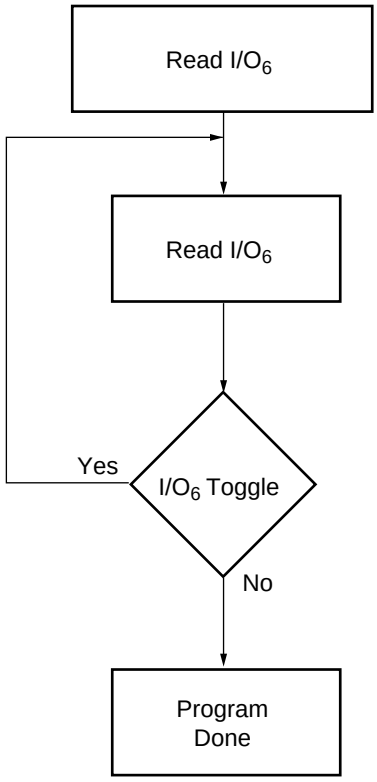
Chip/Sector Erase Algorithm



DATA Polling Algorithm



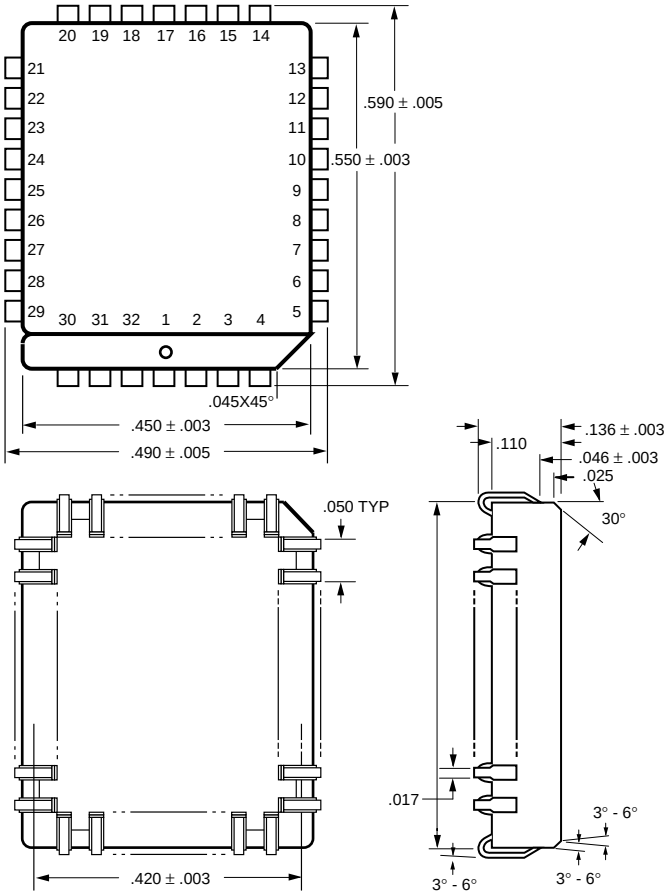
Toggle Bit Algorithm



NOTE:
1. PBA: The byte address to be programmed.

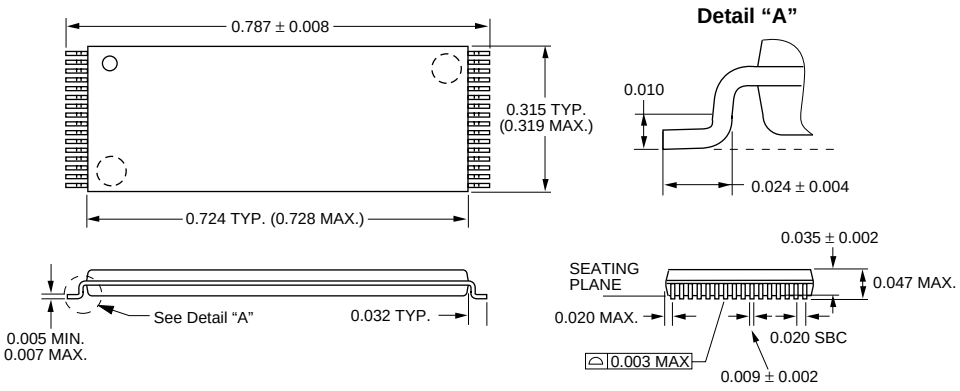
Package Diagrams

32-pin PLCC



32-pin TSOP-I

Units in inches



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