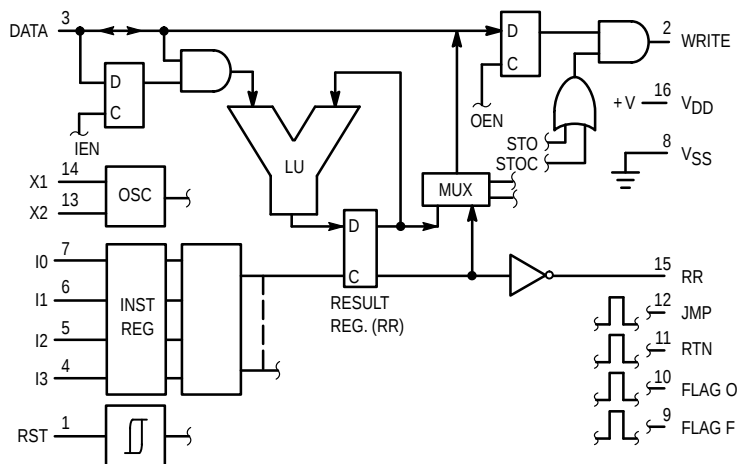


Industrial Control Unit

The MC14500B Industrial Control Unit (ICU) is a single-bit CMOS processor. The ICU is designed for use in systems requiring decisions based on successive single-bit information. An external ROM stores the control program. With a program counter (and output latches and input multiplexers, if required) the ICU in a system forms a stored-program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control. The ICU also may control an MPU or be controlled by an MPU.

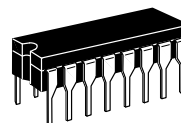
- 16 Instructions
- DC to 1.0 MHz Operation at $V_{DD} = 5\text{ V}$
- On-Chip Clock (Oscillator)
- Executes One Instruction per Clock Cycle
- 3 to 18 V Operation
- Low Quiescent Current Characteristic of CMOS Devices
- Capable of Driving One Low-Power Schottky Load or Two Low-Power TTL Loads over Full Temperature Range

BLOCK DIAGRAM

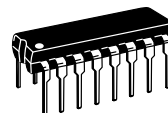


X1 — OSCILLATOR OUTPUT
X2 — OSCILLATOR INPUT

MC14500B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.

PIN ASSIGNMENT

RST	1	16	V_{DD}
WRITE	2	15	RR
DATA	3	14	X1
I3	4	13	X2
I2	5	12	JMP
I1	6	11	RTN
I0	7	10	FLAG O
V_{SS}	8	9	FLAG F

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in} , V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to $V_{DD} + 0.5$	V
I_{in} , I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage “0” Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level $V_{in} = 0$ or V_{DD}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level RST, D, X2 ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	“1” Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Input Voltage # “0” Level I0, I1, I2, I3 ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	—	0.8	—	1.1	0.8	—	0.8	Vdc
		10	—	1.6	—	2.2	1.6	—	1.6	
		15	—	2.4	—	3.4	2.4	—	2.4	
	“1” Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	5.0	2.0	—	2.0	1.9	—	2.0	—	Vdc
		10	6.0	—	6.0	3.1	—	6.0	—	
		15	10	—	10	4.3	—	10	—	
Output Drive Current Source Data, Write ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	I_{OH}	5.0	– 1.2	—	– 1.0	– 2.0	—	– 0.7	—	mAdc
		10	– 3.6	—	– 3.0	– 6.0	—	– 2.1	—	
		15	– 7.2	—	– 6.0	– 12	—	– 4.2	—	
	Sink ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	5.0	1.9	—	1.6	3.2	—	1.1	—	mAdc
		10	3.6	—	3.0	6.0	—	2.1	—	
		15	7.2	—	6.0	12	—	4.2	—	
Output Drive Current Other Outputs ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	I_{OH}	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
	Sink ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Input Current, RST	I _{in}	15	25	—	—	150	—	—	250	μAdc
Input Current	I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (Data)	C _{in}	—	—	—	—	15	—	—	—	pF
Input Capacitance (All Other Inputs)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) I _{out} = 0 μA, V _{in} = 0 or V _{DD}	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
**Total Supply Current at an External Load Capacitance (C _L) on All Outputs	I _T	—	I _T = (1.5 μA/kHz) f + I _{DD} I _T = (3.0 μA/kHz) f + I _{DD} I _T = (4.5 μA/kHz) f + I _{DD}							μAdc

**The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS* (T_A = 25°C; t_r = t_f = 20 ns for X and I inputs; C_L = 50 pF for JMP, X1, RR, Flag O, Flag F; C_L = 130 pF + 1 TTL load for Data and Write.)

Characteristic	Symbol	V _{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Propagation Delay Time, X1 to RR X1 to Flag F, Flag O, RTN, JMP X1 to Write X1 to Data RST to RR RST to X1 RST to Flag F, Flag O, RTN, JMP RST to Write, Data	t _{PLH} , t _{PHL}	5.0	—	250	500	ns
		10	—	125	250	
		15	—	100	200	
		5.0	—	200	400	
		10	—	100	200	
		15	—	85	170	
		5.0	—	225	450	
		10	—	125	250	
		15	—	100	200	
		5.0	—	250	500	
		10	—	120	240	
		15	—	100	200	
		5.0	—	250	500	
		10	—	125	250	
		15	—	100	200	
		5.0	—	450	Note 1	
		10	—	200		
		15	—	150		
		5.0	—	400	800	
		10	—	200	400	
		15	—	150	300	
		5.0	—	450	900	
		10	—	225	450	
		15	—	175	350	
Clock Pulse Width, X1	t _{W(c)}	5.0	400	200	—	ns
		10	200	100	—	
		15	180	90	—	
Rent Pulse Width, RST	t _{W(R)}	5.0	500	250	—	ns
		10	250	125	—	
		15	200	100	—	
Setup Time — Instruction Data	t _{su(I)}	5.0	400	200	—	ns
		10	250	125	—	
		15	180	90	—	
	t _{su(D)}	5.0	200	100	—	
		10	100	50	—	
		15	80	40	—	
Hold Time — Instruction Data	t _{h(I)}	5.0	100	0	—	ns
		10	50	0	—	
		15	50	0	—	
	t _{h(D)}	5.0	200	100	—	
		10	100	50	—	
		15	100	50	—	

NOTE 1. Maximum Reset Delay may extend to one-half clock period.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

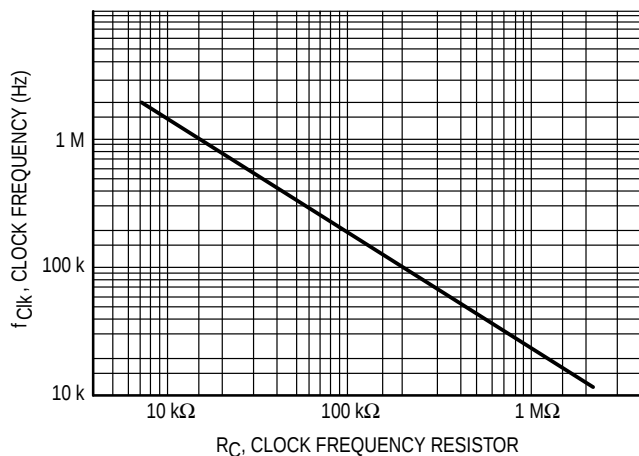


Figure 1. Typical Clock Frequency versus Resistor (R_C)

Pin No.	Function	Symbols
1	Chip Reset	RST
2	Write Pulse	Write
3	Data In/Out	Data
4	MSB Instruction Word	I_3
5	Bit 2 Instruction Word	I_2
6	Bit 1 Instruction Word	I_1
7	LSB Instruction Word	I_0
8	Negative Supply (Ground)	V_{SS}
9	Flag on NOP F	Flag F
10	Flag on NOP O	Flag O
11	Subroutine Return Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	V_{DD}

Table 1. MC14500B Instruction Set

Instruction Code	Mnemonic	Action
0 0000	NOPO	No change in registers. $RR \rightarrow RR$, Flag O $\rightarrow$
1 0001	LD	Load result register. Data $\rightarrow RR$
2 0010	LDC	Load complement. $\overline{\text{Data}} \rightarrow RR$
3 0011	AND	Logical AND. $RR \bullet \text{Data} \rightarrow RR$
4 0100	ANDC	Logical AND complement. $RR \bullet \overline{\text{Data}} \rightarrow RR$
5 0101	OR	Logical OR. $RR + \text{Data} \rightarrow RR$
6 0110	ORC	Logical OR complement. $RR + \overline{\text{Data}} \rightarrow RR$
7 0111	XNOR	Exclusive NOR. If $RR = \text{Data}$, $RR \rightarrow 1$
8 1000	STO	Store. $RR \rightarrow \text{Data Pin}$, Write $\rightarrow$
9 1001	STOC	Store complement. $RR \rightarrow \text{Data Pin}$, Write $\rightarrow$
A 1010	IEN	Input enable. Data $\rightarrow$ IEN Register
B 1011	OEN	Output enable. Data $\rightarrow$ OEN Register
C 1100	JMP	Jump. JMP Flag $\rightarrow$
D 1101	RTN	Return. RTN Flag $\rightarrow$ and skip next instruction
E 1110	SKZ	Skip next instruction if $RR = 0$
F 1111	NOPF	No change in registers. $RR \rightarrow RR$, Flag F $\rightarrow$

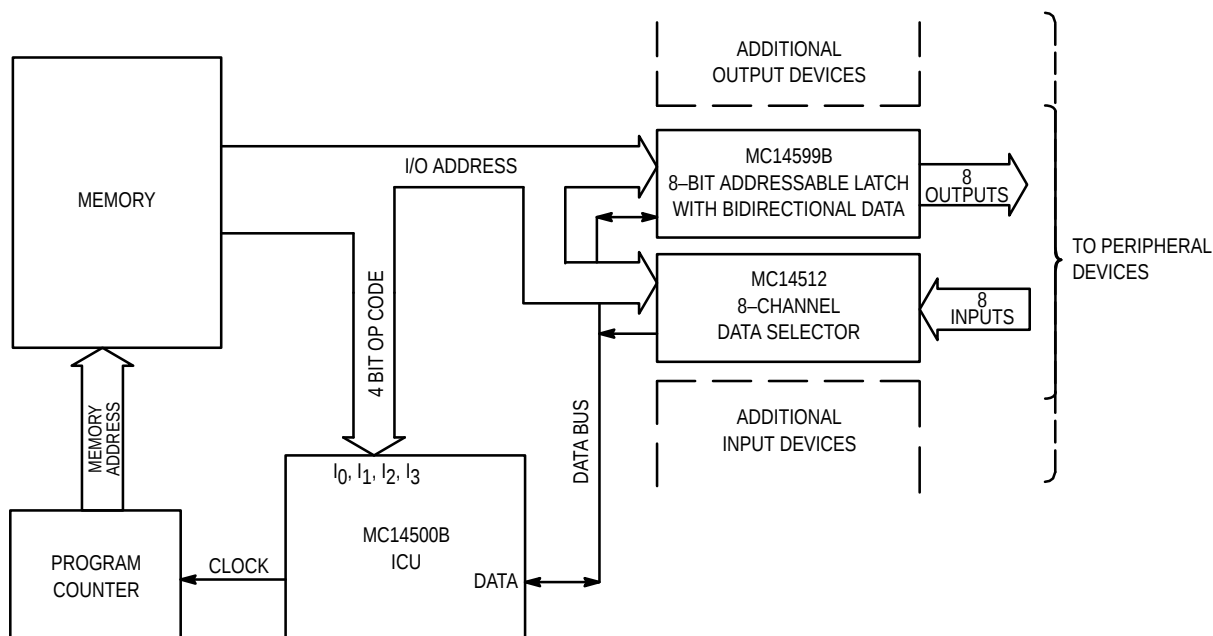
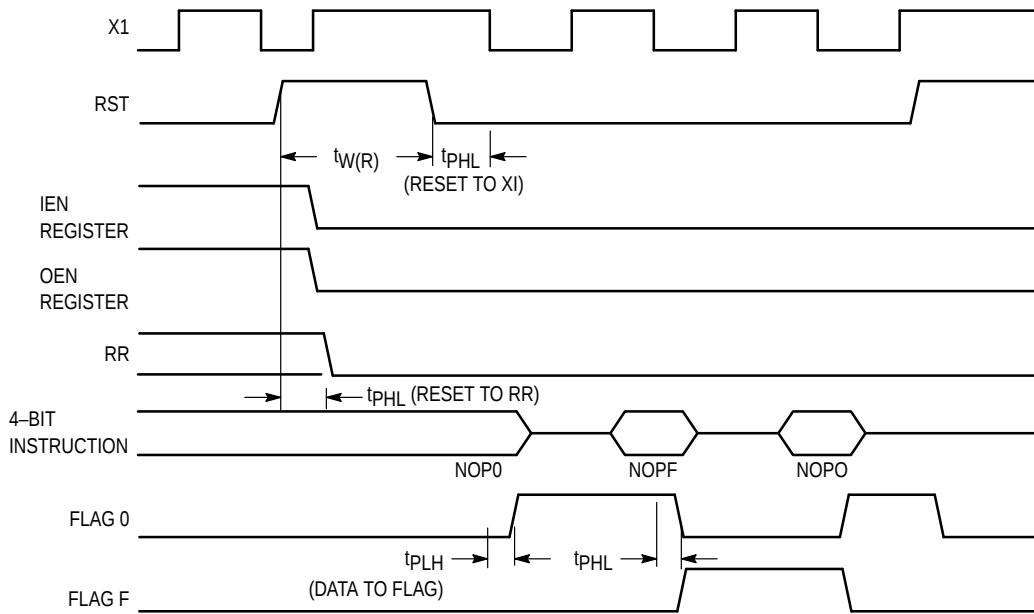


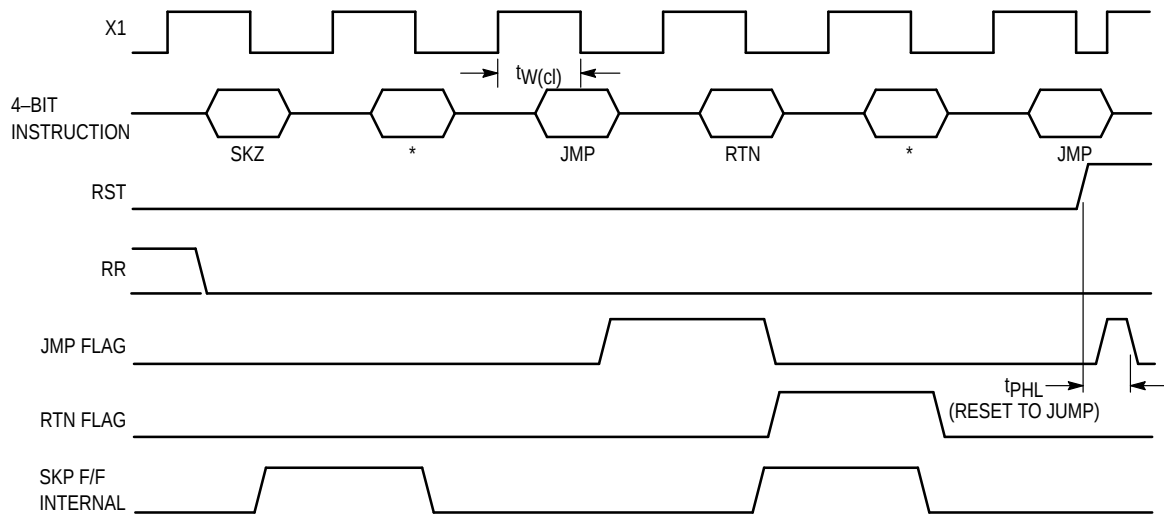
Figure 2. Outline of a Typical Organization for a MC14500B-Based System

TIMING WAVEFORMS

Instructions **NOPO, NOPF**
RR, IEN, OEN remain unaffected



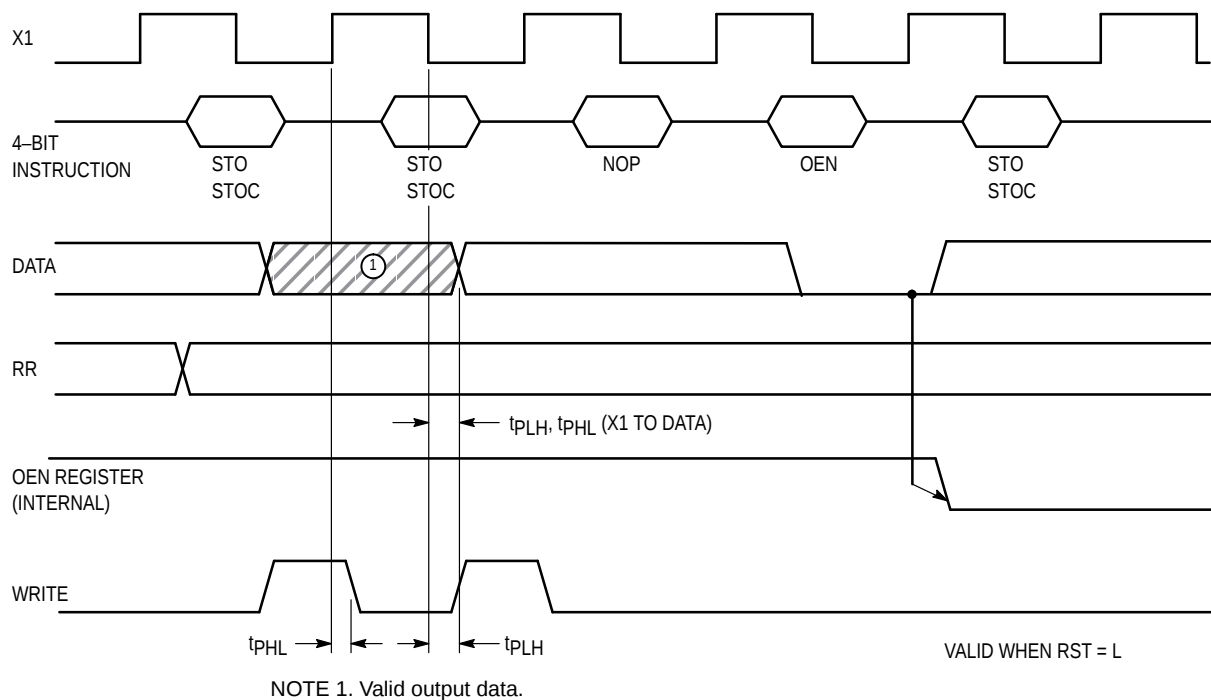
Instructions **SKZ, JMP, RTN**
RR, IEN, OEN remain unaffected



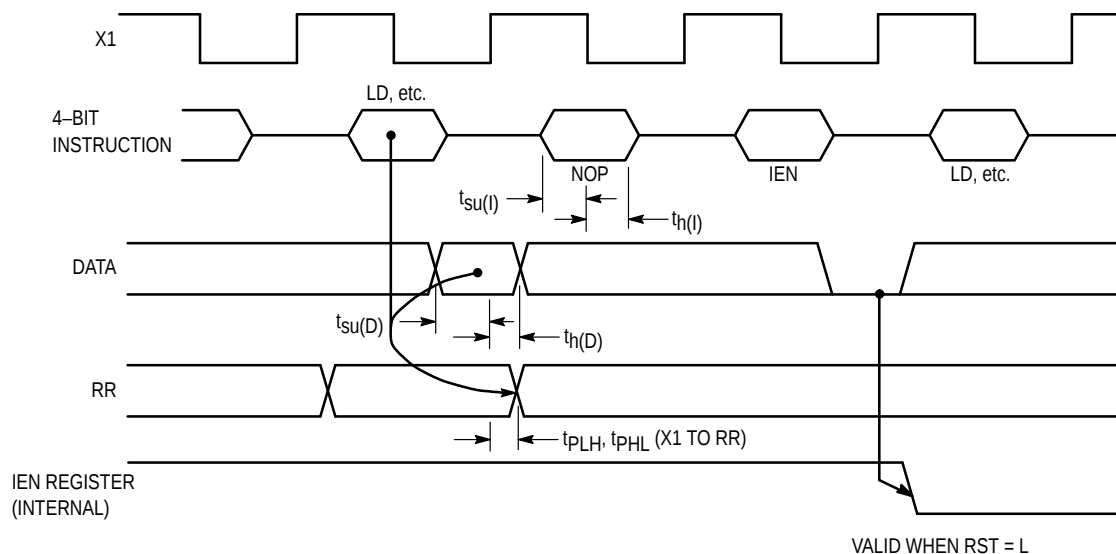
* Instructions Ignored.

TIMING WAVEFORMS

Instructions STO, STOC, OEN

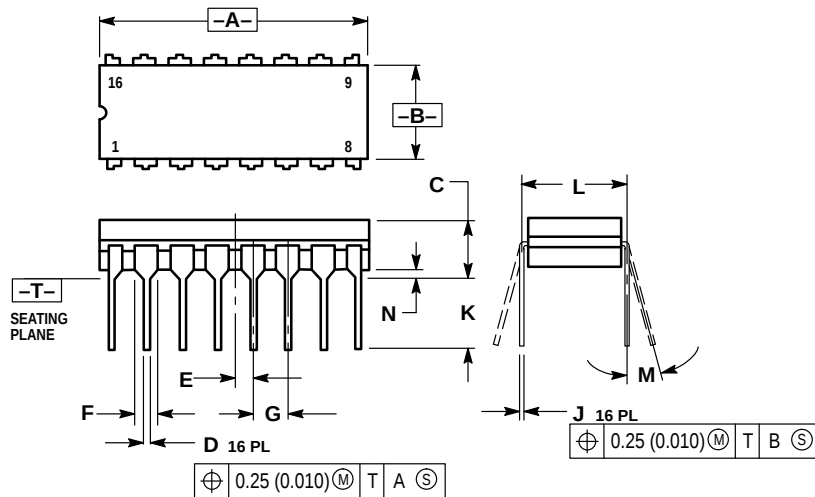


Instructions LD, LDC, AND, ANDC, OR, ORC, XNOR, IEN



OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

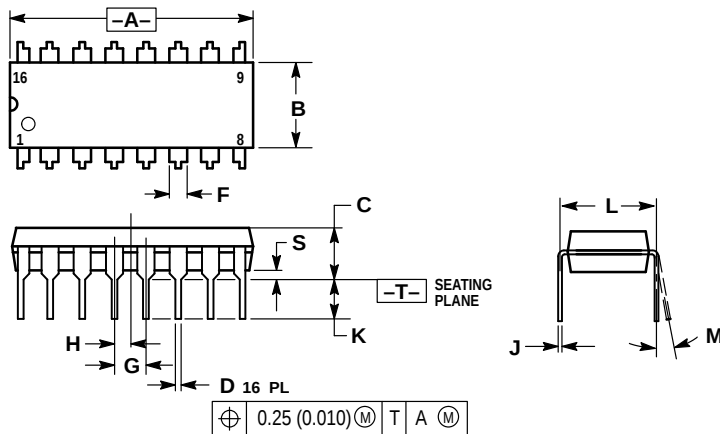


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050	BSC	1.27	BSC
F	0.055	0.065	1.40	1.65
G	0.100	BSC	2.54	BSC
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300	BSC	7.62	BSC
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



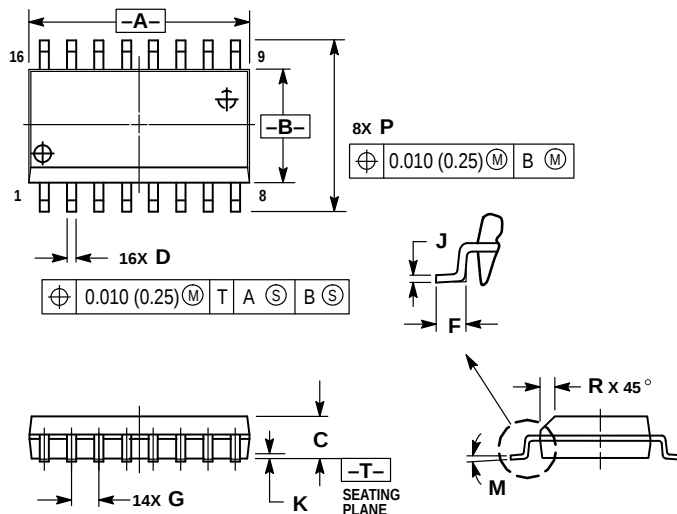
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
H	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

DW SUFFIX PLASTIC SOIC PACKAGE CASE 751G-02 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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MOTOROLA

MC14500B/D

