

Features

- High-speed: 35, 70 ns
- Ultra low DC operating current of 5mA (max.)
- Low Power Dissipation:
 - TTL Standby: 3 mA (Max.)
 - CMOS Standby: 20 μ A (Max.)
- Fully static operation
- All inputs and outputs directly compatible
- Three state outputs
- Ultra low data retention current ($V_{CC} = 2V$)
- Single $5V \pm 10\%$ Power Supply

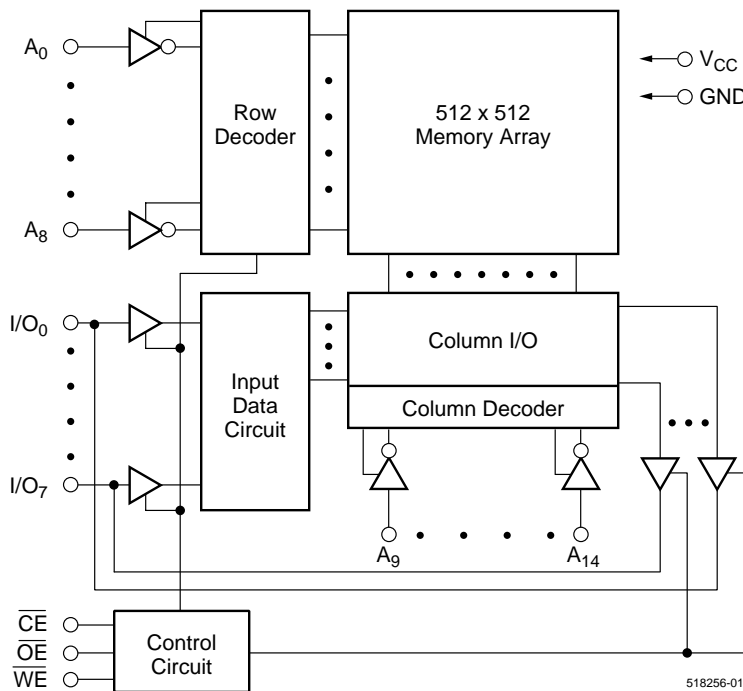
■ Packages

- 28-pin TSOP (Standard)
- 28-pin 600 mil PDIP
- 28-pin 330 mil SOP (450 mil pin-to-pin)

Description

The V62C518256 is a 262,144-bit static random access memory organized as 32,768 words by 8 bits. It is built with MOSEL VITELIC's high performance CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Functional Block Diagram



Device Usage Chart

Operating Temperature Range	Package Outline			Access Time (ns)		Power		Temperature Mark
	T	P	F	35	70	L	LL	
0°C to 70 °C	•	•	•	•	•	•	•	Blank
-40°C to +85°C	•	•	•	•	•	•	•	I

Pin Descriptions

A₀-A₁₄ Address Inputs

These 15 address inputs select one of the 32,768 x 8 bit segments in the RAM.

\overline{CE} Chip Enable Inputs

\overline{CE} is an active LOW input. Chip Enable must be LOW when reading from or writing to the device. When HIGH, the device is in standby mode with I/O pins in the high impedance state.

\overline{OE} Output Enable Input

The Output Enable input is active LOW. When \overline{OE} is LOW with \overline{CE} LOW and \overline{WE} HIGH, data of the selected memory location will be available on the I/O pins. When \overline{OE} is HIGH, the I/O pins will be in the high impedance state.

\overline{WE} Write Enable Input

An active LOW input, \overline{WE} input controls read and write operations. When \overline{CE} and \overline{WE} inputs are both LOW, the data present on the I/O pins will be written into the selected memory location.

I/O₀-I/O₇ Data Input and Data Output Ports

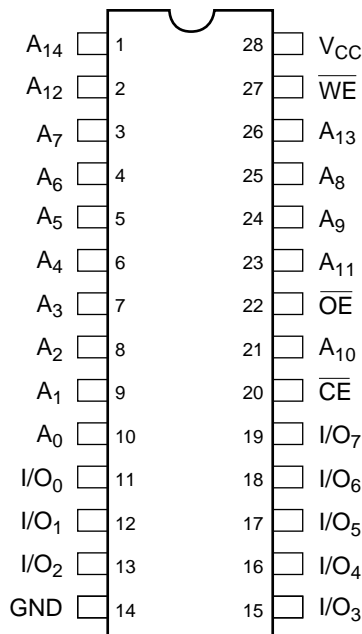
These 8 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

GND Ground

Pin Configurations (Top View)

28-Pin DIP/SOP



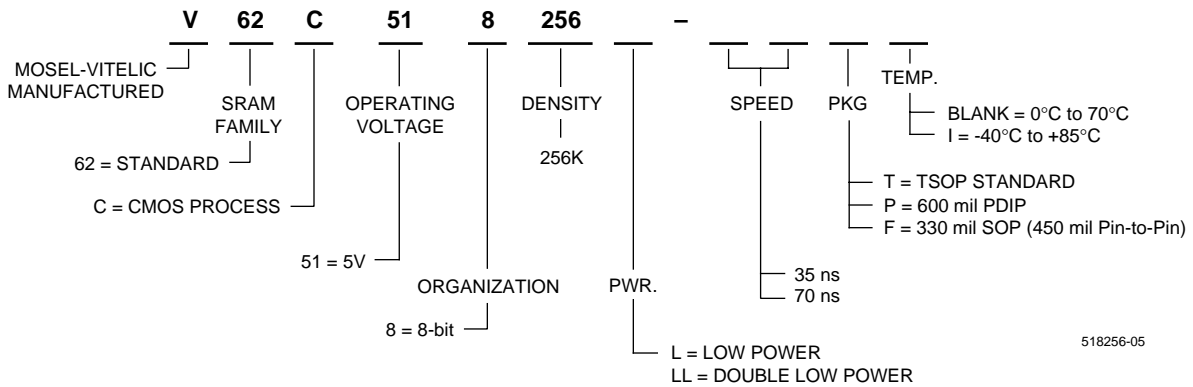
518256-01

28-Pin TSOP (Standard)



518256-03

Part Number Information



Absolute Maximum Ratings (1)

Symbol	Parameter	Commercial	Industrial	Units
V _{CC}	Supply Voltage	-0.5 to +7	-0.5 to +7	V
V _N	Input Voltage	-0.5 to +7	-0.5 to +7	V
V _{DQ}	Input/Output Voltage Applied	V _{CC} + 0.5	V _{CC} + 0.5	V
T _{BIAS}	Temperature Under Bias	-10 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-65 to +150	-65 to +150	°C

NOTE:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance*

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{IO} = 0V	8	pF

NOTE:

* This parameter is guaranteed and not tested.

Truth Table

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D _{OUT}
Read	L	H	H	High Z
Write	L	X	L	D _{IN}

NOTE:

X = Don't Care, L = LOW, H = HIGH

DC Electrical Characteristics (over all temperature ranges, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input LOW Voltage ^(1,2)		-0.5	—	0.8	V
V_{IH}	Input HIGH Voltage ⁽¹⁾		2.2	—	6	V
I_{IL}	Input Leakage Current	$V_{CC} = \text{Max}, V_{IN} = 0V \text{ to } V_{CC}$	-2	—	2	μA
I_{OL}	Output Leakage Current	$V_{CC} = \text{Max}, \overline{CE} = V_{IH}, V_{OUT} = 0V \text{ to } V_{CC}$	-2	—	2	μA
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}, I_{OL} = 2.1\text{mA}$	—	—	0.4	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}, I_{OH} = -1\text{mA}$	2.4	—	—	V

Symbol	Parameter	Power	Com. ⁽⁴⁾	Ind. ⁽⁴⁾	Units
I_{CC}	Operating Power Supply Current, $\overline{CE} = V_{IL}$ Output Open, $V_{CC} = \text{Max.}, f = 0$	READ	5	6	mA
		WRITE	40	50	
I_{CC1}	Average Operating Current, $\overline{CE} \leq V_{IL}$ Output Open, $V_{CC} = \text{Max.}, f = f_{MAX}^{(3)}$		60	70	mA
I_{SB}	TTL Standby Current $CE \geq V_{IH}, V_{CC} = \text{Max.}$	L	4	5	mA
		LL	3	4	
I_{SB1}	CMOS Standby Current, $\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, V_{CC} = \text{Max.}$	L	60	70	μA
		LL	20	30	

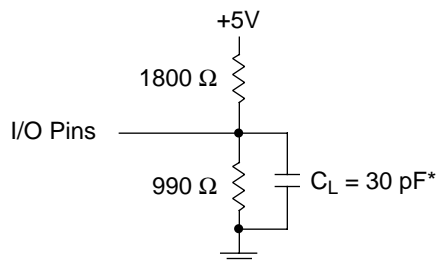
NOTES:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. V_{IL} (Min.) = -3.0V for pulse width < 20ns.
3. $f_{MAX} = 1/t_{RC}$.
4. Maximum values.

AC Test Conditions

Input Pulse Levels	0 to 3V
Input Rise and Fall Times	5 ns
Timing Reference Levels	1.5V
Output Load	see below

AC Test Loads and Waveforms



* Includes scope and jig capacitance

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

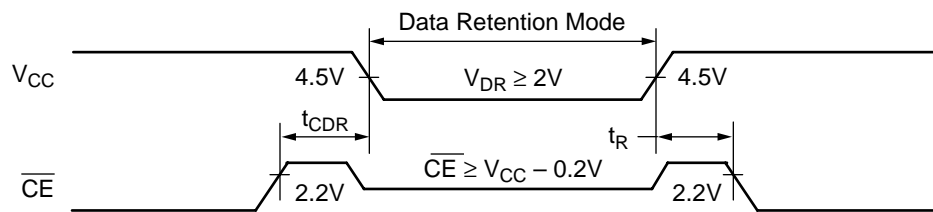
Data Retention Characteristics

Symbol	Parameter	Power	Min.	Typ. ⁽²⁾	Max.	Units	
V_{DR}	V_{CC} for Data Retention $\overline{CE} \geq V_{CC} - 0.2V$		2.0	—	5.5	V	
I_{CCDR}	Data Retention Current $V_{DR} = 3.0V, \overline{CE} \geq V_{DR} - 0.2V$	Com'l	L	—	0.5	50	μA
			LL	—	0.5	15	
		Ind.	L	—	—	70	
			LL	—	—	20	
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns	
t_R	Operation Recovery Time (see Retention Waveform)		$t_{RC}^{(1)}$	—	—	ns	

NOTES:

1. t_{RC} = Read Cycle Time
2. $T_A = +25^\circ C$.

Low V_{CC} Data Retention Waveform



518256-07

AC Electrical Characteristics

(over all temperature ranges)

Read Cycle

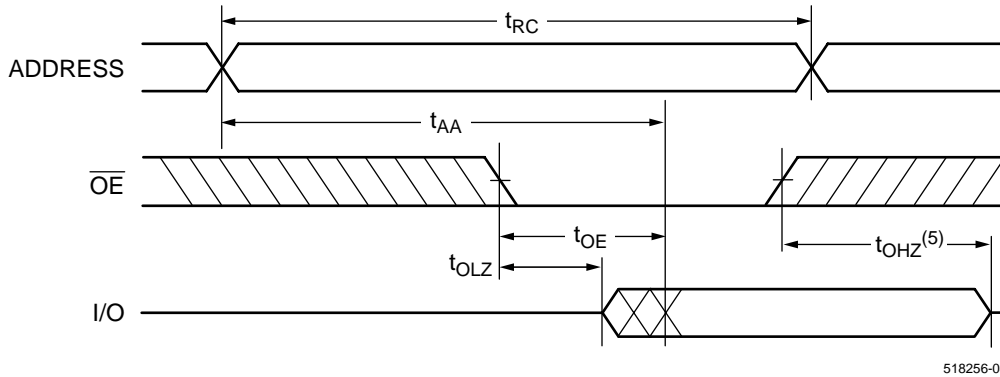
Parameter Name	Parameter	-35		-70		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35	—	70	—	ns
t_{AA}	Address Access Time	—	35	—	70	ns
t_{ACS}	Chip Enable Access Time	—	35	—	70	ns
t_{OE}	Output Enable to Output Valid	—	15	—	30	ns
t_{CLZ}	Chip Enable to Output in Low Z	5	—	5	—	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	ns
t_{CHZ}	Chip Disable to Output in High Z	0	20	0	20	ns
t_{OHZ}	Output Disable to Output in High Z	0	20	0	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	ns

Write Cycle

Parameter Name	Parameter	-35		-70		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	35	—	70	—	ns
t_{CW}	Chip Enable to End of Write	35	—	60	—	ns
t_{AS}	Address Setup Time	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	35	—	60	—	ns
t_{WP}	Write Pulse Width	25	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{WHZ}	Write to Output High-Z	0	20	0	25	ns
t_{DW}	Data Setup to End of Write	25	—	30	—	ns
t_{DH}	Data Hold from End of Write	0	—	0	—	ns
t_{OHZ}	Output Disable to Output in High Z	0	25	0	30	ns
t_{OW}	Output Active from End of Write	5	—	5	—	ns

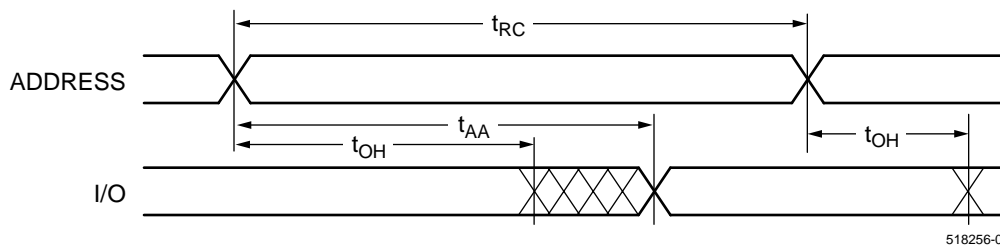
Switching Waveforms (Read Cycle)

Read Cycle 1^(1, 2)



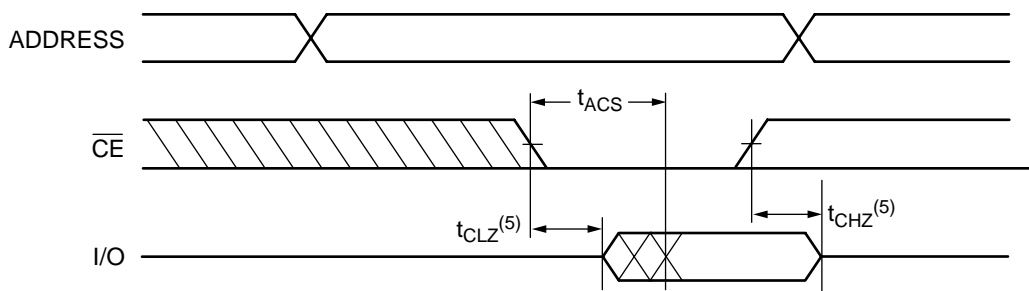
518256-08

Read Cycle 2^(1, 2, 4)



518256-09

Read Cycle 3^(1, 3, 4)



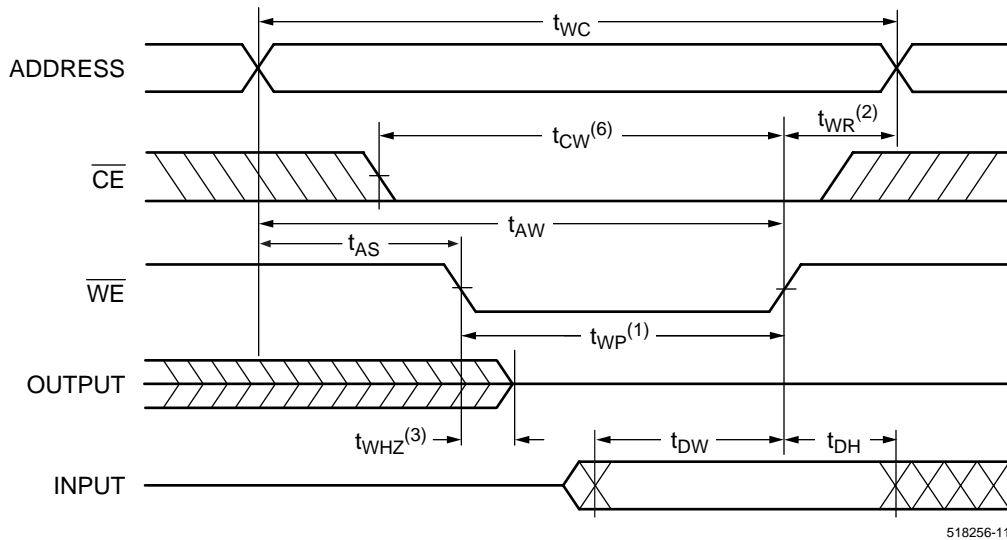
518256-10

NOTES:

1. $\overline{WE} = V_{IH}$.
2. $\overline{CE} = V_{IL}$.
3. Address valid prior to or coincident with \overline{CE} transition LOW.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$. This parameter is guaranteed and not 100% tested.

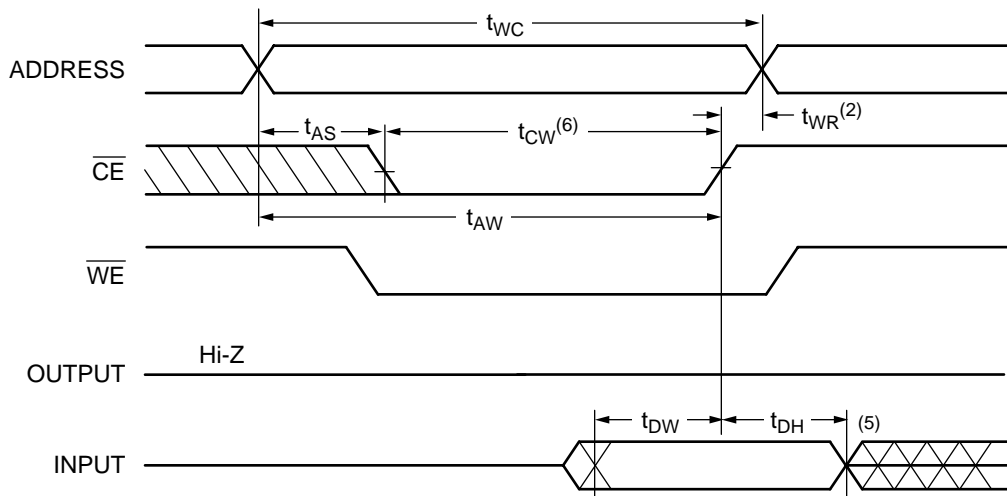
Switching Waveforms (Write Cycle)

Write Cycle 1 (\overline{WE} Controlled)⁽⁴⁾



518256-11

Write Cycle 2 (\overline{CE} Controlled)⁽⁴⁾



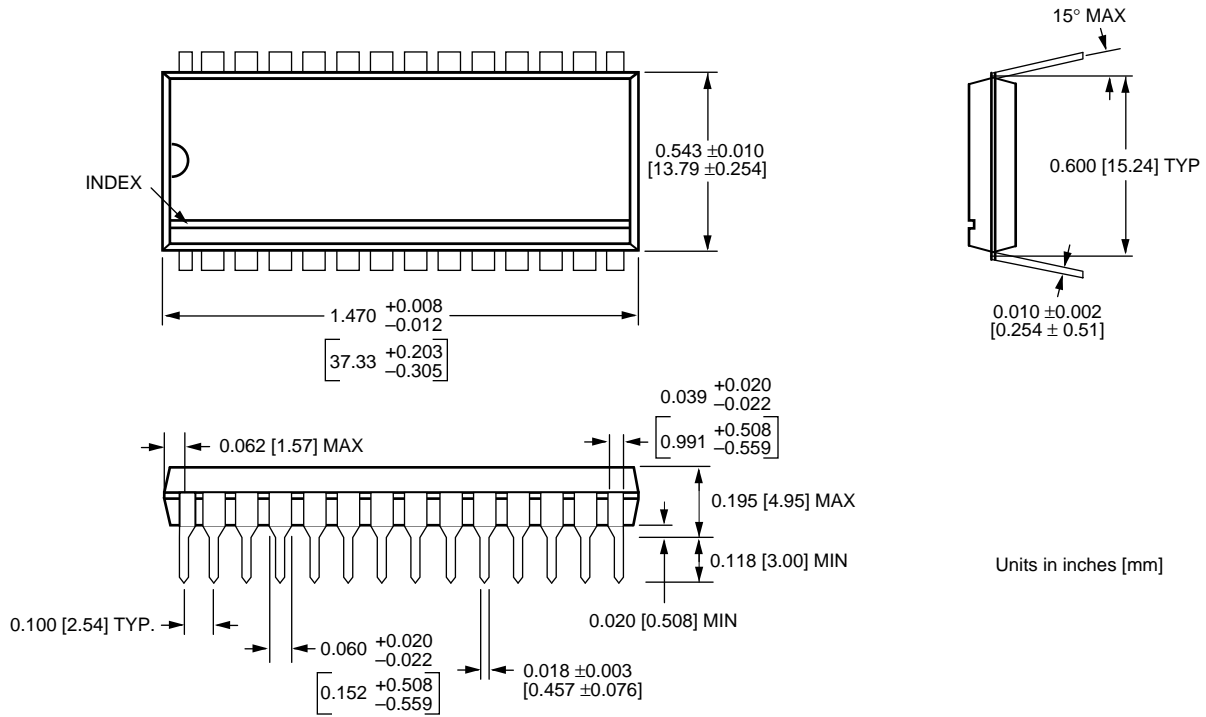
518256-12

NOTES:

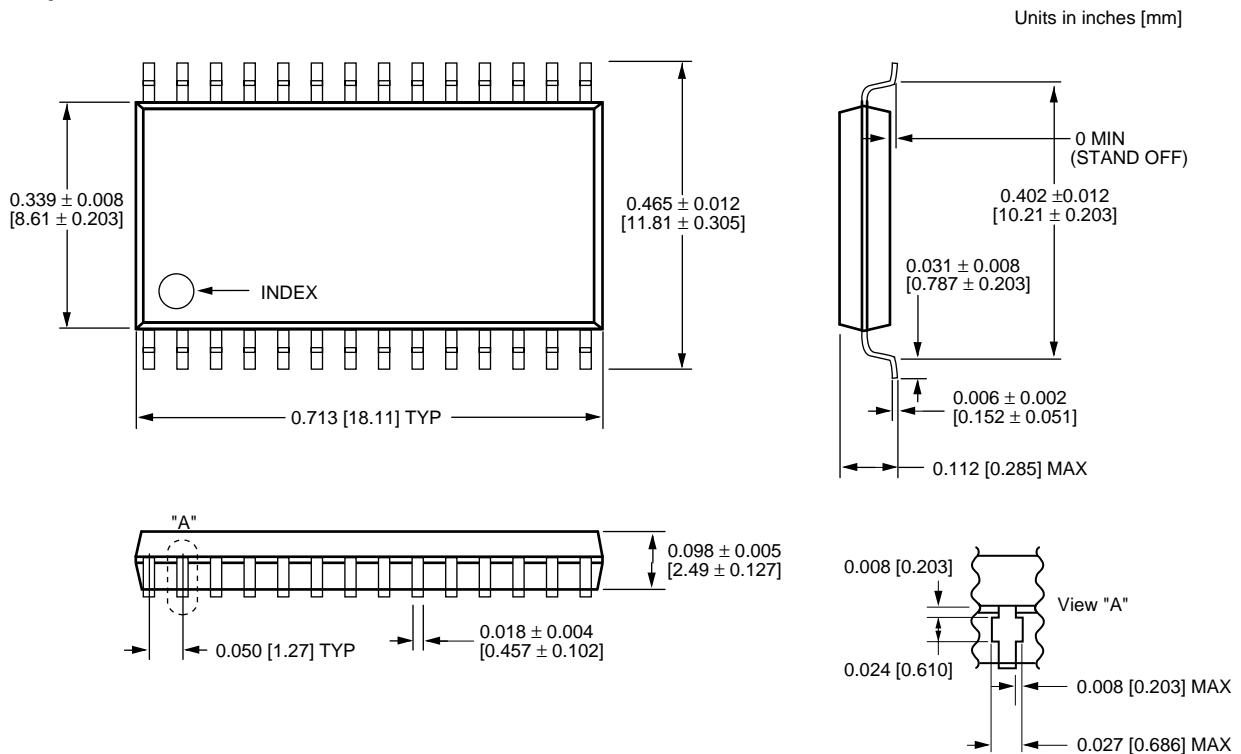
1. The internal write time of the memory is defined by the overlap of \overline{CE} active and \overline{WE} low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
2. t_{WR} is measured from the earlier of \overline{CE} or \overline{WE} going HIGH.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. $\overline{OE} = V_{IL}$ or V_{IH} . However it is recommended to keep \overline{OE} at V_{IH} during write cycle to avoid bus contention.
5. If \overline{CE} is LOW during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. t_{CW} is measured from \overline{CE} going LOW to the end of write.

Package Diagrams

28-pin 600 mil Plastic DIP



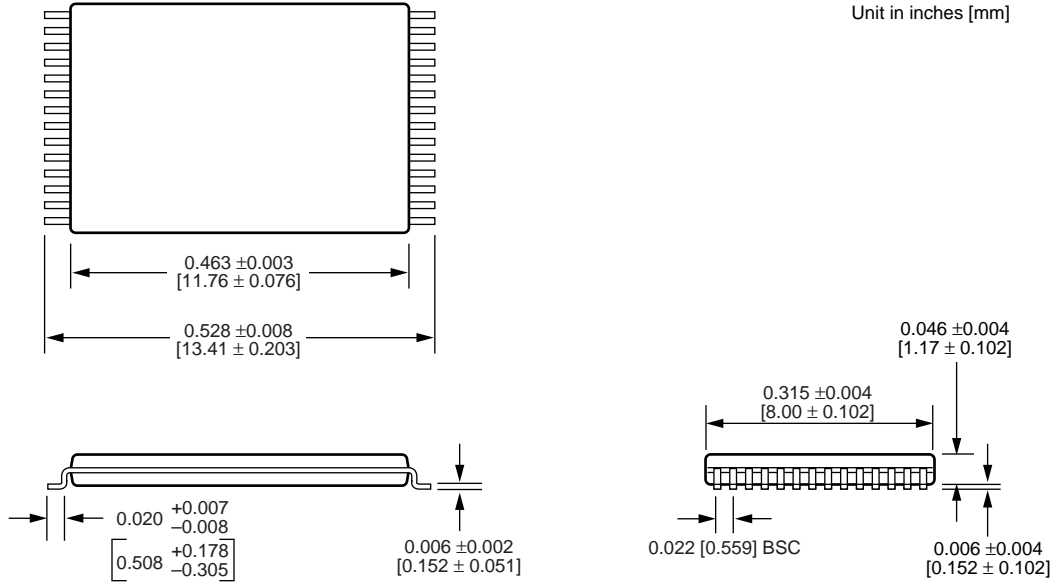
28-pin 330 mil SOP



Package Diagrams (Cont'd)

28-Pin TSOP

Unit in inches [mm]



U.S.A.

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0185

HONG KONG

19 DAI FU STREET
TAIPO INDUSTRIAL ESTATE
TAIPO, NT, HONG KONG
PHONE: 852-2665-4883
FAX: 852-2664-7535

TAIWAN

7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 886-2-2545-1213
FAX: 886-2-2545-1209

1 CREATION ROAD I
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 886-3-578-3344
FAX: 886-3-579-2838

SINGAPORE

10 ANSON ROAD #23-13
INTERNATIONAL PLAZA
SINGAPORE 079903
PHONE: 65-3231801
FAX: 65-3237013

JAPAN

WBG MARINE WEST 25F
6, NAKASE 2-CHOME
MIHAMA-KU, CHIBA-SHI
CHIBA 261-71
PHONE: 81-43-299-6000
FAX: 81-43-299-6555

IRELAND & UK

BLOCK A UNIT 2
BROOMFIELD BUSINESS PARK
MALAHIDE
CO. DUBLIN, IRELAND
PHONE: +353 1 8038020
FAX: +353 1 8038049

**GERMANY
(CONTINENTAL
EUROPE & ISRAEL)**

71083 HERRENBERG
BENZSTR. 32
GERMANY
PHONE: +49 7032 2796-0
FAX: +49 7032 2796 22

U.S. SALES OFFICES**NORTHWESTERN**

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0185

SOUTHWESTERN

SUITE 200
5150 E. PACIFIC COAST HWY.
LONG BEACH, CA 90804
PHONE: 562-498-3314
FAX: 562-597-2174

CENTRAL & SOUTHEASTERN

604 FIELDWOOD CIRCLE
RICHARDSON, TX 75081
PHONE: 972-690-1402
FAX: 972-690-0341

NORTHEASTERN

SUITE 436
20 TRAFALGAR SQUARE
NASHUA, NH 03063
PHONE: 603-889-4393
FAX: 603-889-9347

The information in this document is subject to change without notice.

MOSEL VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.