Freescale Semiconductor
Data Sheet: Advance Information

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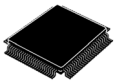
MPC5604P



144 LQFP
20 mm x 20 mm

100 LQFP
14 mm_x_14 mm

MPC5604P Microcontroller Data Sheet

- High performance 64 MHz e200z0h CPU
  - 32-bit Power Architecture Book E CPU
  - Variable Length Encoding (VLE)
- Available memory
  - As much as 512 KB on-chip code flash memory with additional 64 KB for EEPROM emulation (data flash), with ECC, with erase/program controller
  - As much as 40 KB on-chip RAM with ECC
- Fail safe protection
  - Programmable watchdog timer
  - Junction temperature sensor
  - Non-maskable interrupt
  - Fault collection unit
- Nexus L2+ interface
- Interrupts
  - 16 priority level controller
- 16-channel eDMA controller
- General purpose I/Os
  - Individually programmable as input, output or special function
- Two general purpose eTimer units
  - Six timers each with up/down count capabilities
  - 16-bit resolution, cascadable counters
  - Quadrature decode with rotation direction flag
  - Double buffer input capture and output compare
- Communications interfaces
  - Two LINFlex channels (LIN 2.1)
  - Four DSPI channels with automatic chip select generation
  - FlexCAN interface (2.0B Active) with 32 message objects
  - Safety port based on FlexCAN with 32 message objects and up to 7.5 Mbit/s capability; usable as second CAN when not used as safety port
  - FlexRay™ module (V2.1) with dual or single channel, 32 message objects and up to 10 Mbit/s
- Two 10-bit A/D converters
  - Two × 15 input channels, four channels shared among the two A/D converters
  - Conversion time < 1 µs including sampling time at full precision
  - Programmable Cross Triggering Unit (CTU)
  - Four analog watchdogs with interrupt capability
- On-chip CAN/UART/FlexRay Bootstrap loader with Boot Assist Module (BAM)
- FlexPWM unit
  - Eight complementary or independent outputs with ADC synchronization signals
  - Polarity control, reload unit
  - Integrated configurable dead time unit and inverter fault input pins
  - 16-bit resolution, up to 2 × f_{CPU}
  - Lockable configuration
  - Clock generation
  - 4–40 MHz main oscillator
  - 16 MHz internal RC oscillator
  - Software controlled FMPLL capable of speeds as fast as 64 MHz
- Voltage supply
  - 3.3 V or 5 V supply for I/Os and ADC
  - On-chip single supply voltage regulator with external ballast transistor
  - Operating temperature ranges: –40 to 125 °C or –40 to 105 °C

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Table of Contents

1 Overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5604P series of microcontroller units (MCUs). For functional characteristics, refer to the *MPC5604P Microcontroller Reference Manual.*

MPC5604P microcontrollers are members of a new family of next generation microcontrollers built on the Power Architecture™. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

The MPC5604P family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the MPC5604P automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original PowerPC user instruction set architecture (UISA). It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.1 Device comparison

Table 1 provides a summary of different members of the MPC5604P family and their features to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 1. MPC5604P device comparison

Feature	MPC5603P	MPC5604P
Code Flash memory (with ECC)	384 KB	512 KB
Data Flash / EE (with ECC)	64 KB	64 KB
RAM (with ECC)	36 KB	40 KB
Processor core	32-bit e200z0h	
Instruction set	VLE	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) modules	2	
INTC (interrupt controller) channels	147	
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)	
Enhanced DMA (direct memory access) channels	16	
FlexRay	Yes[1]	
FlexCAN (controller area network)	2[2,3]	
Safety port	Yes (via second FlexCAN module)	
FCU (fault collection unit)	Yes	
CTU (cross triggering unit)	Yes	
eTimer channels	2 × 6	
FlexPWM (pulse-width modulation) channels	8	
Analog-to-digital converters (ADC)	Two (10-bit, 16-channel)	
LINFlex modules	2	
DSPI (deserial serial peripheral interface) modules	4	

Table 1. MPC5604P device comparison (continued)

Feature		MPC5603P	MPC5604P
CRC (cyclic redundancy check) unit		Yes	
Junction temperature sensor		Yes	
JTAG interface		Yes	
Nexus port controller (NPC)		Yes (Level 2+)	
Supply	Digital power supply[4]	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		100 LQFP 144 LQFP	
Temperature	Standard ambient temperature	–40 to 125 °C	
	Extended ambient temperature[5]	–40 to 145 °C	

1 32 message buffers, dual-channel.

2 Each FlexCAN module has 32 message buffers.

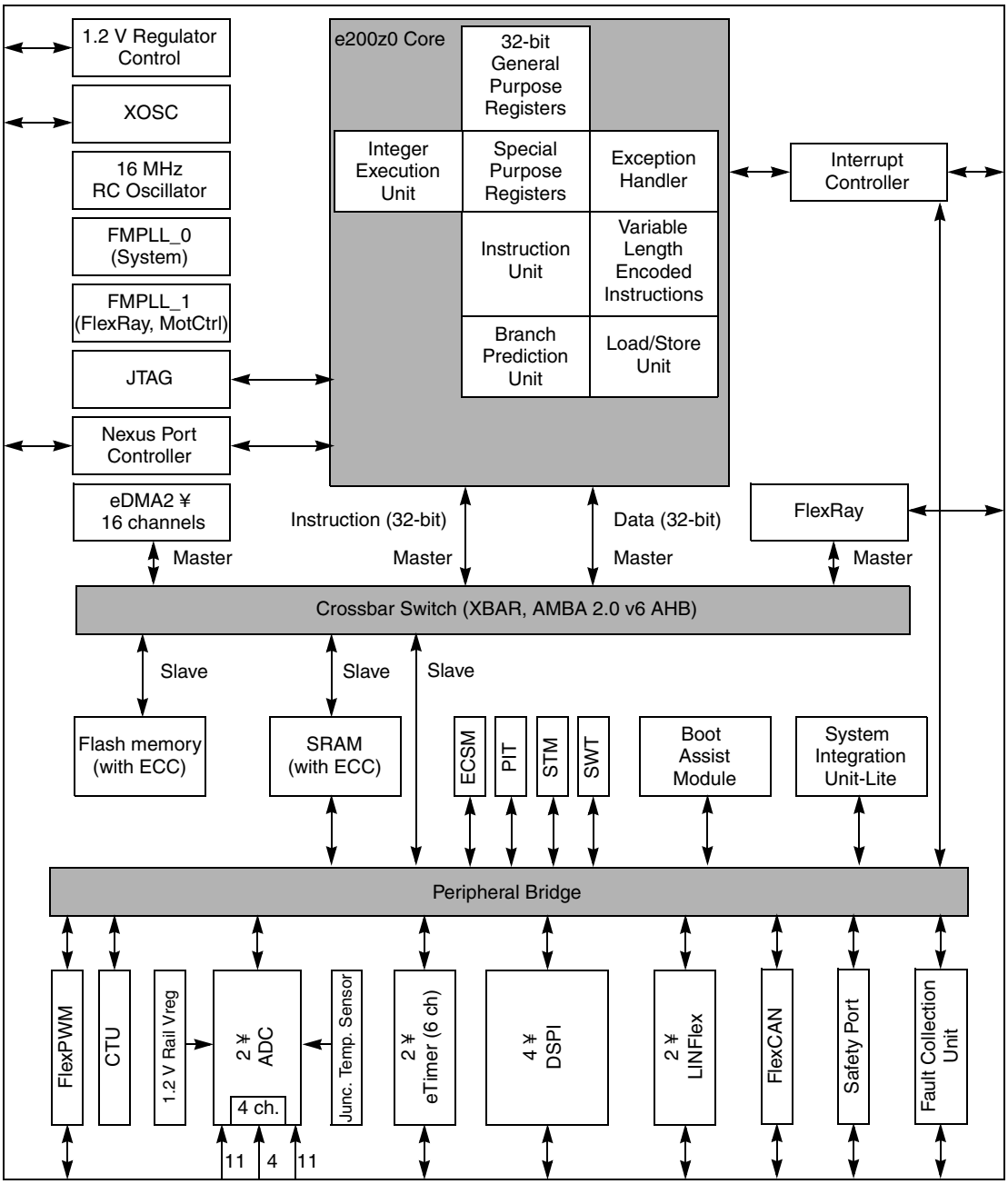
3 One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.

4 3.3 V range and 5 V range correspond to different orderable parts.

5 Thermally enhanced 100-pin and 144-pin LQFP packages are under analysis to support an extended ambient temperature range of –40 to 145 °C. The packages are not yet available.

1.2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5604P MCU.



CTUCross Triggering Unit
DSPIDeserial Serial Peripheral Interface
ECSMError Correction Status Module
eTimerEnhanced Timer
FlexCANFlexible Controller Area Network
FlexPWMFlexible Pulse Width Modulation
FMPLLFrequency-Modulated Phase-Locked Loop
LINFlexSerial Communication Interface (LIN support)
PITPeriodic Interrupt Timer
SRAMStatic Random-Access Memory
STMSystem Timer Module
SWTSoftware Watchdog Timer

Figure 1. MPC5604P block diagram

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures.

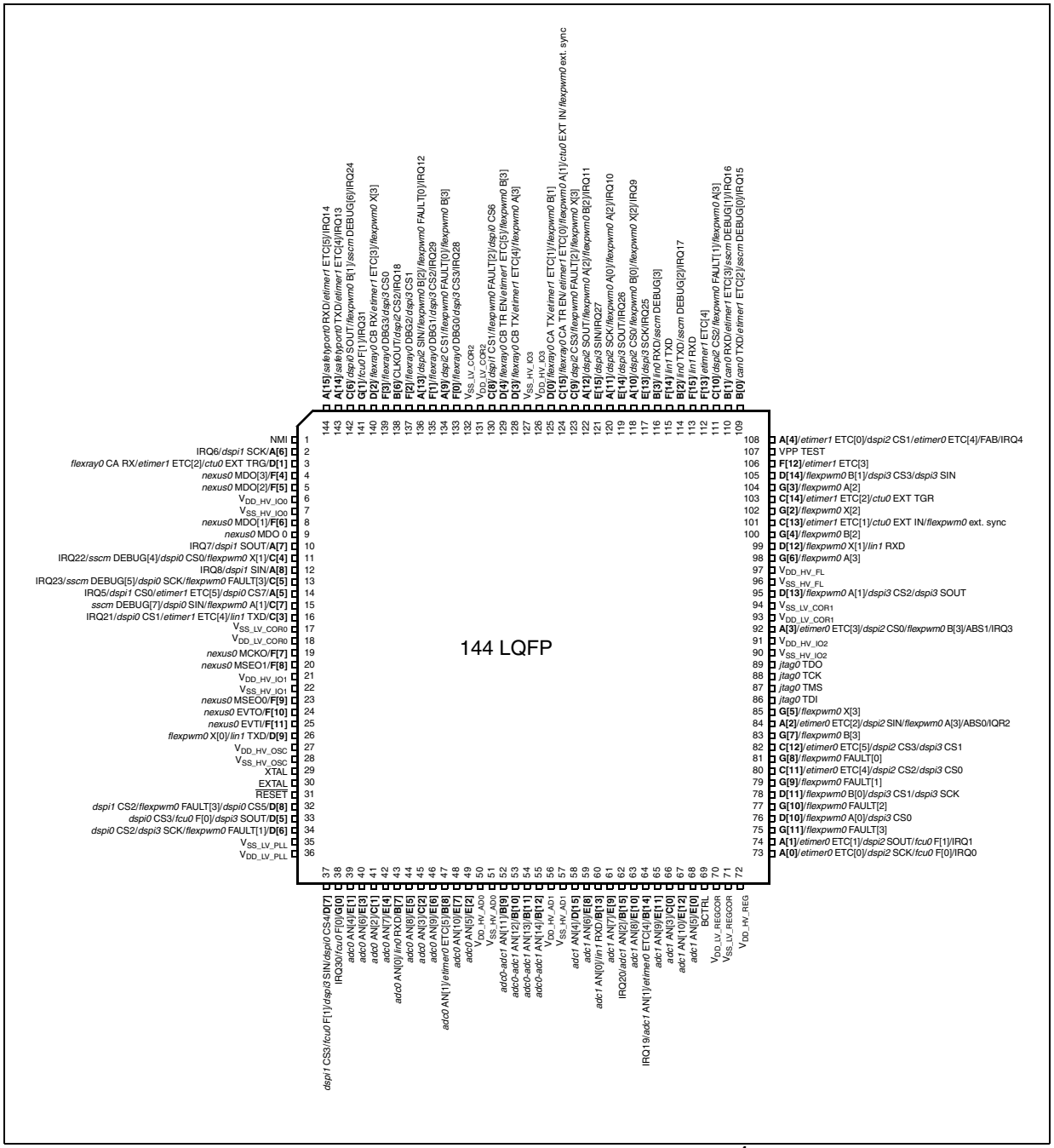


Figure 2. 144-pin LQFP pinout (top view)[1]

1. Availability of port pin alternate functions depends on product selection

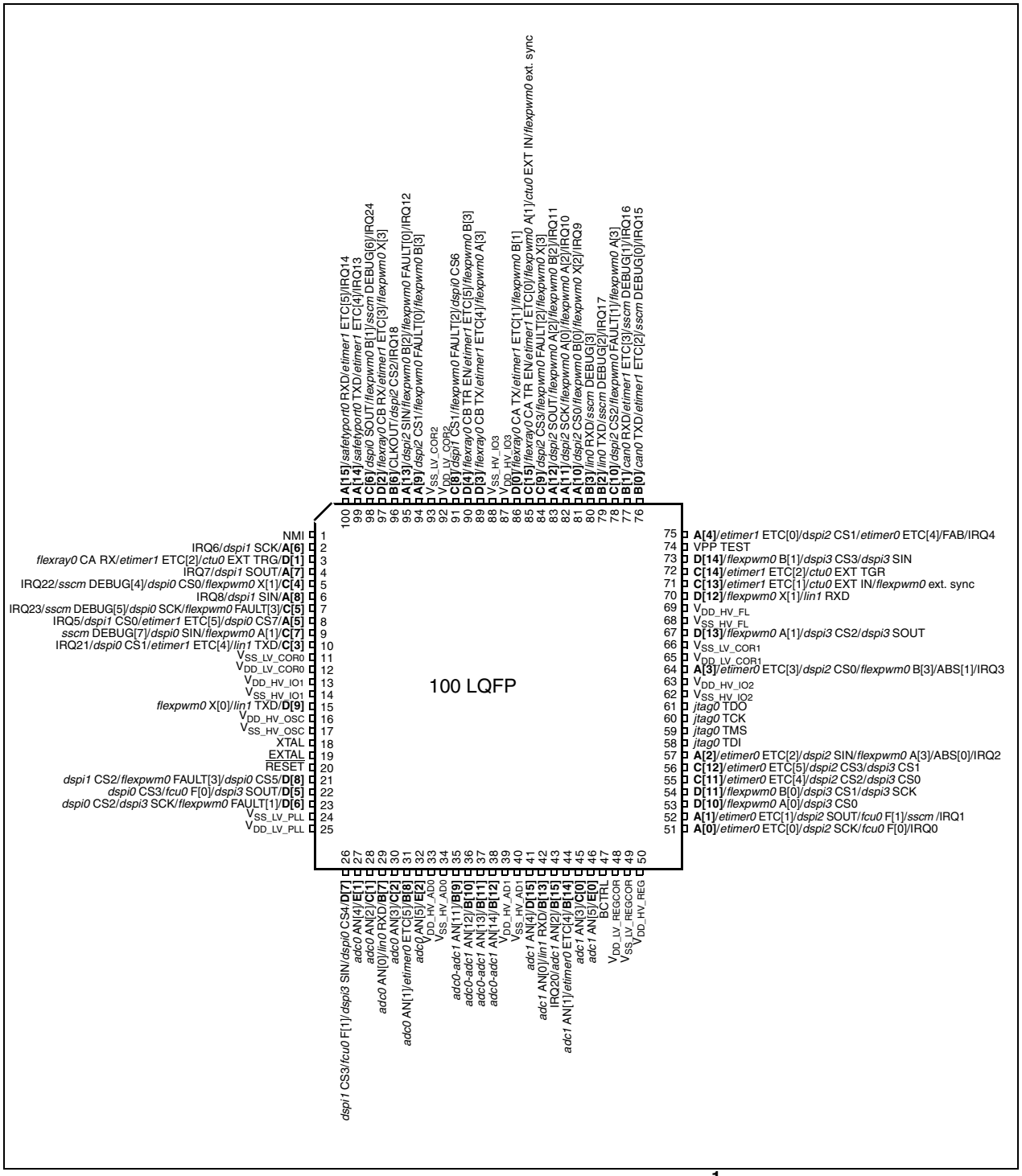


Figure 3. 100-pin LQFP pinout (top view)[1]

1. Availability of port pin alternate functions depends on product selection

2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the MPC5604P devices.

2.2.1 Power supply and reference voltage pins

Table 2 lists the power supply and reference voltage for the MPC5604P devices.

Table 2. Supply pins

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
VREG control and power supply pins. Pins available on 100-pin and 144-pin package.			
BCTRL	Voltage regulator external NPN Ballast base control pin	47	69
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72
$V_{DD\_LV\_REGCOR}$	1.2 V decoupling[1] pins for core logic supply and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling[1] pins for core logic GND and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71
ADC0/ADC1 reference and supply voltage. Pins available on 100-pin and 144-pin package.			
$V_{DD\_HV\_AD0}$[2]	ADC0 supply and high reference voltage	33	50
$V_{SS\_HV\_AD0}$	ADC0 ground and low reference voltage	34	51
$V_{DD\_HV\_AD1}$	ADC1 supply and high reference voltage	39	56
$V_{SS\_HV\_AD1}$	ADC1 ground and low reference voltage	40	57
Power supply pins (3.3 V or 5.0 V). All pins available on 144-pin package. Five pairs (V_{DD}; V_{SS}) available on 100-pin package.			
$V_{DD\_HV\_IO0}$[3]	Input/Output supply voltage	—	6
$V_{SS\_HV\_IO0}$[3]	Input/Output ground	—	7
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	**87**	126
$V_{SS\_HV\_IO3}$	Input/Output ground	**88**	127
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28

Table 2. Supply pins (continued)

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
Power supply pins (1.2 V). All pins available on 100-pin and 144-pin package.			
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0}$ pin.	12	18
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR0}$ pin.	11	17
$V_{DD\_LV\_COR1}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR1}$ pin.	65	93
$V_{SS\_LV\_COR1}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR1}$ pin.	66	94
$V_{DD\_LV\_COR2}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR2}$ pin.	92	131
$V_{SS\_LV\_COR2}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR\ 2}$pin.	93	132
$V_{DD\_LV\_COR3}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR3}$ pin.	25	36
$V_{SS\_LV\_COR3}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 3}$ pin.	24	35

1 See Section 3.6.1, “Voltage regulator electrical characteristics for more details

2 Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on $V_{DD\_HV\_ADx}$/$V_{SS\_HV\_ADx}$ pins.

3 Not available on 100-pin package

2.2.2 System Pins

Table 3 and Table 4 contain information on pin functions for the MPC5604P devices. The pins listed in Table 3 are single-function pins. The pins shown in Table 4 are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 3. System Pins

Symbol	Description	Direction	Pad Speed[1]		Pin	
			SRC=0	SRC=1	100-pin	144-pin
Dedicated pins. All pins available on 144-pin package. MDO 0 not available on 100-pin package.						
MDO 0	Nexus Message Data Output—line 0	Output Only	Fast		—	9
NMI	Non Maskable Interrupt	Input Only	—	—	1	1
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.	—	—	—	18	29
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	—	—	—	19	30
TMS[2]	JTAG state machine control	Input Only	—	—	59	87
TCK[2]	JTAG clock	Input Only	—	—	60	88
TDI[2]	JTAG data input	Input Only	—	—	58	86
TDO[2]	JTAG data output	Output Only	Slow	Fast	61	89
Reset pin, available on 100-pin and 144-pin package.						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31
Test pin, available on 100-pin and 144-pin package.						
VPP TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107

1 SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register

2 In this pin there is an internal pull, refer to JTAGC chapter on MPC5604P Reference Manual for pull direction.

2.2.3 Pin Muxing

Table 4 defines the pin list and muxing for the MPC5604P devices.

Each row of Table 4 shows all the possible ways of configuring each pin, via “alternate functions”. The default function assigned to each pin after reset is the ALT0 function.

Pins marked as external interrupt capable can also be used to resume from STOP and HALT mode.

MPC5604P devices provide four main I/O pad types depending of the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

Table 4. Pin muxing

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
Port A (16-bit). Fully available on 100-pin and 144-pin package.									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIU Lite eTimer0 DSPI2 FCU0 SIU Lite	I/O I/O I/O O I	Slow	Medium	51	73
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIU Lite eTimer0 DSPI2 FCU0 SIU Lite	I/O I/O O O I	Slow	Medium	52	74
A[2][6]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIU Lite eTimer0 — FlexPWM0 DSPI2 mc_rgm SIU Lite	I/O I/O — O I I I	Slow	Medium	57	84
A[3][6]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[1] EIRQ[3]	SIU Lite eTimer0 DSPI2 FlexPWM0 mc_rgm SIU Lite	I/O I/O I/O O I I	Slow	Medium	64	92
A[4][6]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1 ETC[4] FAB EIRQ[4]	SIU Lite eTimer1 DSPI2 eTimer0 mc_rgm SIU Lite	I/O I/O O I/O I I	Slow	Medium	75	108
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0 ETC[5] CS7 EIRQ[5]	SIU Lite DSPI1 eTimer1 DSPI0 SIU Lite	I/O I/O I/O O I	Slow	Medium	8	14
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK — — EIRQ[6]	SIU Lite DSPI1 — — SIU Lite	I/O I/O — — I	Slow	Medium	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 —	GPIO[7] SOUT — — EIRQ[7]	SIU Lite DSPI1 — — SIU Lite	I/O O — — I	Slow	Medium	4	10

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — — — SIN EIRQ[8]	SIU Lite — — — DSPI1 SIU Lite	I/O — — — I I	Slow	Medium	6	12
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3 —	GPIO[9] CS1 — B[3] FAULT[0]	SIU Lite DSPI2 — FlexPWM0 FlexPWM0	I/O O — O I	Slow	Medium	94	134
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3 —	GPIO[10] CS0 B[0] X[2] EIRQ[9]	SIU Lite DSPI2 FlexPWM0 FlexPWM0 SIU Lite	I/O I/O O I/O I	Slow	Medium	81	118
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK A[0] A[2] EIRQ[10]	SIU Lite DSPI2 FlexPWM0 FlexPWM0 SIU Lite	I/O I/O O O I	Slow	Medium	82	120
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT A[2] B[2] EIRQ[11]	SIU Lite DSPI2 FlexPWM0 FlexPWM0 SIU Lite	I/O O O O I	Slow	Medium	83	122
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[13] — B[2] — SIN FAULT[0] EIRQ[12]	SIU Lite — FlexPWM0 — DSPI2 FlexPWM0 SIU Lite	I/O — O — I I I	Slow	Medium	95	136
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD ETC[4] — EIRQ[13]	SIU Lite Safety Port0 eTimer1 — SIU Lite	I/O O I/O — I	Slow	Medium	99	143
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — ETC[5] — RXD EIRQ[14]	SIU Lite — eTimer1 — Safety Port0 SIU Lite	I/O — I/O — I I	Slow	Medium	100	144

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
Port B (16-bit). Fully available on 100-pin and 144-pin package.									
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD ETC[2] DEBUG[0] EIRQ[15]	SIU Lite CAN0 eTimer1 SSCM SIU Lite	I/O O I/O — I	Slow	Medium	76	109
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] — ETC[3] DEBUG[1] RXD EIRQ[16]	SIU Lite — eTimer1 SSCM CAN0 SIU Lite	I/O — I/O — I I	Slow	Medium	77	110
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD — DEBUG[2] EIRQ[17]	SIU Lite LIN0 — SSCM SIU Lite	I/O O — — I	Slow	Medium	79	114
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — — DEBUG[3] RXD	SIU Lite — — SSCM LIN0	I/O — — — I	Slow	Medium	80	116
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] CLKOUT CS2 — EIRQ[18]	SIU Lite Control DSPI2 — SIU Lite	I/O O O — I	Slow	Medium	96	138
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIU Lite — — — ADC0 LIN0	Input Only	—	—	29	43
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIU Lite — — — ADC0 eTimer0	Input Only	—	—	31	47
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIU Lite — — — ADC0 – ADC1	Input Only	—	—	35	52

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIU Lite — — — ADC0 – ADC1	Input Only	—	—	36	53
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3 —	GPIO[27] — — — AN[13]	SIU Lite — — — ADC0 – ADC1	Input Only	—	—	37	54
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — — — AN[14]	SIU Lite — — — ADC0 – ADC1	Input Only	—	—	38	55
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[29] — — — AN[0] RXD	SIU Lite — — — ADC1 LIN1	Input Only	—	—	42	60
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[30] — — — AN[1] ETC[4] EIRQ[19]	SIU Lite — — — ADC1 eTimer0 SIU Lite	Input Only	—	—	44	64
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[31] — — — AN[2] EIRQ[20]	SIU Lite — — — ADC1 SIU Lite	Input Only	—	—	43	62
Port C (16-bit). Fully available on 100-pin and 144-pin package.									
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3 —	GPIO[32] — — — AN[3]	SIU Lite — — — ADC1	Input Only	—	—	45	66
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 —	GPIO[33] — — — AN[2]	SIU Lite — — — ADC0	Input Only	—	—	28	41

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 —	GPIO[34] — — — AN[3]	SIU Lite — — — ADC0	Input Only	—	—	30	45
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 —	GPIO[35] CS1 ETC[4] TXD EIRQ[21]	SIU Lite DSPI0 eTimer1 LIN1 SIU Lite	I/O O I/O O I	Slow	Medium	10	16
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 —	GPIO[36] CS0 X[1] DEBUG[4] EIRQ[22]	SIU Lite DSPI0 FlexPWM0 SSCM SIU Lite	I/O I/O I/O — I	Slow	Medium	5	11
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[37] SCK — DEBUG[5] FAULT[3] EIRQ[23]	SIU Lite DSPI0 — SSCM FlexPWM0 SIU Lite	I/O I/O — — I I	Slow	Medium	7	13
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT B[1] DEBUG[6] EIRQ[24]	SIU Lite DSPI0 FlexPWM0 SSCM SIU Lite	I/O O O — I	Slow	Medium	98	142
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 —	GPIO[39] — A[1] DEBUG[7] SIN	SIU Lite — FlexPWM0 SSCM DSPI0	I/O — O — I	Slow	Medium	9	15
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3 —	GPIO[40] CS1 — CS6 FAULT[2]	SIU Lite DSPI1 — DSPI0 FlexPWM0	I/O O — O I	Slow	Medium	91	130
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3 —	GPIO[41] CS3 — X[3] FAULT[2]	SIU Lite DSPI2 — FlexPWM0 FlexPWM0	I/O O — I/O I	Slow	Medium	84	123
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3 —	GPIO[42] CS2 — A[3] FAULT[1]	SIU Lite DSPI2 — FlexPWM0 FlexPWM0	I/O O — O I	Slow	Medium	78	111

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[4] CS2 CS0	SIU Lite eTimer0 DSPI2 DSPI3	I/O I/O O I/O	Slow	Medium	55	80
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	GPIO[44] ETC[5] CS3 CS1	SIU Lite eTimer0 DSPI2 DSPI3	I/O I/O O O	Slow	Medium	56	82
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[45] ETC[1] — — EXT IN EXT. SYNC	SIU Lite eTimer1 — — ctu0 FlexPWM0	I/O I/O — — I I	Slow	Medium	71	101
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3	GPIO[46] ETC[2] EXT TGR —	SIU Lite eTimer1 ctu0 —	I/O I/O O —	Slow	Medium	72	103
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[47] CA TR EN ETC[0] A[1] EXT IN EXT. SYNC	SIU Lite FlexRay0 eTimer1 FlexPWM0 ctu0 FlexPWM0	I/O O I/O O I I	Slow	Symmetric	85	124
Port D (16-bit). Fully available on 100-pin and 144-pin package.									
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] CA TX ETC[1] B[1]	SIU Lite FlexRay0 eTimer1 FlexPWM0	I/O O I/O O	Slow	Symmetric	86	125
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3 —	GPIO[49] — ETC[2] EXT TRG CA RX	SIU Lite — eTimer1 ctu0 FlexRay0	I/O — I/O O I	Slow	Medium	3	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3 —	GPIO[50] — ETC[3] X[3] CB RX	SIU Lite — eTimer1 FlexPWM0 FlexRay0	I/O — I/O I/O I	Slow	Medium	97	140
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] CB TX ETC[4] A[3]	SIU Lite FlexRay0 eTimer1 FlexPWM0	I/O O I/O I/O	Slow	Symmetric	89	128
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] CB TR EN ETC[5] B[3]	SIU Lite FlexRay0 eTimer1 FlexPWM0	I/O O I/O O	Slow	Symmetric	90	129

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] SOUT	SIU Lite DSPI0 FCU0 DSPI3	I/O O O O	Slow	Medium	22	33
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 SCK — FAULT[1]	SIU Lite DSPI0 DSPI3 — FlexPWM0	I/O O I/O — I	Slow	Medium	23	34
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3 F[1] CS4 SIN	SIU Lite DSPI1 FCU0 DSPI0 DSPI3	I/O O O O I	Slow	Medium	26	37
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3 —	GPIO[56] CS2 — CS5 FAULT[3]	SIU Lite DSPI1 — DSPI0 FlexPWM0	I/O O — O I	Slow	Medium	21	32
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIU Lite FlexPWM0 LIN1 —	I/O I/O O —	Slow	Medium	15	26
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] CS0 —	SIU Lite FlexPWM0 DSPI3 —	I/O O I/O —	Slow	Medium	53	76
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] CS1 SCK	SIU Lite FlexPWM0 DSPI3 DSPI3	I/O O O I/O	Slow	Medium	54	78
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIU Lite FlexPWM0 — — LIN1	I/O I/O — — I	Slow	Medium	70	99
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] CS2 SOUT	SIU Lite FlexPWM0 DSPI3 DSPI3	I/O O O O	Slow	Medium	67	95
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] B[1] CS3 — SIN	SIU Lite FlexPWM0 DSPI3 — DSPI3	I/O O O — I	Slow	Medium	73	105

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[4]	SIU Lite — — — ADC1	Input Only	—	—	41	58
Port E(16-bit). Fully available on 144-pin package. E[0], E[1] and E[2] available on 100-pin package.									
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[5]	SIU Lite — — — ADC1	Input Only	—	—	46	68
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIU Lite — — — ADC0	Input Only	—	—	27	39
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIU Lite — — — ADC0	Input Only	—	—	32	49
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIU Lite — — — ADC0	Input Only	—	—	—	40
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIU Lite — — — ADC0	Input Only	—	—	—	42
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIU Lite — — — ADC0	Input Only	—	—	—	44
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIU Lite — — — ADC0	Input Only	—	—	—	46
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIU Lite — — — ADC0	Input Only	—	—	—	48

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3 —	GPIO[72] — — — AN[6]	SIU Lite — — — ADC1	Input Only	—	—	—	59
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3 —	GPIO[73] — — — AN[7]	SIU Lite — — — ADC1	Input Only	—	—	—	61
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3 —	GPIO[74] — — — AN[8]	SIU Lite — — — ADC1	Input Only	—	—	—	63
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3 —	GPIO[75] — — — AN[9]	SIU Lite — — — ADC1	Input Only	—	—	—	65
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3 —	GPIO[76] — — — AN[10]	SIU Lite — — — ADC1	Input Only	—	—	—	67
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3 —	GPIO[77] SCK — — EIRQ[25]	SIU Lite DSPI3 — — SIU Lite	I/O I/O — — I	Slow	Medium	—	117
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3 —	GPIO[78] SOUT — — EIRQ[26]	SIU Lite DSPI3 — — SIU Lite	I/O O — — I	Slow	Medium	—	119
E[15]	PCR[79]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[79] — — — SIN EIRQ[27]	SIU Lite — — — DSPI3 SIU Lite	I/O — — — I I	Slow	Medium	—	121
Port F (16-bit). Fully available on 144-pin package									
F[0]	PCR[80]	ALT0 ALT1 ALT2 ALT3 —	GPIO[80] DBG0 CS3 — EIRQ[28]	SIU Lite FlexRay0 DSPI3 — SIU Lite	I/O O O — I	Slow	Medium	—	133

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
F[1]	PCR[81]	ALT0 ALT1 ALT2 ALT3 —	GPIO[81] DBG1 CS2 — EIRQ[29]	SIU Lite FlexRay0 DSPI3 — SIU Lite	I/O O O — I	Slow	Medium	—	135
F[2]	PCR[82]	ALT0 ALT1 ALT2 ALT3	GPIO[82] DBG2 CS1 —	SIU Lite FlexRay0 DSPI3 —	I/O O O —	Slow	Medium	—	137
F[3]	PCR[83]	ALT0 ALT1 ALT2 ALT3	GPIO[83] DBG3 CS0 —	SIU Lite FlexRay0 DSPI3 —	I/O O I/O —	Slow	Medium	—	139
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	GPIO[84] MDO[3] — —	SIU Lite nexus0 — —	I/O O — —	Slow	Fast	—	4
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	GPIO[85] MDO[2] — —	SIU Lite nexus0 — —	I/O O — —	Slow	Fast	—	5
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] MDO[1] — —	SIU Lite nexus0 — —	I/O O — —	Slow	Fast	—	8
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	GPIO[87] MCKO — —	SIU Lite nexus0 — —	I/O O — —	Slow	Fast	—	19
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	GPIO[88] MSEO1 — —	SIU Lite nexus0 — —	I/O O — —	Slow	Fast	—	20
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	GPIO[89] MSEO0 — —	SIU Lite nexus0 — —	I/O O — —	Slow	Fast	—	23
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	GPIO[90] EVTO — —	SIU Lite nexus0 — —	I/O O — —	Slow	Fast	—	24
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3 —	GPIO[91] — — — EVTI	SIU Lite — — — nexus0	I/O — — — I	Slow	Medium	—	25

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[3] — —	SIU Lite eTimer1 — —	I/O I/O — —	Slow	Medium	—	106
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3 —	GPIO[93] — — — ETC[4]	SIU Lite — — — eTimer1	I/O — — — I	Slow	Medium	—	112
F[14]	PCR[94]	ALT0 ALT1 ALT2 ALT3	GPIO[94] TXD — —	SIU Lite LIN1 — —	I/O O — —	Slow	Medium	—	115
F[15]	PCR[95]	ALT0 ALT1 ALT2 ALT3 —	GPIO[95] — — — RXD	SIU Lite — — — LIN1	I/O — — — I	Slow	Medium	—	113
Port G (12-bit). Fully available on 144-pin package.									
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3 —	GPIO[96] F[0] — — EIRQ[30]	SIU Lite FCU0 — — SIU Lite	I/O O — — I	Slow	Medium	—	38
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIU Lite FCU0 — — SIU Lite	I/O O — — I	Slow	Medium	—	141
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3	GPIO[98] X[2] — —	SIU Lite FlexPWM0 — —	I/O I/O — —	Slow	Medium	—	102
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] A[2] — —	SIU Lite FlexPWM0 — —	I/O O — —	Slow	Medium	—	104
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] B[2] — —	SIU Lite FlexPWM0 — —	I/O O — —	Slow	Medium	—	100
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] X[3] — —	SIU Lite FlexPWM0 — —	I/O I/O — —	Slow	Medium	—	85

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] A[3] — —	SIU Lite FlexPWM0 — —	I/O O — —	Slow	Medium	—	98
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	GPIO[103] B[3] — —	SIU Lite FlexPWM0 — —	I/O O — —	Slow	Medium	—	83
G[8]	PCR[104]	ALT0 ALT1 ALT2 ALT3 —	GPIO[104] — — — FAULT[0]	SIU Lite — — — FlexPWM0	I/O — — — I	Slow	Medium	—	81
G[9]	PCR[105]	ALT0 ALT1 ALT2 ALT3 —	GPIO[105] — — — FAULT[1]	SIU Lite — — — FlexPWM0	I/O — — — I	Slow	Medium	—	79
G[10]	PCR[106]	ALT0 ALT1 ALT2 ALT3 —	GPIO[106] — — — FAULT[2]	SIU Lite — — — FlexPWM0	I/O — — — I	Slow	Medium	—	77
G[11]	PCR[107]	ALT0 ALT1 ALT2 ALT3 —	GPIO[107] — — — FAULT[3]	SIU Lite — — — FlexPWM0	I/O — — — I	Slow	Medium	—	75

1 ALT0 is the primary (default) function for each port after reset.

2 Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIU module. PCR[PA] = 00 → ALT0; PCR[PA] = 01 → ALT1; PCR[PA] = 10 → ALT2; PCR[PA] = 11 → ALT3. This is intended to select the output functions; to use one of the input-only functions, the PCR[IBE] bit must be written to '1', regardless of the values selected in the PCR[PA] bitfields. For this reason, the value corresponding to an input only function is reported as "—".

3 Module included on the MCU.

4 Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMI[PADSEL*x*] bitfields inside the SIUL module.

5 Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.

6 Weak pull down during reset.

3 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5604P MCU.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “P”, “C”, “T” or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the *input* voltage of a voltage regulator.
- “P”, “C”, “T” or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

NOTE

All values are preliminary and subject to change during characterization.

3.1 Absolute maximum ratings

Table 5. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Min	Max[2]	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$[3]	SR	3.3 V / 5.0 V input/output supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_FL}$	SR	3.3 V / 5.0 V code and data flash supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_FL}$	SR	Code and data flash ground with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V / 5.0 V voltage regulator supply voltage with respect to ground (V_{SS_HV})	—	– 0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	– 0.3	$V_{DD\_HV\_IOx}$ + 0.3	

Table 5. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Min	Max[2]	Unit
$V_{DD\_HV\_AD0}$[4]	SR	3.3 V / 5.0 V ADC0 supply and high reference voltage with respect to ground (V_{SS_HV})	$V_{DD\_HV\_REG}$ < 2.7 V	– 0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	– 0.3	6.0	
$V_{SS\_HV\_AD0}$	SR	ADC0 ground and low reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_AD1}$[4]	SR	3.3 V / 5.0 V ADC0 supply and high reference voltage with respect to ground (V_{SS_HV})	$V_{DD\_HV\_REG}$ < 2.7 V	– 0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	– 0.3	6.0	
$V_{SS\_HV\_AD1}$	SR	ADC1 ground and low reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up[5] with respect to ground (V_{SS_HV})	—	0.5 V/µs	3 V/S	—
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$) with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
I_{VDD_LV}	SR	Low voltage static current sink through V_{DD_LV}	—	—	155	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C

1 Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 The difference between each couple of voltage supplies must be less that 300 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| <$ 300 mV.

4 The difference between ADC voltage supplies must be less that 300 mV, $|V_{DD\_HV\_ADC1} - V_{DD\_HV\_ADC0}| < 300$ mV.

5 Guaranteed by device validation

Figure 4 shows the constraints of the different power supplies.

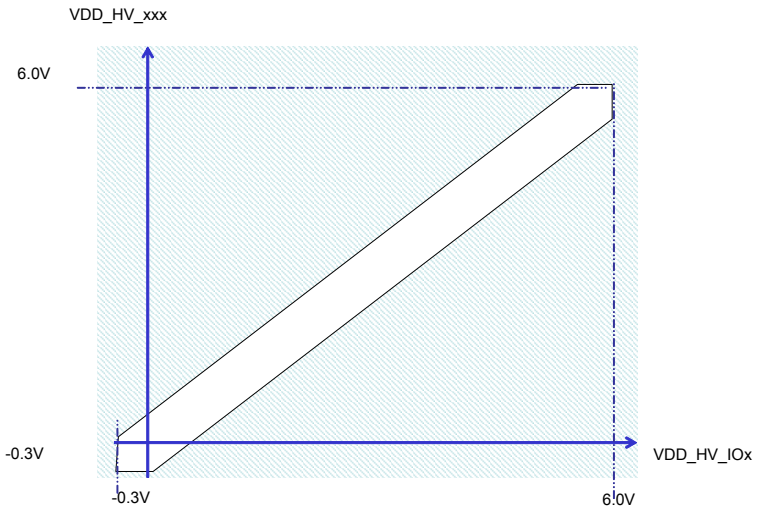


Figure 4. Power supplies constraints

The MPC5604P supply architecture allows of having ADC supply managed independently from standard V_{DD_HV} supply. Figure 5 shows the constraints of the ADC power supply.

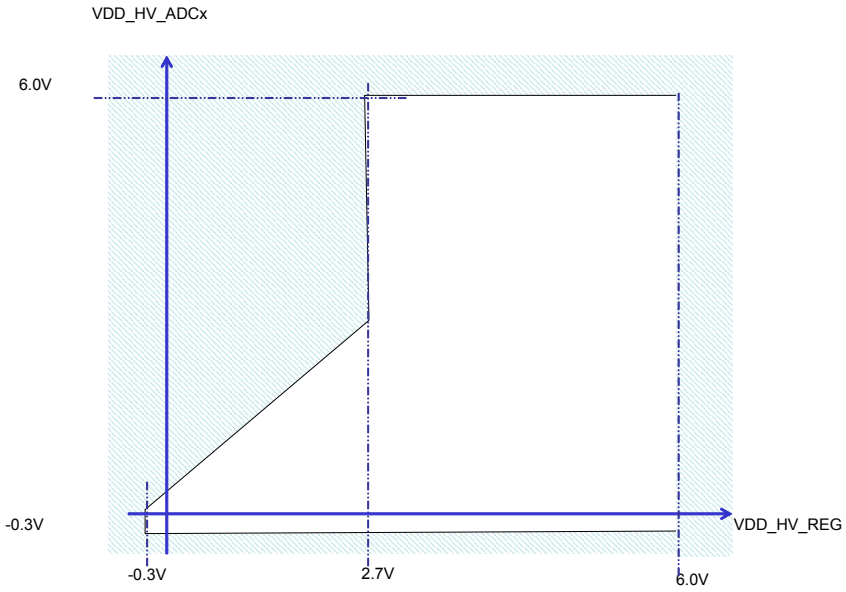


Figure 5. Independent ADC supply

3.2 Recommended operating conditions

Table 6. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$[2]	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	5.0 V code and data flash supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{DD\_HV\_AD0}$[3]	SR	5.0 V ADC0 supply and high reference voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	—	
$V_{SS\_HV\_AD0}$	SR	ADC0 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_AD1}$[3]	SR	5.0 V ADC1 supply and high reference voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	—	
$V_{SS\_HV\_AD1}$	SR	ADC1 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$[4,5]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$[4]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$[4,5]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$[4]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 64 MHz	–40	105	°C
			f_{CPU} = 60 MHz	–40	125	
T_J	SR	Junction temperature under bias	—	–40	150	°C

1 Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 The difference between each couple of voltage supplies must be less that 300 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 100$ mV.

3 The power supply voltage must be identical for ADC0 and ADC1

[4] To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.

[5] The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_RECORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Table 7. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$[2]	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	3.3 V code and data flash supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{DD\_HV\_AD0}$[3]	SR	3.3 V ADC0 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	5.5	
$V_{SS\_HV\_AD0}$	SR	ADC0 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_AD1}$[3]	SR	3.3 V ADC1 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	5.5	
$V_{SS\_HV\_AD1}$	SR	ADC1 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$[4,5]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$[4]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$[4,5]	SR	Internal supply voltage	—	—	—	V

Table 7. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{SS\_LV\_CORx}$[4]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 64 MHz	–40	105	°C
			f_{CPU} = 60 MHz	–40	125	
T_J	SR	Junction temperature under bias	—	–40	150	°C

1 Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 The difference between each couple of voltage supplies must be less that 300 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| <$ 100 mV.

3 The power supply voltage must be identical for ADC0 and ADC1

4 To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.

5 The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_RECORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Figure 6 shows the constraints of the different power supplies:

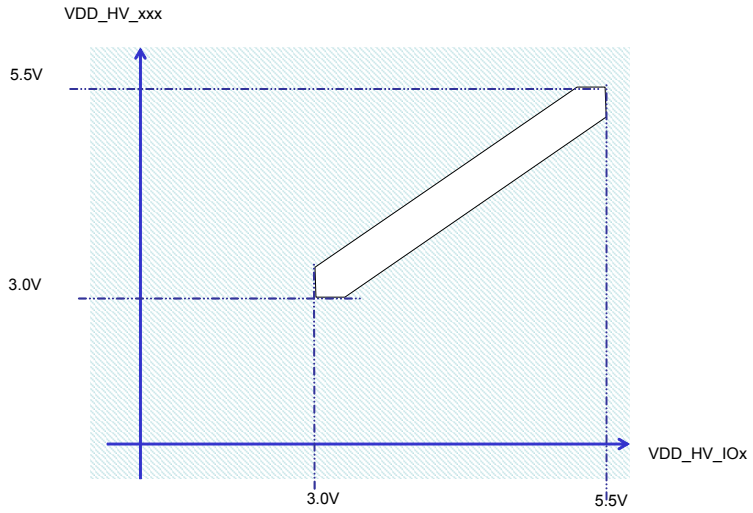


Figure 6. Power supplies constraints

The MPC5604P supply architecture allows of having ADC supply managed independently from standard V_{DD_HV} supply. Figure 7 shows the constraints of the ADC power supply.

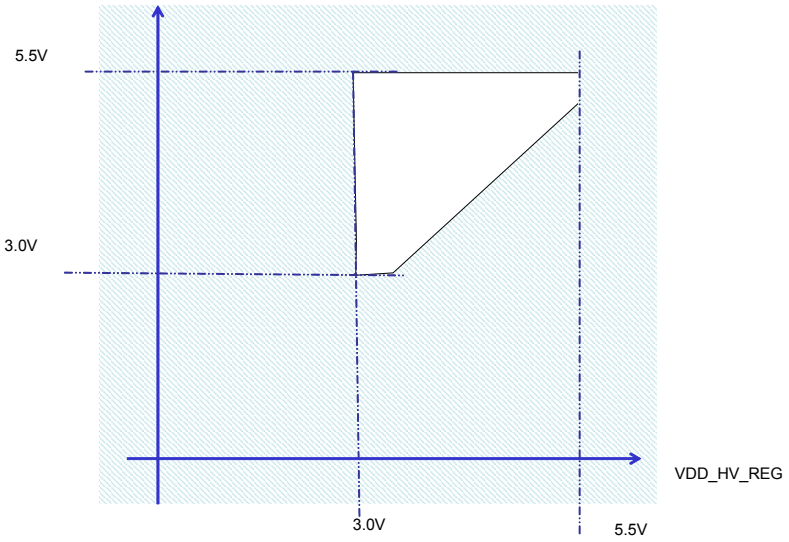


Figure 7. Independent ADC supply

3.3 Thermal characteristics

Table 8. Thermal characteristics for 144-pin LQFP[1]

No.	Symbol	Parameter	Conditions	Typical Value	Unit
1	$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[2]	Single layer board—1s	52	°C/W
2	$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[2]	Four layer board—2s2p	43	°C/W
3	$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], single layer board—1s	43	°C/W
4	$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], four layer board—2s2p	37	°C/W
5	$R_{\theta JB}$	Thermal resistance junction to board[4]	—	31	°C/W
6	$R_{\theta JCtop}$	Thermal resistance junction to case (top)[5]	—	12	°C/W
7	Ψ_{JT}	Junction to package top natural convection[6]	—	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Flow rate of forced air flow.

4 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

5 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 9. Thermal characteristics for 100-pin LQFP[1]

No.	Symbol	Parameter	Conditions	Typical Value	Unit
1	$R_{\theta JA}$	Thermal resistance junction-to-ambient natural convection[2]	Single layer board—1s	56,3	°C/W
2	$R_{\theta JA}$	Thermal resistance junction-to-ambient natural convection[2]	Four layer board—2s2p	43,4	°C/W
3	$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], single layer board—1s	43	°C/W
4	$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], four layer board—2s2p	35	°C/W
5	$R_{\theta JB}$	Thermal resistance junction to board[4]	—	27	°C/W
6	$R_{\theta JCtop}$	Thermal resistance junction to case (Top)[5]	—	14	°C/W
7	Ψ_{JT}	Junction to package top natural convection[6]	—	3	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Flow rate of forced air flow.

4 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

5 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} * P_D) \qquad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$= junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$= junction to case thermal resistance (°C/W)

$R_{\theta CA}$= case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134U.S.A.
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53-58, March 1998.

3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.4 Electromagnetic interference (EMI) characteristics

Table 10. EMI Testing Specifications[1]

Symbol	Parameter	Conditions	f_{OSC}/f_{BUS}	Frequency	Level (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5.5 V; T_A = +25 °C 150 kHz–30 MHz RBW 9 kHz, Step Size 5 kHz 30 MHz–1 GHz RBW 120 kHz, Step Size 80 kHz	16 MHz crystal 40 MHz bus No PLL frequency modulation	150 kHz–50 MHz	20	dBμV
				50–150 MHz	20	
				150–500 MHz	26	
				500–1000 MHz	26	
				IEC Level	K	—
				SAE Level	3	—
			16 MHz crystal 40 MHz bus ±2% PLL frequency modulation	150 kHz–50 MHz	18	dBμV
				50–150 MHz	18	
				15–500 MHz	15	
				500–1000 MHz	15	
				IEC Level	M	—
				SAE Level	2	—

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03.

3.5 Electrostatic discharge (ESD) characteristics

Table 11. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	—	2000	V
$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	—	750 (corners)	V
				500 (other)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

3.6 Power management electrical characteristics

3.6.1 Voltage regulator electrical characteristics

The internal voltage regulator requires an external NPN (BCP56, BCP68, BCX68 or BC817) ballast to be connected as shown in Figure 8 and Figure 9. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

NOTE

The voltage regulator output cannot be used to drive external circuits. Output pins are to be used only for decoupling capacitance.

VDD_LV_COR must be generated using internal regulator and external NPN transistor. It is not possible to provide VDD_LV_COR through external regulator.

For the MPC5604P microcontroller, 10 µF should be placed between each of the three $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ supply pairs and also between the $V_{DD\_LV\_REGCOR}/V_{SS\_LV\_REGCOR}$ pair. Additionally, 40 µF should be placed between the $V_{DD\_HV\_REG}/V_{SS\_HV\_REG}$ pins.

V_{DD} = 3.0 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 to 125 °C, unless otherwise specified.

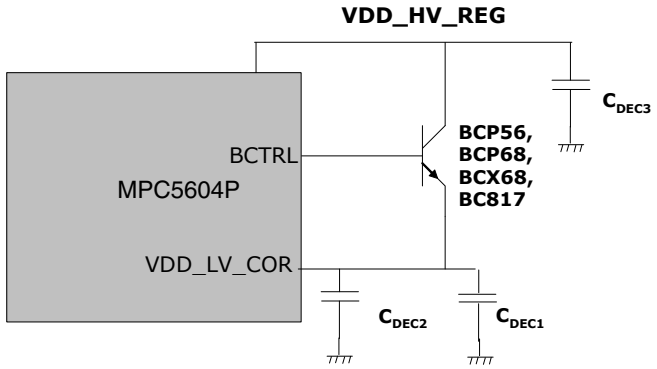


Figure 8. Configuration without resistor on base

Table 12. Voltage regulator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD\_LV\_REGCOR}$	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.145	—	1.4	V
C_{DEC1}	SR	External decoupling/stability ceramic capacitor	4 capacitances	40	56	—	µF
R_{REG}	SR	Resulting ESR of all four C_{DEC1}	absolute maximum value between 100 kHz and 10 MHz	—	—	45	mΩ
C_{DEC2}	SR	External decoupling/stability ceramic capacitor	4 capacitances of 100 nF each	400	—	—	nF
C_{DEC3}	SR	External decoupling/stability ceramic capacitor on VDD_HV_REG	—	40	—	—	µF

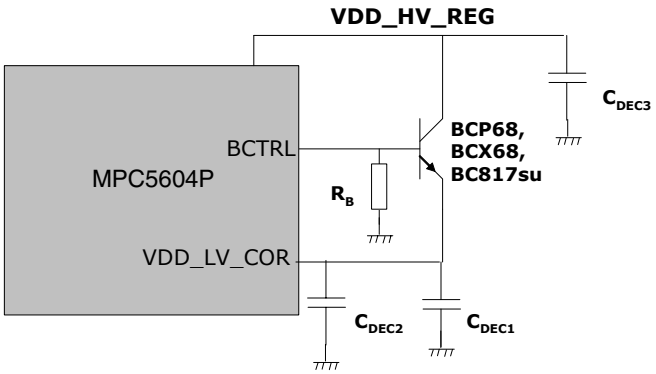


Figure 9. Configuration without resistor on base

Table 13. Voltage regulator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD\_LV\_REGCOR}$	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.145	—	1.4	V
R_B	SR	External Resistance on BJT base	—	18	—	22	kΩ
C_{DEC1}	SR	External decoupling/stability ceramic capacitor	Bipolar BCP68 or BCX68 or BC817. Three capacitances of 10uF	19.5	30	—	µF
			Bipolar BC817. One capacitance of 22uF	14.3	22	—	µF
R_{REG}	SR	Resulting ESR of all four C_{DEC1}	absolute maximum value between 100 kHz and 10 MHz	—	—	45	mΩ
C_{DEC2}	SR	External decoupling/stability ceramic capacitor	4 capacitances of 440 nF each	1760	1200	—	nF
C_{DEC3}	SR	External decoupling/stability ceramic capacitor on VDD_HV_REG	2 capacitances of 10 µF each	2 × 10	—	—	µF

Table 14. Voltage regulator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD\_LV\_REGCOR}$	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.145	—	1.4	V
R_B	SR	External Resistance on BJT base	—	18	—	22	kΩ
C_{DEC1}	SR	External decoupling/stability ceramic capacitor	Bipolar BCP68 or BCX68 or BC817. Three capacitances of 10uF	19.5	30	—	µF
			Bipolar BC817. One capacitance of 22uF	14.3	22	—	µF
R_{REG}	SR	Resulting ESR of all four C_{DEC1}	absolute maximum value between 100 kHz and 10 MHz	—	—	45	mΩ
C_{DEC2}	SR	External decoupling/stability ceramic capacitor	4 capacitances of 440 nF each	1760	1200	—	nF
C_{DEC3}	SR	External decoupling/stability ceramic capacitor on VDD_HV_REG	2 capacitances of 10 µF each	2 × 10	—	—	µF

3.6.2 Voltage monitor electrical characteristics

The device implements a Power On Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state

- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0V ± 10% range
- LVDLVCOR monitors low voltage digital power domain

Table 15. Low voltage monitor electrical characteristics

Symbol		Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25°C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.14	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

[1] V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = –40 to 125°C, unless otherwise specified

3.7 Power up/down sequencing

The MPC5604P implements a precise sequence to ensure each module is started only when all conditions for switching it ON are available. This prevents overstress event or miss-functionality within and outside the device:

- a POWER_ON module working on voltage regulator supply is controlling the correct start-up of the regulator. This is a key module ensuring safe configuration for all Voltage regulator functionality when supply is below 1.5V. Associated POWER_ON (or POR) signal is active low.
- Several Low Voltage Detectors, working on voltage regulator supply are monitoring the voltage of the critical modules (Voltage regulator, I/Os, Flash and Low voltage domain). LVDs are gated low when POWER_ON is active.
- a POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, Flash and RC16 oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated module are set into a safe state.

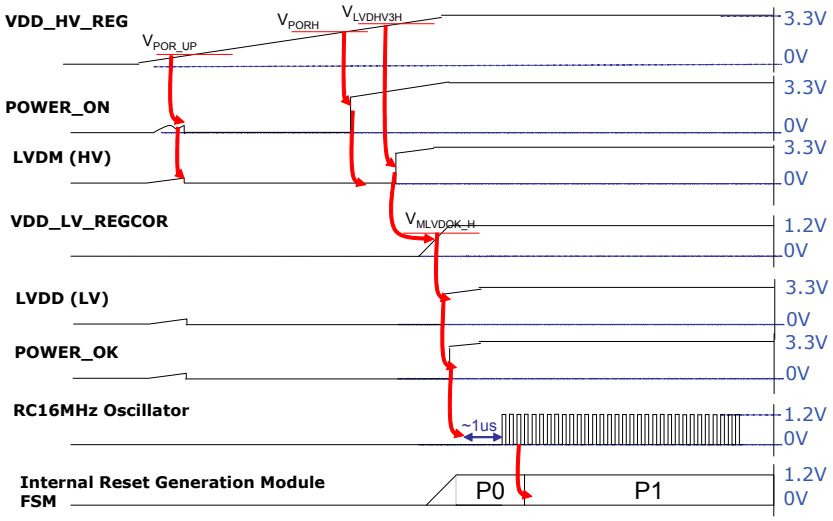


Figure 10. Power-up typical sequence

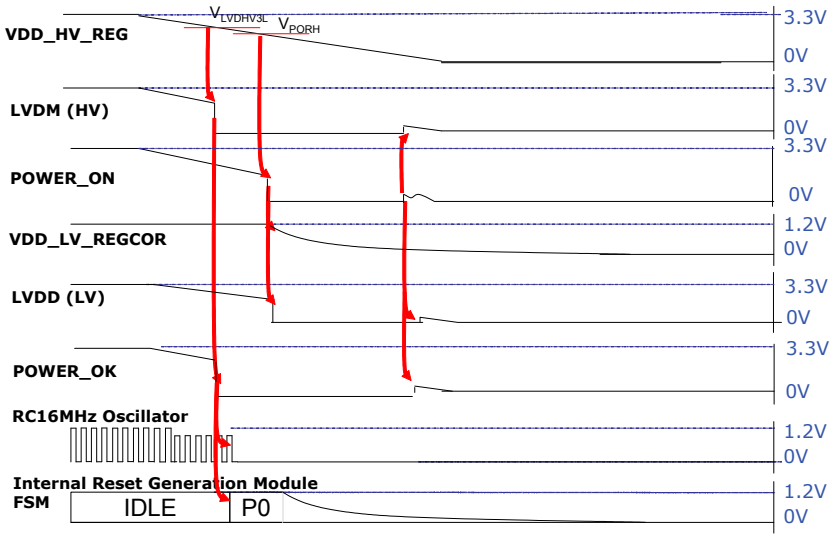


Figure 11. Power-down typical sequence

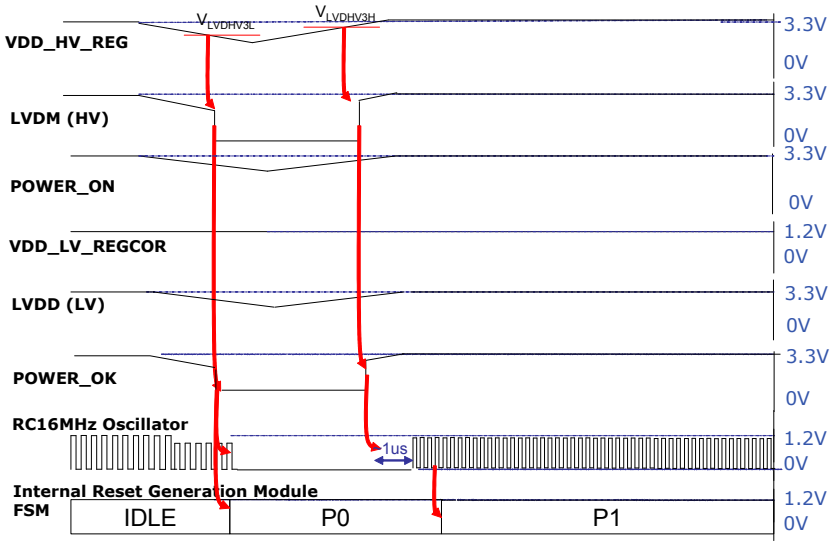


Figure 12. Brown-out typical sequence

3.8 DC electrical characteristics

3.8.1 NVUSRO register

Portions of the MPC5604P device configuration (that is, high voltage supply, oscillator margin, and watchdog enable/disable after reset) are controlled via bit values in the NVUSRO register. NVUSRO[PAD3V5V] controls the device configuration as follows:

Table 16. NVUSRO[PAD3V5V] field description[1]

Value[2]	Description
0	High Voltage supply is 5.0 V
1	High Voltage supply is 3.3 V

1 See the MPC5604P Reference Manual for more information on the NVUSRO register.

2 Default manufacturing value before flash initialization is '1' (3.3 V).

The DC electrical characteristics in the following sections are dependent on the PAD3V5V value as described above.

3.8.2 DC electrical characteristics (5 V)

Table 17 gives the DC electrical characteristics at 5 V ($4.5\ V < V_{DD\_HV\_IOx} < 5.5\ V$, NVUSRO[PAD3V5V]=0) as described in Figure 13.

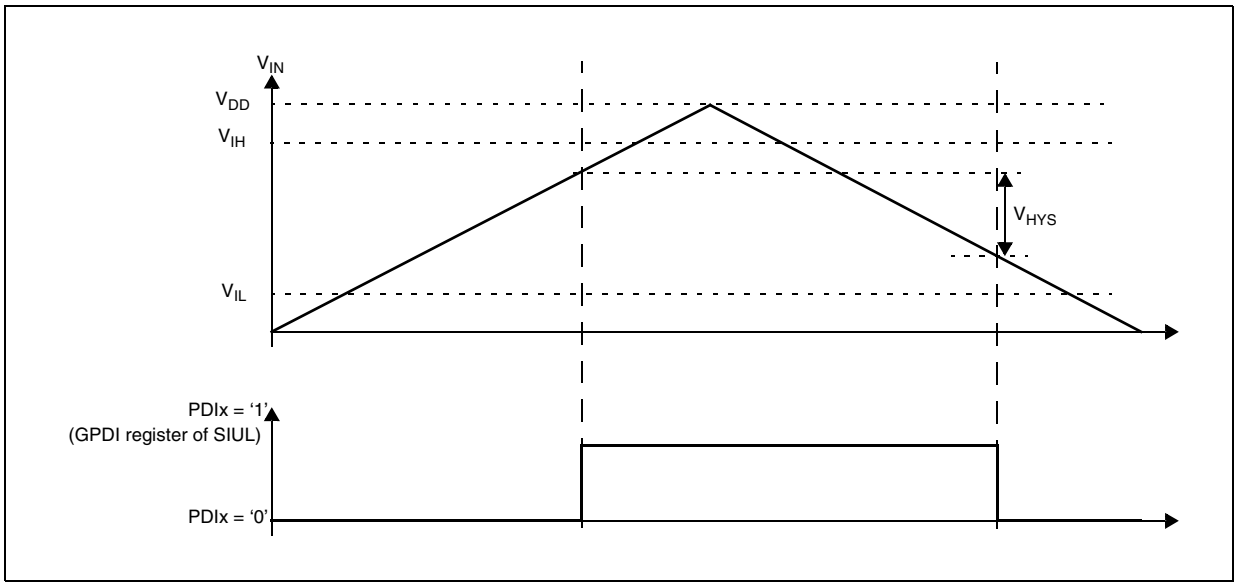


Figure 13. I/O input DC electrical characteristics definition

Table 17. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1[1]	—	V
V_{IL}	P	Maximum level input voltage	—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD\_HV\_IOx}$ + 0.1[1]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8$V_{DD_HV_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
I_{VPP}	P	Input leakage current on V_{PP} leakage pad	—	–5	5	µA
C_{IN}	D	Input capacitance	—	—	10	pF

[1] “SR” parameter values must not exceed the absolute maximum ratings shown in Table 5.

Table 18. Supply current (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter		Conditions		Value[1] Typ	Value[1] Max	Unit
$I_{DD\_LV\_CORE}$	T	Supply current	RUN - Maximum Mode[2]	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	40 MHz	62	77	mA
					64 MHz	71	88	
			RUN - Typical Mode[3]		40 MHz	45	56	
					64 MHz	52	65	
	P		RUN - Maximum Mode[4]	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	64 MHz	60	TBD	
			HALT Mode[5]	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	—	1.5	10	
			STOP Mode[6]	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	—	1	10	
I_{DD_FLASH}	T		FLASH supply current during read	$V_{DD\_HV\_FL}$ at 5.0 V	—	10	12	
			FLASH supply current during erase operation on 1 flash module	$V_{DD\_HV\_FL}$ at 5.0 V	—	15	19	
I_{DD_ADC}	T		ADC supply current - Maximum Mode[2]	$V_{DD\_HV\_AD0}$ at 5.0 V $V_{DD\_HV\_AD1}$ at 5.0 V ADC Freq = 16MHz	ADC1[7]	3.5	5	
					ADC0	3	4	
			ADC supply current - Typical Mode[3]		ADC1[7]	0.8	1	
					ADC0	0.005	0.006	
I_{DD_OSC}	T		OSC supply current	V_{DD_OSC} at 5.0 V	8 MHz	2.6	3.2	

1 All values to be confirmed after characterization/data collection.

2 Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled, 125 °C ambient. I/O supply current excluded.

3 Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only, 105 °C ambient. I/O supply current excluded.

4 Code fetched from Ram, PLL0: 64 MHz system clock (x4 multiplier with 16MHz XTAL), PLL1 is ON @ PHI_div2 = 120 Mhz and PHI_div3 = 80 Mhz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripheral enabled.

5 Halt mode configurations: Code fetched from RAM, C & D FLASH in low power mode, OSC/PLL0/PLL1 are OFF, Core clock frozen, all peripherals are disabled.

6 STOP "P" mode DUT configuration: Code fetched from RAM, C & D FLASH off, OSC/PLL0/PLL1 are OFF, Core clock frozen, all peripherals are disabled.

7 Includes Temperature Sensor current consumption.

3.8.3 DC Electrical characteristics (3.3 V)

Table 19 gives the DC electrical characteristics at 3.3 V ($3.0\ V < V_{DD\_HV\_IOx} < 3.6\ V$, NVUSRO[PAD3V5V]=1) as described in Figure 14.

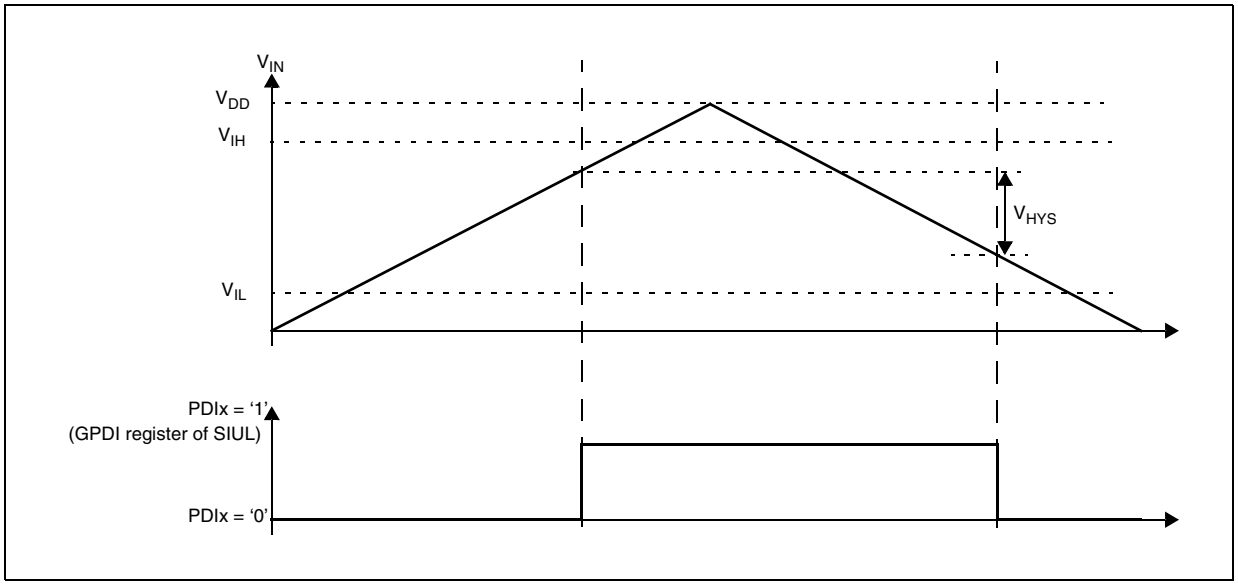


Figure 14. I/O input DC electrical characteristics definition

Table 19. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)[1]

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1[2]	—	V
V_{IL}	P	Maximum low level input voltage	—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD\_HV\_IOx}$ + 0.1[2]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

Table 19. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)[1] (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
I_{VPP}	P	Input leakage current on V_{PP} leakage pad	—	–5	5	µA
C_{IN}	D	Input capacitance	—	—	—	pF

1 These specifications are design targets and subject to change per device characterization.

2 "SR" parameter values must not exceed the absolute maximum ratings shown in Table 5.

Table 20. Supply current (3.3 V, NVUSRO[PAD3V5V]=1)

Symbol		Parameter		Conditions		Value[1]		Unit
						Typ	Max	
$I_{DD\_LV\_CORE}$	T	Supply current	RUN - Maximum Mode[2]	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	40 MHz	62	77	mA
					64 MHz	71	89	
			RUN - Typical Mode[3]		40 MHz	45	56	
					64 MHz	53	66	
	P		RUN - Maximum Mode[4]	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	64 MHz	60	TBD	
			HALT Mode[5]	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	—	1.5	10	
			STOP Mode[6]	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	—	1	10	
I_{DD_FLASH}	T		FLASH supply current during read on single mode	$V_{DD\_HV\_FL}$ at 3.3 V	—	8	10	
			FLASH supply current during erase operation on single mode	$V_{DD\_HV\_FL}$ at 3.3 V	—	10	12	
I_{DD_ADC}	T		ADC supply current - Maximum Mode[2]	$V_{DD\_HV\_AD0}$ at 3.3 V $V_{DD\_HV\_AD1}$ at 3.3 V ADC Freq = 16MHz	ADC1[7]	2.5	4	
					ADC0	2	4	
			ADC supply current - Typical Mode[3]		ADC1[7]	0.8	1	
					ADC0	0.005	0.006	
I_{DD_OSC}	T		OSC supply current	V_{DD_OSC} at 3.3 V	8 MHz	2.4	3	

1 All values to be confirmed after characterization/data collection.

2 Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled, 125 °C ambient. I/O supply current excluded.

[3] Typical mode: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only, 105 °C ambient. I/O supply current excluded.

[4] Code fetched from Ram, PLL0: 64 MHz system clock (x4 multiplier with 16MHz XTAL), PLL1 is ON @ PHI_div2 = 120 Mhz and PHI_div3 = 80 Mhz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripheral enabled.

[5] Halt mode configurations: Code fetched from RAM, C & D FLASH in low power mode, OSC/PLL0/PLL1 are OFF, Core clock frozen, all peripherals are disabled.

[6] STOP "P" mode DUT configuration: Code fetched from RAM, C & D FLASH off, OSC/PLL0/PLL1 are OFF, Core clock frozen, all peripherals are disabled.

[7] Includes Temperature Sensor current consumption.

3.8.4 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 21.

Table 21. I/O supply segment

Package	Supply segment						
	1	2	3	4	5	6	7
144 LQFP	pin8 – pin20	pin23 – pin38	pin39 – pin55	pin58 – pin68	pin73 – pin89	pin92 – pin125	pin128 – pin5
100 LQFP	pin15 – pin26	pin27 – pin38	pin41 – pin46	pin51 – pin61	pin64 – pin86	pin89 – pin10	—

Table 22 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below the 100%.

Table 22. I/O weight

PAD	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
NMI	1%	1%	1%	1%
PAD[6]	6%	5%	14%	13%
PAD[49]	5%	4%	14%	12%
PAD[84]	14%	10%	—	—
PAD[85]	9%	7%	—	—
PAD[86]	9%	6%	—	—
MODO0	12%	8%	—	—
PAD[7]	4%	4%	11%	10%
PAD[36]	5%	4%	11%	9%
PAD[8]	5%	4%	10%	9%
PAD[37]	5%	4%	10%	9%
PAD[5]	5%	4%	9%	8%
PAD[39]	5%	4%	9%	8%
PAD[35]	5%	4%	8%	7%
PAD[87]	12%	9%	—	—

Table 22. I/O weight

PAD	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[88]	9%	6%	—	—
PAD[89]	10%	7%	—	—
PAD[90]	15%	11%	—	—
PAD[91]	6%	5%	—	—
PAD[57]	8%	7%	8%	7%
PAD[56]	13%	11%	13%	11%
PAD[53]	14%	12%	14%	12%
PAD[54]	15%	13%	15%	13%
PAD[55]	25%	22%	25%	22%
PAD[96]	27%	24%	—	—
PAD[65]	1%	1%	1%	1%
PAD[67]	1%	1%	—	—
PAD[33]	1%	1%	1%	1%
PAD[68]	1%	1%	—	—
PAD[23]	1%	1%	1%	1%
PAD[69]	1%	1%	—	—
PAD[34]	1%	1%	1%	1%
PAD[70]	1%	1%	—	—
PAD[24]	1%	1%	1%	1%
PAD[71]	1%	1%	—	—
PAD[66]	1%	1%	1%	1%
PAD[25]	1%	1%	1%	1%
PAD[26]	1%	1%	1%	1%
PAD[27]	1%	1%	1%	1%
PAD[28]	1%	1%	1%	1%
PAD[63]	1%	1%	1%	1%
PAD[72]	1%	1%	—	—
PAD[29]	1%	1%	1%	1%
PAD[73]	1%	1%	—	—
PAD[31]	1%	1%	1%	1%
PAD[74]	1%	1%	—	—
PAD[30]	1%	1%	1%	1%
PAD[75]	1%	1%	—	—

Table 22. I/O weight

PAD	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[32]	1%	1%	1%	1%
PAD[76]	1%	1%	—	—
PAD[64]	1%	1%	1%	1%
PAD[0]	23%	20%	23%	20%
PAD[1]	21%	18%	21%	18%
PAD[107]	20%	17%	—	—
PAD[58]	19%	16%	19%	16%
PAD[106]	18%	16%	—	—
PAD[59]	17%	15%	17%	15%
PAD[105]	16%	14%	—	—
PAD[43]	15%	13%	15%	13%
PAD[104]	14%	13%	—	—
PAD[44]	13%	12%	13%	12%
PAD[103]	12%	11%	—	—
PAD[2]	11%	10%	11%	10%
PAD[101]	11%	9%	—	—
PAD[21]	10%	8%	10%	8%
TMS	1%	1%	1%	1%
TCK	1%	1%	1%	1%
PAD[20]	16%	11%	16%	11%
PAD[3]	4%	3%	4%	3%
PAD[61]	9%	8%	9%	8%
PAD[102]	11%	10%	—	—
PAD[60]	11%	10%	11%	10%
PAD[100]	12%	10%	—	—
PAD[45]	12%	10%	12%	10%
PAD[98]	12%	11%	—	—
PAD[46]	12%	11%	12%	11%
PAD[99]	13%	11%	—	—
PAD[62]	13%	11%	13%	11%
PAD[92]	13%	12%	—	—
VPP_TEST	1%	1%	1%	1%
PAD[4]	14%	12%	14%	12%

Table 22. I/O weight

PAD	144 LQFP		100 LQFP	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[16]	13%	12%	13%	12%
PAD[17]	13%	11%	13%	11%
PAD[42]	13%	11%	13%	11%
PAD[93]	12%	11%	—	—
PAD[95]	12%	11%	—	—
PAD[18]	12%	10%	12%	10%
PAD[94]	11%	10%	—	—
PAD[19]	11%	10%	11%	10%
PAD[77]	10%	9%	—	—
PAD[10]	10%	9%	10%	9%
PAD[78]	9%	8%	—	—
PAD[11]	9%	8%	9%	8%
PAD[79]	8%	7%	—	—
PAD[12]	7%	7%	7%	7%
PAD[41]	7%	6%	7%	6%
PAD[47]	5%	4%	5%	4%
PAD[48]	4%	4%	4%	4%
PAD[51]	4%	4%	4%	4%
PAD[52]	5%	4%	5%	4%
PAD[40]	5%	5%	6%	5%
PAD[80]	9%	8%	—	—
PAD[9]	10%	9%	11%	10%
PAD[81]	10%	9%	—	—
PAD[13]	10%	9%	12%	11%
PAD[82]	10%	9%	—	—
PAD[22]	10%	9%	13%	12%
PAD[83]	10%	9%	—	—
PAD[50]	10%	9%	14%	12%
PAD[97]	10%	9%	—	—
PAD[38]	10%	9%	14%	13%
PAD[14]	9%	8%	14%	13%
PAD[15]	9%	8%	15%	13%

3.9 Temperature sensor electrical characteristics

Table 23. Temperature sensor electrical characteristics

Symbol		Parameter	Conditions	Min	Max	Unit
—	P	Accuracy	T_J = –40 °C to T_A = 25 °C	TBD	TBD	°C
			T_J = T_A to 125 °C	TBD	TBD	°C
T_S	D	Minimum sampling period		1.5	—	µs

3.10 Main oscillator electrical characteristics

The MPC5604P provides an oscillator/resonator driver.

Table 24. Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	6.5	25	mA/V
V_{OSC}	T	Oscillation amplitude on EXTAL pin	1	—	V
t_{OSCSU}	T	Start-up time[1,2]	8	—	ms

1 The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.

2 Value captured when amplitude reaches 90% of EXTAL

Table 25. Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	4	20	mA/V
V_{OSC}	T	Oscillation amplitude on EXTAL pin	1	—	V
t_{OSCSU}	T	Start-up time[1,2]	8	—	ms

1 The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.

2 Value captured when amplitude reaches 90% of EXTAL

Table 26. Input clock characteristics

Symbol		Parameter	Min	Typ	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	64	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.11 FMPLL electrical characteristics

Table 27. PLLMRFM electrical specifications[1]
(V_{DDPLL} = 3.0 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		Parameter		Conditions	Value		Unit
					min	max	
$f_{ref\_crystal}$ f_{ref_ext}	D	PLL reference frequency range[2]		Crystal reference	4	40	MHz
f_{pll_in}	D	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode		—	4	120	MHz
f_{FREE}	P	Free running frequency		Measured using clock division — typically /16	20	150	MHz
f_{sys}	D	On-chip PLL frequency[2]		—	16	120	MHz
t_{CYC}	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window[3]		Lower limit	1.6	3.7	MHz
				Upper limit	24	56	
f_{SCM}	D	Self-clocked mode frequency[4,5]		—	20	150	MHz
C_{JITTER}	T	CLKOUT period jitter[6,7,8,9]	Short-term jitter[10]	f_{SYS} maximum	-4	4	% f_{CLKOUT}
			Long-term jitter (avg. over 2 ms interval)	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz, 4000 cycles	—	10	ns
t_{lpll}	D	PLL lock time [11, 12]		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	-6	6	% f_{sys}
f_{UL}	D	Frequency un-LOCK range		—	-18	18	% f_{sys}
f_{CS} f_{DS}	D	Modulation Depth		Center spread	±0.25	±4.0[13]	%f_{sys}
				Down Spread	-0.5	-8.0	
f_{MOD}	D	Modulation frequency[14]		—	—	70	kHz

1 All values given are initial design targets and subject to change.

2 Considering operation with PLL not bypassed.

3 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.

4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

[5] f_{VCO} self clock range is 20-150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

[6] This value is determined by the crystal manufacturer and board design.

[7] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

[8] Proper PC board layout procedures must be followed to achieve specifications.

[9] Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

[10] Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.

[11] This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.

[12] This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

[13] This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).

[14] Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50kHz.

3.12 16 MHz RC oscillator electrical characteristics

Table 28. 16 MHz RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	-5	—	5	%
$\Delta_{RCMTRIM}$	P	Post Trim Accuracy: The variation of the PTF[1] from the 16 MHz	T_A = 25 °C	-1	—	1	%
$\Delta_{RCMSTEP}$	P	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

[1] PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.13 Analog-to-digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

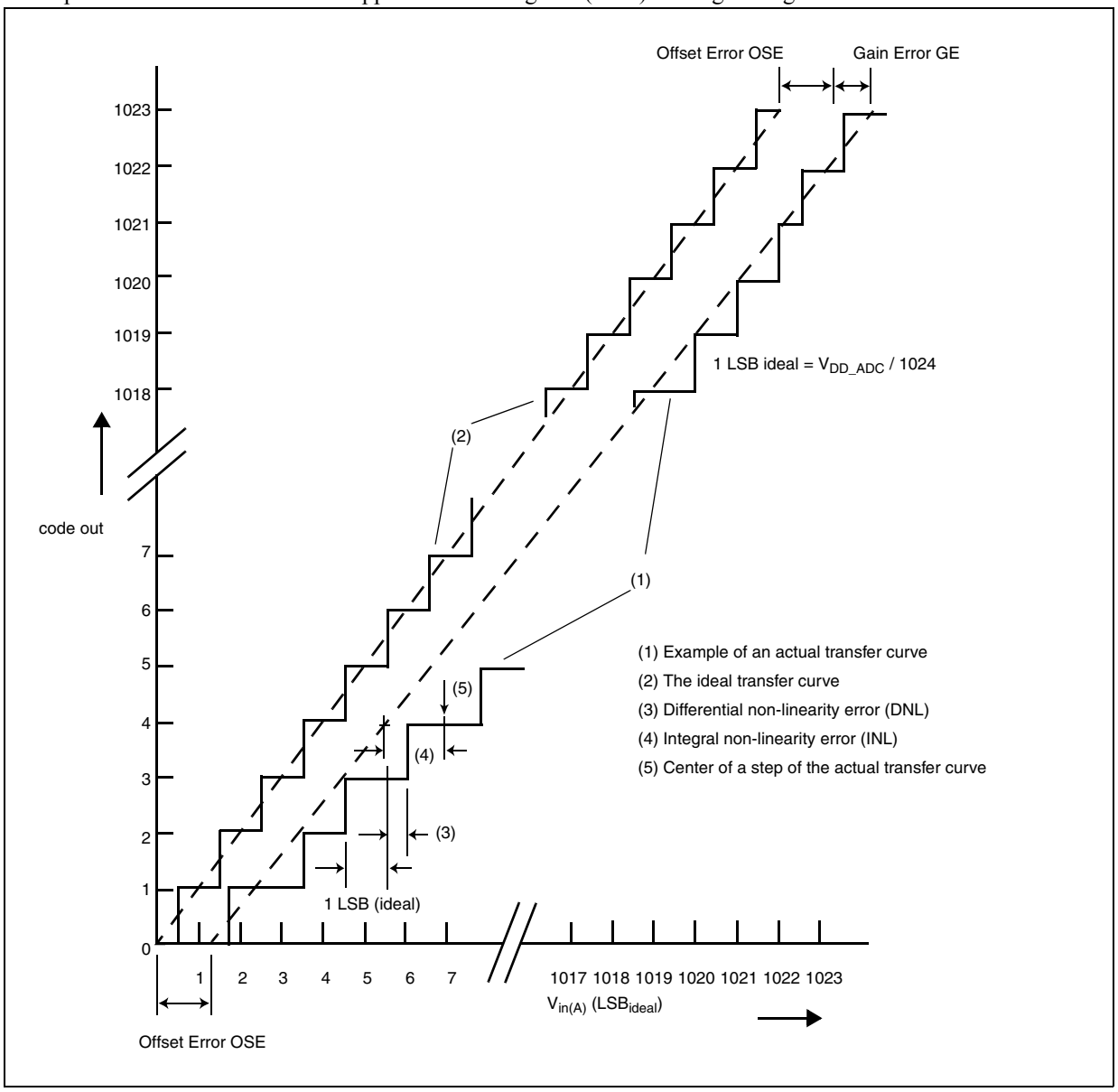


Figure 15. ADC characteristics and error definitions

3.13.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to

be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (fc \times C_S)$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

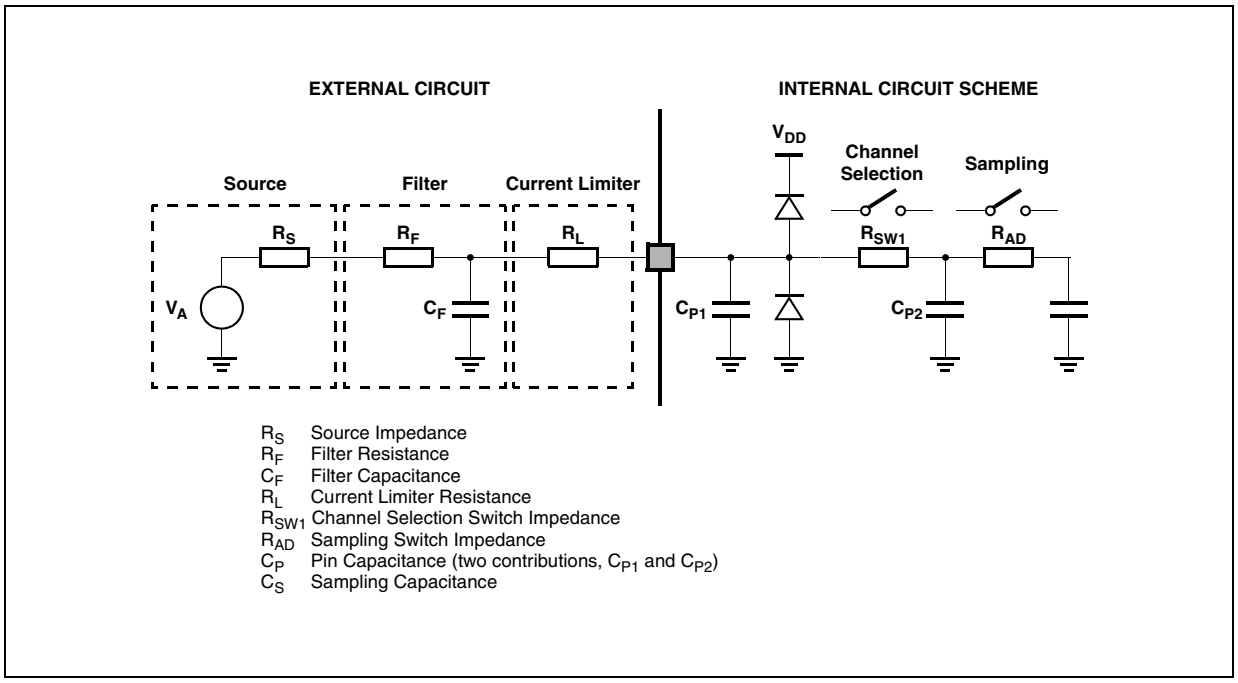


Figure 16. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 16): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

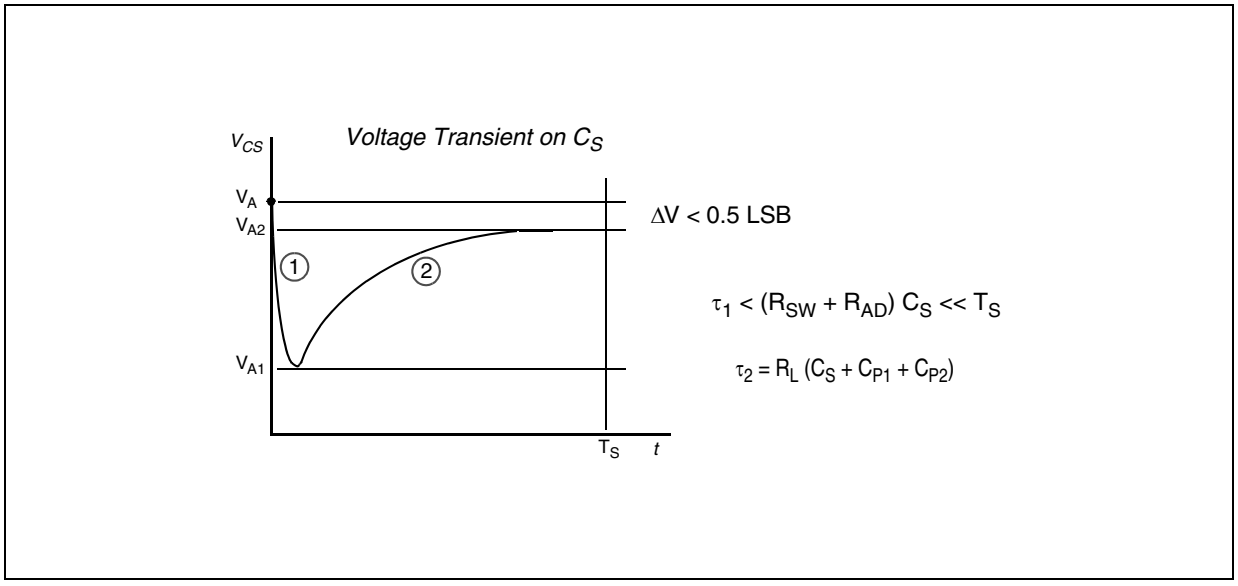


Figure 17. Transient Behavior during Sampling Phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

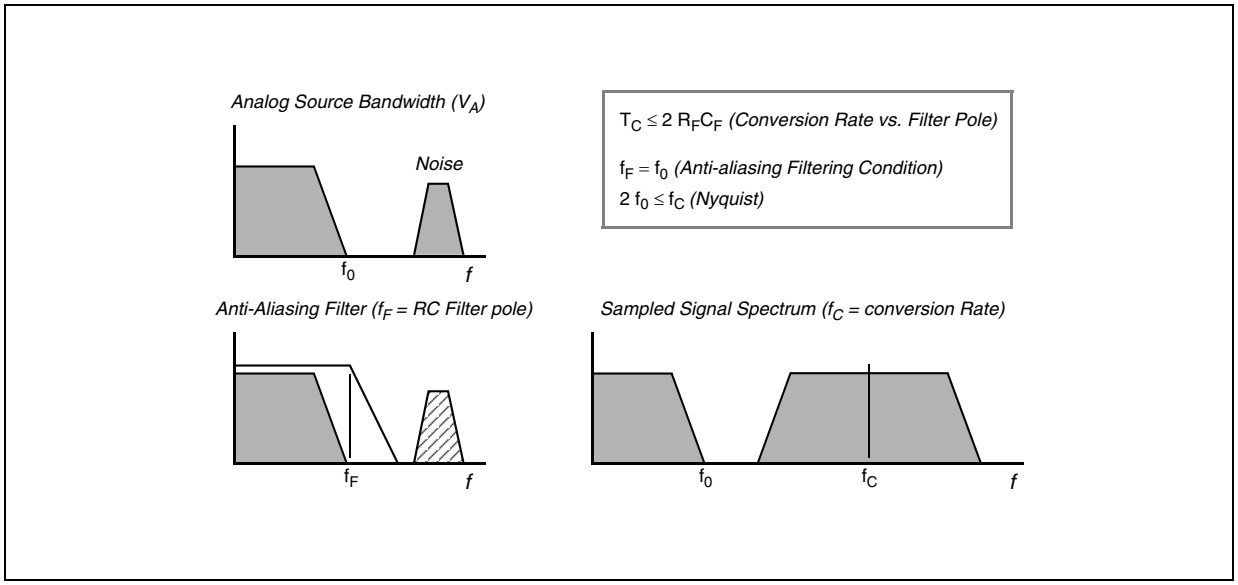


Figure 18. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

3.13.2 ADC conversion characteristics

Table 29. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk[2] frequency)	—	3[3]	—	60	MHz
f_s	SR	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	D	Sample time[4]	f_{ADC} = 20 MHz, INPSAMP = 3	125			ns
			f_{ADC} = 9 MHz, INPSAMP = 255			28.2	µs
t_{ADC_C}	P	Conversion time[5]	f_{ADC} = 20 MHz[6], INPCMP = 1	0.650	—	—	µs
C_S[7]	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[7]	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}[7]	D	ADC input pin capacitance 2	—	—	—	1	pF
R_{SW1}[7]	D	Internal resistance of analog source	$V_{DD\_HV\_ADC}$ = 5 V+/-10%	—	—	0.6	kΩ
			$V_{DD\_HV\_ADC}$ = 3.3 V+/-10%	—	—	3	kΩ
R_{AD}[7]	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	-5	—	5	mA
INL	P	Integral Non Linearity	No overload	–1.5	—	1.5	LSB
DNL	P	Differential Non Linearity	No overload	–1.0	—	1.0	LSB
OFS	T	Offset error	—	—	±1	—	LSB
GNE	T	Gain error	—	—	±1	—	LSB
TUE	P	Total unadjusted error without current injection	—	-2.5	—	2.5	LSB
TUE	T	Total unadjusted error with current injection	—	-3	—	3	LSB

1 V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 to +125 °C, unless otherwise specified and analog input voltage from $V_{SS\_HV\_ADCx}$ to $V_{DD\_HV\_ADCx}$.

2 AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.

4 During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

[5] This parameter includes the sample time t_{ADC_S}.

[6] 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.

[7] See Figure 16.

3.14 Flash memory electrical characteristics

Table 30. Program and erase specifications

Symbol		Parameter	Min Value	Typical Value[1]	Initial Max[2]	Max[3]	Unit
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	—	22	50	500	µs
T_{BKPRG}	P	Bank Program (512KB)[4, 5]	—	1.45	1.65	33	s
	P	Bank Program (64KB)[4, 5]	—	0.18	0.21	4.10	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

[1] Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

[2] Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

[3] The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

[4] Actual hardware programming times. This does not include software overhead.

[5] Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

Table 31. Flash module life[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range (T_J)	—	10,000	100,000 (TBC)	cycles
P/E	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000 (TBC)	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[2]	Blocks with 0 – 1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	5	—	years

[1] TBD: To be defined

[2] Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 32. Flash read access timing

Symbol	C	Parameter	Conditions[1]	Max	Unit
Fmax	C	Maximum working frequency at given number of WS in worst conditions	2 wait states	66	MHz
			0 wait states	18	

[1] VDD = 3.3 V ± 10% / 5.0 V ± 10%, TA = -40 to 125 °C, unless otherwise specified

3.15 AC Specifications

3.15.1 Pad AC Specifications

Table 33. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[3] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
T_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
T_{tr}	CC	D	Output transition time output pin[3] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	
T_{sim}	CC	T	Symmetric, same drive strength between N and P transistor	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	4	ns
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	5	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

[2] All values need to be confirmed during device validation.

[3] C_L includes device and package capacitances (C_{PKG} < 5 pF).

3.16 AC Timing Characteristics

3.16.1 $\overline{\text{RESET}}$ Pin Characteristics

The MPC5604P implements a dedicated bidirectional RESET pin.

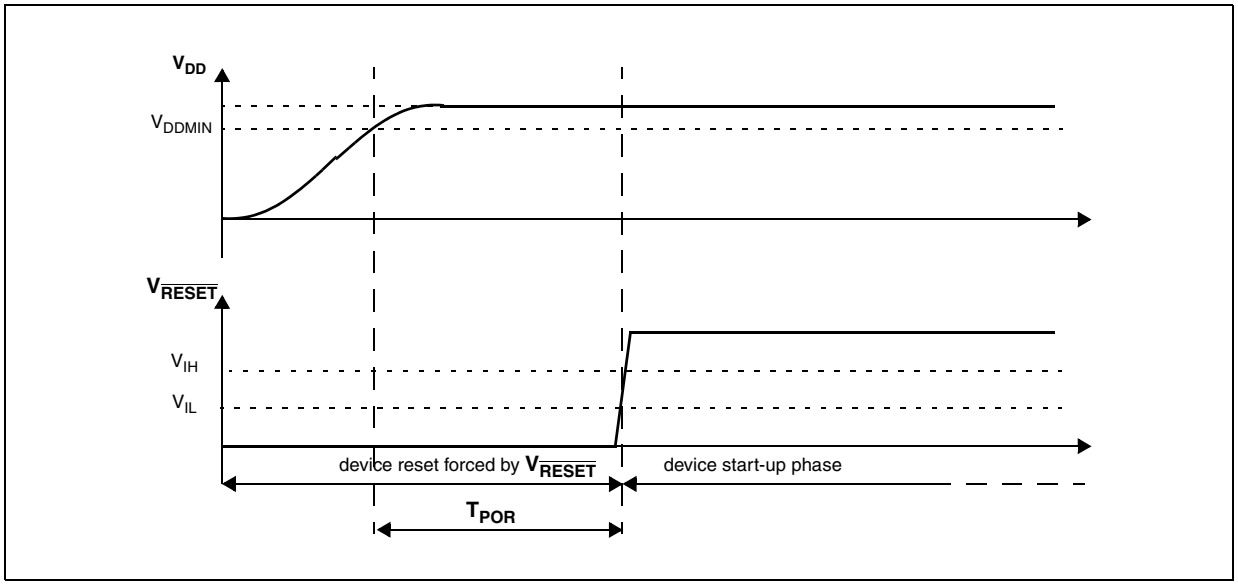


Figure 19. Start-up reset requirements

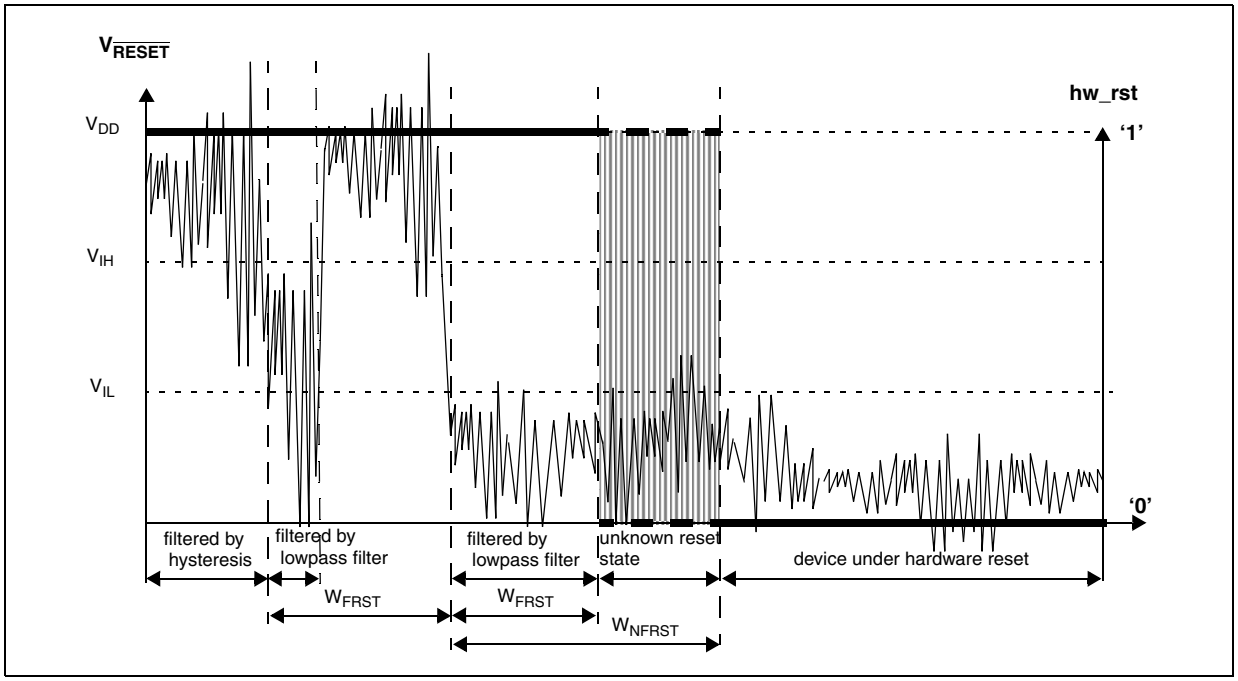


Figure 20. Noise filtering on reset signal

Table 34. $\overline{\text{RESET}}$ electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

Table 34. $\overline{\text{RESET}}$ electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
T_{POR}	CC	D	maximum delay before internal reset is released after all VDD_HV reach nominal supply	monotonic VDD_HV supply ramp	—	—	1	ms
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[5]	10	—	250	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).

4 C_L includes device and package capacitance (C_{PKG} < 5 pF).

5 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.16.2 IEEE 1149.1 interface timing

Table 35. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}$/2)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% - 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns

Table 35. JTAG pin AC electrical characteristics (continued)

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

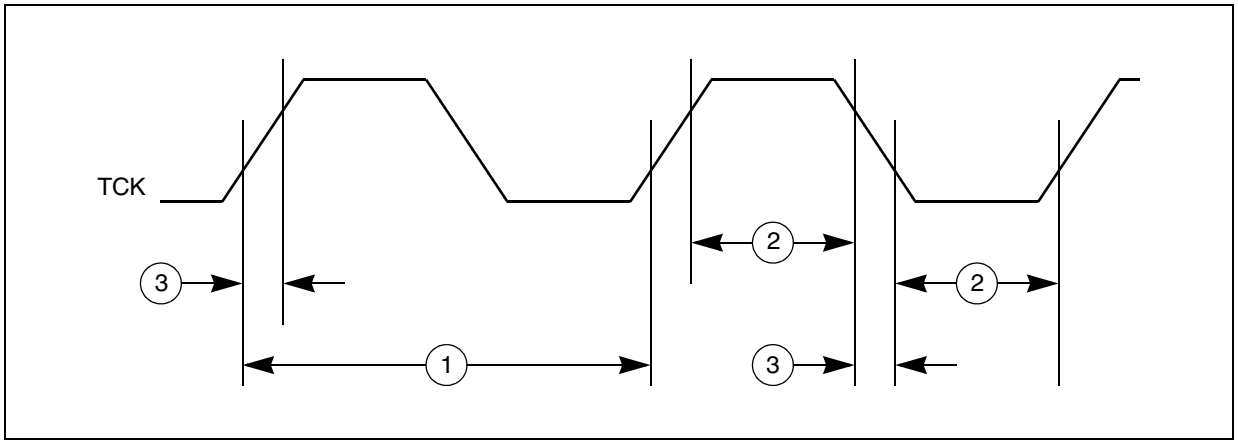


Figure 21. JTAG test clock input timing

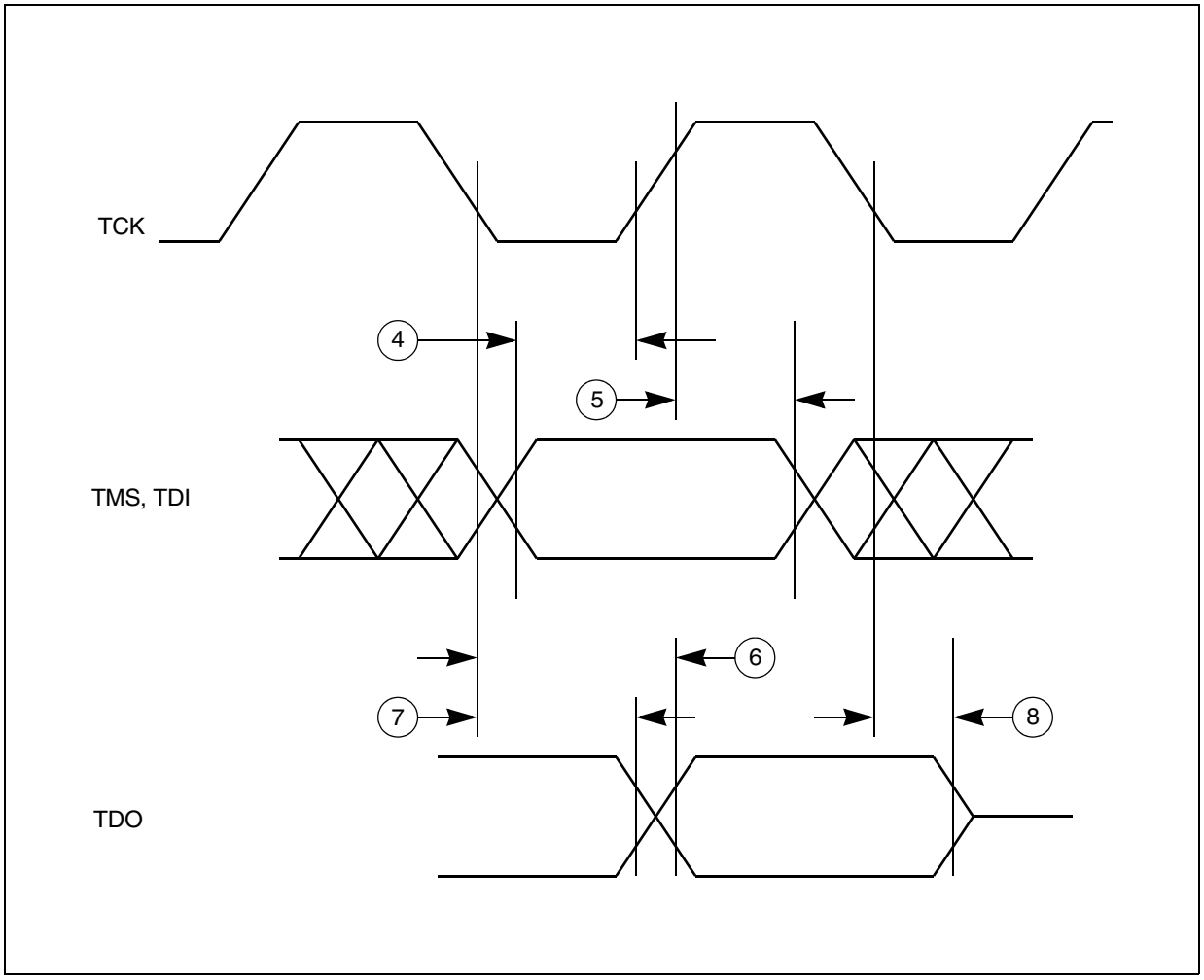


Figure 22. JTAG test access port timing

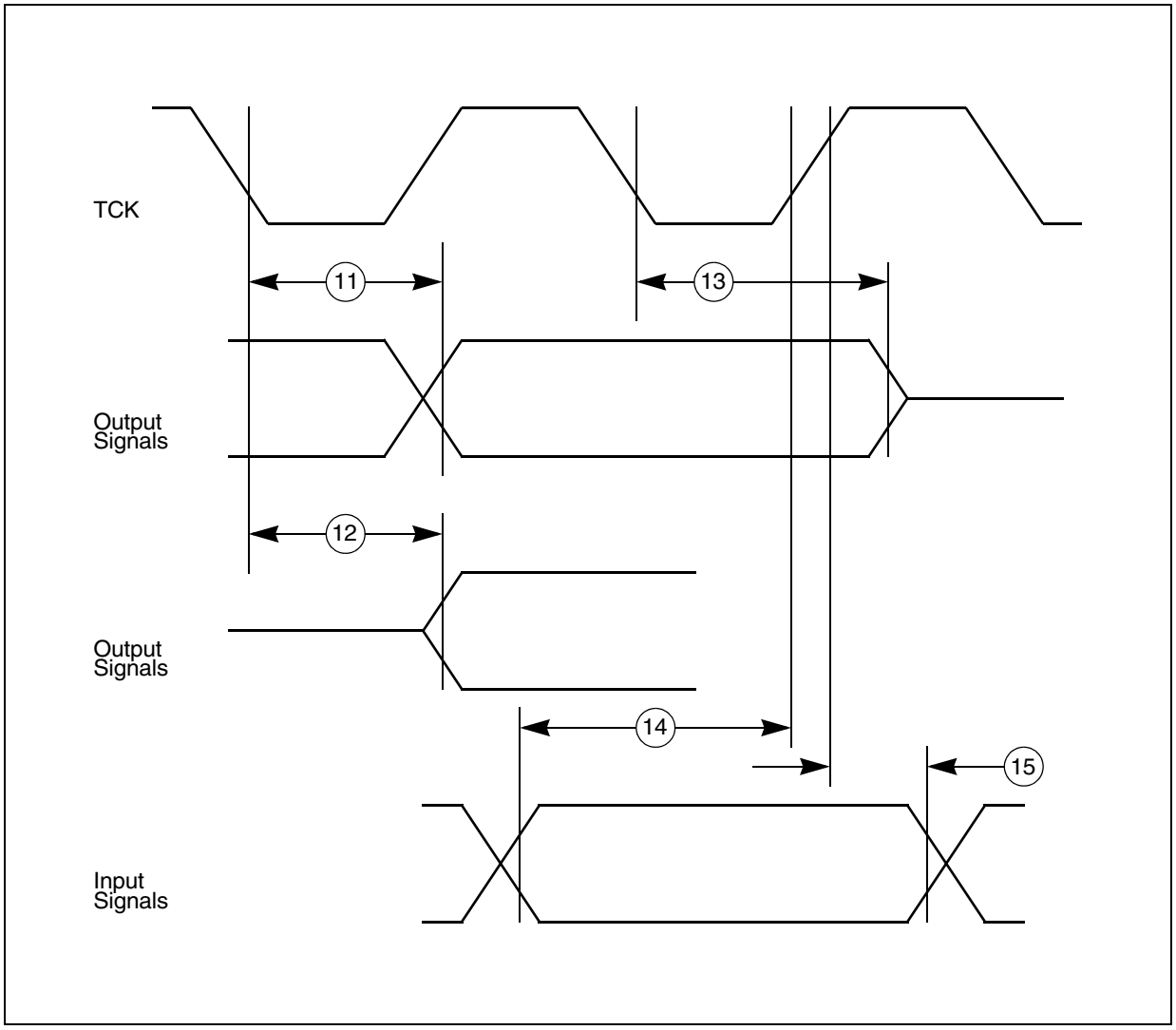


Figure 23. JTAG boundary scan timing

3.16.3 Nexus timing

Table 36. Nexus debug port timing[1]

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
2	t_{MDOV}	CC	D	MCKO low to MDO data valid[2]	—	—	6	ns
3	t_{MSEOV}	CC	D	MCKO low to $\overline{\text{MSEO}}$ data valid[2]	—	—	6	ns
4	t_{EVTOV}	CC	D	MCKO low to $\overline{\text{EVTO}}$ data valid[2]	—	—	6	ns
5	t_{TCYC}	CC	D	TCK cycle time	64[3]	—	—	ns

Table 36. Nexus debug port timing[1] (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t_{NTDIS}	CC	D	TDI data setup time	6	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	6	—	—	ns
7	t_{NTDIH}	CC	D	TDI data hold time	10	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	10	—	—	ns
8	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	35	ns
9	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

3 Lower frequency is required to be fully compliant to standard.

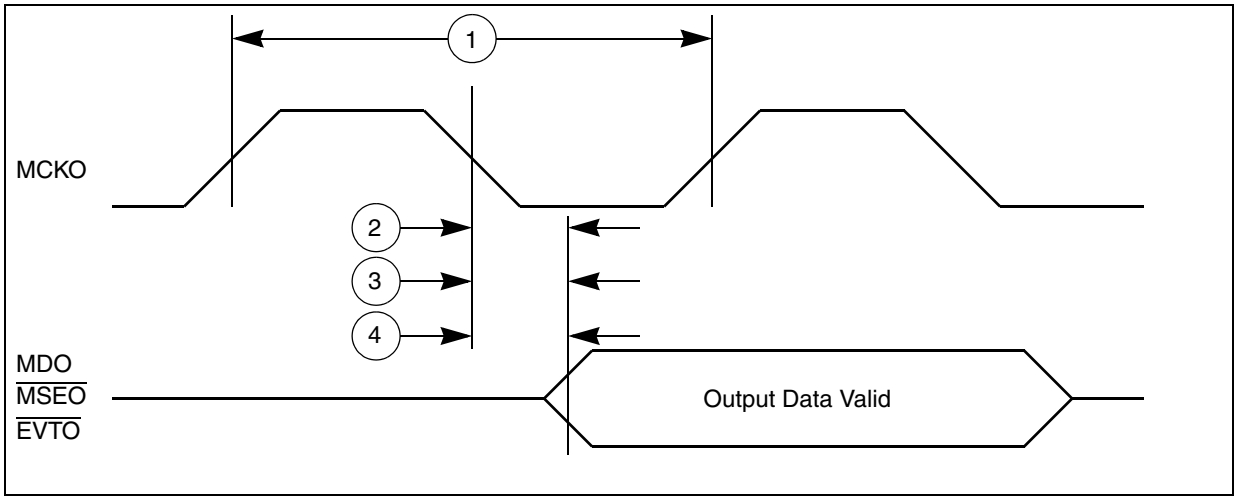


Figure 24. Nexus output timing

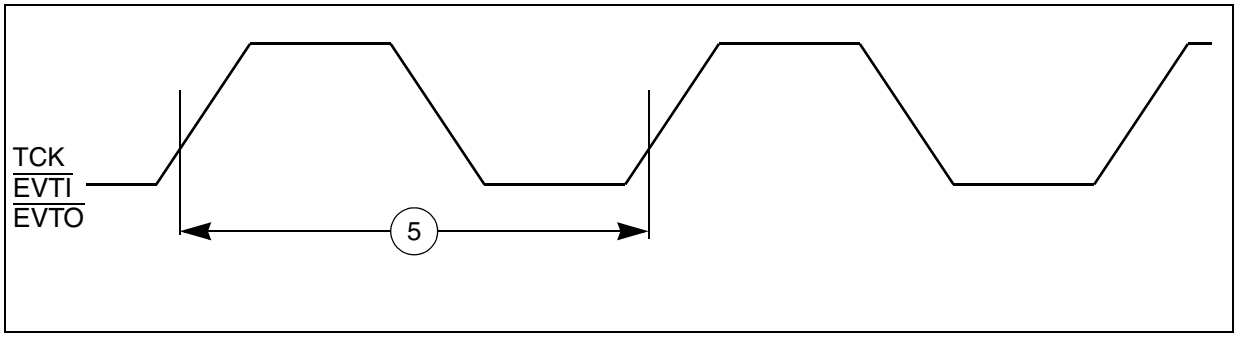


Figure 25. Nexus event trigger and test clock timings

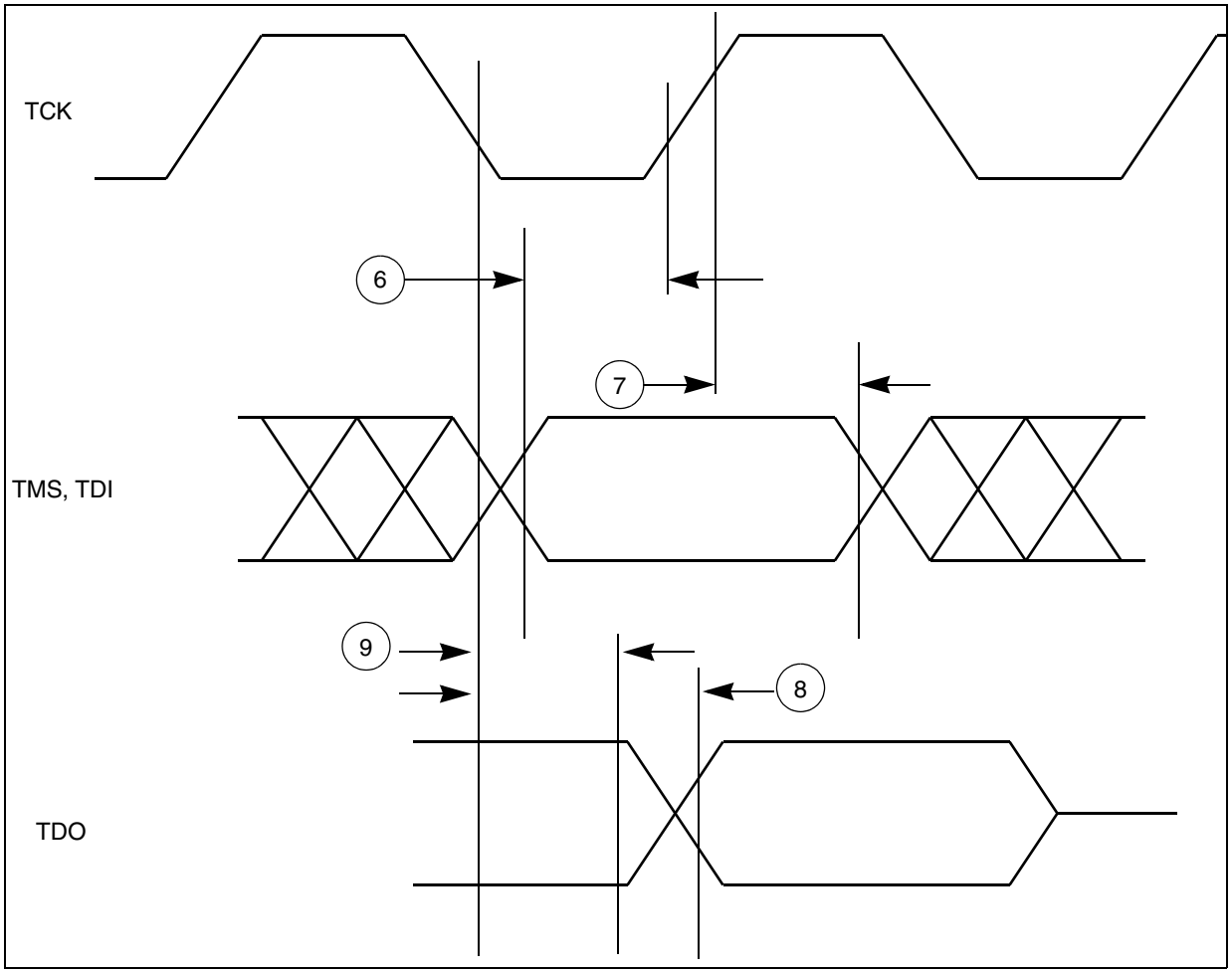


Figure 26. Nexus TDI, TMS, TDO timing

3.16.4 External interrupt timing (IRQ pin)

Table 37. External interrupt timing[1]

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	CC	D	IRQ pulse width low	—	4	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	4	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time[2]	—	4 + N [3]	—	t_{CYC}

1 IRQ timing specified at f_{SYS} = 64 MHz and $V_{DD\_HV\_IOx}$ = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and CL = 200pF with SRC = 0b00.

2 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

3 N= ISR time to clear the flag

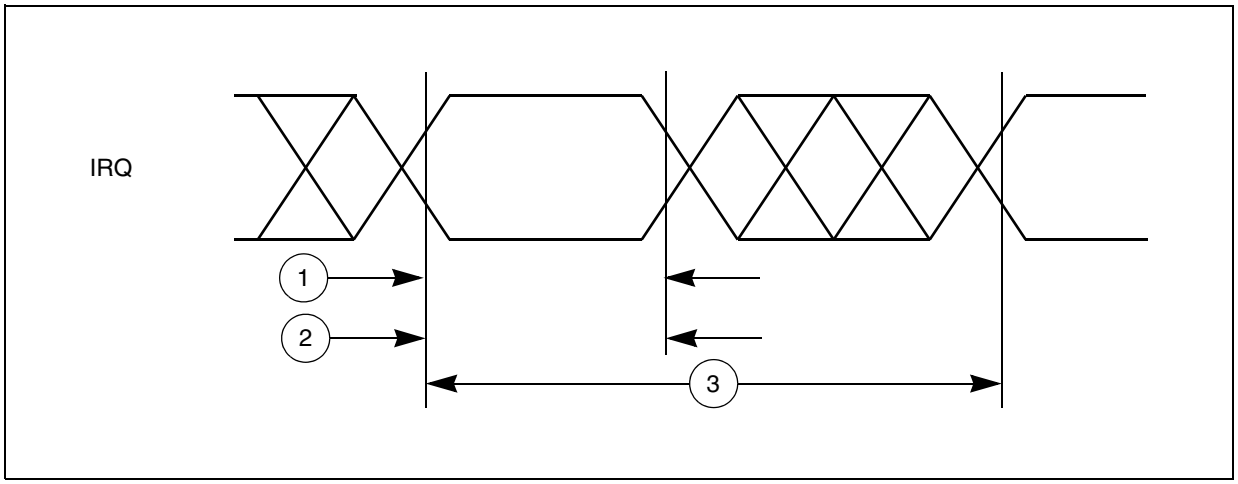


Figure 27. External interrupt timing

3.16.5 DSPI timing

Table 38. DSPI timing

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	60	—	ns
					Slave (MTFE = 0)	60	—	
2	t_{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	26	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	TBD	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	16	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	35	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	35	—	
					Master (MTFE = 1, CPHA = 1)	35	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	-5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	-5	—	

Table 38. DSPI timing (continued)

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	-2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	-2	—	

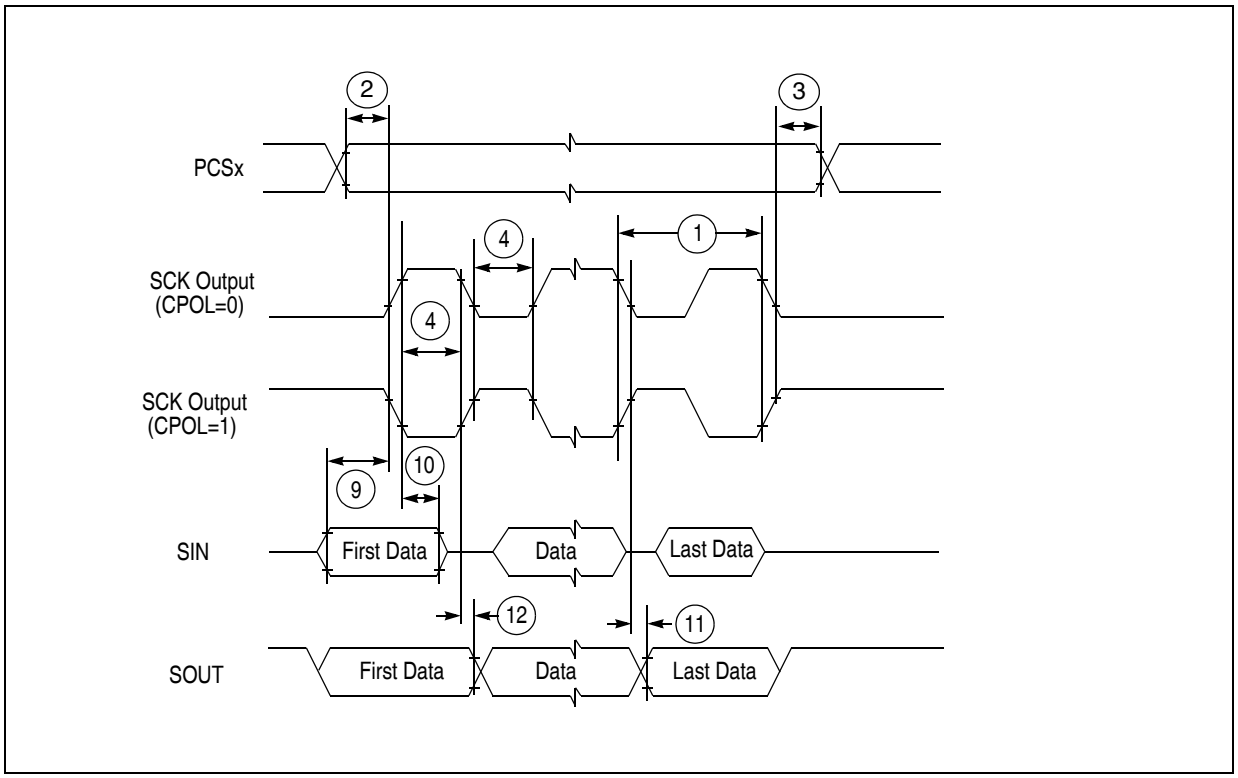


Figure 28. DSPI classic SPI timing - master, CPHA = 0

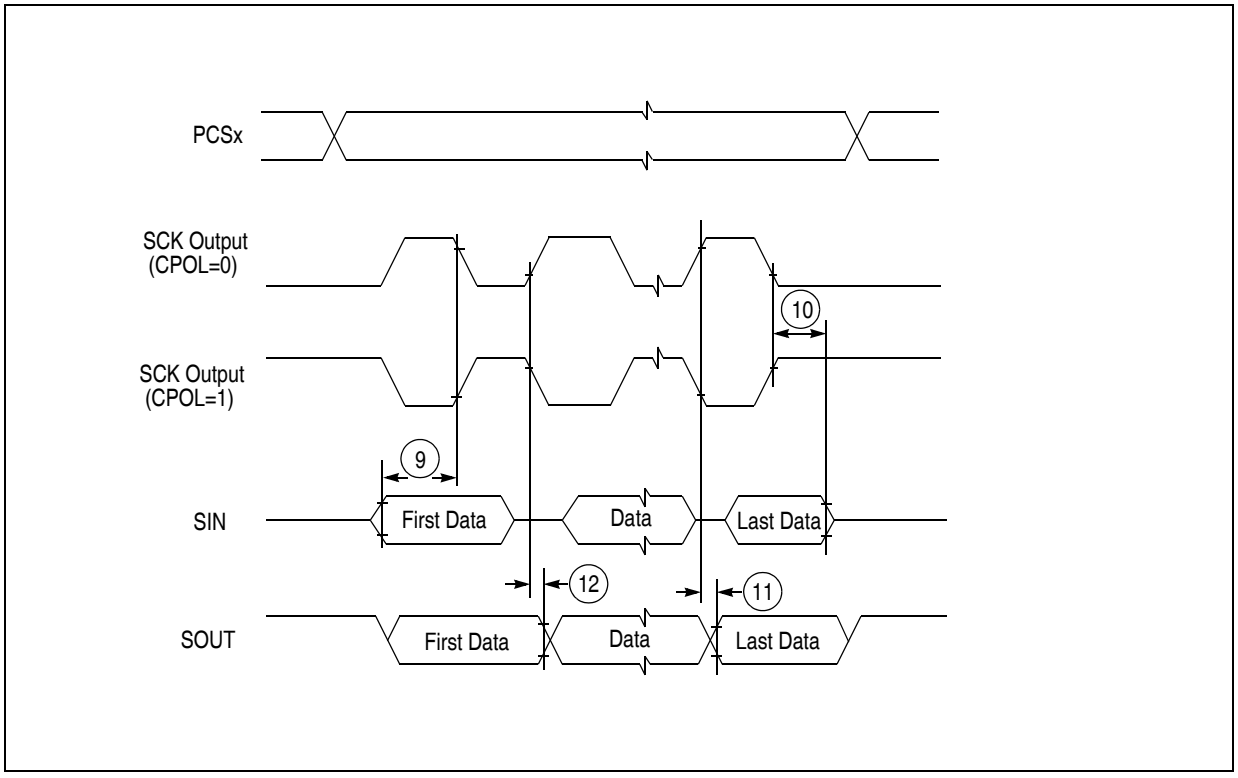


Figure 29. DSPI classic SPI timing - master, CPHA = 1

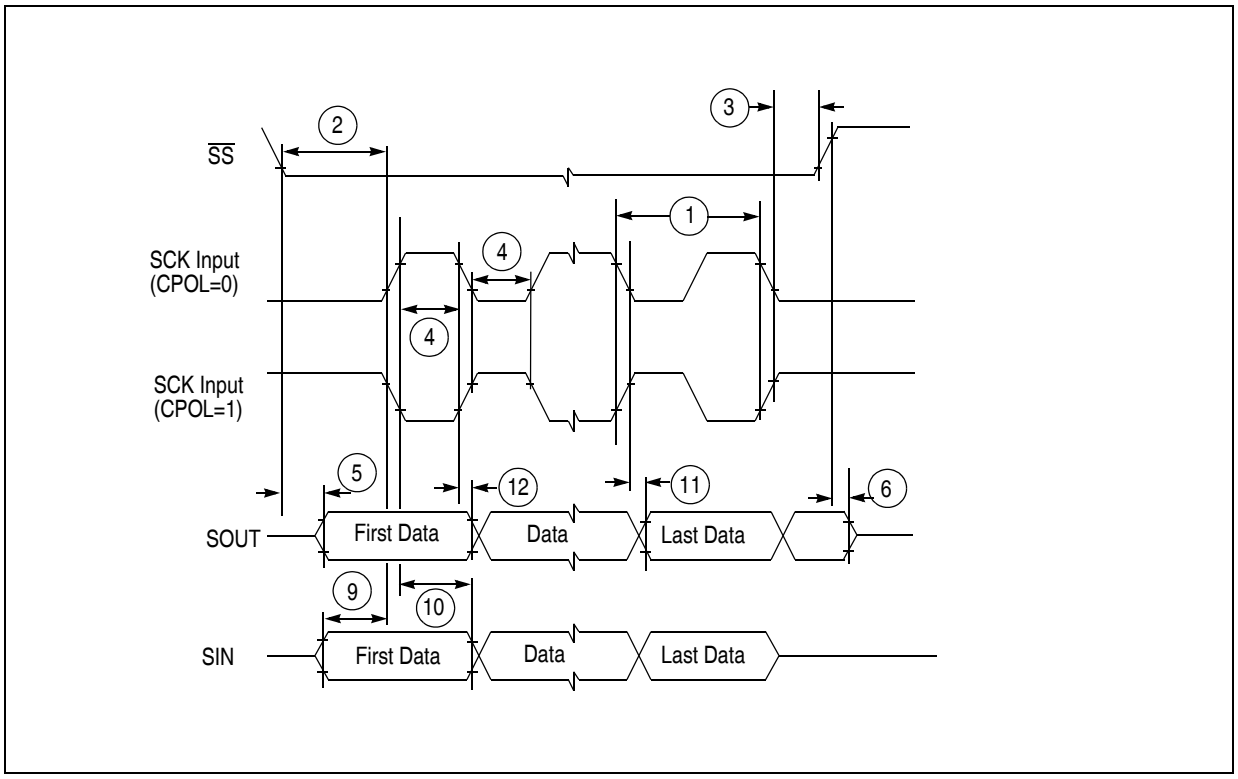


Figure 30. DSPI classic SPI timing - slave, CPHA = 0

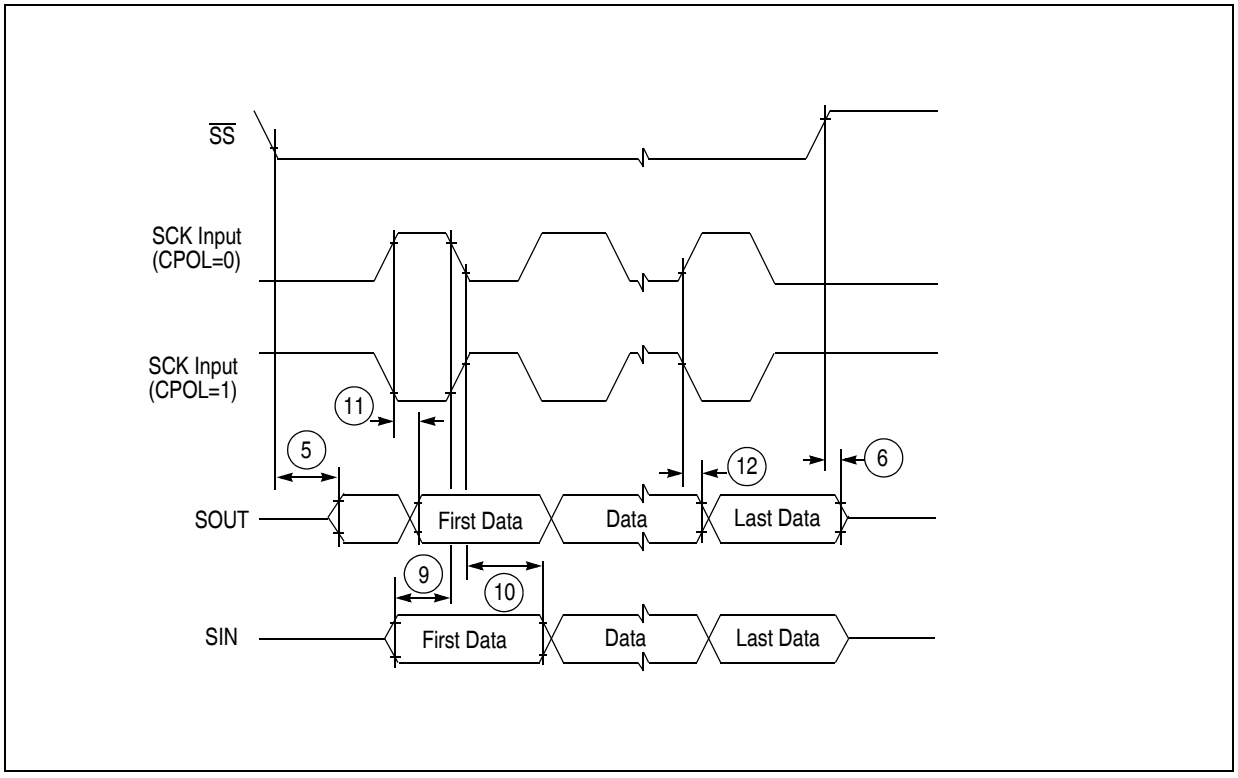


Figure 31. DSPI classic SPI timing - slave, CPHA = 1

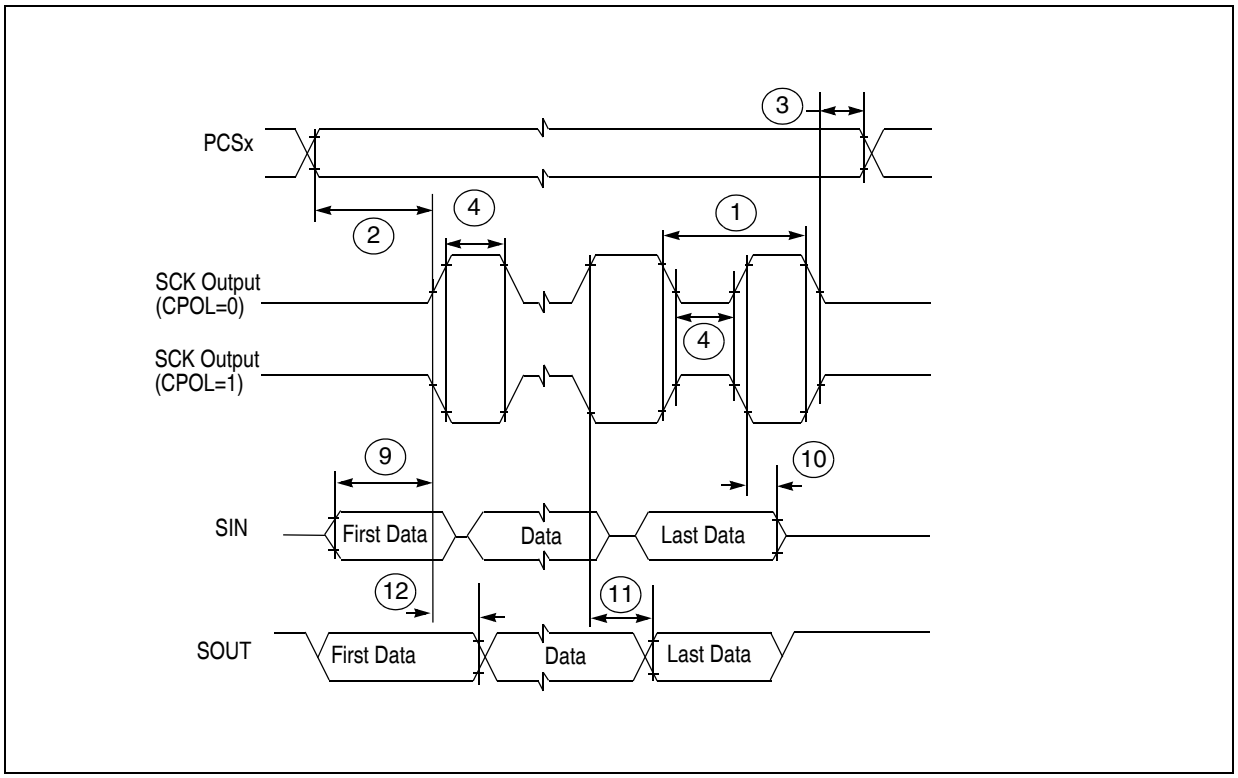


Figure 32. DSPI modified transfer format timing - master, CPHA = 0

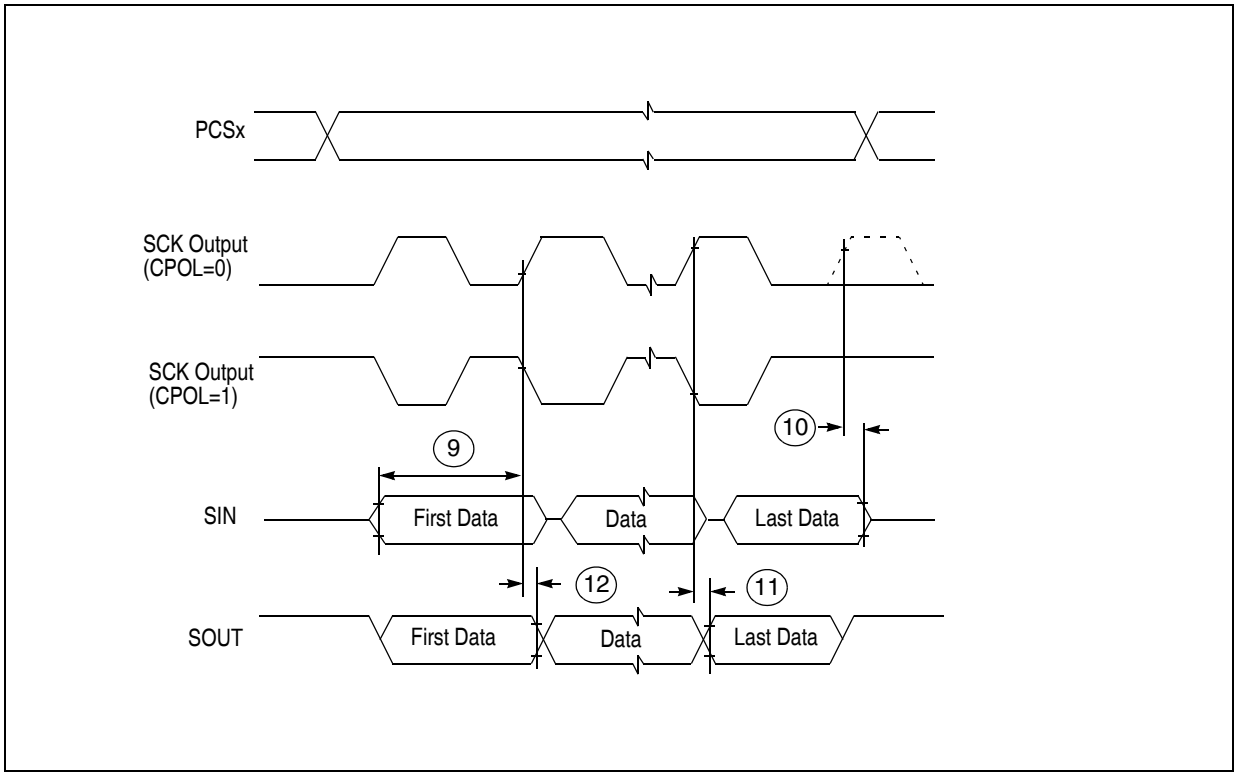


Figure 33. DSPI modified transfer format timing - master, CPHA = 1

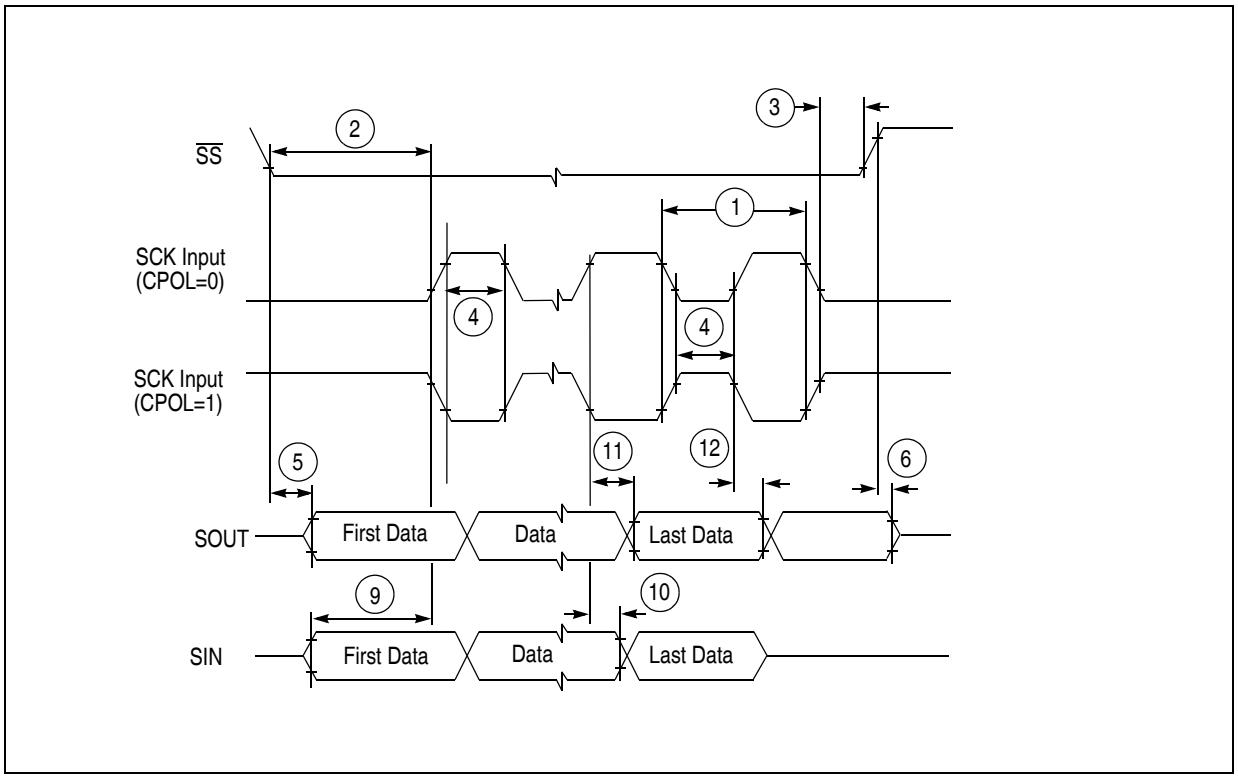


Figure 34. DSPI modified transfer format timing - slave, CPHA = 0

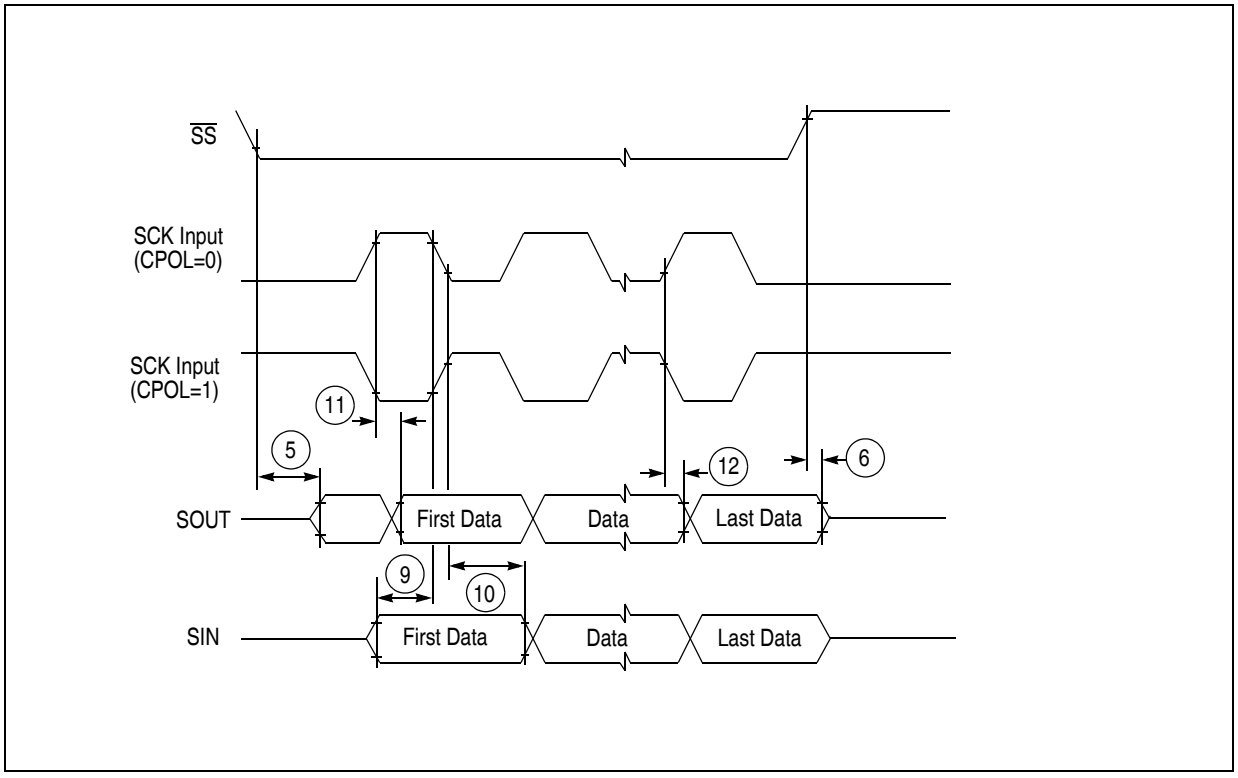


Figure 35. DSPI modified transfer format timing - slave, CPHA = 1

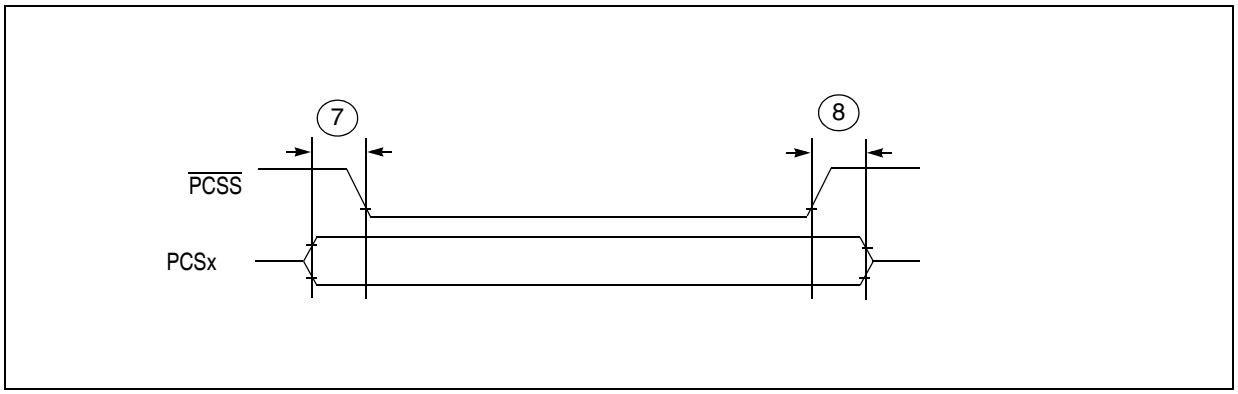


Figure 36. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4 Package characteristics

4.1 Package mechanical data

4.1.1 144 LQFP mechanical outline drawing

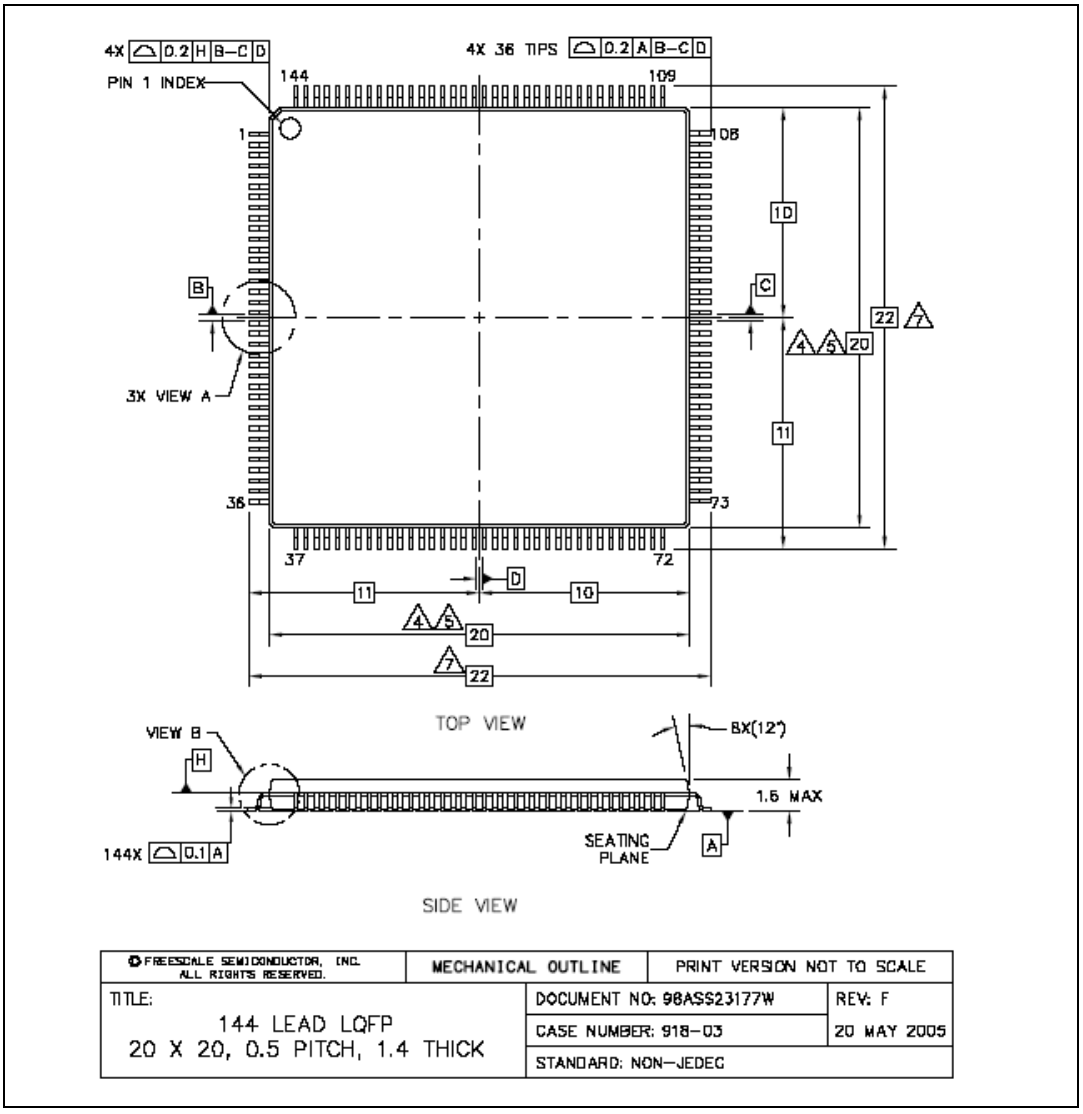


Figure 37. 144 LQFP package mechanical drawing (part 1)

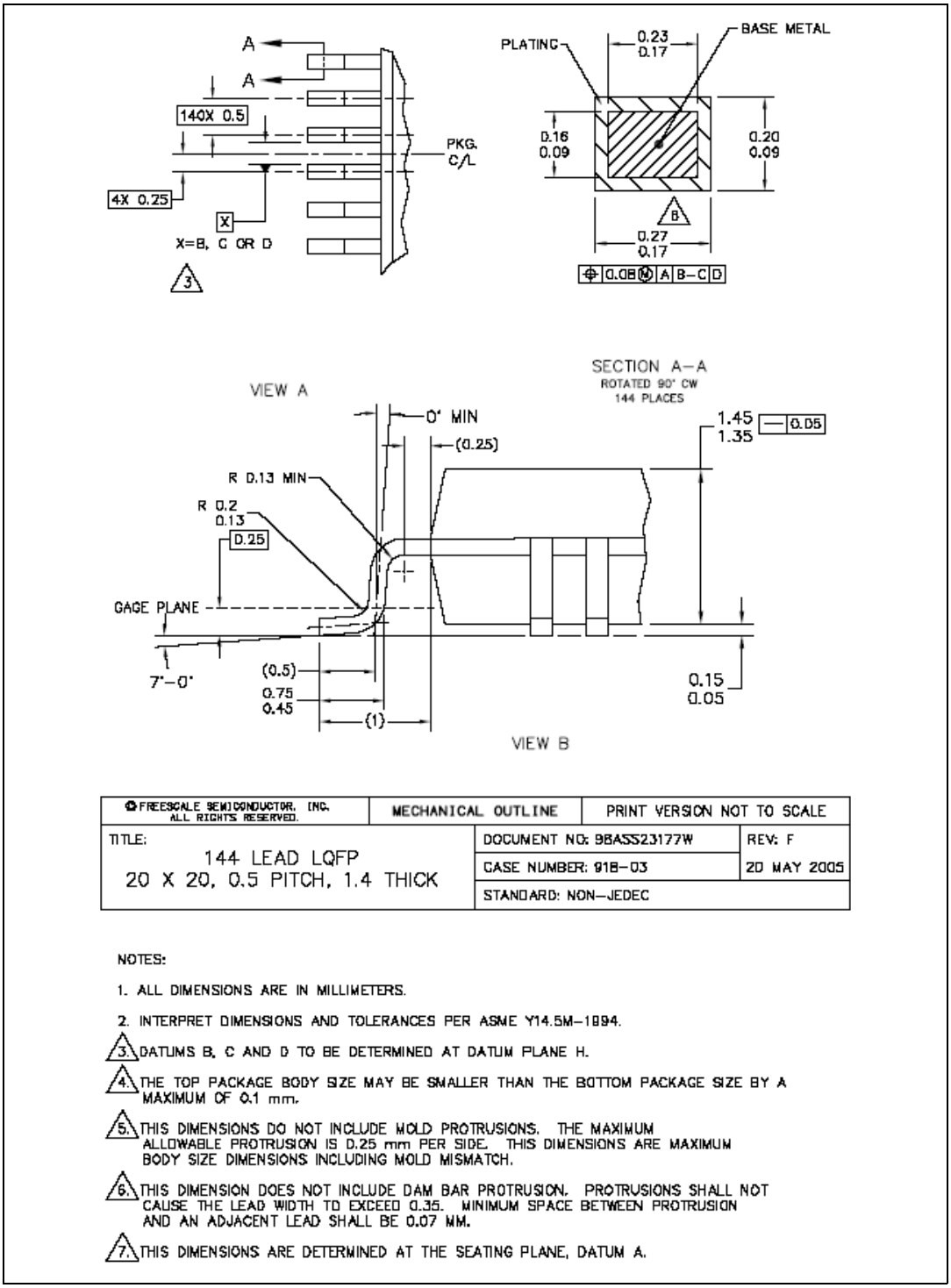


Figure 38. 144 LQFP package mechanical drawing (part 2)

4.1.2 100 LQFP Mechanical Outline Drawing

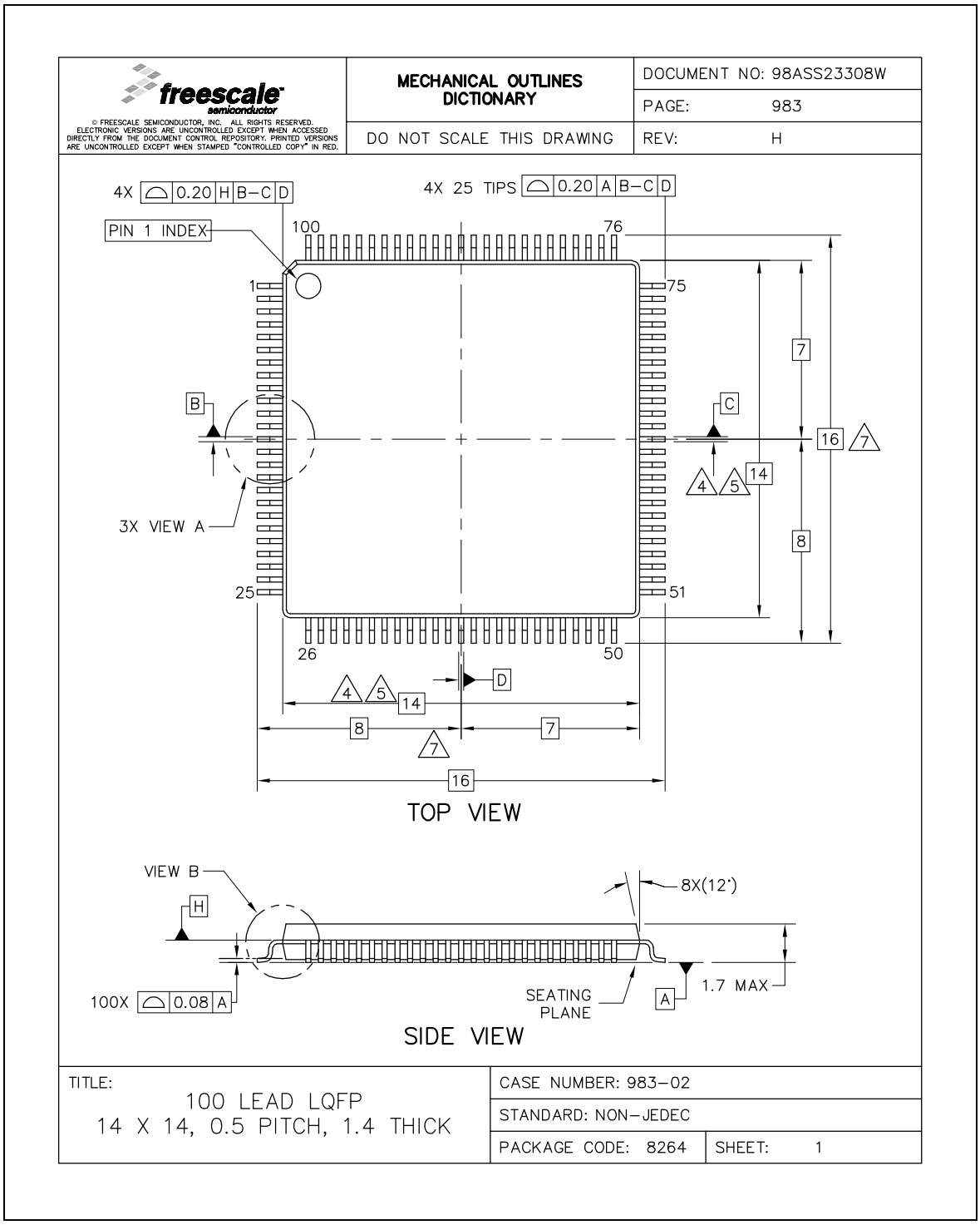


Figure 39. 100 LQFP package mechanical drawing (part 1)

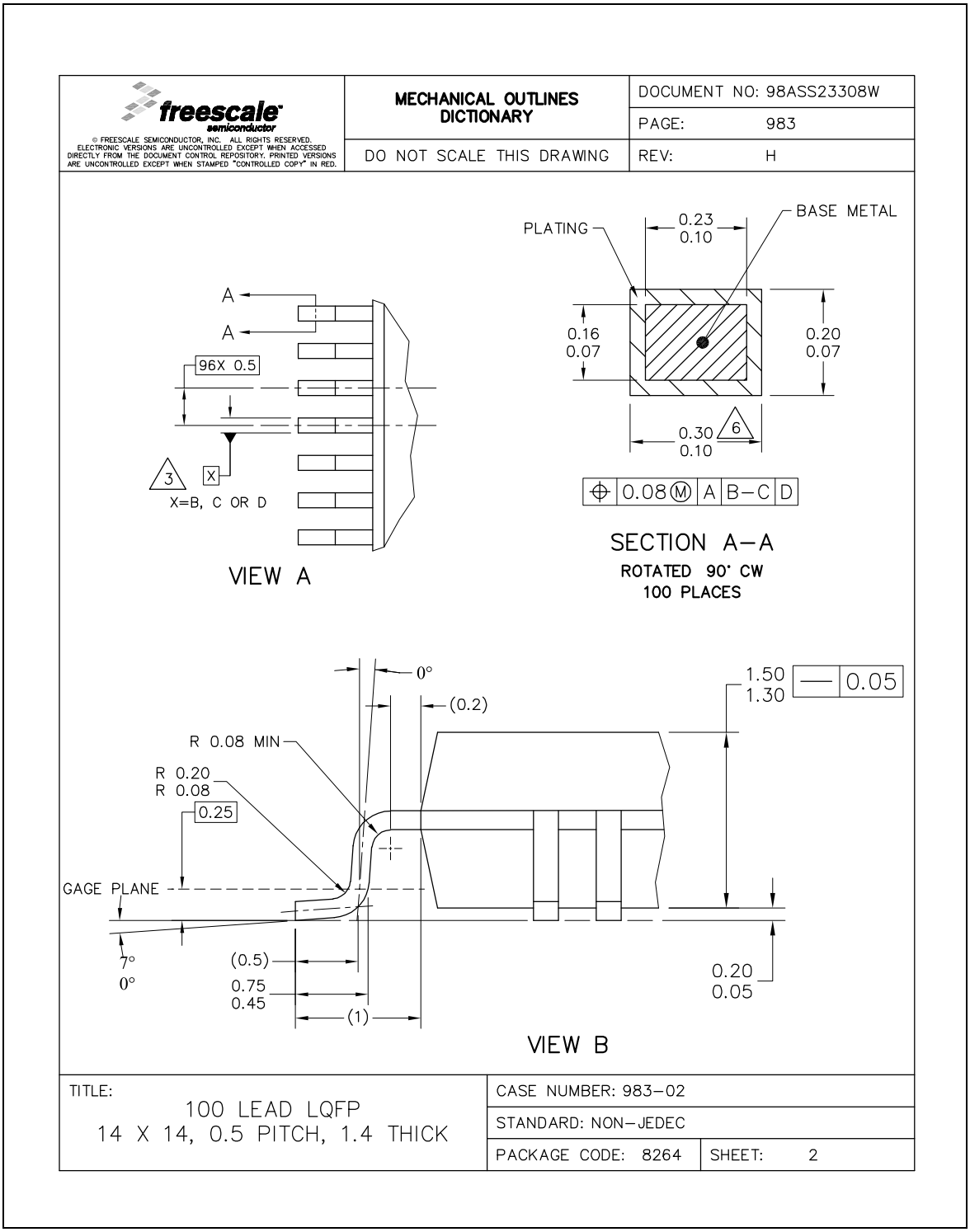


Figure 40. 100 LQFP package mechanical drawing (part 2)

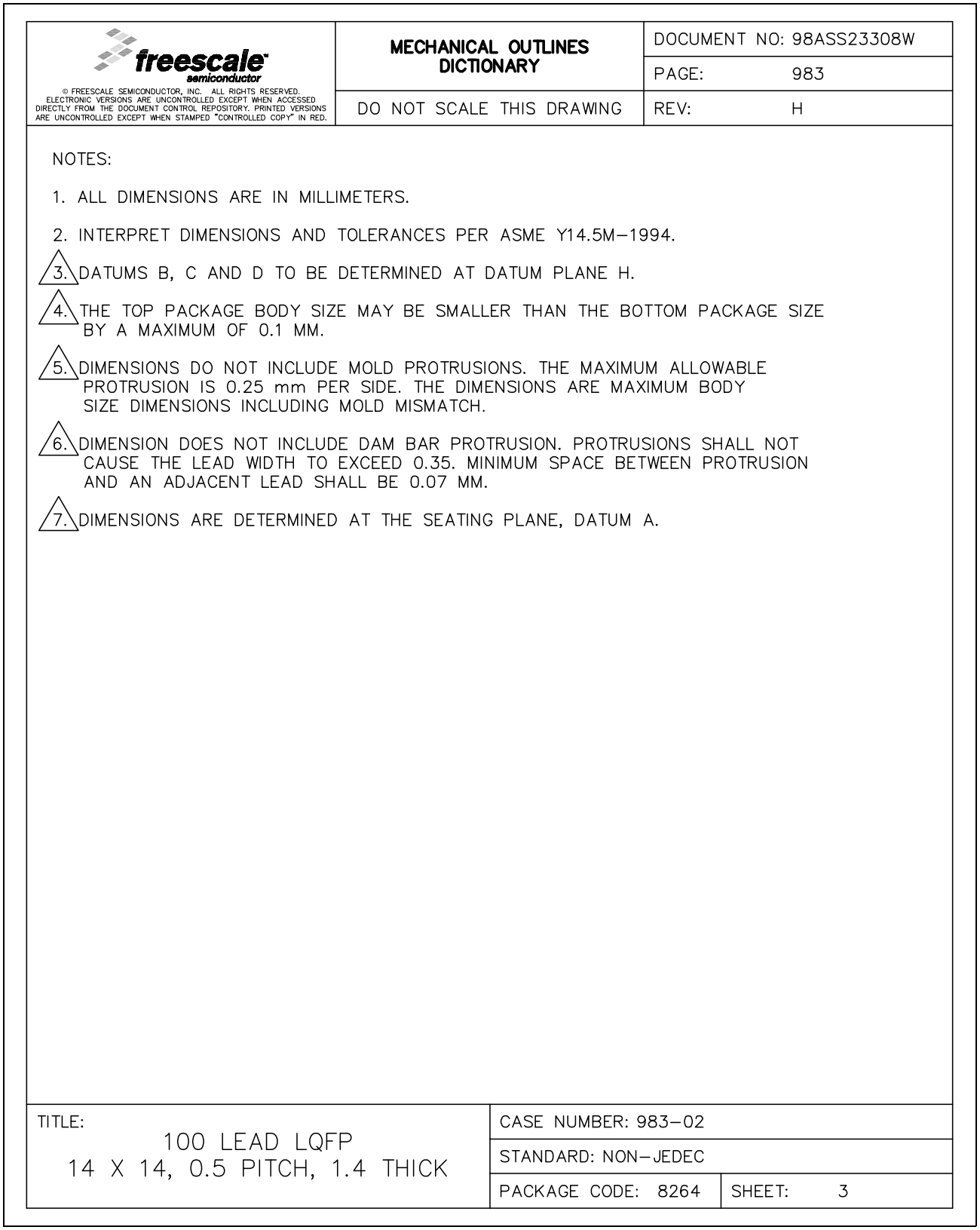


Figure 41. 100 LQFP package mechanical drawing (part 3)

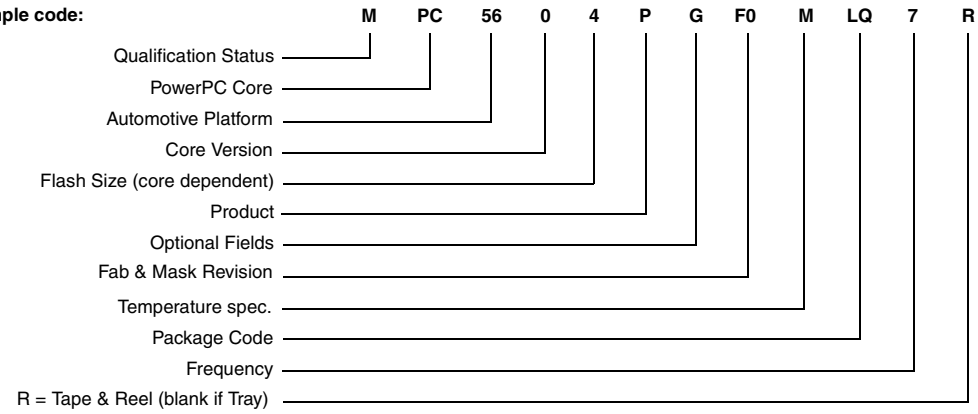
5 Ordering Information

Table 39 shows the orderable part numbers for the MPC5604P series.

Table 39. Orderable Part Number Summary

Part Number	Code Flash / Data Flash (EE) (KB)	SRAM (KB)	Package	Characteristics
MPC5604PEFMLQ	512 / 64	40	144 LQFP	FlexRay
MPC5604PEFMLL	512 / 64	40	100 LQFP	FlexRay
MPC5603PEFMLQ	384 / 64	36	144 LQFP	FlexRay
MPC5603PEFMLL	384 / 64	36	100 LQFP	FlexRay

Commercial product code structure



Qualification Status
M = MC status
S = Automotive qualified
P = PC status

Automotive Platform
56 = PPC in 90nm

Core Version
0 = e200z0

Flash Size (z0 core)
3 = 384 KB
4 = 512 KB

Product
P = Pictus

Optional fields
E = Data Flash (blank if none)
F = FlexRay

Temperature spec.
V = –40°C to 105°C
M = –40°C to 125°C

Package Code
LL = 100 LQFP
LQ = 144 LQFP

Frequency
7= 64 MHz

6 Document revision history

Table 40 summarizes revisions to this document.

Table 40. Revision history

Revision	Date	Substantive changes
Rev. 1	8/2008	Initial release
Rev. 2	11/2008	Table 4: TDO and TDI pins (Port pins B[4:5] are single function pins. Table 8, Table 9: Thermal characteristics added. Table 11, Table 12: EMI testing specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. Table 16, Table 17, Table 19, Table 20: Supply current specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. Table 19: • Values for I_{OL} and I_{OH} (in Conditions column) changed. • Max values for V_{OH_S}, V_{OH_M}, V_{OH_F} and V_{OH_SYM} deleted. • V_{ILR} max value changed. • I_{PUR} min and max values changed. Table 23: Sensitivity value changed. Table 30: Most values in table changed.
Rev. 3	2/2009	• Description of system requirements, controller characteristics and how controller characteristics are guaranteed updated. • Electrical parameters updated. • EMI characteristics are now in one table; values have been updated. • ESD characteristics are now in one table. • Electrical parameters are identified as either system requirements or controller characteristics. Method used to guarantee each controller characteristic is noted in table. • AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections deleted

Table 40. Revision history (continued)

Revision	Date	Substantive changes
Rev. 4	24/6/2009	Through all document: – Replaced all “RESET_B” occurrences with “$\overline{\text{RESET}}$” through all document. – AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections inserted again. – Electrical parameters updated. Section 1, “Overview: – Minor editorial clean-up. – Specified LIN 2.1 in communications interfaces feature. Table 2 – Added row for Data Flash. Table 2 – Added a footnote regarding the decoupling capacitors. Table 4 – Removed the “other function“ column. – Rearranged the contents. Table 12 – Updated definition of Condition column. Table 18 – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". Table 20 – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". Table 28 – Updated the parameter definition of ΔRCMVAR. – Removed the condition definition of ΔRCMVAR. Table 28 – Added t_{ADC_C} and TUE rows. Table 29 – Added t_{ADC_C} and TUE rows. – Removed $R_{sw2.}$ Table 32 – Added. Table 29 – Updated and added footnotes. Section 3.16.1, “RESET Pin Characteristics – Replaces whole section. Table 38 – Renamed the “Flash (KB)“ heading column in “Code Flash / Data Flash (EE) (KB)“ – Replaced the value of RAM from 32 to 36KB in the last four rows.

Table 40. Revision history (continued)

Revision	Date	Substantive changes
Rev. 5	06/10/2009	- Removed B[4] and B[5] rows from “Pin muxing” table and inserted them on “System pins” table. - Updated package pinout. - Rewrote entirely section “Power Up/dpwn Sequencing“ section. - Renamend “$V_{DD\_LV\_PLL}$“ and “$V_{SS\_LV\_PLL}$“ supply pins with respectively “$V_{DD\_LV\_COR3}$“ and “$V_{SS\_LV\_COR3}$”. - Added explicative figures on “Electrical characteristics” section. - Updated “Thermal characteristics“ for 100-pin. - Proposed two different configuration of “voltage regulator. - Inserted Power Up/Down sequence. - Added explicative figures on “DC Electrical characteristics”. - Added “I/O pad current specification” section. - Renamed the “Airbag mode” with “Typical mode“and updated the values on “supply current” tables.

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