LR38269

Digital Signal Processor for Color CCD Cameras

DESCRIPTION

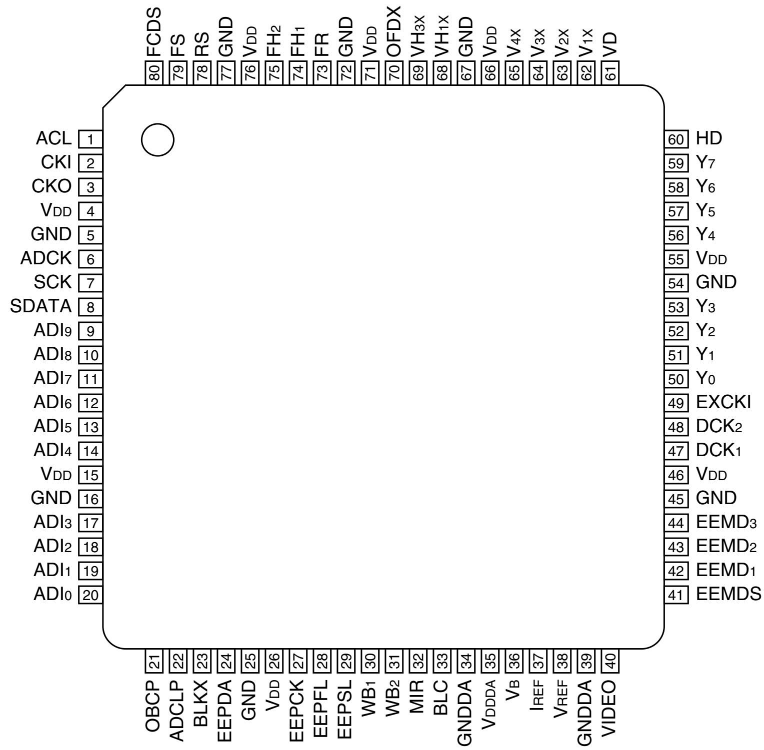
The LR38269 is a CMOS digital signal processor for color CCD camera system of 270 k/320 k-pixel CCD with complementary color filters. The camera system consists of CDS/AGC/ADC IC (IR3Y38M), DSP IC (LR38269), and V driver IC (LR36685) with CCD.

FEATURES

- Designed for 270 k/320 k color CCDs with Mg, G, Cy, and Ye complementary color filters
- Switchable between NTSC and PAL modes
- External control interface input/output
- Variable GAMMA and KNEE response (Select one out of 4 kinds of GAMMA & KNEE response)
- 10-bit digital input
- Analog NTSC/PAL composite output by built-in 9-bit 1 ch DA converter
- Built-in mirror image function
- Built-in timing generator to drive CCD
- Built-in 2 k-bit EEPROM controller to set the camera adjustment data
- Built-in auto exposure control
- Built-in auto white balance control
- Built-in auto carrier balance control
- Single + 3.3 V power supply
- Package :
  80-pin LQFP (LQFP080-P-1212) 0.5 mm pin-pitch

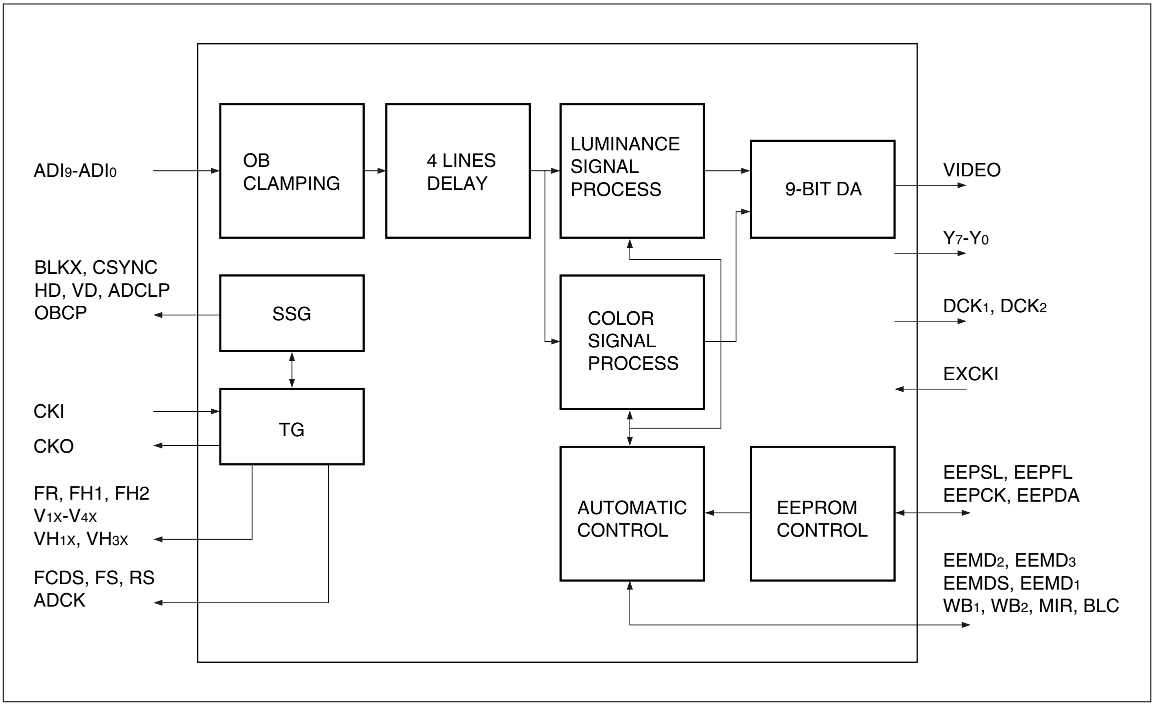
PIN CONNECTIONS

80-PIN LQFP TOP VIEW



(LQFP080-P-1212)

BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>I/O</th><th>POLARITY</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>ACL</td><td>IC</td><td></td><td>Initializing input.</td></tr>
<tr><td>2</td><td>CKI</td><td>OSCI</td><td></td><td>Input for reference clock oscillation. Connect to CKO (pin 3) with R.</td></tr>
<tr><td>3</td><td>CKO</td><td>OSCO</td><td></td><td>Output for reference clock oscillation. The output is the inverse of CKI (pin 2).</td></tr>
<tr><td>4</td><td>V_{DD}</td><td>–</td><td></td><td>Supply of +3.3 V power.</td></tr>
<tr><td>5</td><td>GND</td><td>–</td><td></td><td>A grounding pin.</td></tr>
<tr><td>6</td><td>ADCK</td><td>OBF6M</td><td></td><td>Clock output of AD converter, connected to pin 13 of IR3Y38M.</td></tr>
<tr><td>7</td><td>SCK</td><td>OBF4M</td><td></td><td>Clock output of serial data, connected to pin 16 of IR3Y38M.</td></tr>
<tr><td>8</td><td>SDATA</td><td>OBF4M</td><td></td><td>Serial data output, connected to pin 19 of IR3Y38M.</td></tr>
<tr><td>9</td><td>ADI_9</td><td>IC</td><td></td><td>Digital signal input, fed from pin 12 of IR3Y38M (MSB).</td></tr>
<tr><td>10</td><td>ADI_8</td><td>IC</td><td></td><td>Digital signal input, fed from pin 11 of IR3Y38M.</td></tr>
<tr><td>11</td><td>ADI_7</td><td>IC</td><td></td><td>Digital signal input, fed from pin 10 of IR3Y38M.</td></tr>
<tr><td>12</td><td>ADI_6</td><td>IC</td><td></td><td>Digital signal input, fed from pin 9 of IR3Y38M.</td></tr>
<tr><td>13</td><td>ADI_5</td><td>IC</td><td></td><td>Digital signal input, fed from pin 8 of IR3Y38M.</td></tr>
<tr><td>14</td><td>ADI_4</td><td>IC</td><td></td><td>Digital signal input, fed from pin 5 of IR3Y38M.</td></tr>
<tr><td>15</td><td>V_{DD}</td><td>–</td><td></td><td>Supply of +3.3 V power.</td></tr>
<tr><td>16</td><td>GND</td><td>–</td><td></td><td>A grounding pin.</td></tr>
<tr><td>17</td><td>ADI_3</td><td>IC</td><td></td><td>Digital signal input, fed from pin 4 of IR3Y38M.</td></tr>
<tr><td>18</td><td>ADI_2</td><td>IC</td><td></td><td>Digital signal input, fed from pin 3 of IR3Y38M.</td></tr>
<tr><td>19</td><td>ADI_1</td><td>IC</td><td></td><td>Digital signal input, fed from pin 2 of IR3Y38M.</td></tr>
<tr><td>20</td><td>ADI_0</td><td>IC</td><td></td><td>Digital signal input, fed from pin 1 of IR3Y38M (LSB).</td></tr>
<tr><td>21</td><td>OBCP</td><td>OBF4M</td><td></td><td>Optical clamp pulse output, connected to pin 32 of IR3Y38M.</td></tr>
<tr><td>22</td><td>ADCLP</td><td>OBF4M</td><td></td><td>Clamp pulse output, connected to pin 45 of IR3Y38M.</td></tr>
<tr><td>23</td><td>BLKX</td><td>OBF4M</td><td></td><td>Blanking pulse output, connected to pin 35 of IR3Y38M.</td></tr>
<tr><td>24</td><td>EEPDA</td><td>IO4MU</td><td></td><td>Data input from EEPROM output pin.</td></tr>
<tr><td>25</td><td>GND</td><td>–</td><td></td><td>Supply of +3.3 V power.</td></tr>
<tr><td>26</td><td>V_{DD}</td><td>–</td><td></td><td>A grounding pin.</td></tr>
<tr><td>27</td><td>EEPCK</td><td>IO4MU</td><td></td><td>Clock output to EEPROM clock input pin.
This pin keeps high-impedance under high level of pin 29.</td></tr>
<tr><td>28</td><td>EEPFL</td><td>IC</td><td></td><td>Control pin of EEPROM. Connect to the pull-up resistor.</td></tr>
<tr><td>29</td><td>EEPSL</td><td>IC</td><td></td><td>Control pin of EEPROM. A pull-down resistor should be connected between pin 29 and GND. High level of pin 29 can make data-setting from outside available.</td></tr>
<tr><td>30</td><td>WB_1</td><td>IO4M</td><td></td><td rowspan="2">White balance mode setting by both WB1 and WB2.
<table>
<tr><th>Pin 30</th><th>Pin 31</th><th>White balance mode</th></tr>
<tr><td>0</td><td>0</td><td>AUTO</td></tr>
<tr><td>0</td><td>1</td><td>PRESET WB_1</td></tr>
<tr><td>1</td><td>0</td><td>PRESET WB_2</td></tr>
<tr><td>1</td><td>1</td><td>PRESET WB_3</td></tr>
</table>
In digital output mode, pin 30 is assigned to bit 0 (LSB) of U/V signal and pin 31 is assigned to bit 1.</td></tr>
<tr><td>31</td><td>WB_2</td><td>IO4M</td><td></td></tr>
</table>

PIN NO.	SYMBOL	I/O	POLARITY	DESCRIPTION
32	MIR	IO4M		Video output mode setting. L : Normal H : Mirror In digital output mode, this pin is assigned to bit 2 of U/V signal.
33	BLC	IO4M		Backlight compensation selection. L : OFF H : ON In digital output mode, this pin is assigned to bit 3 of U/V signal.
34	GNDDA	–		A grounding pin of built-in DA converter.
35	V_{DDDA}	–		Supply of +3.3 V power of built-in DA converter.
36	V_B	DAO		Bias voltage output of built-in DA converter, connected to GND through a capacitor.
37	I_{REF}	DAO		Bias current output of built-in DA converter, connected to GND through a resistor.
38	V_{REF}	DAI		Bias voltage input of built-in DA converter, connected to +1.0 V power supply.
39	GNDDA	–		A grounding pin of built-in DA converter.
40	VIDEO	DAO		Analog video signal output.
41	EEMDS	IO4MU		Electronic exposure mode setting by EEMDS, EEMD1, EEMD2 and EEMD3. See "**Electronic Shutter Speed Setting**" in AUTOMATIC CAMERA FUNCTION CONTROL. In digital output mode, 41 to 44 pins are assigned to bits 7 to 4 of U/V signals.
42	$EEMD_1$	IO4MU		
43	$EEMD_2$	IO4MU		
44	$EEMD_3$	IO4MU		
45	GND	–		A grounding pin
46	V_{DD}	–		Supply of +3.3 V power.
47	DCK_1	OBF4M		Clock output for digital signal output. Output mode setting switches to CSYNC output.
48	DCK_2	OBF4M		ID pulse output for U/V output signal. In digital output, this pin outputs KEI-PULSE. **NOTE** : KEI-PULSE At power-on, it keeps low. Both 1/60 s (PAL 1/50 s) as shutter speed and AGC gain more than data of address 78h sets it high.
49	EXCKI	IC		Bit 3 of address 03h sets the function of this pin. 1 : Clock input of 13.5 MHz for digital output 0 : VRI input for analog output
50	Y_0	OBF4M		Bit 0 (LSB) of digital luminance signal output.
51	Y_1	OBF4M		Bit 1 of digital luminance signal output.
52	Y_2	OBF4M		Bit 2 of digital luminance signal output.
53	Y_3	OBF4M		Bit 3 of digital luminance signal output.
54	GND	–		A grounding pin.
55	V_{DD}	–		Supply of +3.3 V power.
56	Y_4	OBF4M		Bit 4 of digital luminance signal output.
57	Y_5	OBF4M		Bit 5 of digital luminance signal output.
58	Y_6	OBF4M		Bit 6 of digital luminance signal output.

PIN NO.	SYMBOL	I/O	POLARITY	DESCRIPTION
59	Y_7	OBF4M		Bit 7 (MSB) of digital luminance signal output
60	HD	OBF4M		Horizontal driving pulse output. Either CCD driving timing or BELL-PULSE is selected by output mode setting. **NOTE** : BELL-PULSE Some period with high level every field.
61	VD	OBF4M		Vertical driving pulse output. Either VD or CSYNC with either driving timing or video output timing is selected by output mode setting.
62	V_{1X}	OBF4M		Vertical driving pulse output, connected to pin 20 of LR36685.
63	V_{2X}	OBF4M		Vertical driving pulse output, connected to pin 21 of LR36685.
64	V_{3X}	OBF4M		Vertical driving pulse output, connected to pin 18 of LR36685.
65	V_{4X}	OBF4M		Vertical driving pulse output, connected to pin 14 of LR36685.
66	V_{DD}	–		Supply of +3.3 V power.
67	GND	–		A grounding pin.
68	VH_{1X}	OBF4M		Vertical driving pulse output, connected to pin 19 of LR36685.
69	VH_{3X}	OBF4M		Vertical driving pulse output, connected to pin 15 of LR36685.
70	OFDX	OBF6M		OFD driving pulse output, connected to pin 22 of LR36685.
71	V_{DD}	–		Supply of +3.3 V power.
72	GND	–		A grounding pin.
73	FR	OBF12M		Reset pulse output, connected to CCD through a capacitor.
74	FH_1	OBF12M		Horizontal driving pulse output, connected to CCD.
75	FH_2	OBF12M		Horizontal driving pulse output, connected to CCD.
76	V_{DD}	–		Supply of +3.3 V power.
77	GND	–		A grounding pin.
78	RS	OBF6M		Sample-hold pulse output, connected to pin 31 of IR3Y38M.
79	FS	OBF6M		Sample-hold pulse output, connected to pin 30 of IR3Y38M.
80	FCDS	OBF6M		Sample-hold pulse output, connected to both pin 28 and pin 29 of IR3Y38M.

IC : Input pin
OBF4M : Output pin
OBF6M : Output pin
OBF12M : Output pin
IO4M : Input/output pin
IO4MU : Input/output pin with pull-up resistor
OSCI : Input pin for oscillation
OSCO : Output pin for oscillation
DAI : Input pin for DA converter
DAO : Output pin for DA converter

INTERNAL COEFFICIENT TABLE

ADDRESS	NAME	BIT	CONTENTS		
00h			Not used		
01h	MODE 1	7	TV mode	0 : NTSC	1 : PAL
		6	Input signal delay	0 : No delay	1 : 1 clock cycle delay
		5	Clock polarity to latch input signal	0 : Normal	1 : Inverted
		4	YL killer	0 : Normal	1 : Killed
		3	Pin mode selection (**NOTE 1**)	0 : Mode input	1 : U/V output
		2	VD output timing selection (**NOTE 1**)		
		1	HD output timing selection	0 : TG	1 : Video output
		0	DCK_1 output selection (**NOTE 1**)		
02h	MODE 2	7-6	Luminance gamma selection		
		5-4	Color gamma selection		
		3	Vertical aperture enhancement	0 : ON	1 : OFF
		2	Horizontal aperture enhancement	0 : ON	1 : OFF
		1	Color killer	0 : ON	1 : OFF
		0	Flicker reduction	0 : ON	1 : OFF
03h	MODE 3	7	Polarity selection of SP_1 and SP_2		
		6	Polarity inverter of HG		
		5	Video format selection	0 : Interlace	1 : Non-interlace
		4	UV dot-sequence selection (output stage)		
		3	UV dot-sequence selection		
		2	Carrier balance tuning	0 : ON	1 : OFF
		1	AGC	0 : Auto	1 : Fixed (gain at address 1Bh)
		0	Digital output clock	0 : 9.6 MHz	1 : Clock of EXCKI pin
04h	REF_IRIS1	7-0	Exposure reference level (target of exposure control)		
05h	CTLD_01	7-0	Higher level of exposure reference level		
06h	CTLD_02	7-0	Lower level of exposure reference level		
07h	REF_IRIS2	7-0	Exposure reference level with backlight compensation		
08h	UW_E1	7-0	Exposure control weighting factor 1		
09h	UW_E2	7-0	Exposure control weighting factor 2		
0Ah	UW_E3	7-0	Exposure control weighting factor 3		
0Bh	UW_E4	7-0	Exposure control weighting factor 4		
0Ch	UW_E5	7-0	Exposure control weighting factor 5		
0Dh	UW_E6	7-0	Exposure control weighting factor 6		
0Eh	UW_E7	7-0	Exposure control weighting factor 7		
0Fh	UW_E8	7-0	Exposure control weighting factor 8		
10h	CW_E	6-0	Weighting factor of exposure window area		
11h	CWP_E	6-0	Top-left point of exposure window area		
12h	CWA_E	6-0	Bottom-right point of exposure window area		

ADDRESS	NAME	BIT	CONTENTS
13h	EE_DIV_STP	6-4	Electronic shutter speed pitch 000 : Slower 111 : Quicker
	LPFE_F	3-2	Exposure response speed selection with flicker reduction 00 : Slower 01 : Normal 10 or 11 : Quicker
	LPFE_N	1-0	Exposure response speed selection 00 : Slower 01 : Normal 10 or 11 : Quicker
14h	P_HEE_IRIS	7-0	Maximum luminance level factor to control exposure
15h	P_LEE_IRIS	7-0	Minimum luminance level factor to control exposure
16h	INT_PEAK	6	Integrated pixels of peak signal 0 : 8 pixels 1 : 4 pixels
	IRIS_DLY1	5	Condition of exposure control under locking-in number of images to control exposure. 0 : 1 image 1 : Integrated 3 images
		4 3	Valid image to control exposure 00 : Every image 01 : Every 2 images 10 : Every 4 images 11 : Every 8 images
	IRIS_DLY2	2	Condition of exposure control under free-running Number of images 0 : 1 image 1 : Integrated 3 images
		1 0	Valid image to control exposure 00 : Every image 01 : Every 2 images 10 : Every 4 images 11 : Every 8 images
17h	AG_DIV_STP	7-5	AGC control data 000 : Slower 111 : Quicker
	AG_GAIN	4-0	Minimum pitch of AGC variable gain DATA should be between 01h (finest pitch) and 1Fh.
18h			Not used
19h	I_AGC_D8	7-0	AGC gain at power-on
1Ah	REF_AGC_D8	7-0	AGC reference gain (more than data of 19h)
1Bh	S_38M_GA	7-0	Fixed AGC gain
1Ch	S_38M_MAX	2-0	AGC maximum gain
1Dh	S_38M_OFS	6	Offset control 0 : Auto 1 : Fixed
		5-0	Offset data
1Eh	CSEPR	7-0	Coefficient to extract red color signal
1Fh	CSEPB	7-0	Coefficient to extract blue color signal
20h	CB_R	7-0	Red signal carrier balance
21h	CB_B	7-0	Blue signal carrier balance
22h	K_T_R	7-0	Basic red WB gain
23h	K_T_B	7-0	Basic blue WB gain
24h	MAX_WBR	7-0	Red WB gain at maximum color temperature
25h	MIN_WBR	7-0	Red WB gain at minimum color temperature
26h	MAX_WBB	7-0	Blue WB gain at minimum color temperature
27h	MIN_WBB	7-0	Blue WB gain red at maximum color temperature
28h	WBR1	7-0	Red WB data (preset 1)
29h	WBB1	7-0	Blue WB data (preset 1)
2Ah	WBR2	7-0	Red WB data (preset 2)
2Bh	WBB2	7-0	Blue WB data (preset 2)
2Ch	WBR3	7-0	Red WB data (preset 3)

ADDRESS	NAME	BIT	CONTENTS
2Dh	WBB3	7-0	Blue WB data (preset 3)
2Eh	K_GA_R	7-0	Correction coefficient of R – Y gain
2Fh	K_GA_B	7-0	Correction coefficient of B – Y gain
30h	REF_GA_R	5-0	Basic gain of R – Y signal
31h	REF_GA_B	5-0	Basic gain of B – Y signal
32h	GA_R1	5-0	R – Y gain data (preset 1)
33h	GA_B1	5-0	B – Y gain data (preset 1)
34h	GA_R2	5-0	R – Y gain data (preset 2)
35h	GA_B2	5-0	B – Y gain data (preset 2)
36h	GA_R3	5-0	R – Y gain data (preset 3)
37h	GA_B3	5-0	B – Y gain data (preset 3)
38h	MAX_IQAREA	7	AWB IQ area selection 0 : Set data 1 : Widest
	LPFIQ_F	6-5	Response speed selection with flicker reduction 00 : Slower 01 : Normal 10 or 11 : Quicker
	LPFIQ_N	4-3	Response speed
	FINE	2	Fine-tuning mode of auto white balance
	AWB_WAIT_C	1-0	AWB time constant after lock-in (upper 2 bits)
39h	AWB_WAIT_C	7-0	AWB time constant after lock-in (lower 8 bits)
3Ah	CMP_CT	7-0	Valid data to control AWB (01h makes all AWB data valid.)
3Bh	AWB_HCL	7-0	Highest luminance level to be available for AWB control
3Ch	AWB_LCL	7-0	Lowest luminance level to be available for AWB control
3Dh	REF_WBPK	7-0	Offset luminance level to control data of 3Bh and 3Ch
3Eh	K_CL	7-0	Maximum luminance level factor to control data of 3Bh and 3Ch
3Fh	K_WBCL	7-0	Weighting factor for data of 3Dh and 3Eh
40h	UW_IQ1	7-0	AWB control weighting factor 1
41h	UW_IQ2	7-0	AWB control weighting factor 2
42h	UW_IQ3	7-0	AWB control weighting factor 3
43h	UW_IQ4	7-0	AWB control weighting factor 4
44h	INT_I_R – Y	7	AWB control data 0 : I/Q 1 : R – Y/B – Y
	CW_IQ	6-0	Weighting factor of AWB window area
45h	CWPA_IQ	7-4	Top-left point of AWB window area
		3-0	Bottom-right point of AWB window area
46h	CTLD_AW0	7-0	Exposure level to erase the area to detect white color

ADDRESS	NAME	BIT	CONTENTS	
47h	AWB_IP_L	7-0	First AWB detector area I-PLUS	**NOTE :** Data to set first area should be larger than data to set second area. Second area should be closer to the cross point of I-axis and Q-axis, compared to first area.
48h	AWB_IM_L	7-0	First AWB detector area I-MINUS	
49h	AWB_QP_L	7-0	First AWB detector area Q-PLUS	
4Ah	AWB_QM_L	7-0	First AWB detector area Q-MINUS	
4Bh	AWB_IP_S	7-0	Second AWB detector area I-PLUS	
4Ch	AWB_IM_S	7-0	Second AWB detector area I-MINUS	
4Dh	AWB_QP_S	7-0	Second AWB detector area Q-PLUS	
4Eh	AWB_QM_S	7-0	Second AWB detector area Q-MINUS	
4Fh	AWB_I_WH_L	6-0	First AWB white zone I-PLUS	
50h	AWB_Q_WH_L	6-0	First AWB white zone Q-PLUS	
51h	AWB_I_WH_S	6-0	Second AWB white zone I-MINUS	
52h	AWB_Q_WH_S	6-0	Second AWB white zone Q-MINUS	
53h	K_MAT_R	7-0	R – Y gain factor for color matrix correction	
54h	K_MAT_B	7-0	B – Y gain factor for color matrix correction	
55h	REF_MAT_R	5-0	Basic R – Y data of color matrix correction	
56h	REF_MAT_B	5-0	Basic B – Y data of color matrix correction	
57h	MAT1	7-0	Color matrix data (preset 1) R – Y 4 bits, B – Y 4 bits	
58h	MAT2	7-0	Color matrix data (preset 2) R – Y 4 bits, B – Y 4 bits	
59h	MAT3	7-0	Color matrix data (preset 3) R – Y 4 bits, B – Y 4 bits	
5Ah	COL_S	7-0	AGC gain to start suppressing color signal	
5Bh	COL_H	5-0	Pitch of color signal suppressing by address 5Ah	
5Ch	CKI_HCL	7-0	Higher luminance level to start suppressing color signal	
5Dh	CKI_LCL	7-0	Lower luminance level to start suppressing color signal	
5Eh	CKI_HLGA	7-4	Color signal suppression gain for higher luminance signal	
		3-0	Color signal suppression gain for lower luminance signal	
5Fh	CKI_HLTI	7-4	Highlight luminance signal position to suppress color –2 to +2	
		3-0	Lowest luminance signal position to suppress color –2 to +2	
60h	CKI_HECL	7-0	Horizontal aperture level to start suppressing color signal	
61h	CKI_EVCL	7-0	Vertical aperture level to start suppressing color signal	
62h	CKI_EGA	7-4	Horizontal aperture gain to suppress color signal by address 60h	
		3-0	Vertical aperture gain to suppress color signal by address 61h	
63h	APT_S	7-0	AGC gain to start suppressing aperture signal	
64h	APT_H	5-0	Gain to suppress aperture signal by address 63h	
65h	NSUP_R	7-0	R – Y signal coring level	
66h	NSUP_B	7-0	B – Y signal coring level	
67h	CKI_IEL	7	Color-killer level 0 : Unity gain 1 : 1/4 gain	
	CKI_ETI	6-4	Horizontal edge signal position to kill color signal –2 to +2	
		3-1	Vertical edge signal position to kill color signal –2 to +2	
68h	APT_HTIM	7-6	Horizontal aperture signal position –1 to +1	
	APT_HGA	5-1	Horizontal aperture gain	

ADDRESS	NAME	BIT	CONTENTS		
69h	APT_HCL	6-0	Horizontal aperture signal coring		
6Ah	APT_VGA	4-0	Vertical aperture gain		
6Bh	APT_VCL	6-0	Vertical aperture signal coring		
6Ch	CBLK_LV	7	CBLK level selection	0 : 00h	1 : 10h
	SETUP	6-1	Set up level		
6Dh	VARI_Y	4-0	luminance signal position		
6Eh	SW_CTRL	7-0	The following setting is available under both EEPSL = H and digital output mode WB1 (LSB), WB2, BACK, EEMDS, EEMD1 EEMD2, EEMD3, MIR (MSB)		
6Fh	TG_SEL1	7-5	ADCK phase setting (6 steps per 60˚)		
		4-2	FS phase setting (±2 ns x 3)		
70h	TG_SEL2	7-5	FCDS phase setting (±2 ns x 3)		
		4-2	FR phase setting (±2 ns x 3)		
71h	ENC_MUTE	7	Encoder muting	0 : OFF	1 : ON
	SYNC_SW	6	SYNC adder	0 : ON	1 : OFF
	SEL_RB	5	Serial digital data setting		
	OUT_GAIN	4-0	Gain of video output amplifier		
72h	SYNC_LEV	7-0	SYNC level (80h = 40 IRE)		
73h	BAS_R	7-0	BURST level of R – Y		
74h	BAS_B	7-0	BURST level of B – Y		
75h	MUTE_OUT	7	Muting at power-on		
		6-0	Muting period (data multiplied by 1 field period)		
76h	TEST	2-0	Test data (EEPROM data must be 00h)		
77h	VRI	2	EXCKI pin function	1 : VRI function	0 : Clock input
	TEST	1	Test data (EEPROM data must be 0)		
	TEST	0	Test data (EEPROM data must be 0)		
78h	KEI_AGC	8	AGC gain to set KEI-PULSE high		

(NOTE 1)

ADDRESS 01			SIGNAL OUTPUT		
Bit 3	Bit 2	Bit 0	DCK_1 (Pin 47)	VD (Pin 61)	HD (Pin 60)
DIGITAL 1	1	0	DCK_1	VD for video out	HD
	0	0	DCK_1	VD for CCD driving	HD
	x	1	DCK_1	CSYNC	HD
ANALOG 0	1	0	CSYNC	VD for video out	HD
	0	0	CSYNC	VD for CCD driving	HD
	1	1	CSYNC	VD for video out	BELL
	0	1	CSYNC	VD for CCD driving	BELL

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power supply voltage	V_{DD}	−0.3 to +4.3	V
Input voltage	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O	−0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	−55 to +150	˚C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating temperature	T_{OPR}	−20	+25	+70	˚C
Input clock frequency	f_{CK}		28.6		MHz

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0 to 3.6 V, T_{OPR} = −20 to +70 ˚C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}				0.2 V_{DD}	V	1
Input "High" voltage	V_{IH}		0.8 V_{DD}			V	
Input "Low" current	$\lvert I_{IL1} \rvert$	V_{IN} = 0 V		100		μA	2
Output "Low" voltage	V_{OL1}	I_{OL} = 4 mA			0.2 V_{DD}	V	3
Output "High" voltage	V_{OH1}	I_{OH} = −4 mA	0.8 V_{DD}			V	
Output "Low" voltage	V_{OL2}	I_{OL} = 6 mA			0.2 V_{DD}	V	4
Output "High" voltage	V_{OH2}	I_{OH} = −6 mA	0.8 V_{DD}			V	
Output "Low" voltage	V_{OL3}	I_{OL} = 12 mA			0.2 V_{DD}	V	5
Output "High" voltage	V_{OH3}	I_{OH} = −12 mA	0.8 V_{DD}			V	
Output "Low" voltage	V_{OL4}	I_{OL} = 3 mA			0.2 V_{DD}	V	6
Output "High" voltage	V_{OH4}	I_{OH} = −2 mA	0.8 V_{DD}			V	
Resolution	RES			9		bit	7
Linearity error	EL	V_{REF} = 1.0 V			±3.0	LSB	
Differential error	ED	R_{REF}= 4.8 kΩ			±1.0	LSB	
Full scale current	$\lvert I_{FS} \rvert$	R_{OUT} = 75 Ω		13		mA	
Reference voltage	V_{REF}			1.0		V	8
Reference resistance	R_{REF}			4.8		kΩ	9
Output load resistance	R_{OUT}			75		Ω	7

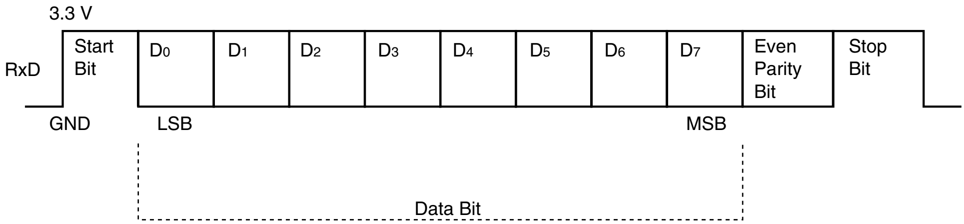
NOTES :

1. Applied to inputs (IC, IO4M, IO4MU).
2. Applied to input (IO4MU).
3. Applied to outputs (OBF4M, IO4M, IO4MU).
4. Applied to output (OBF6M).
5. Applied to output (OBF12M).
6. Applied to output (OSCO).
7. Applied to output (VIDEO).
8. Applied to input (V_{REF}).
9. Applied to output (I_{REF}).

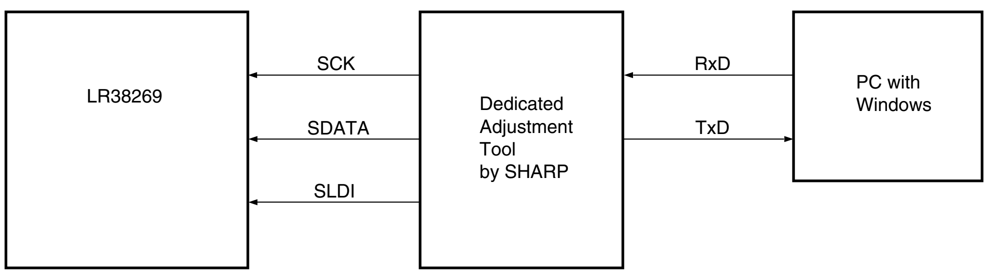
Data Interface

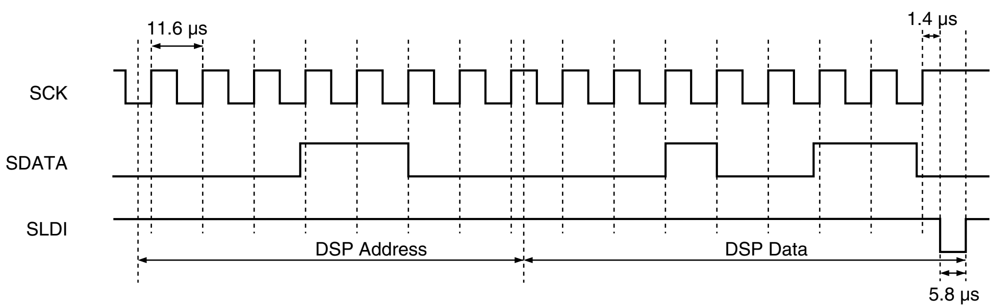
(1) Format of data transfers

- Format of transfers : Asynchronous (Based on RS-232C standard)
- Bit rate : 9 600 bps
- Data length : 8 bits
- Parity check : 1 even parity bit
- Start bit : 1 bit
- Stop bit : 1 bit
- Signal voltage level (CMOS)



- System configuration





AUTOMATIC CAMERA FUNCTION CONTROL

Automatic Electronic Exposure Control

Electronic shutter speed is controlled so that the exposure control data approach to the data of address 04h.

Under BLC mode, the data of address 07h is available instead of address 04h.

After the exposure control data is less than the data of address 05h, an electronic shutter speed is hold. And then AGC gain is controlled so that the exposure control data will be less than the data of address 06h.

In the case of coming more than the data of address 07h, exposure control starts again.

Electronic Shutter Speed Setting

By either hardware or coefficient data, electronic shutter speed below is selectable.

EEMDS	$EEMD_1$	$EEMD_2$	$EEMD_3$	ELECTRONIC SHUTTER SPEED	
				NTSC	PAL
0	0	0	0	1/60 s	1/50 s
0	0	0	1	1/100 s	1/120 s
0	0	1	0	1/250 s	1/250 s
0	0	1	1	1/500 s	1/500 s
0	1	0	0	1/1 000 s	1/1 000 s
0	1	0	1	1/2 000 s	1/2 000 s
0	1	1	0	1/5 000 s	1/5 000 s
0	1	1	1	1/10 000 s	1/10 000 s
1	0	0	0	1/20 000 s	1/20 000 s
1	0	0	1	1/50 000 s	1/50 000 s
1	0	1	0	1/100 000 s	1/100 000 s
1	0	1	1	1/30 s	1/25 s
1	1	0	0	1/15 s	1/12.5 s
1	1	0	1	1/7.5 s	1/6.25 s
1	1	1	0	AUTO 1/60 to 1/100 000 s	AUTO 1/50 to 1/100 000 s
1	1	1	1	AUTO 1/60 to 1/100 000 s	AUTO 1/50 to 1/100 000 s

Slower shutter speed less than 1/60 s (1/50 s of PAL) can make images whose interval is every two fields, every four fields, etc..

VD pulse is also converted to the same frequency as the output image rate.

Electronic exposure control data comes from below equation using averaged luminance levels of 64 areas in one image, made by DSP.

Electronic exposure control data =
[{Weighted data 1 ① x (64 – address 10h)
+ weighted data 2 ② x address 10h} ÷ 64
x (256 – address 14h – address 15h)
+ top level ③ x address 14h
+ bottom level ④ x address 15h] ÷ 256

Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}	Y_{16}	Y_{17}	Y_{18}
Y_{21}	Y_{22}	Y_{23}	Y_{24}	Y_{25}	Y_{26}	Y_{27}	Y_{28}
Y_{31}	Y_{32}	Y_{33}	Y_{34}	Y_{35}	Y_{36}	Y_{37}	Y_{38}
Y_{41}	Y_{42}	Y_{43}	Y_{44}	Y_{45}	Y_{46}	Y_{47}	Y_{48}
Y_{51}	Y_{52}	Y_{53}	Y_{54}	Y_{55}	Y_{56}	Y_{57}	Y_{58}
Y_{61}	Y_{62}	Y_{63}	Y_{64}	Y_{65}	Y_{66}	Y_{67}	Y_{68}
Y_{71}	Y_{72}	Y_{73}	Y_{74}	Y_{75}	Y_{76}	Y_{77}	Y_{78}
Y_{81}	Y_{82}	Y_{83}	Y_{84}	Y_{85}	Y_{86}	Y_{87}	Y_{88}

① Weighted data 1
This comes from the following equation weighting in horizontal.
Weighting factors are the data from address 08h to address 0Fh.

{(Y_{11} + Y_{12} ··· + Y_{18}) ÷ 8 x address 08h
+ (Y_{21} + Y_{22} ··· + Y_{28}) ÷ 8 x address 09h
:
+ (Y_{81} + Y_{82} ··· + Y_{88}) ÷ 8 x address 0Fh} ÷ 256
= Weighted data 1

The sum from address 08h to address 0Fh shall be 256.

② Weighted data 2
Weighting area can be set by the data of address 11h and address 12h. (see **"NOTES" in Gamma Characteristic Option**)
This comes from the following equation weighting in selected areas.
(Y_{33} + Y_{34} ··· + Y_{66})/number of areas to be selected
= Weighted data 2

③ Top level : The highest luminance data in one image by averaging either 4 pixels or 8 pixels in horizontal.

④ Bottom level : The lowest luminance data in one image by averaging either 4 pixels or 8 pixels in horizontal.

Auto White Balance Control

White balance control data less than the data of address 51h and address 52h stops AWB.
White balance control data less than the data of address 4Fh and address 50h makes AWB active so that white balance control data is less than the data of address 51h and address 52h.
In the case of larger than the data of address 4Fh and address 50h, AWB will be active again.

White balance data comes from the following equation using averaged I and Q data of 16 areas in one image.

I_{11}	I_{12}	I_{13}	I_{14}
I_{21}	I_{22}	I_{23}	I_{24}
I_{31}	I_{32}	I_{33}	I_{34}
I_{41}	I_{42}	I_{43}	I_{44}

Q_{11}	Q_{12}	Q_{13}	Q_{14}
Q_{21}	Q_{22}	Q_{23}	Q_{24}
Q_{31}	Q_{32}	Q_{33}	Q_{34}
Q_{41}	Q_{42}	Q_{43}	Q_{44}

White balance data =
{Weighted data 3 ① x (64 – address 44h)
+ weighted data 4 ② x address 44h} ÷ 64

① Weighted data 3
I (or Q) data comes from the following equation using the weighting data from address 40h to address 43h.

$\{(I_{11} + I_{12} \cdots + I_{14}) \div 4$ x address 40h
$+ (I_{21} + I_{22} \cdots + I_{24}) \div 4$ x address 41h
:
$+ (I_{41} + I_{42} \cdots + I_{44}) \div 4$ x address 43h} ÷ 256
= Weighted data 3

The sum from the data of address 40h to the data of address 43h shall be 256.

② Weighted data 4
Weighting area can be selected by address 45h. (see **"NOTES" in Gamma Characteristic Option**.) Weighted data comes from averaged data in selected area.

③ White balance area setting
The sum of I and Q can be regulated by the luminance level and the color level.
Setting target zone : address 47h to address 4Ah
White balance data less than the data of address 51h and address 52h changes the target zone of auto white balance to the zone by the data from address 4Bh to 4Eh.

Above regulation comes from the following equation along the luminance level.

Setting available luminance level range :
Highest luminance level limiter =
address 3Bh + [{address 3Eh x H peak level + (256 – address 3Eh) x exposure control data} ÷ 256 – address 3Dh] x address 3Fh

Lowest luminance level limiter =
address 3Ch + [{address 3Eh x H peak level + (256 – address 3Eh) x exposure control data} ÷ 256 – address 3Dh] x address 3Fh

Auto Color Matrix Compensation

Color matrix compensation can be done by
R – Y = R – Y ± (Data 1 x B – Y)
B – Y = B – Y ± (Data 2 x R – Y)

Above data comes from below equation along the variation of color temperature.

Data 2 =
address 55h + {(working R white balance data – address 25h + (address 26h – working B white balance data)} ÷ 32 x address 53h ÷ 8

Data 2 =
address 56h + {(working R white balance data – address 25h) + (address 26h – working B white balance data)} ÷ 32 x address 54h ÷ 8

Auto Color Level Compensation

Color level can be auto-controlled by the following equation along the variation of color temperature.

B – Y level =
address 30h + {(working R white balance data – address 25h) x address 22h + (address 26h – working B white balance data) x address 23h} ÷ 32 x address 2Eh ÷ 8

R – Y level =
address 31h + {(working R white balance data – address 25h) x address 22h + (address 26h – working B white balance data) x address 23h} ÷ 32 x address 2Fh ÷ 8

Color Level Suppression Under Lower Illuminance

Working AGC gain can control both R – Y level and B – Y level by the following equation.

R – Y level =
address 31h x {16 – (working AGC gain – address 5Ah) x address 5Bh ÷ 16} ÷ 16
B – Y level =
address 30h x {16 – (working AGC gain – address 5Ah) x address 5Bh ÷ 16} ÷ 16

{16 – (working AGC gain – address 5Ah) x address 5Bh ÷ 16} ≤ 16

When (working AGC gain – address 5Ah) ≤ 0, ( ) = 0.

Aperture Level Suppression Under Illuminance

Working AGC gain can control both the horizontal aperture level and the vertical aperture level by the following equation.

Horizontal aperture level =
address 68h x {16 – (working AGC gain – address 63h) x address 64h ÷ 16} ÷ 16

Vertical aperture level =
address 6Ah x {16 – (working AGC gain – address 63h) x address 64h ÷ 16} ÷ 16

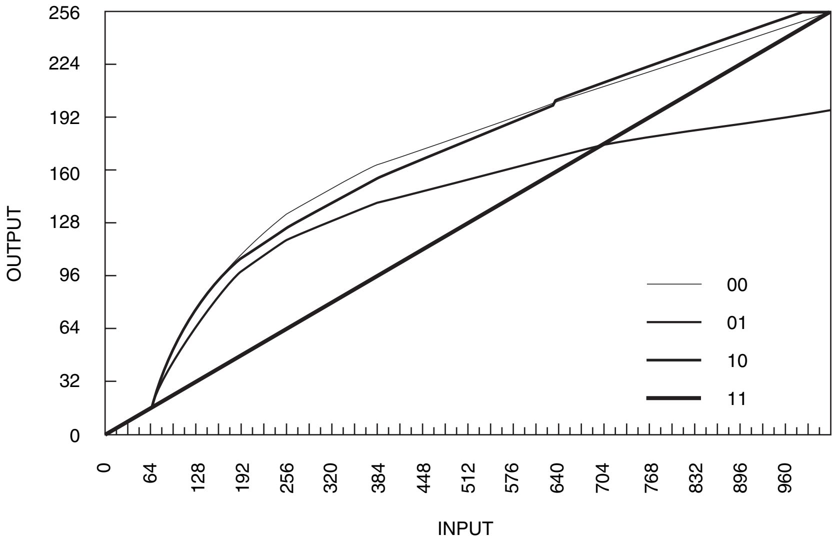
{16 – (working AGC gain – address 63h) x address 64h ÷ 16} ≤ 16

When (working AGC gain – address 63h) ≤ 0, ( ) = 0.

Gamma Characteristic Option

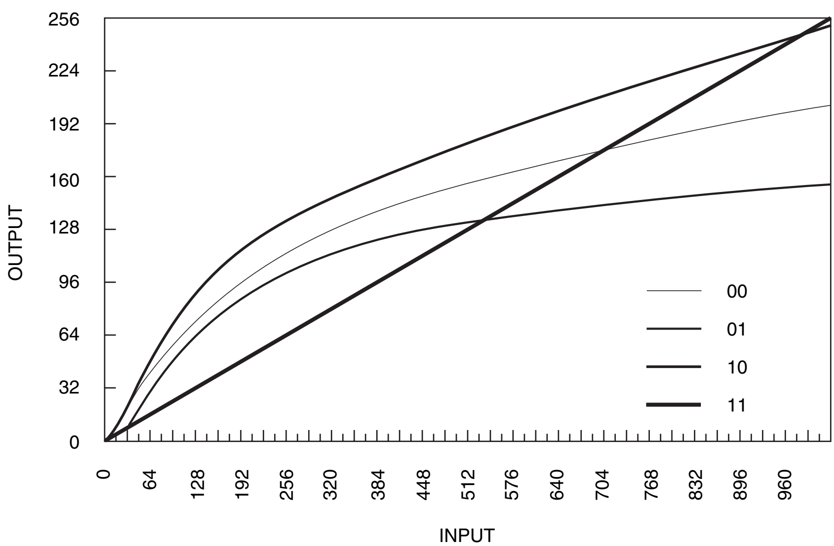
(1) Luminance Signal Gamma Option

Bit 7 and bit 6 of address 02h can select one out of 4 responses below.



(2) Color Signal Gamma Option

Bit 5 and bit 4 of address 02h can select one out of 4 responses below.



NOTES :

- Weighting position of auto electronic exposure control (address 11h)

00h	08h	·	30h	38h
01h	09h	·	31h	39h
·	·	·	·	·
06h	0Eh	·	36h	3Eh
07h	0Fh	·	37h	3Fh

- Weighting area of auto electronic exposure control (address 12h)

00h	08h	·	30h	38h
01h	09h	·	31h	39h
·	·	·	·	·
06h	0Eh	·	36h	3Eh
07h	0Fh	·	37h	3Fh

- Weighting position of auto white balance control (address 45h)

00h	04h	08h	0Ch
01h	05h	09h	0Dh
02h	06h	0Ah	0Eh
03h	07h	0Bh	0Fh

- Weighting area of auto white balance control (address 45h)

00h	04h	08h	0Ch
01h	05h	09h	0Dh
02h	06h	0Ah	0Eh
03h	07h	0Bh	0Fh

PACKAGE

(Unit : mm)

80 LQFP (LQFP080-P-1212)