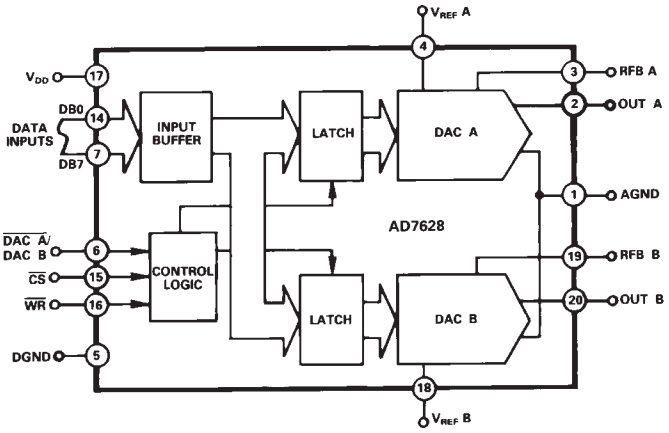
CMOS Dual 8-Bit Buffered Multiplying DAC

AD7628

FEATURES
On-Chip Latches for Both DACs
+12 V to +15 V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible from +12 V to +15 V
Latch Free (Protection Schottkys not Required)

APPLICATIONS
Disk Drives
Programmable Filters
X-Y Graphics
Gain/Attenuation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7628 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in small 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7628's load cycle is similar to the write cycle of a random access memory, and the device is bus compatible with most 8-bit microprocessors, including 6502, 6809, 8085, Z80.

The device operates from a +12 V to +15 V power supply and is TTL-compatible over this range. Power dissipation is a low 20 mW.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7628 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7628's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7628 to be packaged in a small 20-pin 0.3" wide DIP, 20-pin SOIC, 20-terminal PLCC and 20-terminal LCC.
3. TTL-Compatibility: All digital inputs are TTL-compatible over a +12 V to +15 V power supply range.

REV. A

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AD7628–SPECIFICATIONS (V_{DD} = +10.8 V to +15.75 V, V_{REF} A = V_{REF} B = +10 V; OUT A = OUT B = 0 V unless otherwise noted)

Parameter	T_A = +25°C[1]	T_A = –40°C to +85°C	T_A = –55°C to +125°C[1]	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]					
Resolution	8	8	8	Bits	
Relative Accuracy	±1/2	±1/2	±1/2	LSB max	This is an Endpoint Linearity Specification
Differential Nonlinearity	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	±2	±3	±3	LSB max	Measured Using Internal RFB A and RFB B. Both DAC Latches Loaded with 11111111. Gain Error is Adjustable Using Circuits of Figures 4 and 5.
Gain Temperature Coefficient[3]					
ΔGain/ΔTemperature		±0.0035	±0.0035	%/°C max	
Output Leakage Current					
OUT A (Pin 2)	±50	±200	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	±50	±200	±200	nA max	
Input Resistance (V_{REF}A, V_{REF}B)	8	8	8	kΩ min	Input Resistance TC = –300 ppm/°C, Typical
	15	15	15	kΩ max	Input Resistance is 11 kΩ
V_{REF}A/V_{REF}B Input Resistance Match	±1	±1	±1	% max	
DIGITAL INPUTS[4]					
Input High Voltage (V_{IH})	2.4	2.4	2.4	V min	
Input Low Voltage (V_{IL})	0.8	0.8	0.8	V max	
Input Current (I_{IN})	±1	±10	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance					
DB0–DB7	10	10	10	pF max	
$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB	15	15	15	pF max	
SWITCHING CHARACTERISTICS[3] See Timing Diagram					
Chip Select to Write Set Up Time (t_{CS})	160	160	210	ns min	
Chip Select to Write Hold Time (t_{CH})	10	10	10	ns min	
DAC Select to Write Set Up Time (t_{AS})	160	160	210	ns min	
DAC Select to Write Hold Time (t_{AH})	10	10	10	ns min	
Data Valid to Write Set Up Time (t_{DS})	160	160	210	ns min	
Data Valid to Write Hold Time (t_{DH})	10	10	10	ns min	
Write Pulse Width (t_{WR})	150	170	210	ns min	
POWER SUPPLY					See Figure 3
I_{DD}, K Grade	2	2		mA	All Digital Inputs V_{IL} or V_{IH}
B, T Grades	2	2.5	2.5	mA	All Digital Inputs V_{IL} or V_{IH}
All Grades	100	500	500	μA	All Digital Inputs 0 V or V_{DD}

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS These characteristics are included for Design Guidance only and are not subject to test. V_{DD} = +10.8 V to +15.75 V. (Measured Using Recommended PC Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	T_A = +25°C[1]	T_A = –40°C to +85°C[1]	T_A = –55°C to +125°C[1]	Units	Test Conditions/Comments
DC SUPPLY REJECTION ($\Delta GAIN/\Delta V_{DD}$)	0.01	0.02	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME	350	400	400	ns max	To 1/2 LSB OutA/OutB Load = 100 Ω. $\overline{WR}$ = $\overline{CS}$ = 0 V. DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V
DIGITAL-TO-ANALOG GLITCH IMPULSE	330			nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE					
C_{OUT}A	25	25	25	pF max	DAC Latches Loaded with 00000000
C_{OUT}B	25	25	25	pF max	
C_{OUT}A	60	60	60	pF max	DAC Latches Loaded with 11111111
C_{OUT}B	60	60	60	pF max	
AC FEEDTHROUGH					
V_{REF}A to OUT A	–70	–65	–65	dB max	V_{REF}A, V_{REF}B = 20 V p-p Sine Wave
V_{REF}B to OUT B	–70	–65	–65	dB max	@ 10 kHz
CHANNEL-TO-CHANNEL ISOLATION					Both DAC Latches Loaded with 11111111.
V_{REF}A to OUT B	–80			dB typ	V_{REF}A = 20 V p-p Sine Wave @ 10 kHz V_{REF}B = 0 V See Figure 6.
V_{REF}B to OUTA	–80			dB typ	V_{REF}B = 20 V p-p Sine Wave @ 10 kHz V_{REF}A = 0 V See Figure 6.
DIGITAL CROSSTALK	60			nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	–85			dB typ	V_{IN} = 6 V rms @ 1 kHz

NOTES
[1]Temperature Ranges are K Version; –40°C to +85°C; B Version; –40°C to +85°C; T Version; –55°C to +125°C.
[2]Specification applies to both DACs in AD7628.
[3]Guaranteed by design but not production tested.
[4]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1 nA.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... 0 V, +17 V
V_{DD} to DGND ..... 0 V, +17 V
AGND to DGND ..... V_{DD} + 0.3 V
DGND to AGND ..... V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V, V_{DD} + 0.3 V
V_{PIN2}, V_{PIN20} to AGND ..... –0.3 V, V_{DD} + 0.3 V
V_{REF} A, V_{REF} B to AGND ..... ±25 V
V_{RFB} A, V_{RFB} B to AGND ..... ±25 V
Power Dissipation (Any Package) to +75°C ..... 450 mW
Derates above +75°C by ..... 6 mW/°C
Operating Temperature Range
Commercial (K) Grades ..... –40°C to +85°C
Industrial (B) Grades ..... –40°C to +85°C
Extended (T) Grades ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Gain Error	Package Option[2]
AD7628KN	–40°C to +85°C	±1/2 LSB	±2 LSB	N-20
AD7628KP	–40°C to +85°C	±1/2 LSB	±2 LSB	P-20A
AD7628KR	–40°C to +85°C	±1/2 LSB	±2 LSB	R-20
AD7628BQ	–40°C to +85°C	±1/2 LSB	±2 LSB	Q-20
AD7628TQ	–55°C to +125°C	±1/2 LSB	±2 LSB	Q-20
AD7628TE	–55°C to +125°C	±1/2 LSB	±2 LSB	E-20A

NOTES
[1]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

TERMINOLOGY

Relative Accuracy:
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full-scale, and is normally expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity:
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

Gain Error:
Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC latches after offset error has been adjusted out. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance:
Capacitance from OUT A or OUT B to AGND.

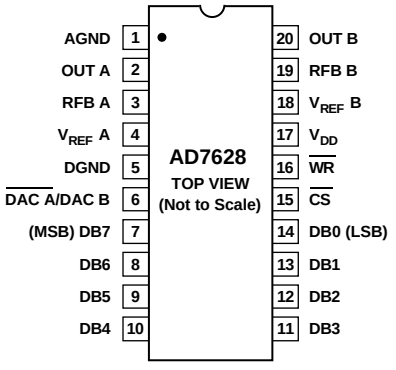
Digital-to-Analog Glitch Impulse:
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs, depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{REF} A, V_{REF} B = AGND.

Channel-to-Channel Isolation:
The proportion of input signal from one DAC's reference input that appears at the output of the other DAC, expressed as a ratio in dB.

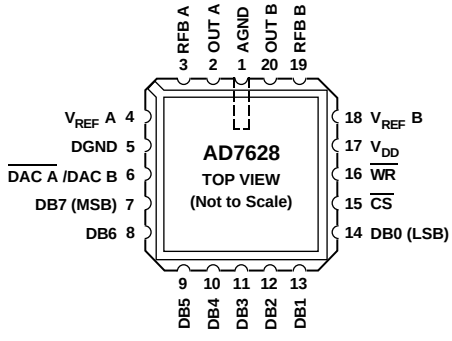
Digital Crosstalk:
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

PIN CONFIGURATIONS

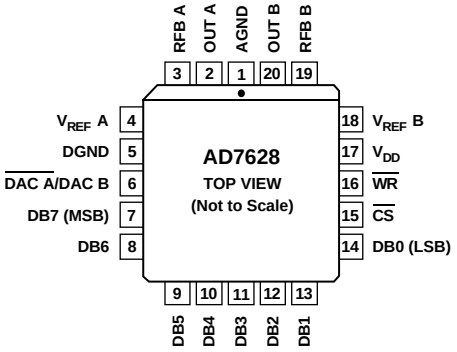
DIP, SOIC



LCCC



PLCC



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7628 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

INTERFACE LOGIC INFORMATION

DAC Selection

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode

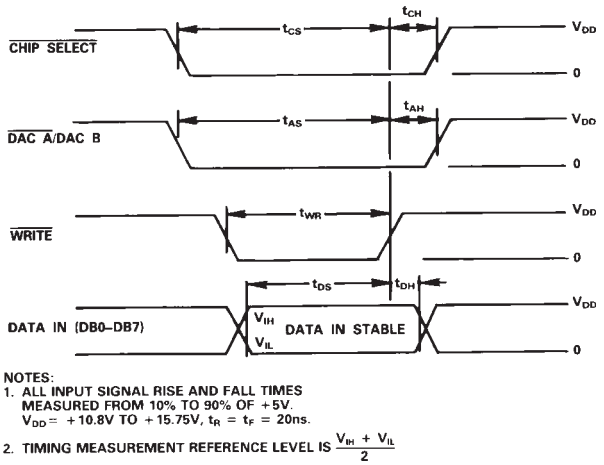
The selected DAC latch retains the data that was present on DB0–DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Mode Selection Table

$\overline{\text{DAC A}}$/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State, H = High State, X = Don't Care

WRITE CYCLE TIMING DIAGRAM



CIRCUIT INFORMATION—D/A SECTION

The AD7628 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used; that is, binary weighted currents are switched between the DAC output and AGND, thus maintaining fixed currents in each ladder leg independent of switch state.

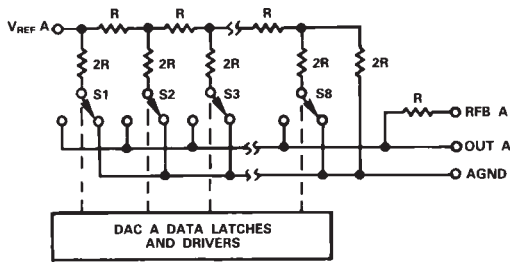


Figure 1. Simplified Functional Circuit for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the AD7628's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor Ro, as shown in Figure 2, is the equivalent output resistance of the device, which varies with input code (excluding all 0s code) from 0.8R to 2R. R is typically 11 kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50 pF to 120 pF, depending on the digital input. $g(V_{REF}\ A, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

For further information on CMOS multiplying D/A converters, refer to "CMOS DAC Application Guide, 2ND Edition" available from Analog Devices, Publication Number G872a–15–4/86.

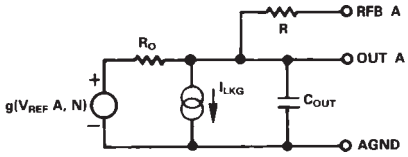


Figure 2. Equivalent Analog Output Circuit of DAC A

CIRCUIT INFORMATION–DIGITAL SECTION

The input buffers are simple CMOS level-shifters designed so that when the AD7628 is operated with V_{DD} from 10.8 V to 15.75 V, the buffer converts TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When V_{IN} is in the region of 1.0 volt to 2.0 volts, the input buffers operate in their linear region and pass a quiescent current (see Figure 3). To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as practicably possible.

The AD7628 may be operated with any supply voltage in the range $10.8 \le V_{DD} \le 15.75$ volts.

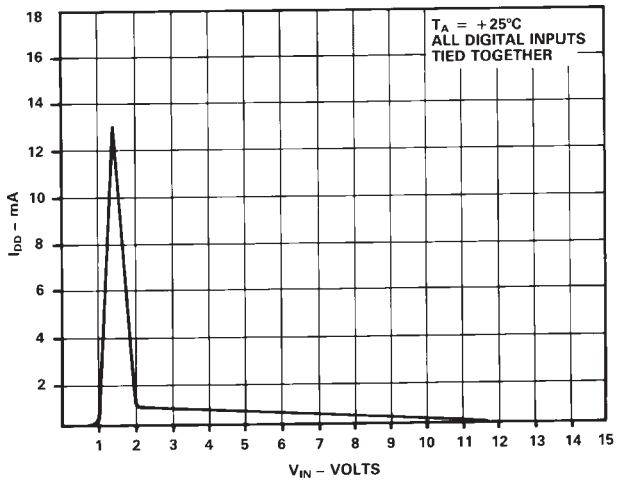
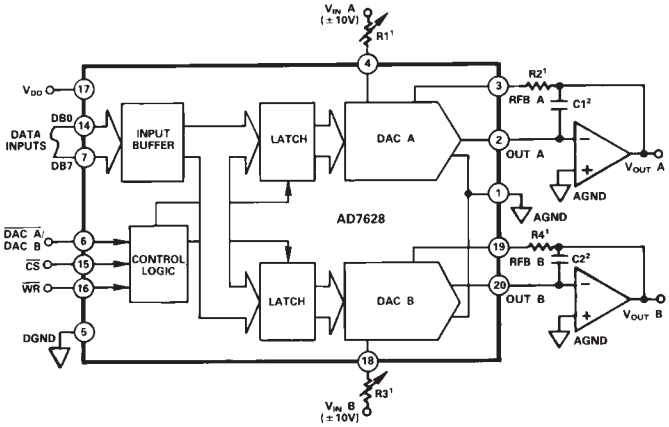
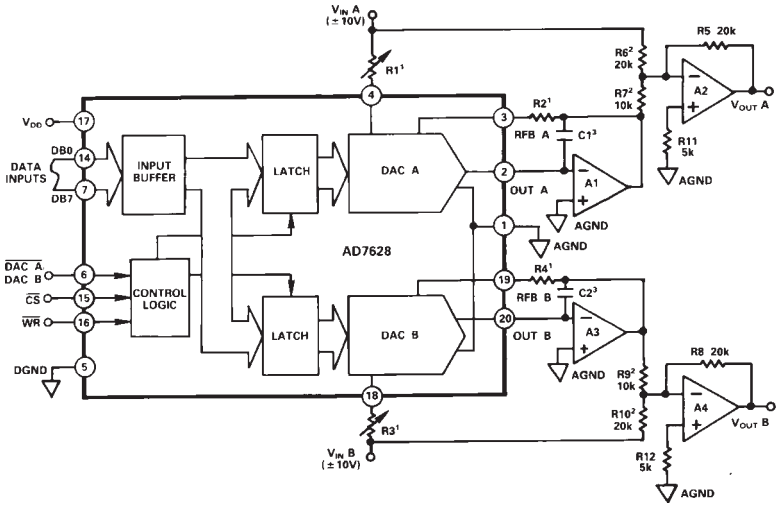


Figure 3. Typical Plot of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN} to V_{DD} = +15 V



NOTES:
¹R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
²C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table I.



NOTES:
¹R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES. ADJUST R1 FOR V_{OUT} A = 0V WITH CODE 10000000 IN DAC A LATCH. ADJUST R3 FOR V_{OUT} B = 0V WITH CODE 10000000 IN DAC B LATCH.
²MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
³C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BY REQUIRED IF A1/A3 IS A HIGH-SPEED AMPLIFIER.

Figure 5. Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table II.

Table I. Unipolar Binary Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{256}\right)=-\frac{V_{IN}}{2}$
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{0}{256}\right)=0$

NOTE: 1 LSB = $(2^{-8})(V_{IN}) = \frac{1}{256}\left(V_{IN}\right)$

Table II. Bipolar (Offset Binary) Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{128}\right)$

NOTE: 1 LSB = $(2^{-7})(V_{IN}) = \frac{1}{128}\left(V_{IN}\right)$

Table III. Recommended Trim Resistor Values

Trim Resistor	K/B/T
R1; R3	500
R2; R4	150

APPLICATIONS INFORMATION

Application Hints

To ensure system performance consistent with AD7628 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the AD7628 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7628. In more omplex systems where the AGND–DGND intertie is on the backplane, it is recommended that diodes be connected in inverse parallel between the AD7628 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which, in turn, causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output that depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.
3. HIGH FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

DYNAMIC PERFORMANCE

The dynamic performance of the two DACs in the AD7628 will depend on the gain and phase characteristics of the output amplifiers, together with the optimum choice of the PC board layout and decoupling components. Figure 6 shows the relationship between input frequency and channel-to-channel isolation.

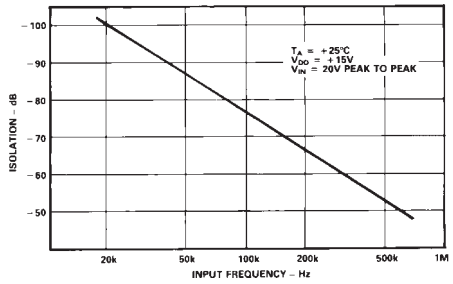


Figure 6. Channel-to-Channel Isolation

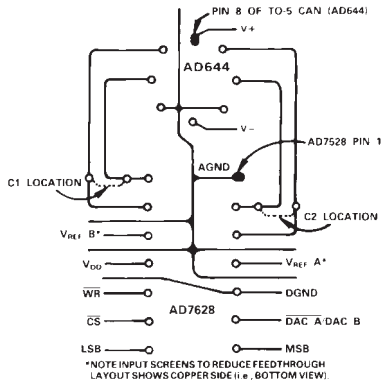


Figure 7. Suggested PC Board Layout for AD7628 with AD644 Dual Op Amp

Figure 7 shows a printed circuit layout for the AD7628 and the AD644 dual op amp, which minimizes feedthrough and crosstalk.

SINGLE SUPPLY APPLICATIONS

The AD7628 DAC R-2R ladder termination resistors are connected to AGND within the device. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between DGND and V_{DD}. Figure 8 shows a circuit that provides two +5 V to +8 V analog outputs by biasing AGND +5 V up from DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the constant and matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1, and R1 is adjusted until the V_{REF} A and V_{REF} B inputs are at +2 V. The two analog output voltages range from +5 V to +8 V for DAC codes 00000000 to 11111111.

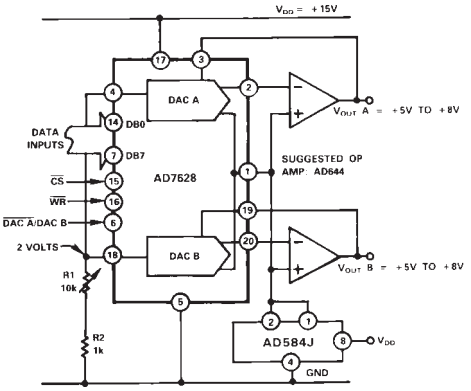


Figure 8. AD7628 Single Supply Operation

Figure 9 shows DAC A of the AD7628 connected in a positive reference, voltage switching mode. This configuration is useful because V_{OUT} is the same polarity as V_{IN}, allowing single supply operation. However, to retain specified linearity, V_{IN} must be in the range 0 V to +2.5 V and the output buffered or loaded with a high impedance (see Figure 10). Note that the input voltage is connected to the DAC OUT A, and the output voltage is taken from the DAC V_{REF} A pin.

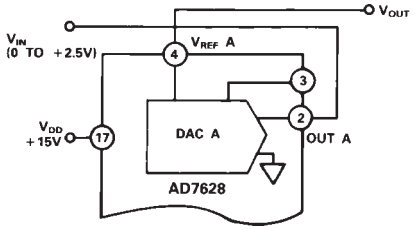


Figure 9. AD7628 Single Supply, Voltage Switching Mode

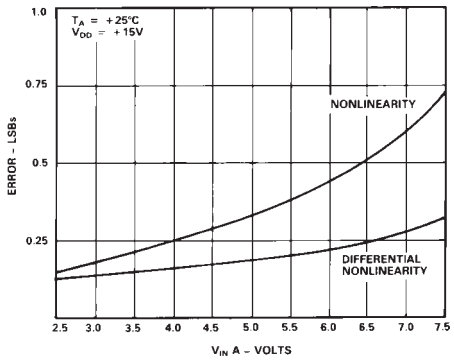


Figure 10. Typical AD7628 Performance in Single Supply Voltage Switching Mode

MICROPROCESSOR INTERFACE

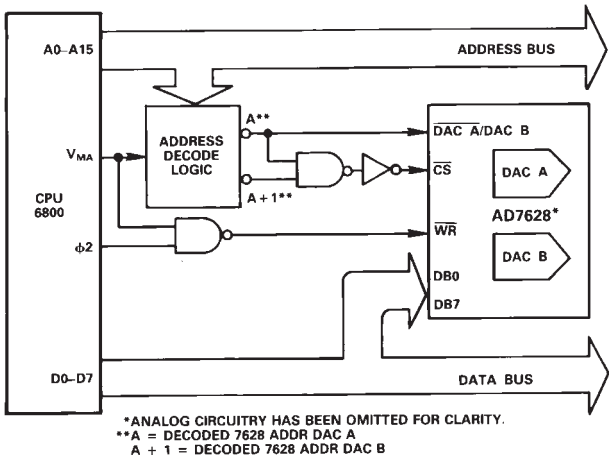


Figure 11. AD7628 Dual DAC to 6800 CPU Interface

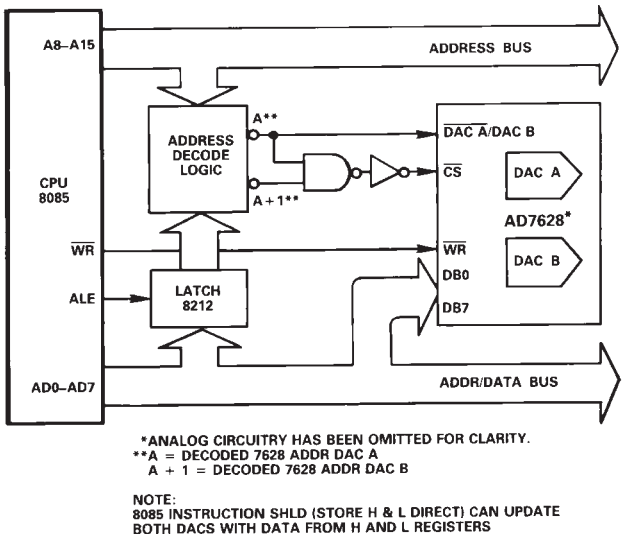


Figure 12. AD7628 Dual DAC to 8085 CPU Interface

PROGRAMMABLE WINDOW COMPARATOR

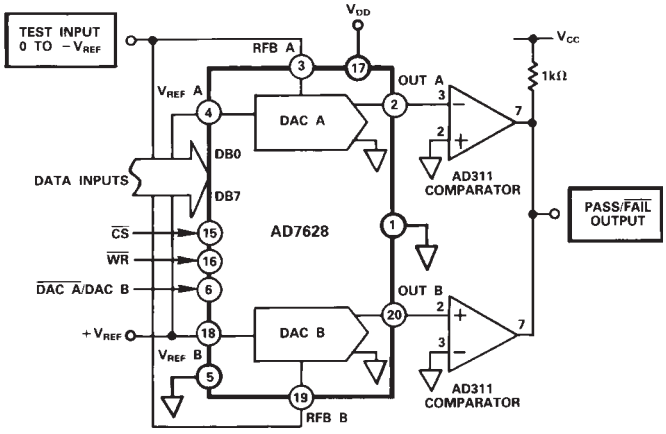


Figure 13. Digitally Programmable Window Comparator (Upper and Lower Limit Detector)

In the circuit of Figure 13, the AD7628 is used to implement a programmable window comparator. DACs A and B are loaded with the required upper and lower voltage limits for the test, respectively. If the test input is not within the programmed limits, the pass/fail output will indicate a fail (logic zero).

PROGRAMMABLE STATE VARIABLE FILTER

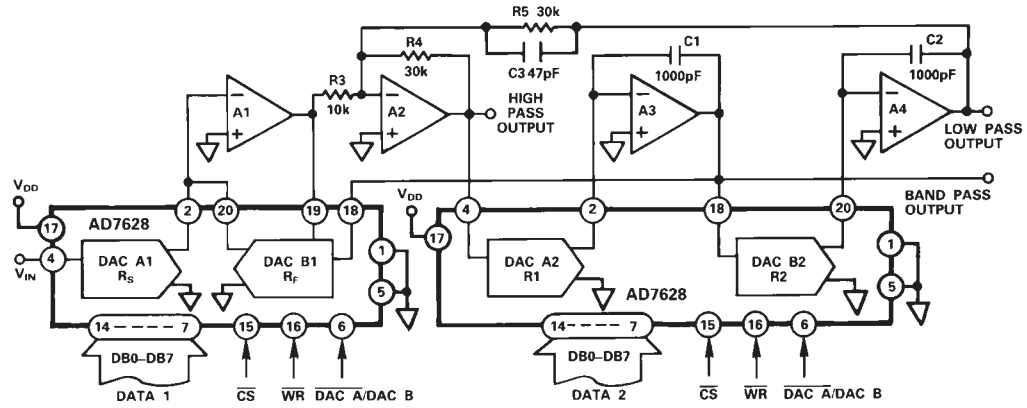


Figure 14. Digitally Controlled State Variable Filter

CIRCUIT EQUATIONS

$C_1 = C_2$, $R_1 = R_2$, $R_4 = R_5$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_O = -\frac{R_F}{R_S}$$

NOTE
DAC equivalent resistance equals

$$\frac{256 \times (DAC\ Ladder\ resistance)}{DAC\ Digital\ Code}$$

In this state, variable or universal filter configuration (Figure 14) for DACs A1 and B1 control the gain and Q of the filter characteristic, while DACs A2 and B2 control the cutoff frequency, f_C. DACs A2 and B2 must track accurately for the simple expression for f_C to hold. This is readily accomplished by the AD7628. Op amps are 2 × AD644. C3 compensates for the effects of op amp gain-bandwidth limitations.

The filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required, e.g., equalizer, tone controls, etc.

Programmable range for component values shown is f_C = 0 kHz to 15 kHz and Q = 0.3 to 4.5.

DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

In this configuration, the AD7628 functions as a 2-channel digitally controlled attenuator; ideal for stereo audio and telephone signal level control applications. Table IV gives input codes vs. attenuation for a 0 dB to 15.5 dB range.

$$\text{Input Code} = 256 \times 10 \exp\left(-\frac{\text{Attenuation, dB}}{20}\right)$$

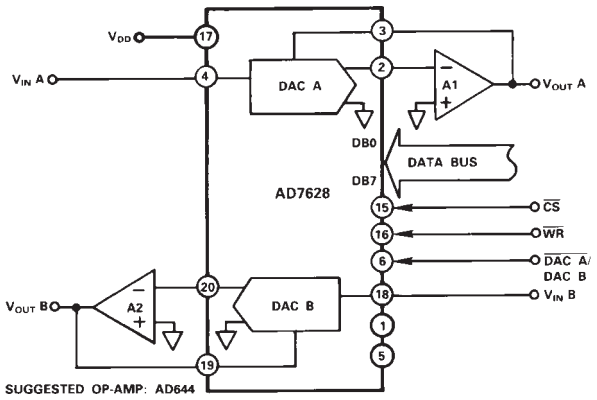


Figure 15. Digitally Controlled Dual Telephone Attenuator

Table IV. Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 15

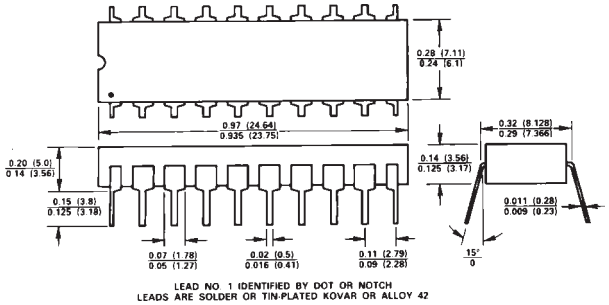
Attn. dB	DAC Input Code	Code in Decimal	Attn. dB	DAC Input Code	Code in Decimal
0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 0 0 0 0	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1	51
6.5	0 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

MECHANICAL INFORMATION

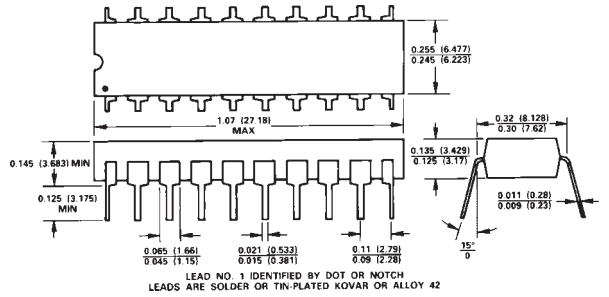
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

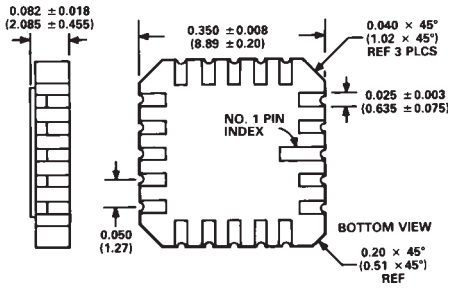
20-Pin Cerdip (Q Suffix)



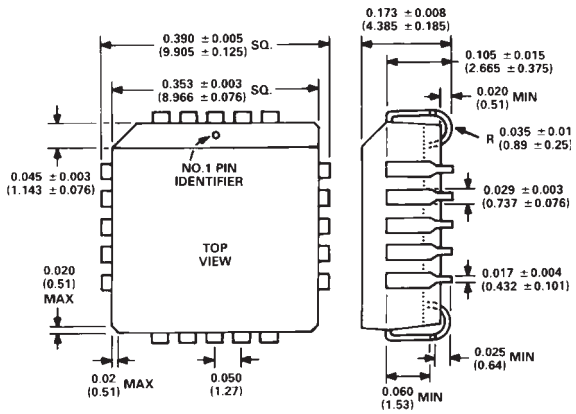
20-Pin Plastic DIP (N Suffix)



20-Terminal Leadless Chip Carrier (E Suffix)



20-Terminal Plastic Leaded Chip Carrier (P Suffix)



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