ASM1233D, ASM1233D-L, ASM1233M

Low Power, 5 V/3.3 V, μP Reset, Active LOW, Open-Drain Output

Description

The ASM1233D−L/1233D/1233M are voltage supervisors with low−power, 5/3.3 V μP Reset, with an active LOW, open−drain output. Maximum supply current over temperature is 15 μA for 3.3 V devices and 20 μA for 5 V devices.

The ASM1233D−L/1233D/1233M generates an active LOW reset signal whenever the monitored supply is out of tolerance. A precision reference and comparator circuit monitors power supply (V_{CC}) level. The tolerances are 5%, 10% and 15%. When an out−of−tolerance condition is detected, an internal power−fail signal is generated which forces an active LOW reset signal. After V_{CC} returns to an in−tolerance condition, the reset signal remains active for 350 ms to allow the power supply and system microprocessor to stabilize.

The ASM1233D−L/1233D/1233M is designed with an open drain output stage and operates over the extended industrial temperature range. These devices are available in compact SOT−223, SO−8 and TO−92 packages.

Other low power products in this family include ASM1810/11/12/15/16/17.

Features

- Low Supply Current
- 15 μA Maximum (≤ 3.6 V), 20 μA Maximum (5.5 V)
- Automatically Restarts a Microprocessor after Power Failure
- 350 ms Reset Delay after V_{CC} Returns to an In−tolerance Condition
- Active LOW Power−up Reset, 5 kΩ Internal Pull−up
- Precision Temperature−compensated Voltage Reference and Comparator
- Eliminates External Components
- Low−cost SOT−223/SO−8/TO−92 Packages
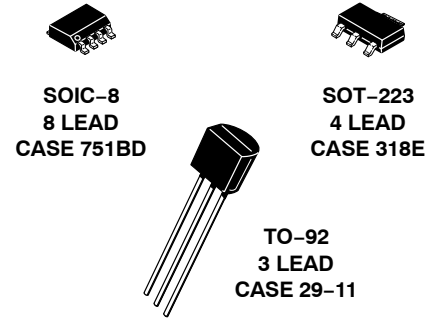- Operating Temperature: −40°C to +85°C

Applications

- Set−top Boxes
- Cellular Phones
- PDAs
- Energy Management Systems
- Embedded Control Systems
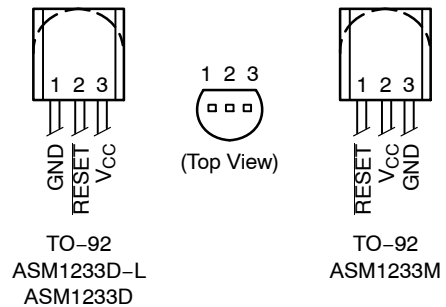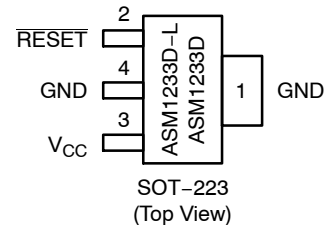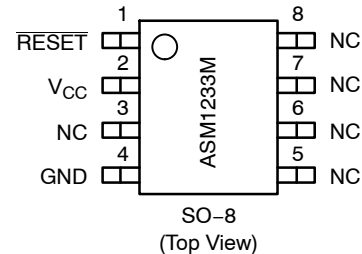- Printers
- Single Board Computers

SOIC−8
8 LEAD
CASE 751BD

SOT−223
4 LEAD
CASE 318E

TO−92
3 LEAD
CASE 29−11

PIN CONFIGURATIONS

ASM1233M

1 RESET	8 NC
2 V_{CC}	7 NC
3 NC	6 NC
4 GND	5 NC

SO−8
(Top View)

ASM1233D−L / ASM1233D

2 RESET
4 GND
3 V_{CC}
1 GND

SOT−223
(Top View)

1 2 3
GND RESET V_{CC}

(Top View)

1 2 3
RESET V_{CC} GND

TO−92
ASM1233D−L
ASM1233D

TO−92
ASM1233M

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.
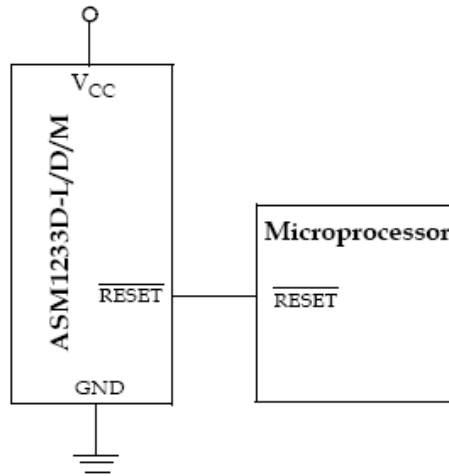
ASM1233D, ASM1233D−L, ASM1233M
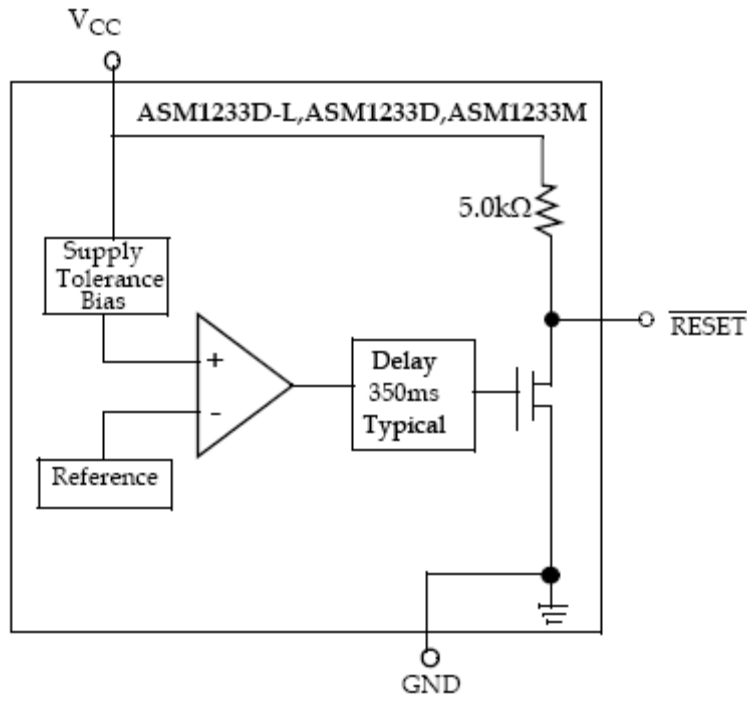

Figure 1. Typical Operating Circuit

Figure 2. Block Diagram

ASM1233D, ASM1233D−L, ASM1233M

Table 1. PIN DESCRIPTION

Pin #				Pin Name	Description
TO−92 ASM1233D−L ASM1233D	TO−92 ASM1233M	SO−8	SOT−223		
1	3	4	1,4	GND	Ground.
2	1	1	2	$\overline{\text{RESET}}$	Active LOW reset output.
3	2	2	3	V_{CC}	Power supply input.
		3, 5, 6, 7 & 8		NC	No connection.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	Unit
Voltage on V_{CC} (Note 1)		−0.5	7	V
Voltage on $\overline{\text{RESET}}$ (Note 1)		−0.5	V_{CC} + 0.5	V
Operating Temperature Range		−40	+85	°C
Soldering Temperature (for 10 sec)			+260	°C
Storage Temperature		−55	+125	°C
ESD rating	HBM		2	KV
	MM		200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Voltages are measured with respect to ground.

Table 3. DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5 V ±10% and specifications are over the operating temperature range of −40°C to +85°C. All voltages are referenced to ground.) (Note 2)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		1.2		5.5	V
Output Voltage	V_{OL}	$\overline{RESET}$ asserted			0.4	V
	V_{OH}	I_{OUT} < 500 μA	V_{CC}−0.5 V	V_{CC}−0.1 V		
Output Current	I_{OL}	Output = 0.4 V	8			mA
Operating Current	I_{CC}	V_{CC} < 5.5 V, $\overline{RESET}$ output open		8	20	μA
		V_{CC} ≤ 3.6 V, $\overline{RESET}$ output open		6	15	
V_{CC} Trip Point	V_{CCTP}	ASM1233D−LZ−5	2.98	3.06	3.15	V
		ASM1233D−LZ−10	2.8	2.88	2.97	
		ASM1233D−LZ−15	2.64	2.72	2.8	
		ASM1233DZ−5	4.5	4.625	4.74	
		ASM1233DZ−10	4.25	4.375	4.49	
		ASM1233DZ−15	4.0	4.125	4.24	
		ASM1233M−5	4.25	4.375	4.49	
		ASM1233M−55	4.5	4.625	4.75	
		ASM1233M−3	2.64	2.72	2.8	
Voltage High Trip Level	V_{HTL}	ASM1233D, ASM1233MS−5, ASM1233MS−55			4.75	V
		ASM1233MS−3			3.14	
		ASM1233D−L			3.06	
Voltage Low Trip Level	V_{LTL}	ASM1233D, ASM1233MS−5, ASM1233MS−55			4.00	V
		ASM1233MS−3			2.48	
		ASM1233D−L			2.3	
Internal Pull−up Resistor	R_P		3.5	5.0	7.5	kΩ
Output Capacitance	C_{OUT}				10	pF
V_{CC} Detect to $\overline{RESET}$ Low	t_{RPD}			2	10	μs
V_{CC} Detect to $\overline{RESET}$ High	t_{RPU}	ASM1233D−L, ASM1233M	200	350	500	ms
		ASM1233D	250	350	450	
V_{CC} Slew Rate (V_{HTL} − V_{LTL})	t_F		300			μs
V_{CC} Slew Rate (V_{LTL} − V_{HTL})	t_R		0			ns

2. A 1 kΩ resistor may be required in some applications for proper operation of the microprocessor reset control circuit.

Table 4. FAMILY SELECTION GUIDE

Part #	RESET Voltage (V)	RESET Time (ms)	Output Stage	RESET Polarity
ASM1810	4.620, 4.370, 4.120	150	Push−Pull	LOW
ASM1811	4.620, 4.350, 4.130	150	Open−Drain	LOW
ASM1812	4.620, 4.350, 4.130	150	Push−Pull	HIGH
ASM1815	3.060, 2.880, 2.550	150	Push−Pull	LOW
ASM1816	3.060, 2.880, 2.550	150	Open−Drain	LOW
ASM1817	3.060, 2.880, 2.550	150	Push−Pull	HIGH
ASM1233D	4.625, 4.375, 4.125	350	Open−Drain	LOW
ASM1233M	4.625, 4.375, 2.720	350	Open−Drain	LOW
ASM1233D−L	3.060, 2.880, 2.720	350	Open−Drain	LOW

Application Information

Operation − Power Monitor

The ASM1233D−L/1233D/1233M detects out−of−tolerance Power supply conditions. It resets a processor during powerup, Power−down and generates a reset to the system Processor when the monitored power supply voltage is below the reset threshold. When an out−of−tolerance V_{CC} voltage is detected, the $\overline{RESET}$ signal is asserted. On power−up, $\overline{RESET}$ is kept active (LOW) for approximately 350 ms after the power supply voltage has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RESET}$ is released.
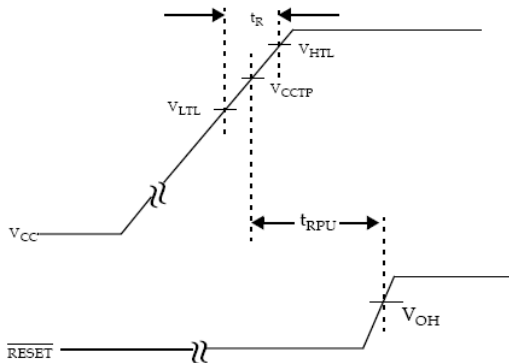
Figure 3. Timing Diagram: Power−Up
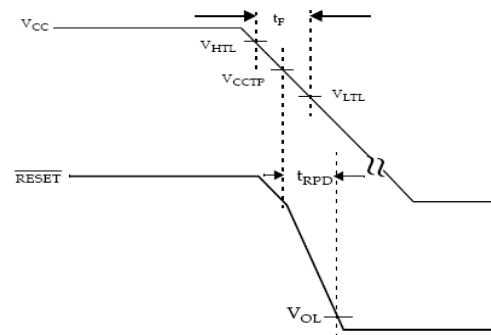
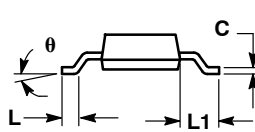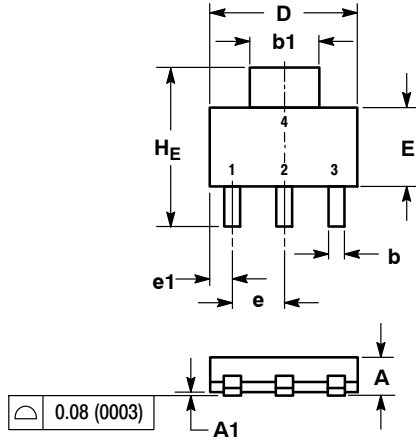Figure 4. Timing Diagram: Power−Down

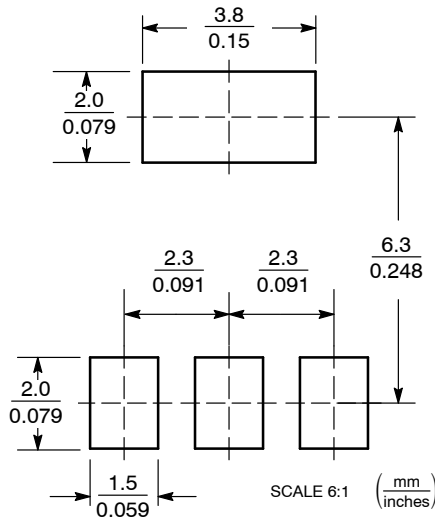## PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE N

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT

$$\frac{3.8}{0.15}$$

$$\frac{2.0}{0.079}$$

$$\frac{2.3}{0.091} \quad \frac{2.3}{0.091} \quad \frac{6.3}{0.248}$$

$$\frac{2.0}{0.079}$$

$$\frac{1.5}{0.059}$$

SCALE 6:1 $\left(\dfrac{mm}{inches}\right)$

PACKAGE DIMENSIONS

TO−92 (TO−226)
CASE 29−11
ISSUE AM
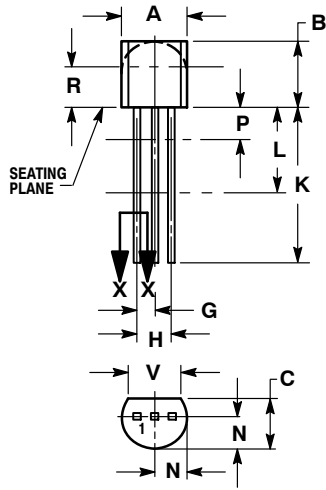
STRAIGHT LEAD
BULK PACK
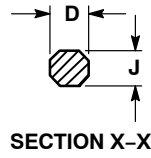
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

SECTION X−X

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

ASM1233D, ASM1233D−L, ASM1233M

PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

TOP VIEW

PIN # 1
IDENTIFICATION
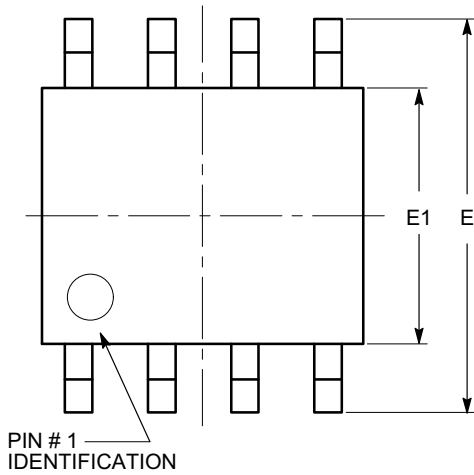
SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°
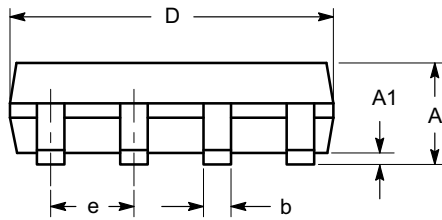
SIDE VIEW
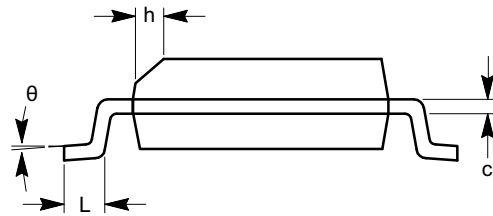
END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

ASM1233D, ASM1233D−L, ASM1233M

Table 5. ORDERING INFORMATION

Part Number	RESET Output Voltage	RESET Tolerance	RESET Time	Open Drain Output	RESET Polarity	Package	Package Marking
TIN − LEAD DEVICES							
ASM1233D−L−5 (ASM1233A−5)	3.06	5%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−5
ASM1233D−L−10 (ASM1233A−10)	2.88	10%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−10
ASM1233D−L−15 (ASM1233A−15)	2.72	15%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−15
ASM1233D−LZ−5 (ASM1233AZ−5)	3.06	5%	350 ms	♦	LOW	4L SOT−223	RVLL
ASM1233D−LZ−10 (ASM1233AZ−10)	2.88	10%	350 ms	♦	LOW	4L SOT−223	RWLL
ASM1233D−LZ−15 (ASM1233AZ−15)	2.72	15%	350 ms	♦	LOW	4L SOT−223	RXLL
ASM1233D−5	4.625	5%	350 ms	♦	LOW	3L TO−92	ASM1233D−5
ASM1233D−10	4.375	10%	350 ms	♦	LOW	3L TO−92	ASM1233D−10
ASM1233D−15	4.125	15%	350 ms	♦	LOW	3L TO−92	ASM1233D−15
ASM1233DZ−5	4.625	5%	350 ms	♦	LOW	4L SOT−223	RSLL
ASM1233DZ−10	4.375	10%	350 ms	♦	LOW	4L SOT−223	RTLL
ASM1233DZ−15	4.125	15%	350 ms	♦	LOW	4L SOT−223	RULL
ASM1233M−55	4.625	5%	350 ms	♦	LOW	3L TO−92	ASM1233M−55
ASM1233M−5	4.375	10%	350 ms	♦	LOW	3L TO−92	ASM1233M−5
ASM1233M−3	2.72	15%	350 ms	♦	LOW	3L TO−92	ASM1233M−3
ASM1233MS−55	4.625	5%	350 ms	♦	LOW	8L SOIC	ASM1233MS−55
ASM1233MS−5	4.38	10%	350 ms	♦	LOW	8L SOIC	ASM1233MS−5
ASM1233MS−3	2.72	15%	350 ms	♦	LOW	8L SOIC	ASM1233MS−3
LEAD FREE DEVICES							
ASM1233D−L−5F	3.06	5%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−5F
ASM1233D−L−10F	2.88	10%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−10F
ASM1233D−L−15F	2.72	15%	350 ms	♦	LOW	3L TO−92	ASM1233D−L−15F
ASM1233D−LZ−5F	3.06	5%	350 ms	♦	LOW	4L SOT−223	KVLL
ASM1233D−LZ−10F	2.88	10%	350 ms	♦	LOW	4L SOT−223	KWLL
ASM1233D−LZ−15F	2.72	15%	350 ms	♦	LOW	4L SOT−223	KXLL
ASM1233D−5F	4.625	5%	350 ms	♦	LOW	3L TO−92	ASM1233D−5F
ASM1233D−10F	4.375	10%	350 ms	♦	LOW	3L TO−92	ASM1233D−10F
ASM1233D−15F	4.125	15%	350 ms	♦	LOW	3L TO−92	ASM1233D−15F
ASM1233DZ−5F	4.625	5%	350 ms	♦	LOW	4L SOT−223	KSLL
ASM1233DZ−10F	4.375	10%	350 ms	♦	LOW	4L SOT−223	KTLL
ASM1233DZ−15F	4.125	15%	350 ms	♦	LOW	4L SOT−223	KULL
ASM1233M−5F	4.375	5%	350 ms	♦	LOW	3L TO−92	ASM1233M−5F
ASM1233M−55F	4.625	10%	350 ms	♦	LOW	3L TO−92	ASM1233M−55F
ASM1233M−3F	2.72	15%	350 ms	♦	LOW	3L TO−92	ASM1233M−3F
ASM1233MS−5F	4.38	5%	350 ms	♦	LOW	8L SOIC	ASM1233MS−5F
ASM1233MS−55F	4.625	10%	350 ms	♦	LOW	8L SOIC	ASM1233MS−55F
ASM1233MS−3F	2.72	15%	350 ms	♦	LOW	8L SOIC	ASM1233MS−3F