To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

EOL announced

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M66252P/FP

1152 x 8-BIT LINE MEMORY (FIFO)

DESCRIPTION

The M66252P/FP is a high-speed line memory with a FIFO (First In First Out) structure of 1152-word × 8-bit configuration which uses high-performance silicon gate CMOS process technology.

It has separate clock, enable and reset signals for write and read and is most suitable as a buffer memory between devices with different data processing throughput.

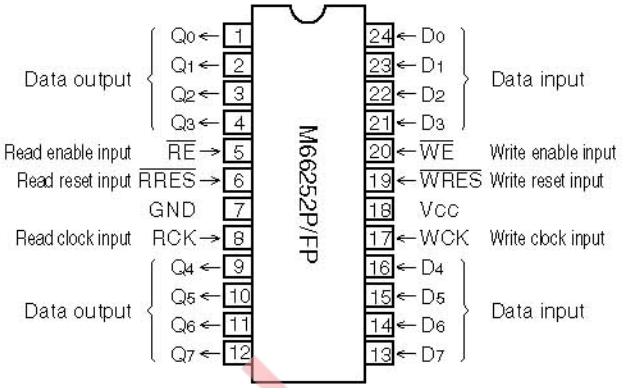
FEATURES

- Memory construction ..... 1152words x 8bits (dynamic memory)
- High-speed cycle ..... 50ns (min.)
- High-speed access ..... 40ns (max.)
- Output hold ..... 5ns (min.)
- Fully independent, asynchronous write and read operations
- Variable-length delay bit
- Output 3-state

APPLICATION

Digital photocopiers, high-speed facsimiles, laser beam printers.

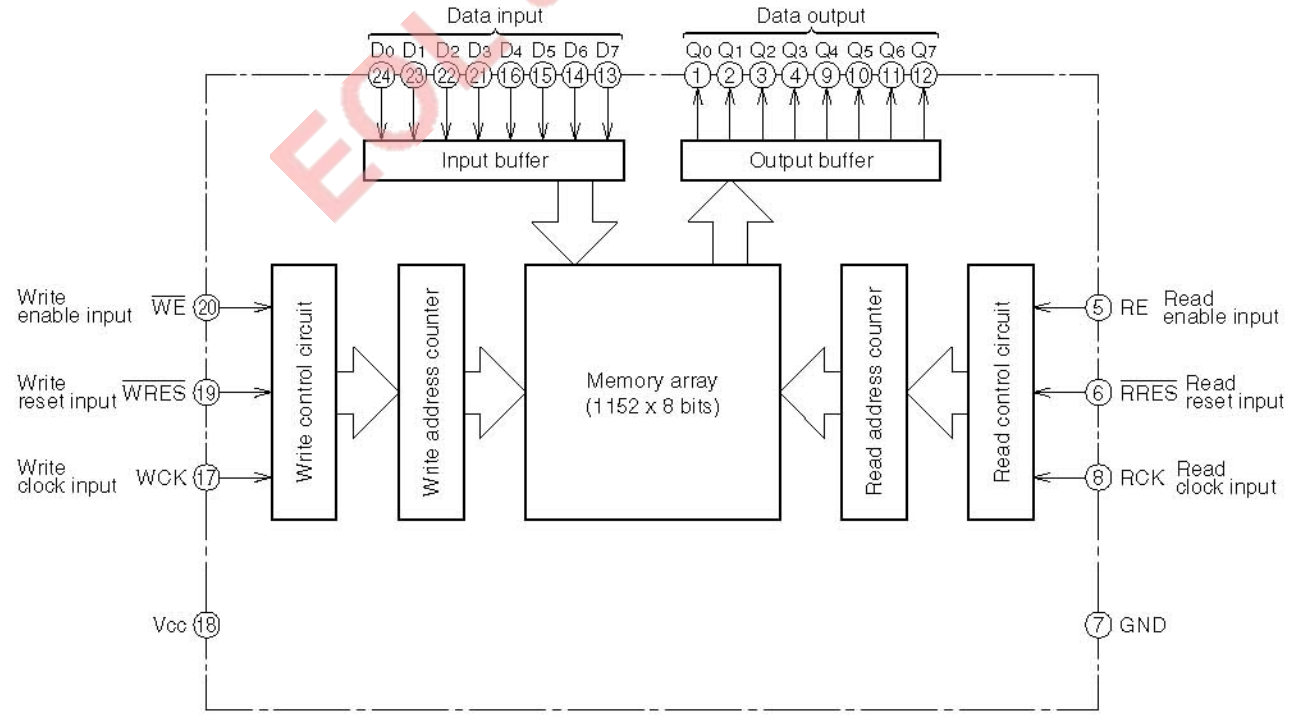
PIN CONFIGURATION (TOP VIEW)



Outline 24P4Y
24P2W-A

EOL announced

BLOCK DIAGRAM



FUNCTION

When the status of write enable input $\overline{WE}$ is "L," data on D_0 thru D_7 are written on the memory synchronously with write clock input WCK rise edges. At this time, write address counter executes counting.
The following write-related operations are also performed synchronously with WCK rise edges.
When $\overline{WE}$ is "H," writing on memory is inhibited, and write address counter stops counting.
When write reset input $\overline{WRES}$ is "L," write address counter is initialized.

When read enable input $\overline{RE}$ is "L," data on memory are output to Q_0 thru Q_7 synchronously with read clock input RCK rise edges. At this time, read address counter executes counting.
The following read-related operations are also performed synchronously with RCK rise edges.
When $\overline{RE}$ is "H," reading from memory is inhibited, and read address counter stops counting. The status of Q_0 thru Q_7 becomes high-impedance.
When read reset input $\overline{RRES}$ is "L," read address counter is initialized.

ABSOLUTE MAXIMUM RATINGS (Ta = –20 ~ 70°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Reference pin: GND	–0.5 ~ +7.0	V
V_I	Input voltage		–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage		–0.5 ~ V_{CC} + 0.5	V
Pd	Power dissipation	Ta = 25°C	550 (Note 1)	mW
Tstg	Storage temperature		–65 ~ 150	°C

Note 1: Ta ≥ 62°C are derated at –8.8mW/°C (24P4Y)
Ta ≥ 51°C are derated at –7.5mW/°C (24P2W)

RECOMMENDED OPERATIONAL CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
Topr	Ambient temperature	–20		70	°C

ELECTRICAL CHARACTERISTICS (Ta = –20 ~ 70°C, V_{CC} = 5V±10%, GND = 0V)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	"H" input voltage			2.0			V
V_{IL}	"L" input voltage					0.8	V
V_{OH}	"H" output voltage	I_{OH} = –4mA		V_{CC} – 0.8			V
V_{OL}	"L" output voltage	I_{OL} = 4mA				0.55	V
I_{IH}	"H" input current	$V_I = V_{CC}$	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK Do~D7			1.0	µA
I_{IL}	"L" input current	V_I = GND	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK Do~D7			–1.0	µA
I_{OZH}	"H" output current under "off" condition	$V_O = V_{CC}$				5.0	µA
I_{OZL}	"L" output current under "off" condition	V_O = GND				–5.0	µA
I_{CC}	Average supply current during operation	V_I = V_{IH}, V_{IL}, Outputs are open t_{WCK}, t_{RCK} = 100ns				100	mA
CI	Input capacitance	f = 1MHz				10	pF
CO	Output capacitance under "off" condition	f = 1MHz				15	pF

EOL announced

SWITCHING CHARACTERISTICS (Ta = −20 ~ 70°C, Vcc = 5V±10%, GND = 0V)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tAC	Access time			40	ns
tOH	Output hold time	5			ns
tOEN	Output enable time	5		40	ns
tODIS	Output disable time	5		40	ns

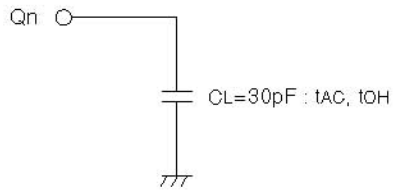
TIMING CHARACTERISTICS (Ta = −20 ~ 70°C, Vcc = 5V±10%, GND = 0V)

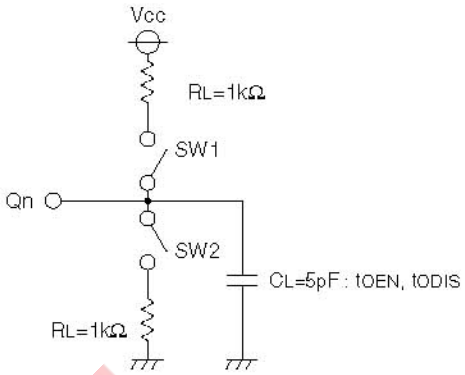
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tWCK	Write clock (WCK) cycle time	50			ns
tWCKH	Write clock (WCK) "H" pulse width	25			ns
tWCKL	Write clock (WCK) "L" pulse width	25			ns
tRCK	Read clock (RCK) cycle time	50			ns
tRCKH	Read clock (RCK) "H" pulse width	25			ns
tRCKL	Read clock (RCK) "L" pulse width	25			ns
tDS	Input data setup time (in response to WCK)	15			ns
tDH	Input data hold time (in response to WCK)	5			ns
tRESS	Reset setup time (in response to WCK and RCK)	15			ns
tRESH	Reset hold time (in response to WCK and RCK)	5			ns
tNRESS	Reset non-select setup time (in response to WCK and RCK)	15			ns
tNRESH	Reset non-select hold time (in response to WCK and RCK)	5			ns
tWES	$\overline{WE}$ setup time (in response to WCK)	15			ns
tWEH	$\overline{WE}$ hold time (in response to WCK)	5			ns
tNWES	$\overline{WE}$ non-select setup time (in response to WCK)	15			ns
tNWEH	$\overline{WE}$ non-select hold time (in response to WCK)	5			ns
tRES	$\overline{RE}$ setup time (in response to RCK)	15			ns
tREH	$\overline{RE}$ hold time (in response to RCK)	5			ns
tNRES	$\overline{RE}$ non-select setup time (in response to RCK)	15			ns
tNREH	$\overline{RE}$ non-select hold time (in response to RCK)	5			ns
tr, tf	Input pulse rise time and fall time			35	ns
tH	Data hold time (Note 1)			20	ms

Note 1. The following conditions should be met for each line access:
$\overline{WE}$ "H" level period ≤ 20ms - 1152 · tWCK - $\overline{WRES}$ "L" level period
$\overline{RE}$ "H" level period ≥ 20ms - 1152 · tRCK - $\overline{RRES}$ "L" level period
2. Perform reset operation after turning on power supply.

Not announced

TEST CIRCUIT

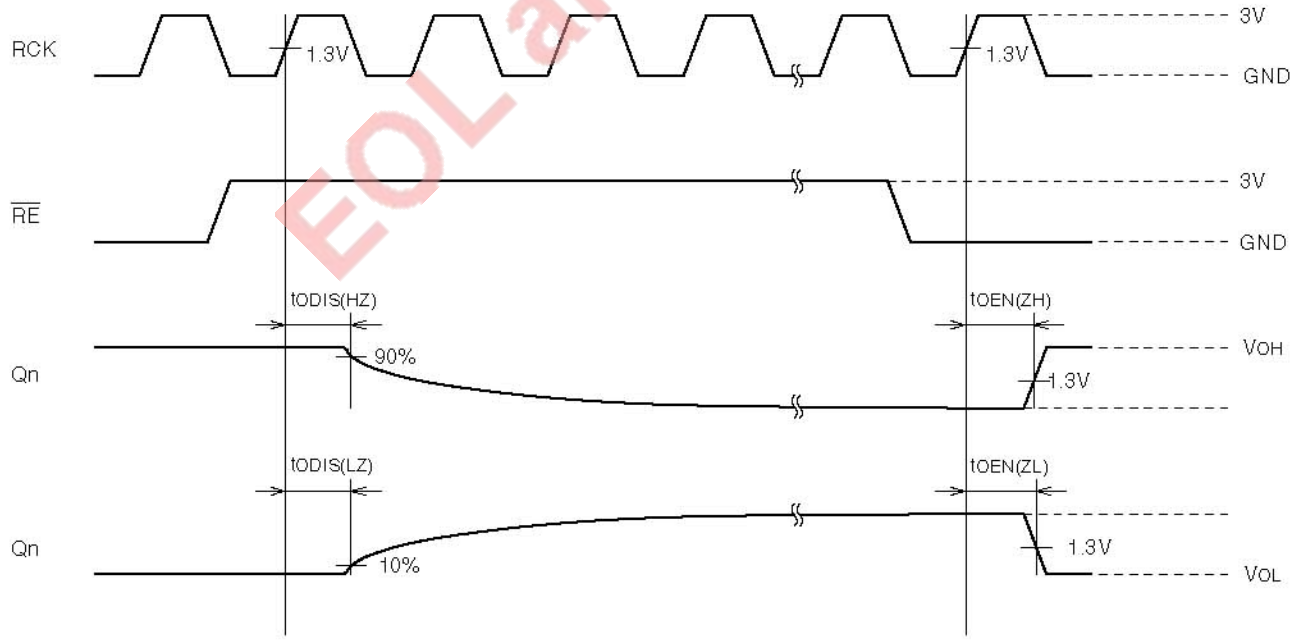




Input pulse level: 0 ~ 3V
Input pulse rise time and fall time: 3ns
Measurement reference level, input: 1.3V
Measurement reference level, output: 1.3V (Note: tODIS (LZ) is tested at 10% output amplitude, and tODIS (HZ) is tested at 90% output amplitude.)
Load capacitance CL includes floating capacitance and probe input capacitance.

Parameter	SW1	SW2
tODIS(LZ)	Closed	Open
tODIS(HZ)	Open	Closed
tOEN(ZL)	Closed	Open
tOEN(ZH)	Open	Closed

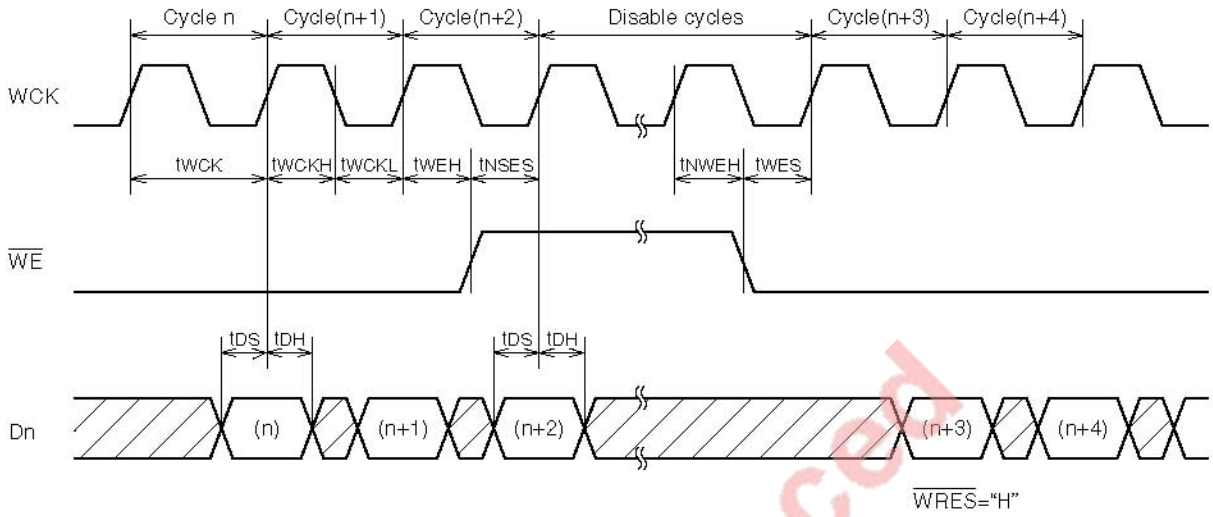
TEST CONDITIONS FOR OUTPUT DISABLE TIME tODIS AND OUTPUT ENABLE TIME tOEN



EOL announced

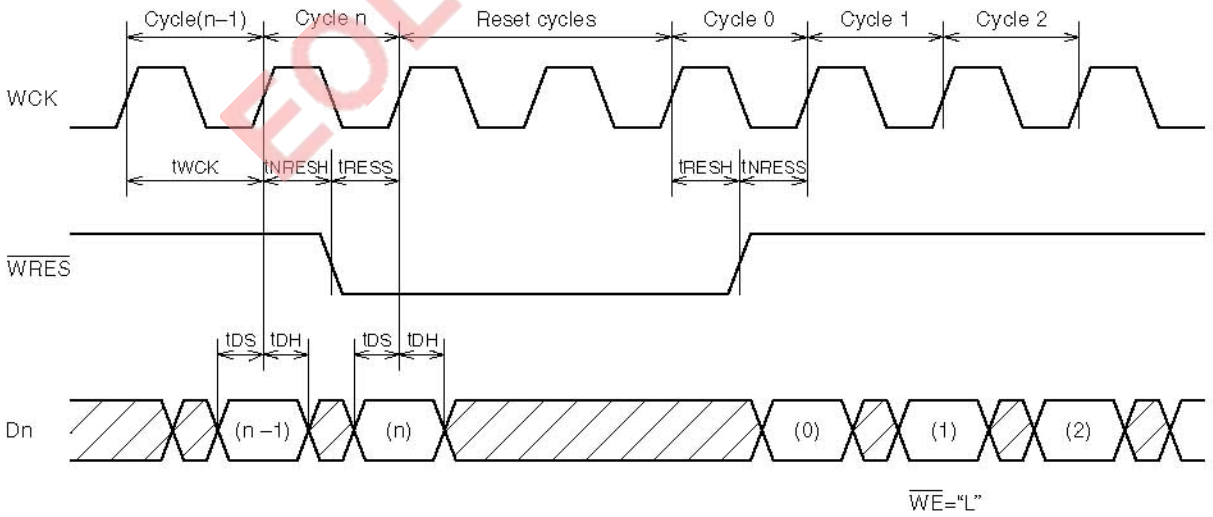
TIMING CHARTS

• Write Cycles

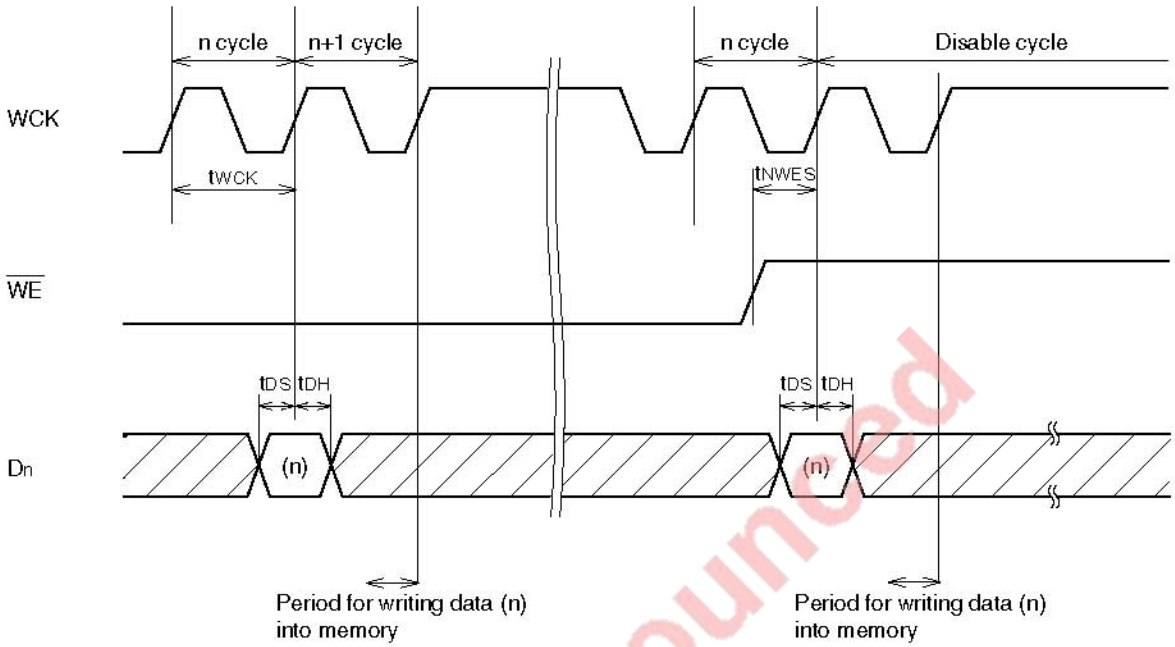


EOL announced

• Write Reset Cycles



• Matters that needs attention when WCK stops

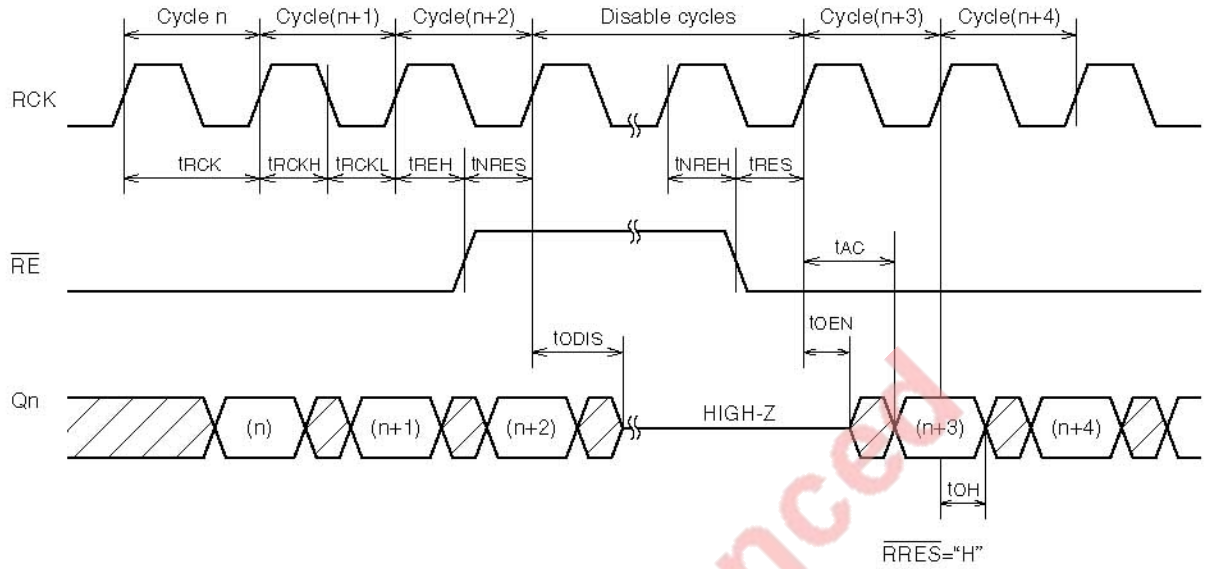


$\overline{WRES}$ = "H"

Input data of n cycle is read at the rising edge after WCK of n cycle and writing operation starts in the WCK low-level period of n+1 cycle. The writing operation is complete at the falling edge after n+1 cycle.
To stop reading write data at n cycle, enter WCK before the rising edge after n+1 cycle.
When the cycle next to n cycle is a disable cycle, WCK for a cycle requires to be entered after the disable cycle as well.

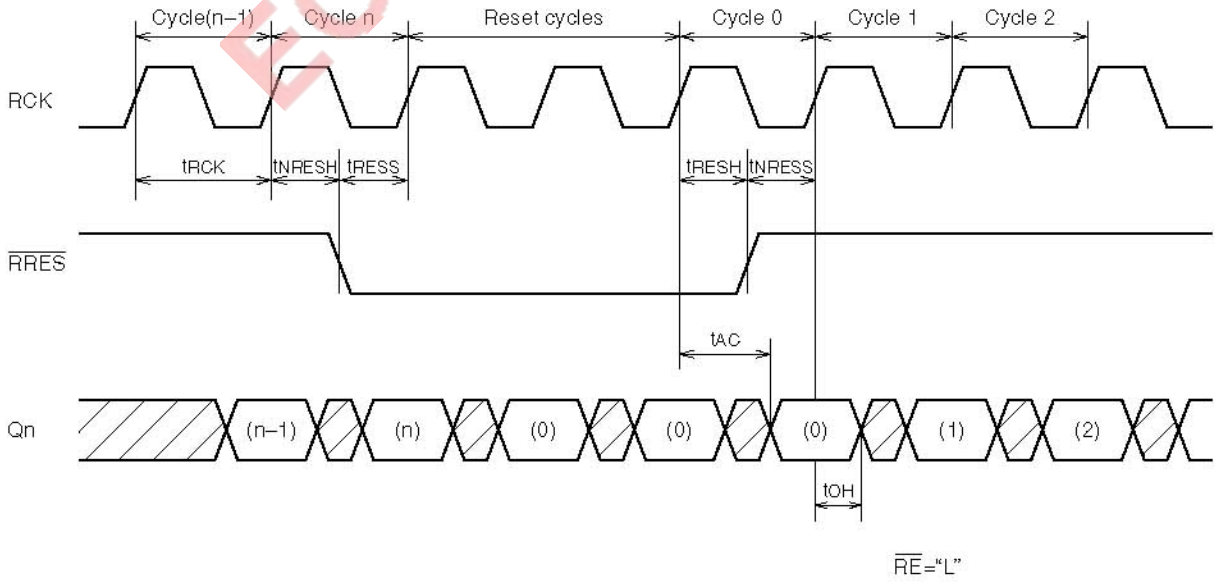
EOL announced

• Read Cycles



EOL announced

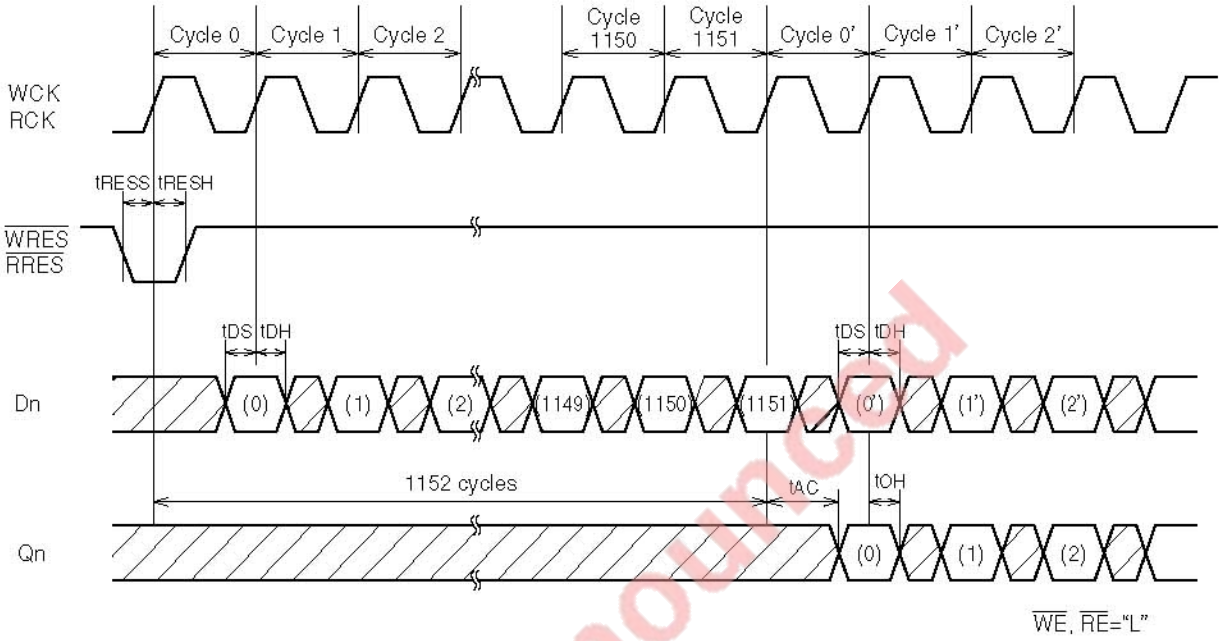
• Read Reset Cycles



VARIABLE-LENGTH DELAY BITS

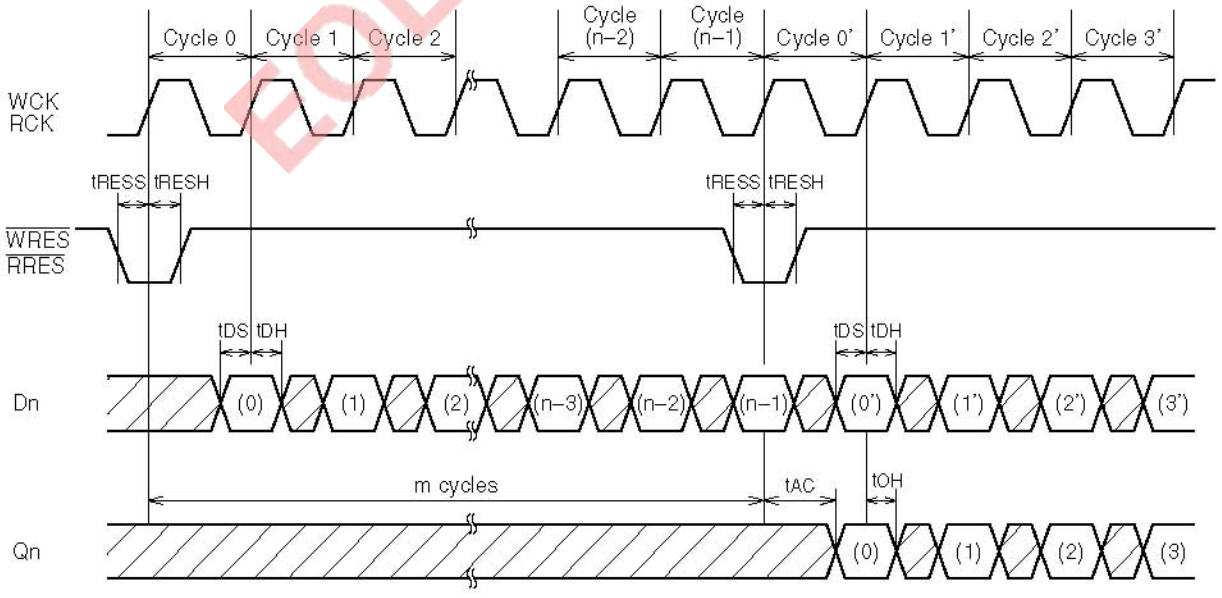
• 1-line (1152-bit) delay

A write input data is written into memory at the second rise edge of WCK in the cycle, and a read output data is output from memory at the first rise edge of RCK in the cycle, so that 1-line delay can be made easily.



WE, RE="L"

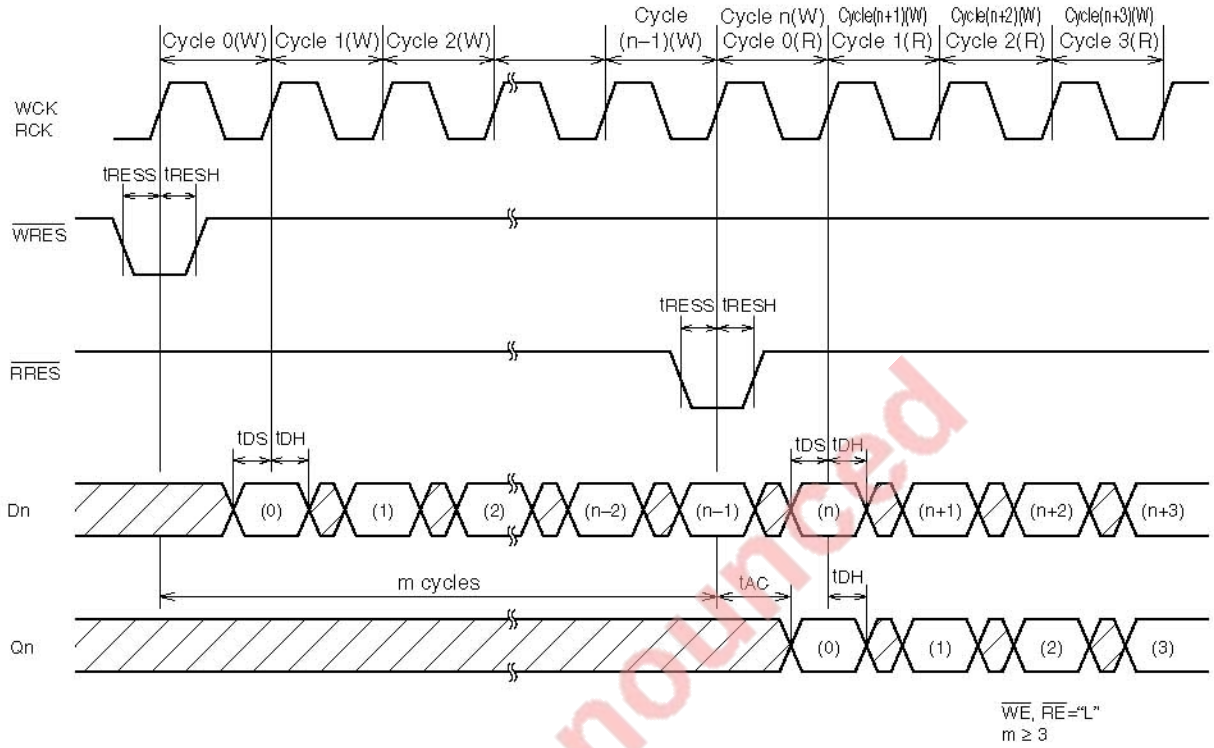
• n-bit delay 1
(Making a reset at a cycle corresponding to delay length)



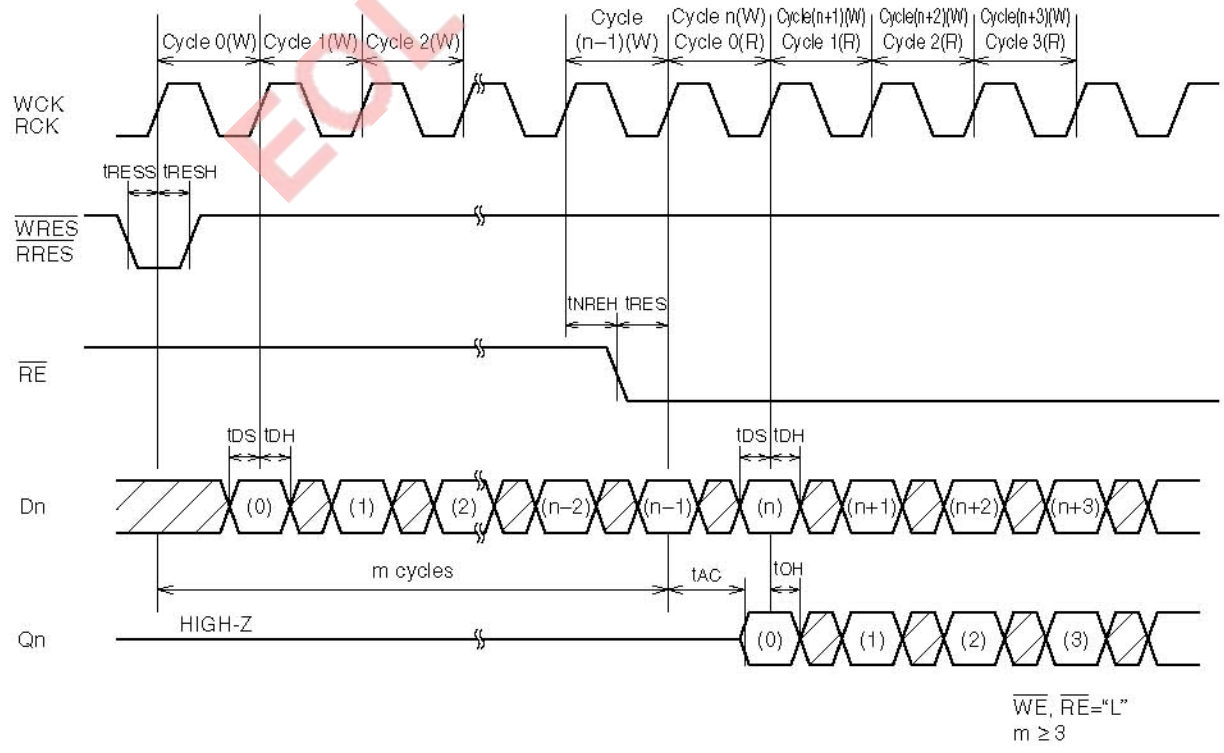
WE, RE="L"
m ≥ 3

EOL announced

• n-bit delay 2
(Sliding $\overline{WRES}$ and $\overline{RRES}$ at a cycle corresponding to delay length)



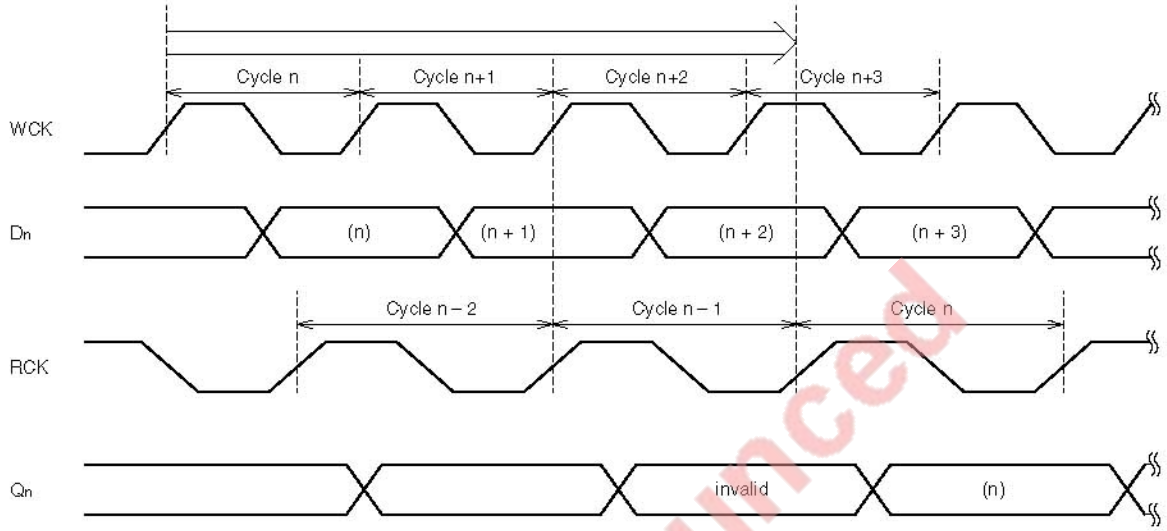
• n-bit delay 3
(Disabling $\overline{RE}$ at a cycle corresponding to delay length)



EOL announced

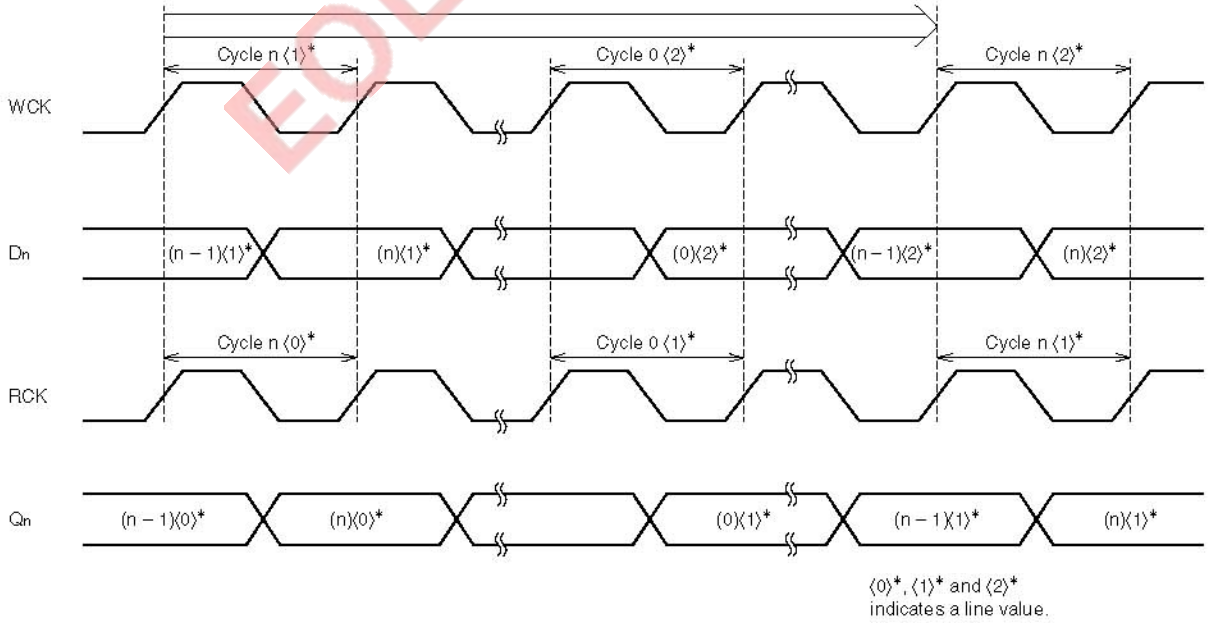
• Shortest read of data "n" written in cycle n
Cycle n−1 on read side should be started after end of cycle n+1 on write side

When the start of cycle n−1 on read side is earlier than the end of cycle n+1 on write side, output Qn of cycle n becomes invalid. In the figure shown below, the read of cycle n−1 is invalid.



• Longest read of data "n" written in cycle n: 1-line delay
Cycle n <1>* on read side should be started when cycle n <2>* on write is started

Output Qn of n cycle <1>* can be read until the start of reading side n cycle <1>* and the start of writing side n cycle <2>* overlap each other.

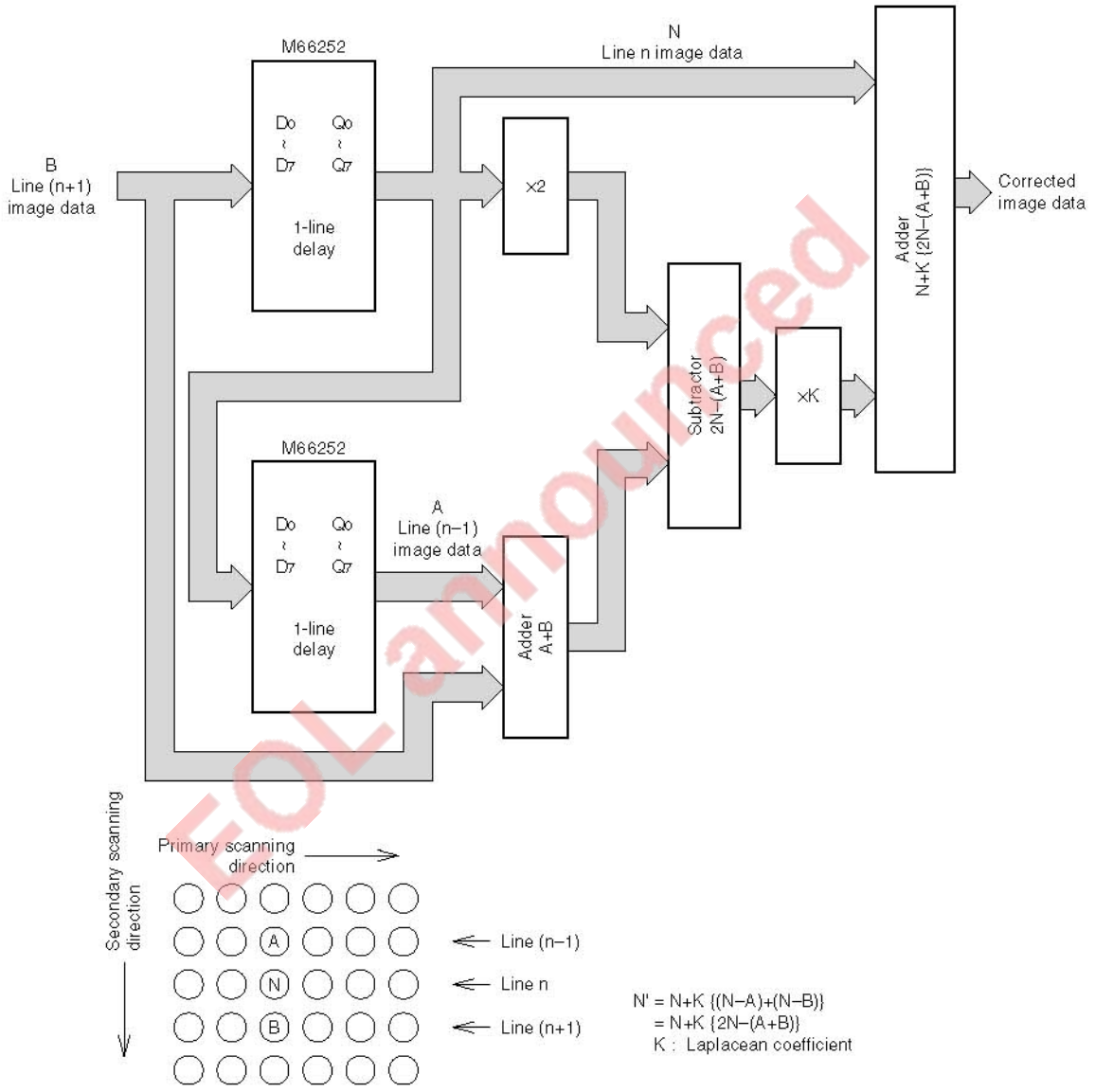


〈0〉*, 〈1〉* and 〈2〉*
indicates a line value.

EOL announced

APPLICATION EXAMPLE

Laplacian Filter Circuit for Correction of Resolution in the Secondary Scanning Direction.



FOLannounced