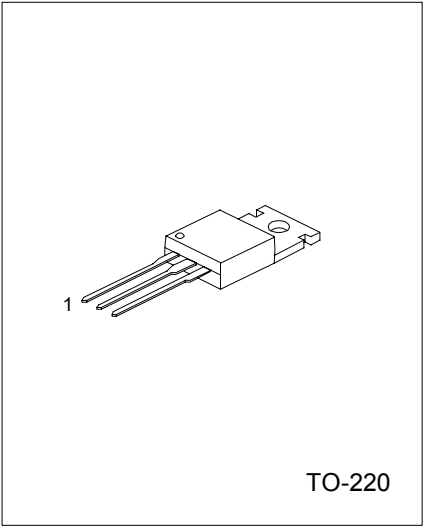


SCRs

DESCRIPTION

The UTC US112S/N is suitable to fit all modes of control found in applications such as overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, in-rush current limiting circuits, capacitive discharge ignition, voltage regulation circuits.



1: CATHODE 2: ANODE 3: GATE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING		UNIT
		US112S	US112N	
Repetitive peak off-state voltages US112S/N-4 US112S/N-6 US112S/N-8	V_{DRM} V_{RRM}	400 600 800		V
RMS on-state current (180° conduction angle) ($T_c = 105^\circ\text{C}$)	$I_{T(RMS)}$	12		A
Average on-state current (180° conduction angle) ($T_c = 105^\circ\text{C}$)	$I_{T(AV)}$	8		A
Non repetitive surge peak on-state current ($T_j = 25^\circ\text{C}$) $t_p=8.3\text{ms}$ $t_p=10\text{ms}$	I_{TSM}	146 140		A
I^2t Value for fusing ($t_p = 10\text{ ms}$, $T_j = 25^\circ\text{C}$)	I^2t	98		A ² S
Critical rate of rise of on-state current ($I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ n s}$, $F = 60\text{ Hz}$, $T_j = 125^\circ\text{C}$,)	di/dt	50		A/ μs
Peak gate current ($t_p=20\mu\text{s}$, $T_j = 125^\circ\text{C}$)	I_{GM}	4		A
Maximum peak reverse gate voltage	V_{RGM}		5	V
Average gate power dissipation ($T_j = 125^\circ\text{C}$)	$P_{G(AV)}$	1		W
Storage junction temperature range	T_{stg}	-40 ~ +150		$^\circ\text{C}$
Operating junction temperature range	T_j	-40 ~ +125		$^\circ\text{C}$

UTC US112S(SENSITIVE) ELECTRICAL CHARACTERISTICS

(T_J=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX.	UNIT
Gate trigger Current	I _{GT}	V _D = 12 V, R _L = 140Ω		200	μA
Gate trigger Voltage	V _{GT}	V _D = 12 V, R _L = 140Ω		0.8	V
Gate non-trigger voltage	V _{GD}	V _D = V _{DRM} , R _L = 3.3 kΩ, R _{GK} = 1kΩ T _J = 125°C	0.1		V
Reverse gate voltage	V _{RG}	I _{RG} = 10 μA	8		V
Holding Current	I _H	I _T = 50 mA, R _{GK} = 1 kΩ		5	mA
Latching Current	I _L	I _G = 1 mA, R _{GK} = 1 kΩ		6	mA
Circuit Rate Of Change Of off-state Voltage	dV/dt	V _D = 67 % V _{DRM} , R _{GK} = 220 Ω T _J = 125°C	5		V/μs
On-state voltage	V _{TM}	I _{TM} = 24A, t _p = 380 μs, T _J = 25°C		1.6	V
Threshold Voltage	V _{t0}	T _J = 125°C		0.85	V
Dynamic Resistance	R _d	T _J = 125°C		30	mΩ
Off-state Leakage Current	I _{DRM}	V _{DRM} = V _{RRM} , R _{GK} = 220 Ω T _J = 25°C		5	μA
	I _{RRM}	T _J = 125°C		2	mA

UTC US112N(STANDARD) ELECTRICAL CHARACTERISTICS

(T_J=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX.	UNIT
Gate trigger Current	I _{GT}	V _D = 12 V, R _L = 33Ω	2	15	mA
Gate trigger Voltage	V _{GT}	V _D = 12 V, R _L = 33Ω		1.3	V
Gate non-trigger voltage	V _{GD}	V _D = V _{DRM} , R _L = 3.3 kΩ, T _J = 125°C	0.2		V
Holding Current	I _H	I _T = 500 mA, Gate open		30	mA
Latching Current	I _L	I _G = 1.2 I _{GT}		60	mA
Circuit Rate Of Change Of off-state Voltage	dV/dt	V _D = 67 % V _{DRM} , Gate open, T _J = 125°C	200		V/μs
On-state voltage	V _{TM}	I _{TM} = 24A, t _p = 380 μs, T _J = 25°C		1.6	V
Threshold Voltage	V _{t0}	T _J = 125°C		0.85	V
Dynamic Resistance	R _d	T _J = 125°C		30	mΩ
Off-state Leakage Current	I _{DRM}	V _{DRM} = V _{RRM} , T _J = 25°C		5	μA
	I _{RRM}	T _J = 125°C		2	mA

THERMAL RESISTANCES

PARAMETER	SYMBOL	VALUE	UNIT
Junction to case (DC)	R _{th(j-c)}	1.3	K/W
Junction to ambient	R _{th(j-a)}	60	K/W

Figure.1:Maximum average power dissipation vs average on-state current.

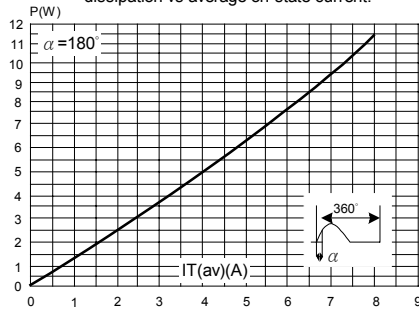


Figure.2:Average and D.C. on-state current vs case temperature

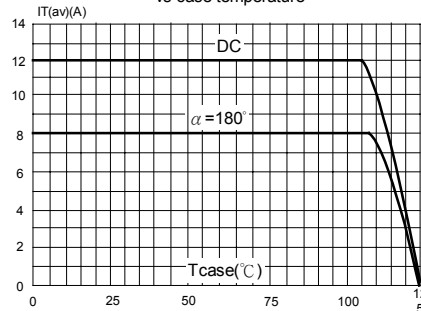


Fig.3-1:Relative variation of thermal impedance junction to case vs pulse duration.

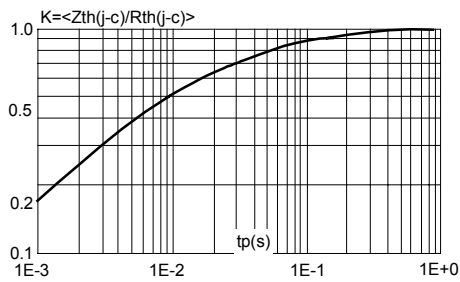


Fig.3-2:Relative variation of thermal impedance junction to ambient vs pulseduration (recommended pad layout,FR4 PC board)

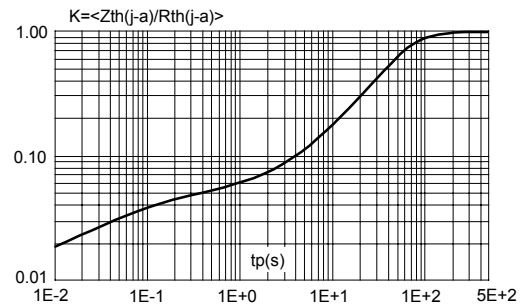


Figure.4-1:Relative variation of gate trigger current,holding current and latching vs junction temperature (US112S)

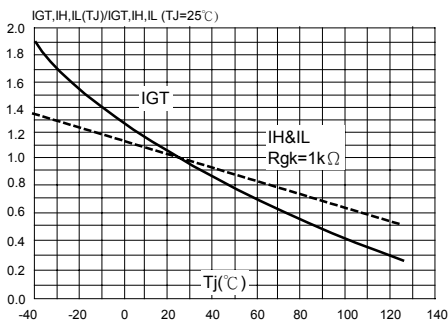


Figure.4-2: Relative variation of gate trigger current,holding current and latching current vs junction temperature (US112N).

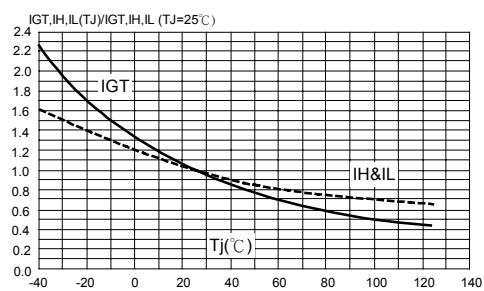


Figure.5:Relative variation of holding current vs gate-cathode resistance(typical values) (US112S)

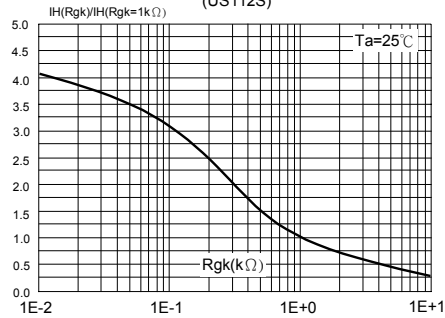


Fig.6: Relative variation of dV/dt immunity vs gate-cathode resistance(typical values) (US112S)

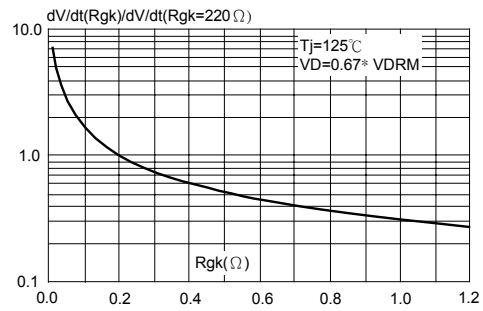


Fig.7: Relative variation of dV/dt immunity vs gate-cathode capacitance(typical values) (US112S)

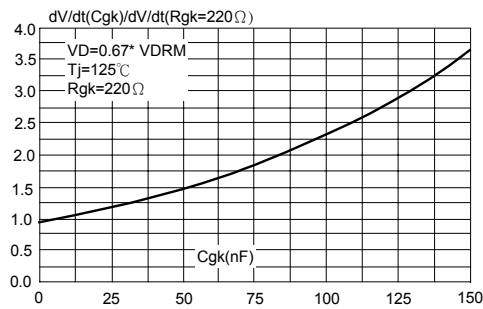


Fig.8: Surge peak on-state current vs number of cycles

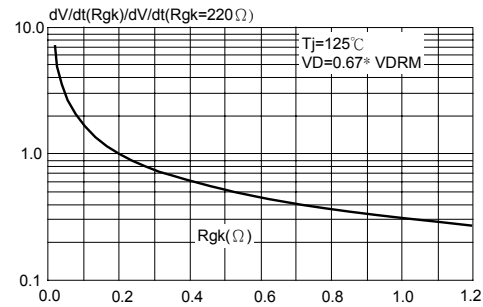


Fig.9:Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ms}$, and corresponding values of I^2t .

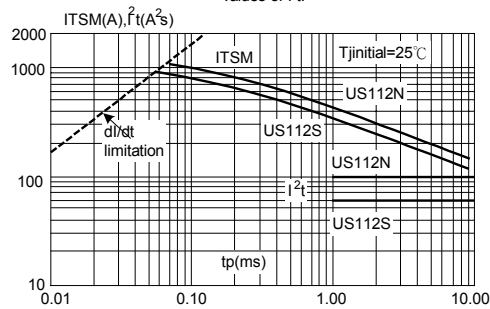


Fig.10: On-state characteristics(maximum values).

