

24-Bit, 192kHz Stereo ADC

DESCRIPTION

The WM8782 is a high performance, low cost stereo audio ADC designed for recordable media applications.

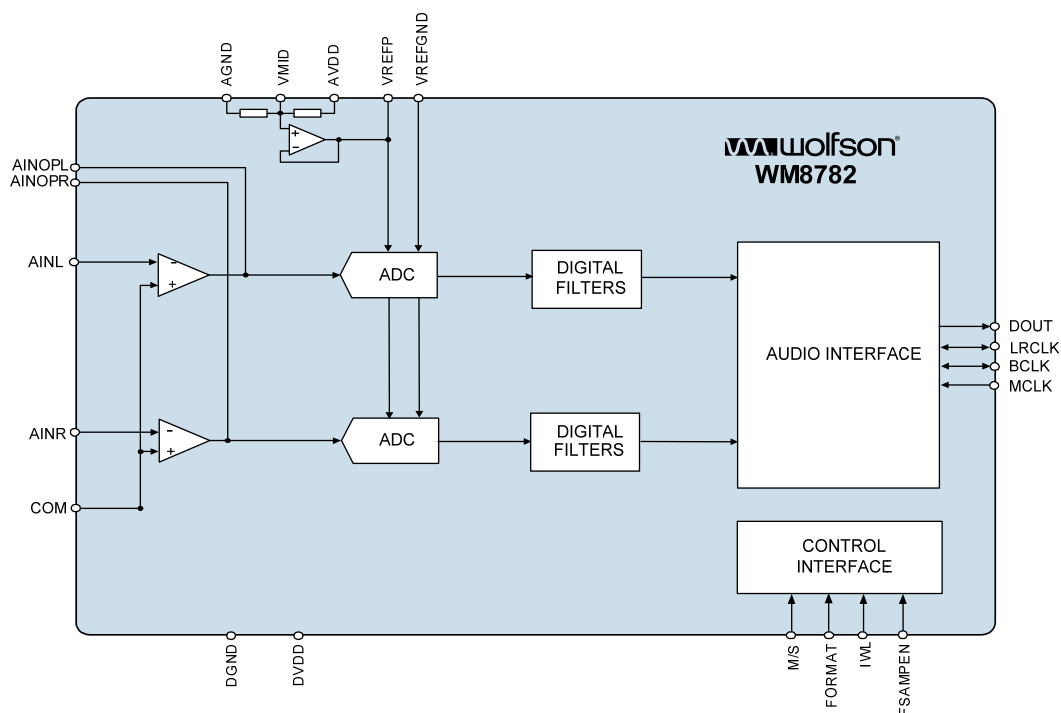
The device offers stereo line level inputs along with two control input pins (FORMAT, IWL) to allow operation of the audio interface in three industry standard modes. An internal op-amp is integrated on the front end of the chip to accommodate analogue input signals greater than 1V_{rms}. The device also has a high pass filter to remove residual DC offsets.

WM8782 offers Master or Slave mode clocking schemes. A control input pin M/S is used to allow Slave mode operation or Master mode operation. A stereo 24-bit multi-bit sigma-delta ADC is used with 128x, 64x or 32x over-sampling, according to sample rate. Digital audio output word lengths from 16-24 bits and sampling rates from 8kHz to 192kHz are supported.

The device is a hardware controlled device and is supplied in a 20-lead SSOP package.

The device is available over a functional temperature range of -40°C to +85°C

BLOCK DIAGRAM



FEATURES

- SNR 100dB ('A' weighted @ 48kHz)
- THD -93dB (at -1dB)
- Sampling Frequency: 8 – 192kHz
- Master or Slave Clocking Mode
- System Clock (MCLK): 128fs, 192fs, 256fs, 384fs, 512fs, 768fs
 - Audio Data Interface Modes
- 16-24 bit I²S, 16-24 bit Left, 16-24 bit Right Justified
- Supply Voltages
 - Analogue: 2.7 to 5.5V
 - Digital core: 2.7V to 3.6V
- 20-lead SSOP or 20-lead TSSOP package
- Accelerated Lifetime Screened Devices available.

APPLICATIONS

- Recordable DVD Players
- Personal Video Recorders
- STB
- Studio Audio Processing Equipment
- Automotive

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PIN CONFIGURATION

| | | | | | | |
|---------|--------------------------|----|---|----|--------------------------|---------|
| MCLK | <input type="checkbox"/> | 1 | ● | 20 | <input type="checkbox"/> | M/S |
| DOUT | <input type="checkbox"/> | 2 | | 19 | <input type="checkbox"/> | AINL |
| LRCLK | <input type="checkbox"/> | 3 | | 18 | <input type="checkbox"/> | AINOPL |
| DGND | <input type="checkbox"/> | 4 | | 17 | <input type="checkbox"/> | COM |
| DVDD | <input type="checkbox"/> | 5 | | 16 | <input type="checkbox"/> | AINR |
| BCLK | <input type="checkbox"/> | 6 | | 15 | <input type="checkbox"/> | AINOPR |
| IWL | <input type="checkbox"/> | 7 | | 14 | <input type="checkbox"/> | AGND |
| FSAMPEN | <input type="checkbox"/> | 8 | | 13 | <input type="checkbox"/> | AVDD |
| FORMAT | <input type="checkbox"/> | 9 | | 12 | <input type="checkbox"/> | VREFP |
| VMID | <input type="checkbox"/> | 10 | | 11 | <input type="checkbox"/> | VREFGND |

ORDERING INFORMATION

| DEVICE | TEMPERATURE RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---------------|-------------------|--|----------------------------|----------------------------|
| WM8782SEDS/V | -40°C to +85°C | 20-lead SSOP (Pb-free) | MSL2 | 260°C |
| WM8782SEDS/RV | -40°C to +85°C | 20-lead SSOP (Pb-free, tape and reel) | MSL2 | 260°C |

Note:

Reel quantity = 2,000

PIN DESCRIPTION

| PIN NO. | NAME | TYPE | DESCRIPTION |
|---------|---------|------------------------|---|
| 1 | MCLK | Digital Input | Master Clock |
| 2 | DOUT | Digital Output | ADC Digital Audio Data |
| 3 | LRCLK | Digital Input / Output | Audio Interface Left / Right Clock |
| 4 | DGND | Supply | Digital Negative Supply |
| 5 | DVDD | Supply | Digital Positive Supply |
| 6 | BCLK | Digital Input / Output | Audio Interface Bit Clock |
| 7 | IWL | Digital Tristate Input | Word Length 0 = 16 bit 1 = 20 bit Z = 24 bit |
| 8 | FSAMPEN | Digital Tristate Input | Fast Sampling Rate Enable 0 = 48kHz 1 = 96kHz Z = 192kHz |
| 9 | FORMAT | Digital Tristate Input | Audio Mode Select 0 = RJ 1 = LJ Z = I2S |
| 10 | VMID | Analogue Output | Mid rail Voltage Decoupling Capacitor |
| 11 | VREFGND | Supply | Negative Supply and Substrate Connection |
| 12 | VREFP | Analogue Output | Positive Reference Voltage Decoupling Pin; 10uF external decoupling |
| 13 | AVDD | Supply | Analogue Positive Supply |
| 14 | AGND | Supply | Analogue Negative Supply and Substrate Connection |
| 15 | AINOPR | Analogue Output | Right Channel Internal Op-Amp Output |
| 16 | AINR | Analogue Input | Right Channel Input |
| 17 | COM | Analogue Input | Common mode high impedance input should be set to midrail. |
| 18 | AINOPL | Analogue Output | Left Channel Internal Op-Amp Output |
| 19 | AINL | Analogue Input | Left Channel Input |
| 20 | M/S | Digital Input | Interface Mode Select 0 = Slave mode (128fs, 192fs, 256fs, 384fs, 512fs, 768fs) 1 = Master mode (256fs, 128fs) (fs=word clock frequency) |

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level is specified in Ordering Information.

| CONDITION | MIN | MAX |
|--|------------|-------------|
| Digital supply voltage | -0.3V | +4.5V |
| Analogue supply voltage | -0.3V | +7V |
| Voltage range digital inputs | DGND -0.3V | DVDD + 0.3V |
| Voltage range analogue inputs | AGND -0.3V | AVDD +0.3V |
| Ambient temperature (supplies applied) | -55°C | +125°C |
| Storage temperature | -65°C | +150°C |
| Pb free package body temperature (reflow 10 seconds) | | +260°C |
| Package body temperature (soldering 2 minutes) | | +183°C |

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

THERMAL PERFORMANCE

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----------------|-----|------------------|-----|------|
| Thermal resistance – junction to ambient | $R_{\theta JA}$ | | | 81 See note 1 | | °C/W |

Notes:

1. Figure given for package mounted on 4-layer FR4 according to JESD51-7. (No forced air flow is assumed).
2. Thermal performance figures are estimated.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|----------------|-----------------------------|-----|-----|-----|------|
| Digital supply range | DVDD | WM8782SEDS, WM8782SEDS/R | 2.7 | | 3.6 | V |
| Analogue supply range | AVDD | WM8782SEDS, WM8782SEDS/R | 2.7 | | 5.5 | V |
| Ground | DGND,AGND | | | 0 | | V |
| Operating temperature range | T _A | WM8782SEDS, WM8782SEDS/R | -40 | | +85 | °C |

Notes:

- Digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

DVDD = 3.3V, AVDD = 5.0V, T_A = +25°C, 1kHz signal, A-weighted, fs = 48kHz, MCLK = 256fs, 24-bit audio data, Slave Mode unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------|---|-----|--------|-----|------------------|
| ADC Performance – WM8782SEDS, WM8782SEDS/R (+25°C) | | | | | | |
| Full Scale Input Signal Level (for ADC 0dB Input) | | | | 1.0 | | V _{rms} |
| Input resistance, using recommended external resistor network on p22. | | | | 10 | | kΩ |
| Input capacitance | | | | 20 | | pF |
| Signal to Noise Ratio (see Terminology note 1,2,4) | SNR | weighted, @ fs = 48kHz | 93 | 100 | | dB |
| | | Unweighted, @ fs = 48kHz | | 98 | | dB |
| | | weighted, @ fs = 48kHz, AVDD = 3.3V | | 98 | | dB |
| Signal to Noise Ratio (see Terminology note 1,2,4) | SNR | weighted, @ fs = 96kHz | | 98 | | dB |
| | | Unweighted, @ fs = 96kHz | | 98 | | dB |
| | | weighted, @ fs = 96kHz AVDD = 3.3V | | 98 | | dB |
| Total Harmonic Distortion | THD | 1kHz, -1dB Full Scale @ fs = 48kHz | | -93 | | dB |
| | | 1kHz, -1dB Full Scale @ fs = 96kHz | | -93 | | dB |
| | | 1kHz, -1dB Full Scale @ fs = 192kHz | | -92 | | dB |
| Dynamic Range | DNR | -60dBFS | 93 | 100 | | dB |
| Channel Separation (see Terminology note 4) | | 1kHz Input | | 90 | | dB |
| Channel Level Matching | | 1kHz signal | | 0.1 | | dB |
| Channel Phase Deviation | | 1kHz signal | | 0.0001 | | Degree |
| Power Supply Rejection Ratio | PSRR | 1kHz 100mVpp, applied to AVDD, DVDD | | 50 | | dB |

Test Conditions

DVDD = 3.3V, AVDD = 5.0V, $T_A = +25^{\circ}\text{C}$, 1kHz signal, A-weighted, $f_s = 48\text{kHz}$, MCLK = 256fs, 24-bit audio data, Slave Mode unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------|--------------------------------|--------------------------|-----------|--------------------------|---------------|
| Digital Logic Levels (TTL Levels) | | | | | | |
| Input LOW level | V_{IL} | | | | 0.8 | V |
| Input HIGH level | V_{IH} | | 2.0 | | | V |
| Input leakage current – digital pad | | | -1 | ± 0.2 | +1 | μA |
| Input leakage current – digital tristate input (Note 3) | | | | 85 | | μA |
| Input capacitance | | | | 5 | | pF |
| Output LOW | V_{OL} | $I_{OL} = 1\text{mA}$ | | | $0.1 \times \text{DVDD}$ | V |
| Output HIGH | V_{OH} | $I_{OH} = -1\text{mA}$ | $0.9 \times \text{DVDD}$ | | | V |
| Analog Reference Levels | | | | | | |
| Midrail Reference Voltage | VMID | AVDD to VMID and VMID to VREFN | -4% | AVDD/2 | +4% | V |
| Potential Divider Resistance | R_{VMID} | | | 70 | | k Ω |
| Buffered Reference Voltage | VREFP | | -4% | AVDD/2 | +4% | V |
| VREF source current | I_{VREF} | | | | 5 | mA |
| VREF sink current | I_{VREF} | | | | 5 | mA |
| Supply Current | | | | | | |
| Analogue supply current | | AVDD = 5V | | 26 | | mA |
| Digital supply current | | DVDD = 3.3V | | 5 | | mA |
| Power Down | | | | 0.5 | | mA |

Notes:

1. All performance measurements are done with a 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although this is not audible, it may affect dynamic specification values.
2. VMID is decoupled with 10 μF and 0.1 μF capacitors close to the device package. Smaller capacitors may reduce performance.
3. This high leakage current is due to the topology of the instate pads. The pad input is connected to the midpoint of an internal resistor string to pull input to vmid if undriven.

TERMINOLOGY

1. Signal-to-noise ratio (dB) – Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, over a 20Hz to 20kHz bandwidth. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) – DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB = -32dB, DR = 92dB).
3. THD+N (dB) – THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) – Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

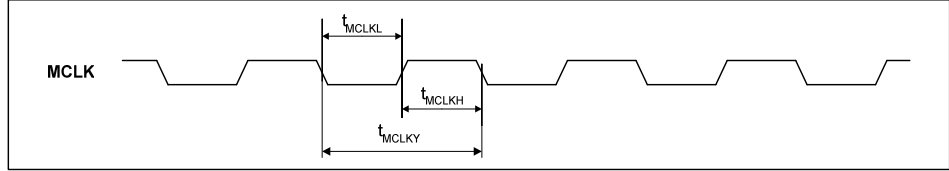


Figure 1 System Clock Timing Requirements

Test Conditions

DVDD = 3.3V, DGND = 0V, $T_A = +25^\circ\text{C}$, $f_s = 48\text{kHz}$, Slave Mode, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|--|--------------|-------|-----|-------|------|
| System Clock Timing Information | | | | | |
| MCLK System clock pulse width high | T_{MCLKL} | 11 | | | ns |
| MCLK System clock pulse width low | T_{MCLKH} | 11 | | | ns |
| MCLK System clock cycle time | T_{MCLKY} | 28 | | | ns |
| MCLK duty cycle | T_{MCLKDS} | 40:60 | | 60:40 | |

Table 1 Master Clock Timing Requirements

AUDIO INTERFACE TIMING – MASTER MODE

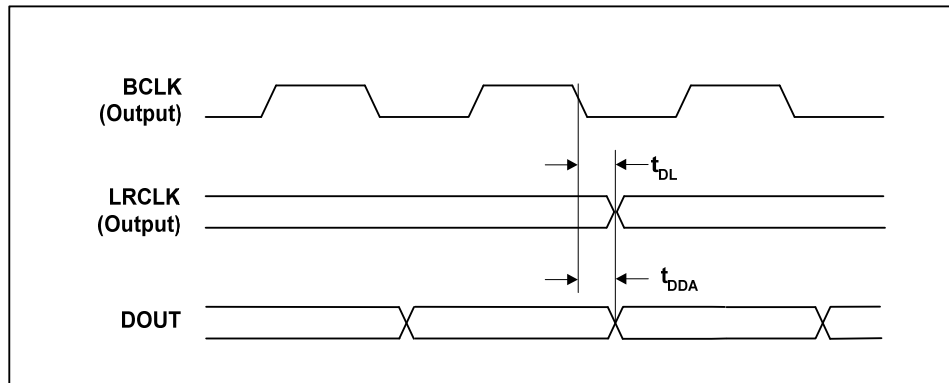


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DVDD = 3.3V, DGND = 0V, $T_A = +25^\circ\text{C}$, Master Mode, $f_s = 48\text{kHz}$, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|--|-----------|-----|-----|-----|------|
| Audio Data Input Timing Information | | | | | |
| LRCLK propagation delay from BCLK falling edge | t_{DL} | 0 | | 10 | ns |
| DOUT propagation delay from BCLK falling edge | t_{DDA} | 0 | | 10 | ns |

Table 2 Digital Audio Data Timing – Master Mode

AUDIO INTERFACE TIMING – SLAVE MODE

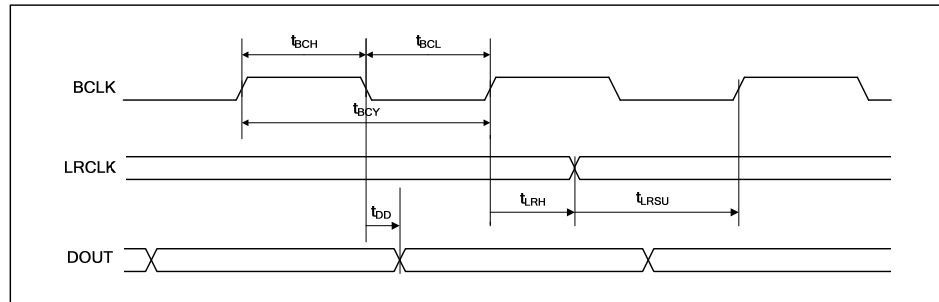


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DVDD = 3.3V, DGND = 0V, $T_A = +25^{\circ}\text{C}$, Slave Mode, $f_s = 48\text{kHz}$, $\text{MCLK} = 256\text{fs}$, 24-bit data, unless otherwise stated.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|------------|-----|-----|-----|------|
| Audio Data Input Timing Information | | | | | |
| BCLK cycle time | t_{BCY} | 50 | | | ns |
| BCLK pulse width high | t_{BCH} | 20 | | | ns |
| BCLK pulse width low | t_{BCL} | 20 | | | ns |
| LRCLK set-up time to BCLK rising edge | t_{LRSU} | 10 | | | ns |
| LRCLK hold time from BCLK rising edge | t_{LRH} | 10 | | | ns |
| DOUT propagation delay from BCLK falling edge | t_{DD} | 0 | | 10 | ns |

Table 3 Digital Audio Data Timing – Slave Mode

Note:

LRCLK should be synchronous with MCLK.

SLAVE MODE MCLK / BCLK TIMING

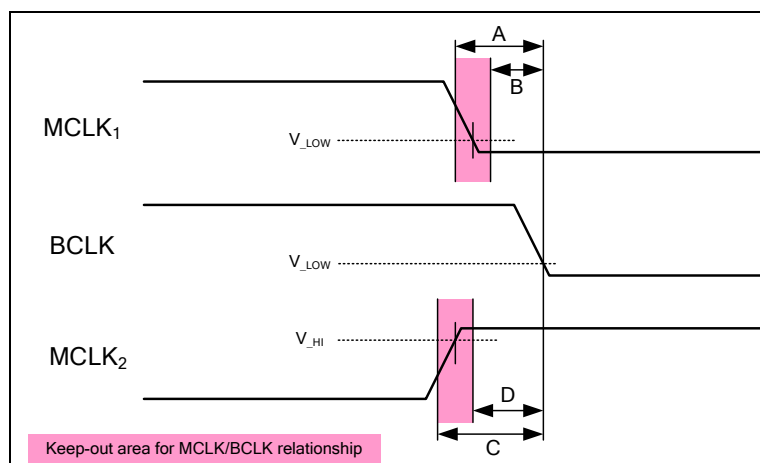


Figure 4 MCLK / BCLK prohibited timing relationship in slave mode

| TIMING | TIME (ns) | DESCRIPTION |
|--------|-----------|--|
| A | 9 | MCLK falling edge to BCLK falling edge keep-out window |
| B | 4 | |
| C | 9 | MCLK rising edge to BCLK falling edge keep-out window |
| D | 4 | |

Table 4 Prohibited area timings

In slave mode operation, there are two windows where the BCLK falling edge relative to the MCLK falling/rising edge is not allowed, as defined in Figure 4 and Table 4. Any device with clocks operating in this area may cause incorrect operation of the ADC, as detailed in WTR0444.

This specification is guaranteed by design rather than test, and the timings are related to the switching level of the MCLK and BCLK pads. Simulation has shown the switching level range for both the MCLK and BCLK pads across process, voltage and temperature to be as per the table below.

| SWITCHING LEVEL | MIN (V) | MAX (V) |
|------------------|---------|---------|
| V _{LOW} | 1.1 | 1.4 |
| V _{HI} | 1.3 | 1.6 |

Table 5 Simulated switching area range

If the above timing constraints cannot be met in slave mode, it is recommended that WM8782A silicon is used in place of WM8782.

DEVICE DESCRIPTION

INTRODUCTION

The WM8782 is a stereo 24-bit ADC designed for demanding recording applications such as DVD recorders, studio mixers, PVRs, and AV amplifiers. The WM8782 consists of stereo line level inputs, followed by a sigma-delta modulator and digital filtering.

The device offers stereo line level inputs along with two control input pins (FORMAT, IWL) to allow operation of the audio interface in three industry standard modes (left justified, right justified or I²S). An internal op-amp is integrated on the front end of the chip to accommodate analogue input signals greater than 1V_{rms}. The device also has a high pass filter to remove residual DC offsets.

The WM8782 offers Master or Slave mode clocking schemes. A control input pin M/S is used to allow Slave mode or Master mode operation. The WM8782 supports master clock rates from 128fs to 768fs and digital audio output word lengths from 16-24 bits. Sampling rates from 8kHz to 192kHz are supported, delivering high SNR operating with 128x, 64x or 32x over-sampling, according to the sample rate.

The line inputs are biased internally through the operational amplifier to V_{MID}.

ADC

The WM8782 uses a multi-bit over sampled sigma-delta ADC. A single channel of the ADC is illustrated in Figure 5.

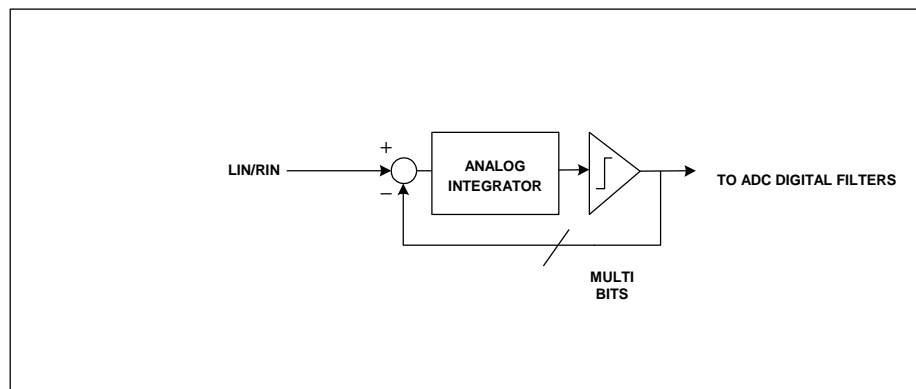


Figure 5 Multi-Bit Oversampling Sigma Delta ADC Schematic

The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise.

The ADC Full Scale input is 1.0V rms at AVDD = 5.0 volts. Any input voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input has a linear relationship with AVDD. The internal op-amp and appropriate resistors can be used to reduce signals greater than 1Vrms before they reach the ADC.

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface.

ADC OUTPUT PHASE

In the input to output data-path, the digital output data DOUT, is a phase inverted representation of the analogue input signal.

ADC DIGITAL FILTER

The ADC digital filters contain a digital high pass filter. The high-pass filter response detailed in Digital Filter Characteristics. The operation of the high pass filter removes residual DC offsets that are present on the audio signal.

DIGITAL AUDIO INTERFACE

The digital audio interface uses three pins:

- DOUT: ADC data output
- LRCLK: ADC data alignment clock
- BCLK: Bit clock, for synchronisation

The digital audio interface takes the data from the internal ADC digital filters and places it on DOUT and LRCLK. DOUT is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. LRCLK is an alignment clock that controls whether Left or Right channel data is present on the DOUT line. DOUT and LRCLK are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. DOUT is always an output. BCLK and LRCLK may be inputs or outputs depending whether the device is in Master or Slave mode. (see Master and Slave Mode Operation, below).

Three different audio data formats are supported:

- Left justified
- Right justified
- I²S

MASTER AND SLAVE MODE OPERATION

The WM8782 can be configured as either a master or slave mode device. As a master device the WM8782 generates BCLK and LRCLK and thus controls sequencing of the data transfer on DOUT. In slave mode, the WM8782 responds with data to clocks it receives over the digital audio interface. The mode can be selected by setting the MS input pin (see Table 6 Master/Slave selection below). Master and slave modes are illustrated below.

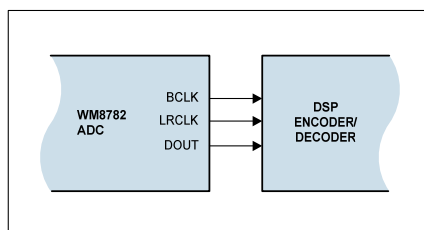


Figure 6 Master Mode

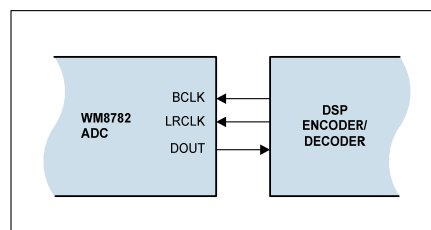


Figure 7 Slave Mode

| PIN | DESCRIPTION |
|-----|---|
| M/S | Master/Slave Selection 0 = Slave Mode 1 = Master Mode |

Table 6 Master/Slave selection

AUDIO INTERFACE CONTROL

The Input Word Length and Audio Format mode can be selected by using IWL and FORMAT pins.

| PIN | DESCRIPTION |
|--------|---|
| IWL | Word Length 0 = 16 bit 1 = 20 bit Z = 24 bit |
| FORMAT | Audio Mode Select 0 = RJ 1 = LJ Z = I2S |

Table 7 Audio Data Format Control

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

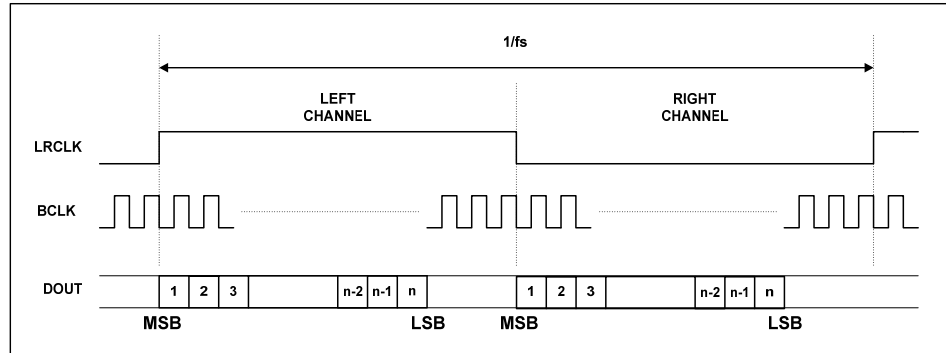


Figure 8 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

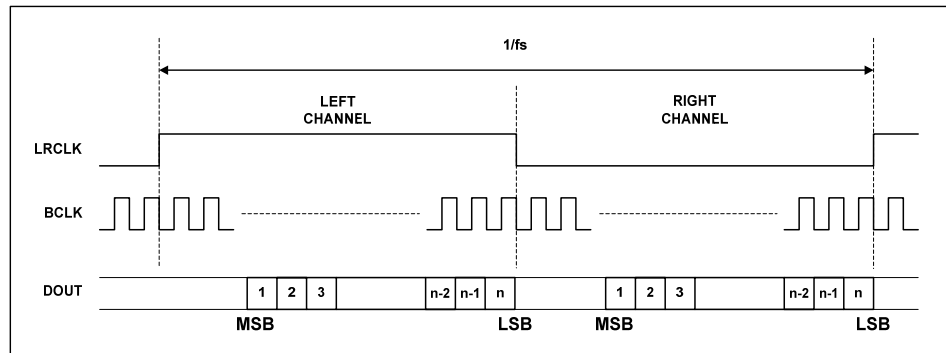


Figure 9 Right Justified Audio Interface (assuming n-bit word length)

In I²S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

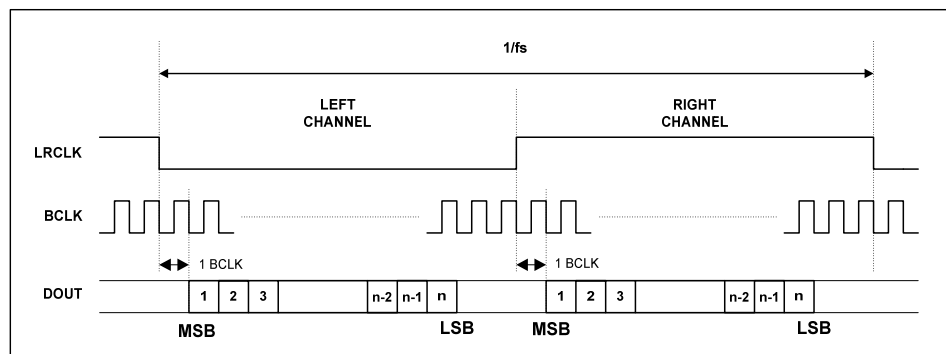


Figure 10 I²S Audio Interface (assuming n-bit word length)

MASTER CLOCK AND AUDIO SAMPLE RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock (MCLK). The external master system clock can be applied directly through the MCLK input pin. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the ADC.

The master clock is used to operate the digital filters and the noise shaping circuits. The WM8782 supports master clocks of 128fs, 192fs, 256fs, 384fs, 512fs and 768fs, where fs is the audio sampling frequency (LRCLK). In Slave Mode, the WM8782 automatically detects the audio sample rate. In Master Mode, LRCLK is generated for rate 256fs, unless the user changes this to 128fs using the FSAMPEN pin = z (see Table 9 below). BCLK is also generated in Master Mode. BCLK=MCLK/4 for 256fs, and BCLK=MCLK/2 for 128fs.

Table 8 shows the common MCLK frequencies for different sample rates.

| SAMPLING RATE (LRCLK) | Master Clock Frequency (MHz) | | | | | |
|--------------------------|------------------------------|--------|---------|---------|---------|---------|
| | 128fs | 192fs | 256fs | 384fs | 512fs | 768fs |
| 8kHz | 1.024 | 1.536 | 2.048 | 3.072 | 4.096 | 6.144 |
| 16kHz | 2.048 | 3.072 | 4.096 | 6.144 | 8.192 | 12.288 |
| 32kHz | 4.096 | 6.144 | 8.192 | 12.288 | 16.384 | 24.576 |
| 44.1kHz | 5.6448 | 8.467 | 11.2896 | 16.9340 | 22.5792 | 33.8688 |
| 48kHz | 6.144 | 9.216 | 12.288 | 18.432 | 24.576 | 36.864 |
| 96kHz | 12.288 | 18.432 | 24.576 | 36.864 | - | - |
| 192kHz | 24.576 | 36.864 | - | - | - | - |

Table 8 Master Clock Frequency Selection

In Slave mode, the WM8782 has a master detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 system clocks). If there is a greater than 32 clocks error the interface sets itself to the highest rate available (768fs). There must be a fixed number of MCLKS per LRCLK, although the WM8782 is tolerant of phase variations or jitter on these clocks.

FSAMPEN

The FSAMPEN pin controls the over sampling rate of the ADC. The WM8782 can operate at sample rates from 8kHz to 192kHz. The WM8782 uses a sigma-delta modulator that operates at an optimal frequency of 6.144MHz.

By default the WM8782 generates the ADC frequency at 128xOSR. At fs=48kHz, the ADC frequency is 128xOSR = 128x48kHz = 6.144MHz.

If fs=96kHz, the FSAMPEN pin must be set to 1. In this case, the ADC frequency is 64xOSR = 64x96kHz = 6.144MHz.

If fs=192kHz, the FSAMPEN pin must be set to z. In this case, the ADC frequency is 32xOSR = 32x192kHz = 6.144MHz.

It is recommended that the above settings are used for both master and slave mode.

| PIN | DESCRIPTION |
|---------|--|
| M/S | Master/Slave Selection 0 = Slave Mode (128fs, 192fs, 256fs, 384fs, 512fs, 768fs) 1 = Master Mode (256fs, 128fs when FSAMPEN=z) |
| FSAMPEN | Fast sampling rate enable 0 = 48ken (128x OSR) 1 = 96ken (64x OSR) z = 192ken (32x OSR) |

Table 9 Master/Slave and Sampling Rate Enable Selection

POWER DOWN CONTROL

The WM8782 can be powered down by stopping MCLK. Power down mode using MCLK is entered after 65536/fs clocks. On power-up, the WM8782 applies the power-on reset sequence described below.

When MCLK is stopped DOUT is forced to zero.

POWER ON RESET

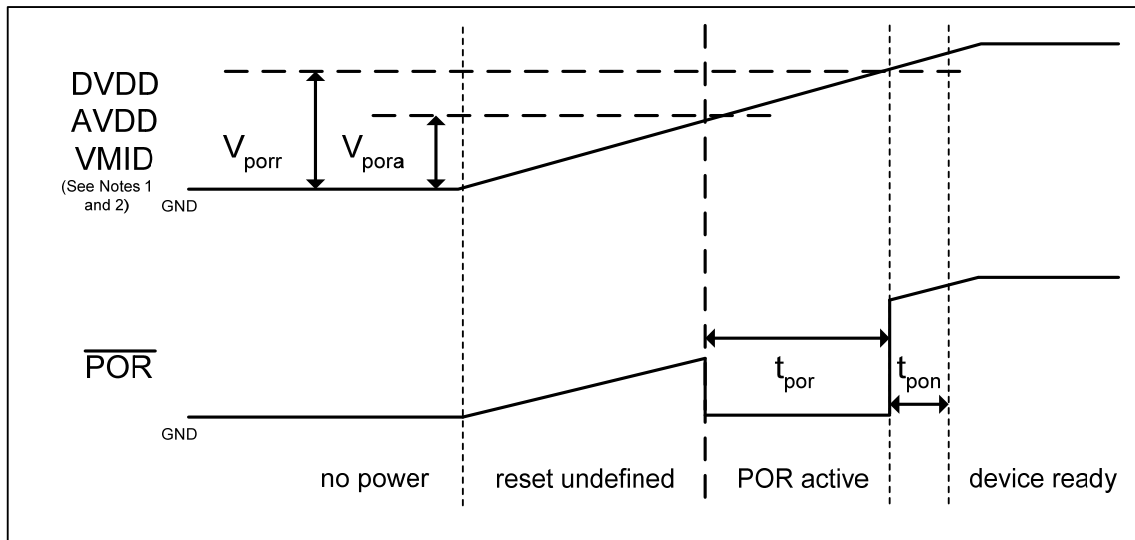


Figure 11 Power Supply Timing Requirements – Power-on

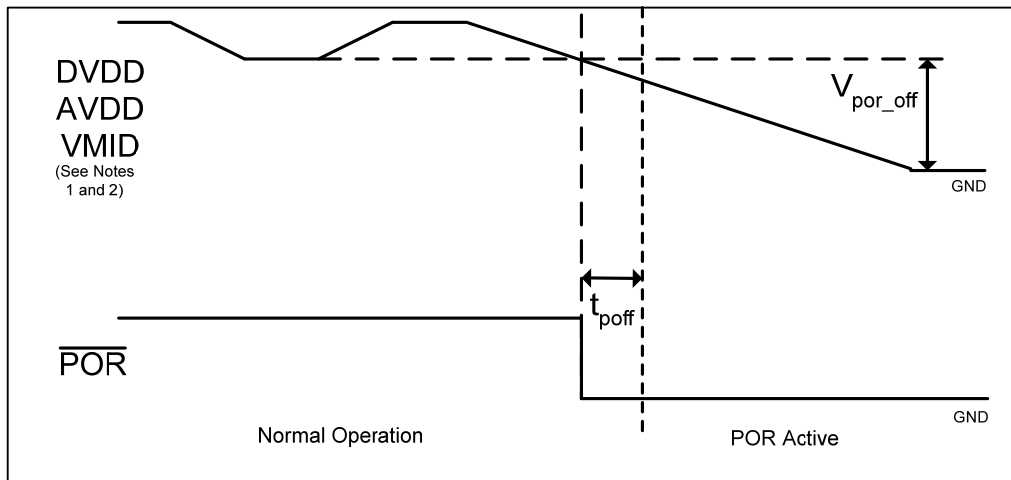


Figure 12 Power Supply Timing Requirements – Power-down

Test ConditionsAVDD = 5V, DVDD = 3.3V, AGND = DGND = 0V, T_A = +25°C

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------|---|----------------|---|-----|------|
| Power Supply Input Timing Information | | | | | | |
| DVDD level to activate POR – power on | V _{pora} | Measured from DGND | | 0.7 | | V |
| AVDD level to activate POR – power on | V _{pora} | Measured from AGND | | 0.7 | | V |
| VMID level to activate POR – power on | V _{pora} | Measured from AGND | | 0.7 | | V |
| DVDD level to release POR – power on (see notes 1 and 2) | V _{porr} | Measured from DGND | | DVDD Min | | V |
| AVDD level to release POR – power on (see notes 1 and 2) | V _{porr} | Measured from AGND | | AVDD Min | | V |
| VMID level to release POR – power on (see notes 1 and 2) | V _{porr} | Measured from AGND | | 1 | | V |
| POR active period (see notes 1 and 2) | t _{por} | Measured from POR active to POR release | 30 (note 6) | Defined by DVDD/AVDD/ VMID Rise Time | | μs |
| DVDD level to activate POR – power off (see note 5) | V _{por_off} | Measured from DGND | | 0.8 | | V |
| AVDD level to activate POR – power off (see note 5) | V _{por_off} | Measured from AGND | | 0.8 | | V |
| VMID level to activate POR – power off (see note 5) | V _{por_off} | Measured from AGND | | 0.7 | | V |
| Power on – POR propagation delay through device | t _{pon} | Measured from rising EDGE of POR | | 30 | | μs |
| Power down – POR propagation delay through device | t _{poff} | Measured from falling EDGE of POR | | 30 | | μs |

Notes:

- POR is activated when DVDD or AVDD or VMID reach their stated V_{pora} level (Figure 11)
- POR is only released when DVDD and AVDD and VMID have all reached their stated V_{porr} levels (Figure 11).
- The rate of rise of VMID depends on the rate of rise of AVDD, the internal 50kΩ resistance and the external decoupling capacitor. Typical tolerance of 50K resistor can be taken as +/-20%.
- If AVDD, DVDD or VMID suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{por_off}), then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
- The chip will enter reset at power down when AVDD or DVDD or VMID falls below V_{por_off}. This may be important if the supply is turned on and off frequently by a power management system.
- The minimum t_{por} period is maintained even if DVDD, AVDD and VMID have zero rise time. This specification is guaranteed by design rather than test.

DIGITAL FILTER CHARACTERISTICS

The WM8782 digital filter characteristics scale with sample rate.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|----------|----------|----------|------|
| ADC Sample Rate (Single Rate – 48Hz typically) | | | | | |
| Passband | +/- 0.01dB | 0 | | 0.4535fs | |
| | -6dB | | 0.4892fs | | |
| Passband Ripple | | | | +/- 0.01 | dB |
| Stopband | | 0.5465fs | | | |
| Stopband Attenuation | f > 0.5465fs | -65 | | | dB |
| Group Delay | | | 22 | | fs |
| ADC Sample Rate (Dual Rate – 96kHz typically) | | | | | |
| Passband | +/- 0.01dB | 0 | | 0.4535fs | |
| | -6dB | | 0.4892fs | | |
| Passband Ripple | | | | +/- 0.01 | dB |
| Stopband | | 0.5465fs | | | |
| Stopband Attenuation | f > 0.5465fs | -65 | | | dB |
| Group Delay | | | 22 | | fs |

Table 10 Digital Filter Characteristics

ADC FILTER RESPONSES

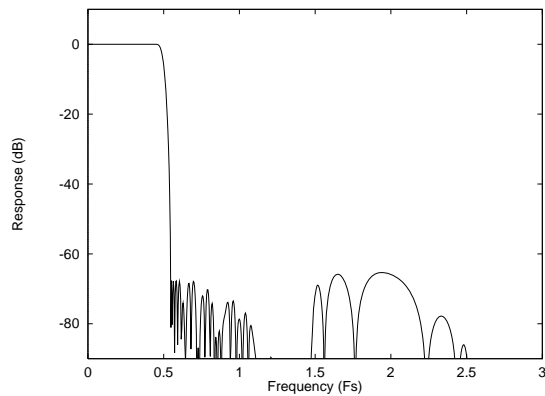


Figure 13 Digital Filter Frequency Response

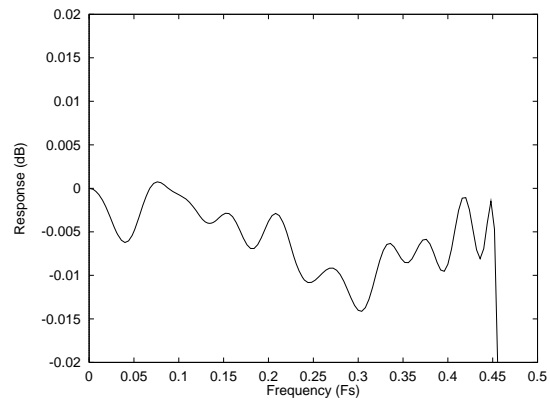


Figure 14 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8782 has a digital highpass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

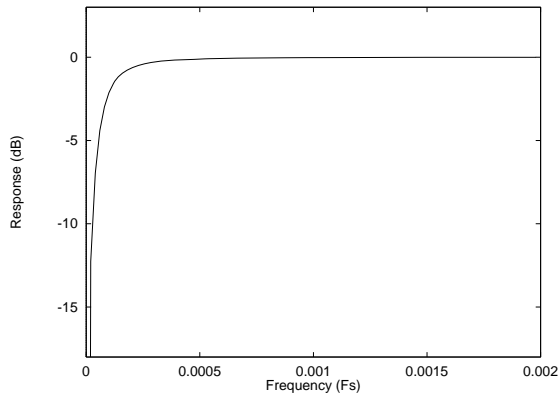


Figure 15 ADC Highpass Filter Response

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

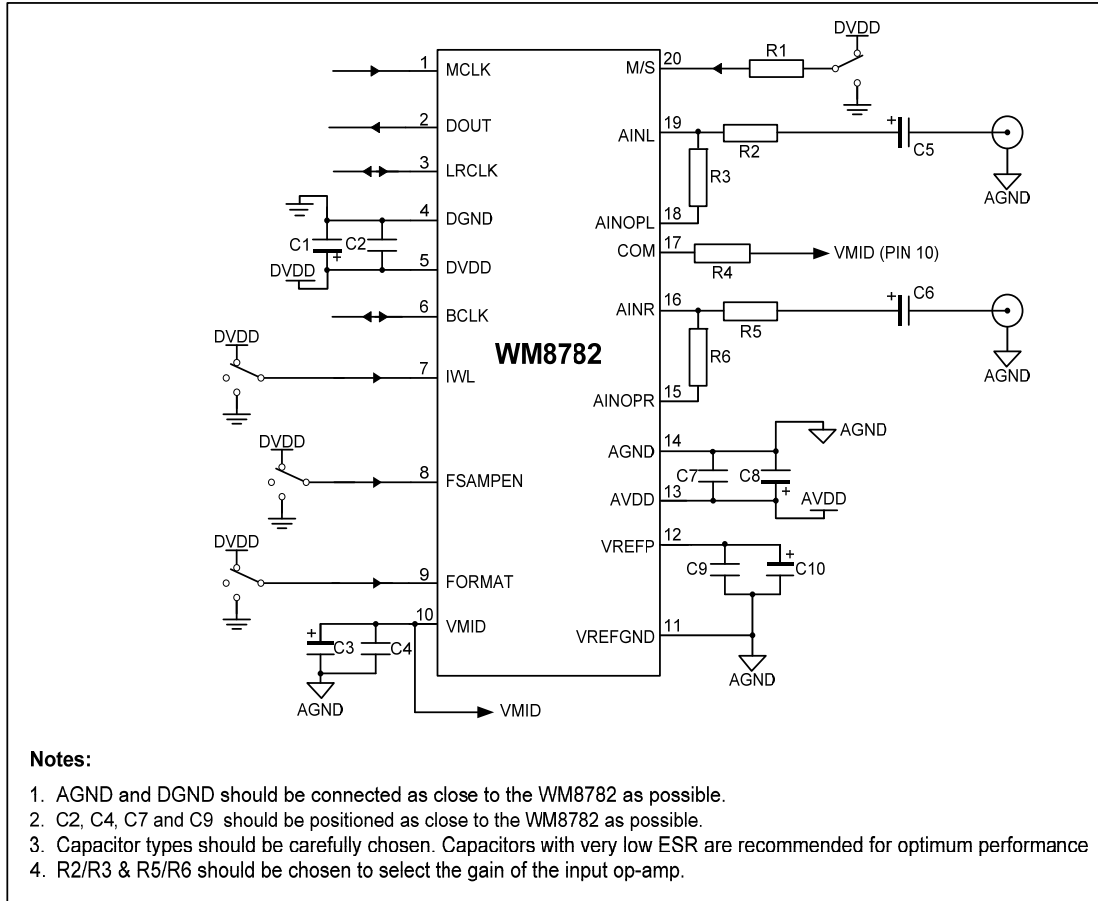


Figure 16 External Components Diagram

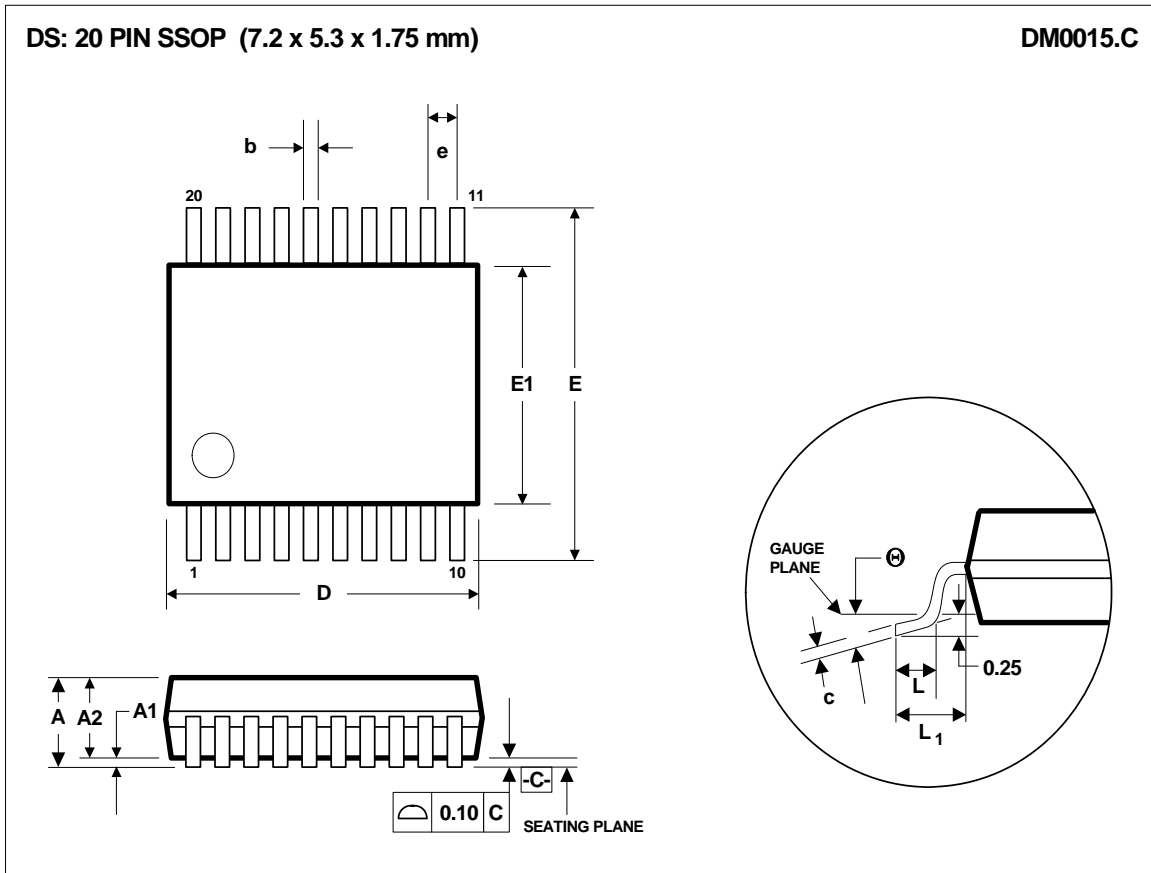
RECOMMENDED EXTERNAL COMPONENTS VALUES

| COMPONENT REFERENCE | SUGGESTED VALUE | DESCRIPTION |
|---------------------|-----------------|--|
| C1 and C8 | 10µF | De-coupling for DVDD and AVDD |
| C2 and C7 | 0.1µF | De-coupling for DVDD and AVDD |
| C5 and C6 | 10µF | Analogue input AC coupling caps |
| R1 | 10kΩ | Current limiting resistors |
| R2 and R5 | 10kΩ | Internal op-amp input resistor |
| R3 and R6 | 5kΩ | Internal op-amp feedback resistor |
| R4 | 3.3kΩ | Common mode resistor |
| C4 | 0.1µF | Reference de-coupling capacitors for VMID pin |
| C3 | 10µF | |
| C9 | 0.1µF | Reference de-coupling capacitors for VREFP pin |
| C10 | 10µF | |

Table 11 External Components Description

The above Table 11 shows resistor values which will give a gain of 0.5. This assumes an input signal of 2Vrms to C4 and C5.

PACKAGE DIMENSIONS



| Symbols | Dimensions (mm) | | |
|----------------|------------------|------|------|
| | MIN | NOM | MAX |
| A | ---- | ---- | 2.0 |
| A ₁ | 0.05 | ---- | ---- |
| A ₂ | 1.65 | 1.75 | 1.85 |
| b | 0.22 | 0.30 | 0.38 |
| c | 0.09 | ---- | 0.25 |
| D | 6.90 | 7.20 | 7.50 |
| e | 0.65 BSC | | |
| E | 7.40 | 7.80 | 8.20 |
| E ₁ | 5.00 | 5.30 | 5.60 |
| L | 0.55 | 0.75 | 0.95 |
| L ₁ | 1.25 REF | | |
| θ | 0° | 4° | 8° |
| REF: | JEDEC.95, MO-150 | | |

- NOTES:
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
 D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.