Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

TEXAS INSTRUMENTS

CY74FCT2245T

SCCS037 - July 1994 - Revised March 2000

8-Bit Transceiver

Features

- **Function and pinout compatible with FCT and F logic**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 4.1 ns max.**
  FCT-A speed at 4.6 ns max.
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 12 mA**
  Source current 15 mA
- **Extended commercial temp. range of –40˚C to +85˚C**
- **Three-state outputs**

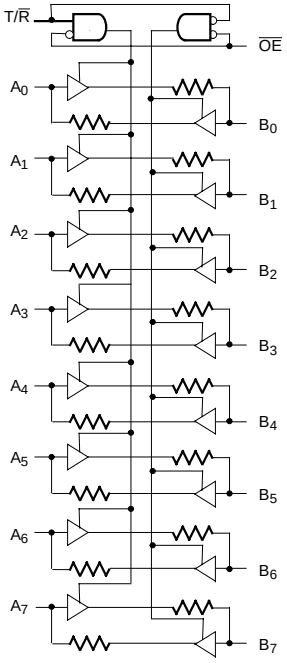
Functional Description

The FCT2245T contains eight non-inverting, bidirectional buffers with three-state outputs intended for bus oriented applications. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. For this reason, the FCT2245T can be used in an existing design to replace the FCT245T. The FCT2245T current sinking capability is 12 mA at the A and B ports.

The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (Active HIGH) enables data from A ports to B ports; receive (Active LOW) enables data from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both the A and B ports by putting them in a High Z condition.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

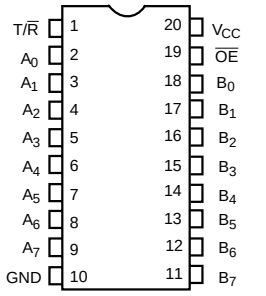
Logic Block Diagram



FCT2245T–1

Pin Configurations

DIP/SOIC/QSOP
Top View



FCT2245T–3

Function Table[1]

Inputs		Output
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

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Maximum Ratings[2,3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Input Voltage.....–0.5V to +7.0V

DC Output Voltage.....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....120 mA

Power Dissipation 0.5W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	T, AT, CT	–40°C to +85°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–15 mA	Com'l	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=12 mA	Com'l		0.3	0.55	V
R_{OUT}	Output Resistance	V_{CC}=Min., I_{OL}=12 mA	Com'l	20	25	40	Ω
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		–60	–120	–225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25˚C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $T/\overline{R}=\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $T/\overline{R}=\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $T/\overline{R}=\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $T/\overline{R}=\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $T/\overline{R}=\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics—Over the Operating Range[12]

Parameter	Description	FCT2245T Commercial		FCT2245AT Commercial		FCT2245CT Commercial		Unit	Fig. No.[13]
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.5	7.0	1.5	4.6	1.5	4.1	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	9.5	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.5	1.5	5.0	1.5	4.5	ns	1, 7, 8

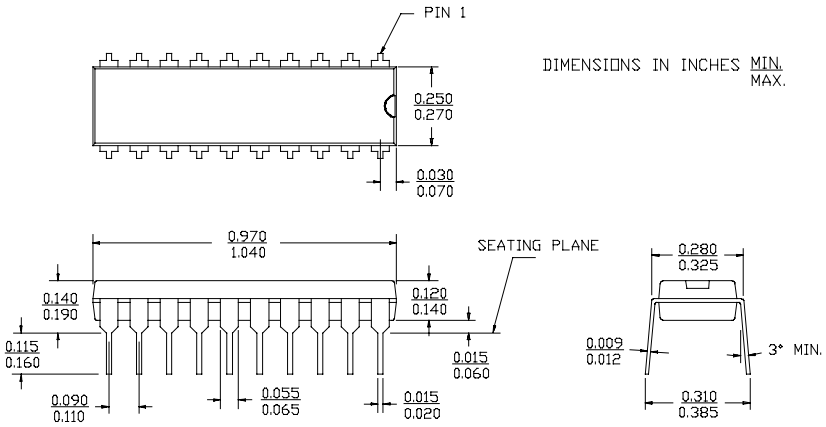
Ordering Information—FCT2245T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT2245CTQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2245CTSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	
4.6	CY74FCT2245ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2245ATQCT	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2245ATSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	
7.5	CY74FCT2245TQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2245TSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	

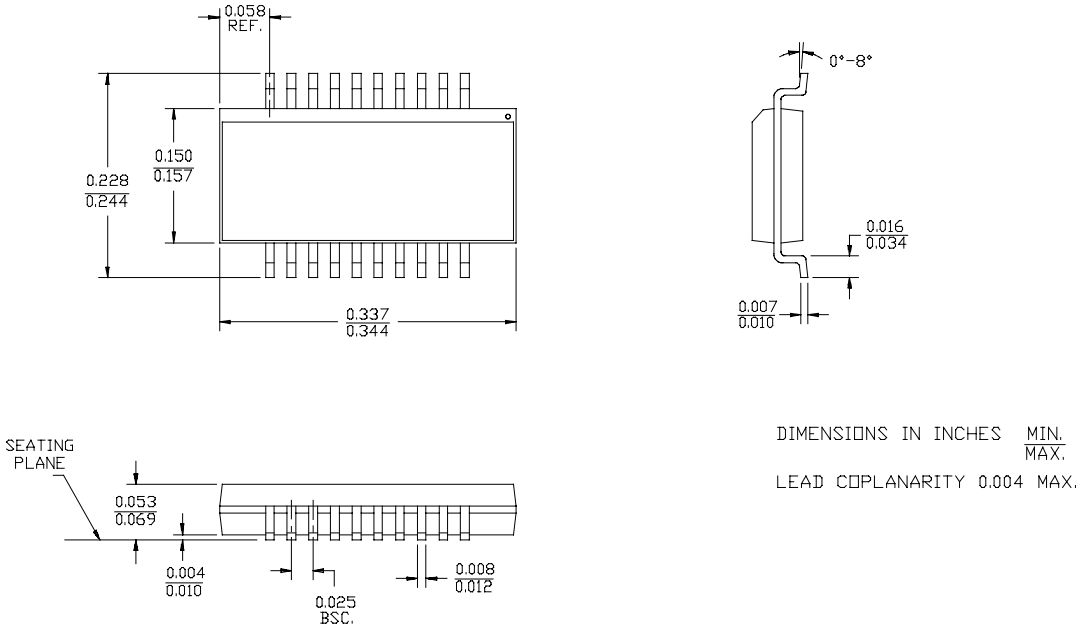
Notes:
12. Minimum limits are specified but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.

Package Diagrams

20-Lead (300-Mil) Molded DIP P5

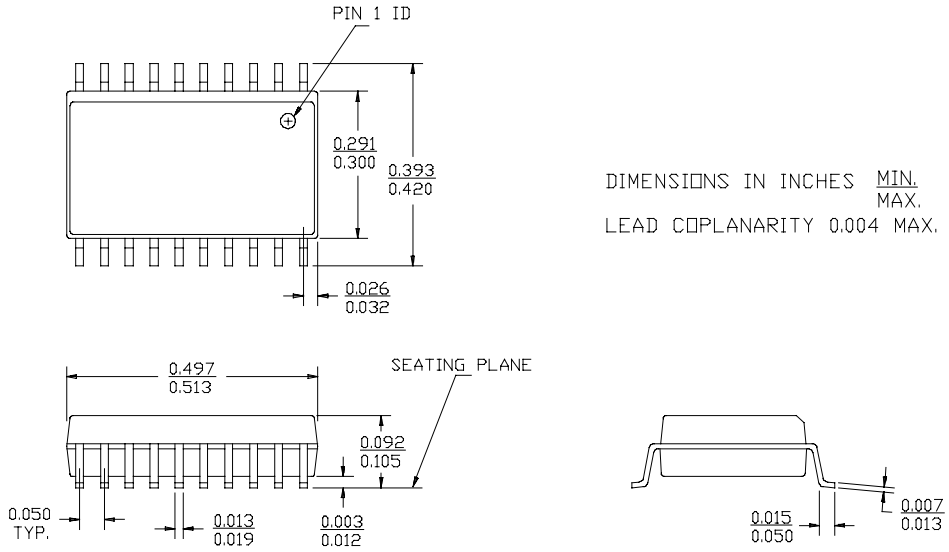


20-Lead Quarter Size Outline Q5



Package Diagrams (continued)

20-Lead (300-Mil) Molded SOIC S5



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