Product Summary

VSC8123

10Mb/s to 2.7Gb/s Rate Agile, Adaptive Clock and Data Recovery

Features

- Continuous NRZ Frequency Coverage from 10Mb/s to 2.7Gb/s data rates
- Programmable Acquisition and Tuning of Frequency, Phase and Voltage—No Reference Clock Required
- Built-In Bit Level Error Rate Monitoring Operates Independently of In-Service Data Channel
- User-Definable Control Algorithms for Acquisition, Tracking, and Error Profiling
- Integrated High-Gain AGC Front End with Offset Correction and On-Die Termination
- Secondary High-Level Input for Backup Data Input or hint/LOS Clock
- 80-Pin PQFP Package

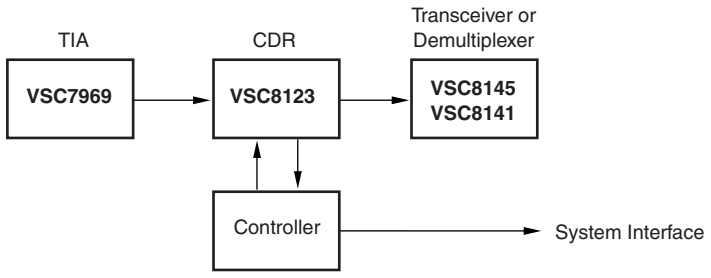
General Description

The VSC8123 is a universal clock and data recovery system designed for a broad range of system applications. The integrated frequency synthesizer provides continuous coverage from 10Mb/s to OC-48+FEC data rates with SONET quality output. In addition to its broadband capability, the VSC8123 is designed for the most demanding applications, where signal integrity is low and the absolute maximum voltage and timing margin is required. The VSC8123 offers signal acquisition capabilities far beyond what conventional CDRs offer, in a highly monolithic form.

In addition to the broadband synthesizer capability, the VSC8123 also has the ability to dynamically modify its acquisition point in both voltage and phase. This enables the VSC8123 to acquire data in the presence of significant symmetry distortion or "bad spots" in the data eye. Integrated voltage and phase adjustment is provided to offset the sampling point over the entire voltage and phase range of the input data eye. Additional circuitry is provided to measure relative bit-error rates without affecting the integrity of the active data stream. Using an external controller, the VSC8123 can acquire frequency, scan the incoming data eye and automatically set its position to optimize margin in both voltage and phase. This optimization can be one-time on power-up, or set to continuously repeat without taking the data stream off-line—no errors will be introduced into the output data stream as the chip tracks the center of the data eye.

Through the controller interface, the VSC8123 can provide telemetry on the condition of the incoming data eye and the quality of the acquisition without taking the data off-line, enabling eye profiling, Q-testing, signal strength measurements, and bit-level error detection/prediction—all non-invasively.

System Block Diagram



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