18V Dual Input Micropower PowerPath Prioritizer

FEATURES

- **Selects Highest Priority Valid Supply from Two Inputs**
- **Wide 1.8V to 18V Operating Range**
- **Internal Dual 2Ω, 0.5A Switches**
- **Low 3.6µA Operating Current**
- **Low 320nA V2 Current When V1 Connected to OUT**
- **Blocks Reverse and Cross Conduction Currents**
- **Reverse Supply Protection to –15V**
- V2 Freshness Seal/Ship Mode
- ±1.5% Accurate Adjustable Switchover Threshold
- Two Auxiliary ±2.3% Accurate Voltage Comparators
- Overcurrent and Thermal Protection
- Thermally Enhanced 10-Pin 3mm × 3mm DFN and 12-Lead Exposed Pad MSOP Packages

APPLICATIONS

- Low Power Battery Backup
- Portable Equipment
- Point-of-Sale (POS) Equipment

DESCRIPTION

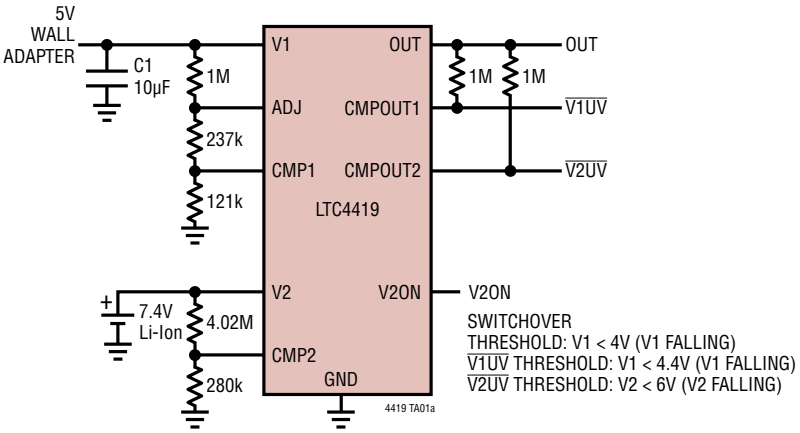
The LTC®4419 is a dual input monolithic PowerPath™ prioritizer with low operating current, that provides backup switchover for keeping critical circuitry alive during brown out and power loss conditions. Unlike diode-OR products, little current is drawn from the inactive supply even if its voltage is greater than the active supply.

Internal 2Ω, current limited PMOS switches provide power path selection from a primary input (V1) or a backup input (V2) to the output. An adjustable voltage monitor set via an external resistive divider provides flexibility in setting the V1 to V2 switchover threshold. When primary input V1 drops, the ADJ monitor input causes OUT to be switched to V2. Fast non-overlap switchover circuitry prevents both reverse and cross conduction while minimizing output droop.

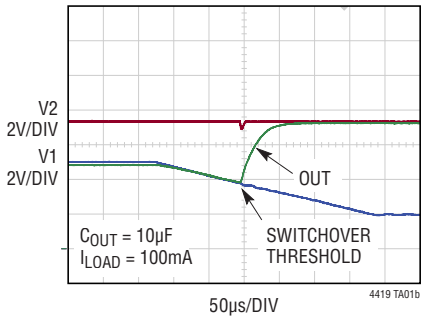
The LTC4419 has two auxiliary comparators with open-drain outputs that provide flexible voltage monitoring. The V2ON output indicates if V2 is powering OUT. Freshness seal mode prevents V2 battery discharge during storage or shipment.

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TYPICAL APPLICATION



Typical Switchover Waveforms



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Input Supply Voltage
- V1, V2 ..... –15V to 24V
- OUT ..... –0.3V to 24V
- OUT – V2 ..... –24V to 39V
- OUT – V1 ..... –24V to 39V

Input Voltages
- ADJ, CMP1, CMP2 (Note 3) ..... –0.3V to 24V

Output Voltages
- CMPOUT1, CMPOUT2, V2ON (Note 3) .. –0.3V to 24V

Pin Currents (Note 2)
- ADJ, CMP1, CMP2, CMPOUT1, CMPOUT2, V2ON ..... –1mA

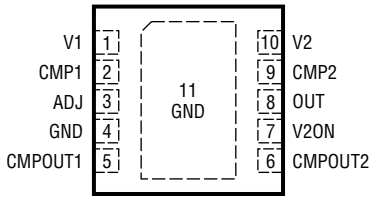
Operating Ambient Temperature Range
- LTC4419C ..... 0°C to 70°C
- LTC4419I ..... –40°C to 85°C

Junction Temperature (Notes 4, 5)..... 125°C

Storage Temperature Range ..... –65°C to 150°C

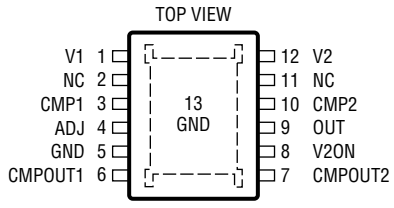
Lead Temperature (Soldering, 10 sec)
- MSOP Package ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LTC4419#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4419CDD#PBF	LTC4419CDD#TRPBF	LGMS	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4419IDD#PBF	LTC4419IDD#TRPBF	LGMS	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4419CMSE#PBF	LTC4419CMSE#TRPBF	4419	12-Lead Plastic Exposed Pad MSOP	0°C to 70°C
LTC4419IMSE#PBF	LTC4419IMSE#TRPBF	4419	12-Lead Plastic Exposed Pad MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V1 = 3.6V, V2 = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage and Currents							
V1, V2	Operating Voltage Range		●	1.8		18	V
I_{V1}	V1 Current, V1 Powering OUT V1 Current, V2 Powering OUT	I_{OUT} = 0, V1 = 8.4V, V2 = 3.6V V1 = 8.4V, V2 = 3.6V	● ●		3.6 500	6.3 800	µA nA
I_{V2}	V2 Current, V2 Powering OUT V2 Current, V1 Powering OUT V2 Current in Freshness Seal Mode	I_{OUT} = 0, V1 = 3.6V, V2 = 8.4V V1 = 3.6V, V2 = 8.4V V1 = GND, V2 = 5V	● ● ●		3.3 320 120	6 650 220	µA nA nA
R_{ON}	Switch Resistance	V1 = V2 = 5V, I_{OUT} = –100mA	●	1	2	5	Ω
$t_{VALID(V1)}$	Input Qualification Time	V1 Rising, ADJ Rising	●	34	64	94	ms
Input Comparators							
V_{THA}	ADJ Threshold	ADJ Falling	●	1.032	1.047	1.062	V
V_{HYSTA}	ADJ Comparator Hysteresis	ADJ Rising	●	30	50	70	mV
V_{THC}	CMP1, CMP2 Threshold	CMP1, CMP2 Falling	●	0.378	0.387	0.396	V
V_{HYSTC}	CMP1, CMP2 Hysteresis	CMP1, CMP2 Rising	●	7.5	10	12.5	mV
t_{PDA}	ADJ Comparator Falling Response Time	10% Overdrive	●	4	7.3	12	µs
t_{PDC}	CMP1, CMP2 Comparator Response Times	20% Overdrive	●		30	65	µs
Power Path Function							
I_{LIM}	Output Current Limit	V1, V2 = 8.4V	●	0.5	1.1	1.6	A
V_{REV}	Reverse Comparator Threshold	(V1, V2) – V_{OUT} for Power Path Turn-On	●	25	50	75	mV
t_{SWITCH}	Break-Before-Make Switchover Time	V1 = V2 = 5V, I_{OUT} < –10mA	●	1	2.5	5	µs
I/O Specifications							
V_{OL}	Output Voltage Low, CMPOUT1, CMPOUT2 and V2ON	I = 100µA I = 1mA	● ●		15 120	50 250	mV mV
V_{OH}	V2ON Output High Voltage	I = –1µA, V2 = 5V	●	1.05	1.65	2.3	V
I_{OH}	CMPOUT1, CMPOUT2 and V2ON, Output High Leakage	CMPOUT1, CMPOUT2, V2ON = 18V	●		±50	±150	nA
$I_{PU(V2ON)}$	V2ON Pull-Up Current	V2 = 5V, ADJ = 0V, V2ON = 0V	●	–2.7	–5	–8	µA
I_{LEAK}	ADJ, CMP1, CMP2 Leakage Current	ADJ, CMP1, CMP2 = 0V, 1.5V	●		±1	±5	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 3: These pins can be tied to voltages down to –5V through a resistor that limits the current to less than –1mA.

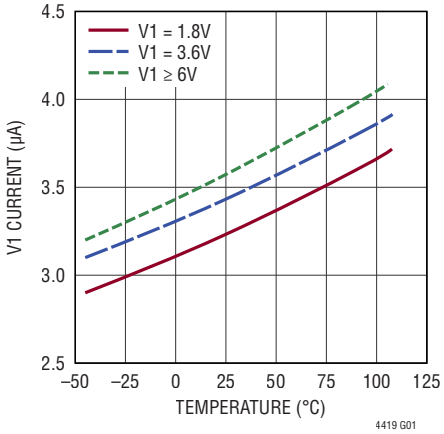
Note 4: The LTC4419 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: The LTC4419 is tested under pulsed load conditions such that $T_J \approx T_A$. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

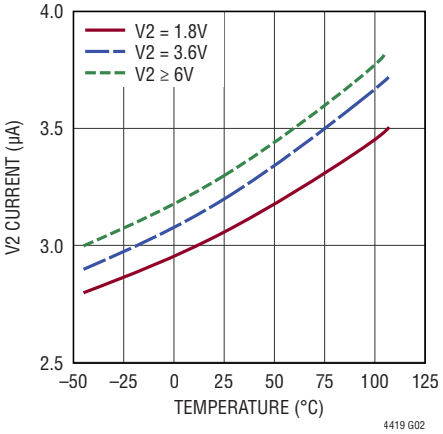
$$T_J = T_A + (P_D \bullet \theta_{JA})$$

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, V1 = V2 = 3.6V unless otherwise indicated).

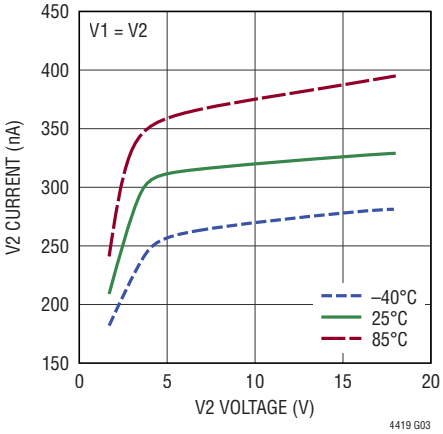
V1 Current, V1 Powers OUT (I_{OUT} = 0)



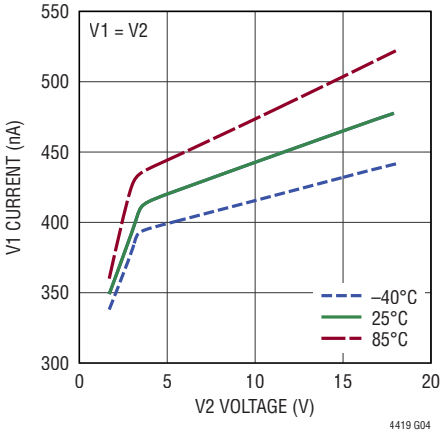
V2 Current, V2 Powers OUT (I_{OUT} = 0)



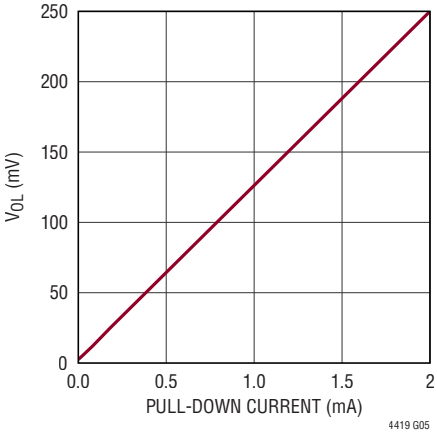
V2 Current, V1 Powers OUT



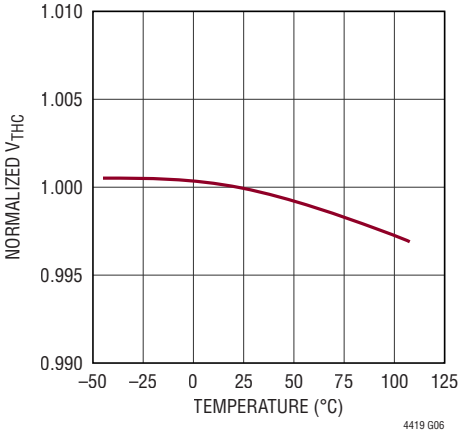
V1 Current, V2 Powers OUT



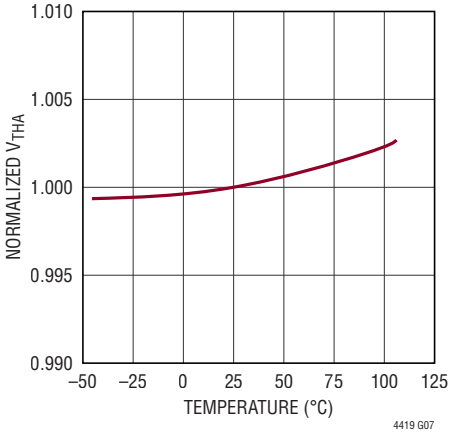
Open-Drain (CMPOUT1, CMPOUT2, V2ON) V_{OL} vs Pull-Down Current



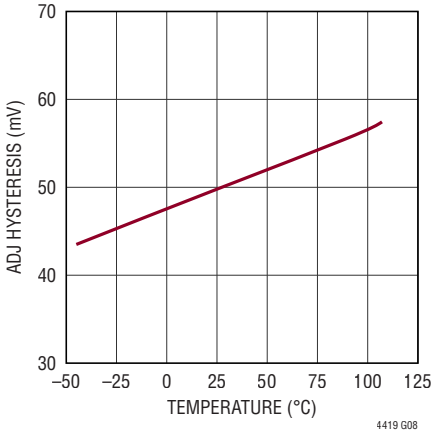
Normalized CMP1 and CMP2 Falling Thresholds vs Temperature



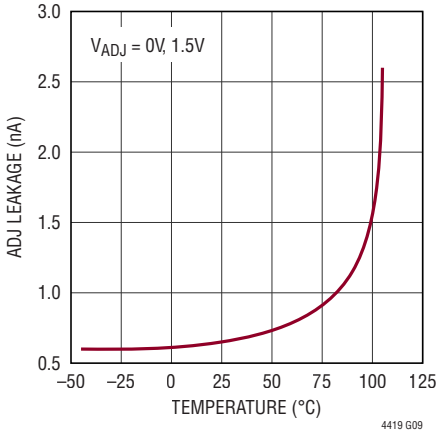
Normalized Falling ADJ Threshold vs Temperature



ADJ Hysteresis vs Temperature

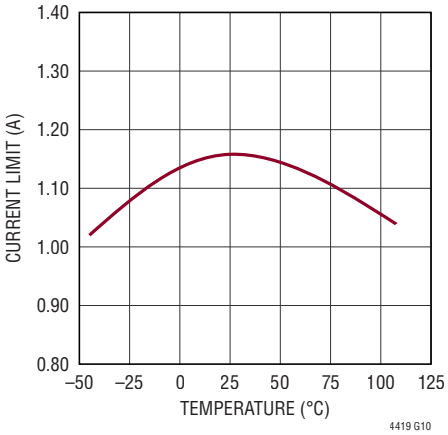


ADJ Leakage vs Temperature

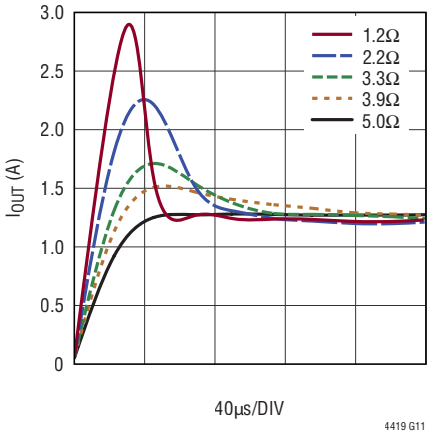


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, V1 = V2 = 3.6V unless otherwise indicated).

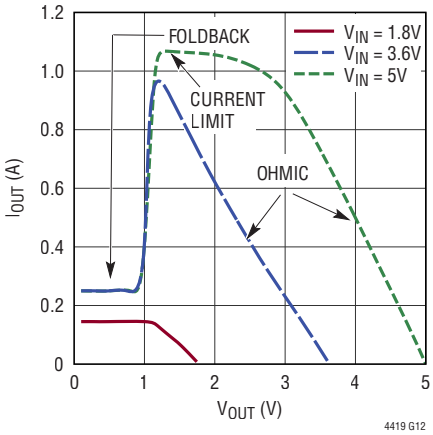
Output Current Limit vs Temperature



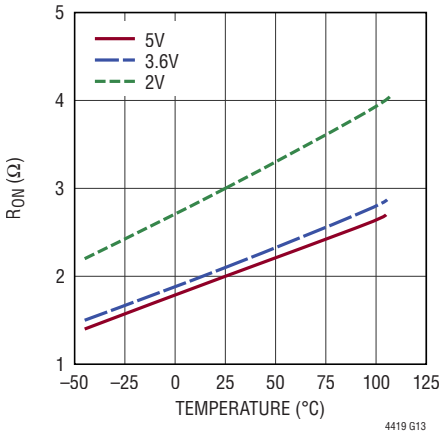
Output Current I_{OUT} Response for Different Shorting Impedances



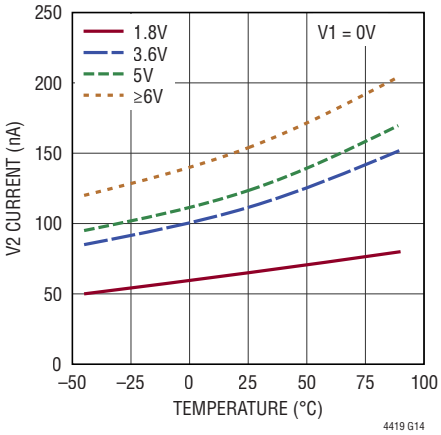
I_{OUT} vs V_{OUT} for Different Input Supply Voltages



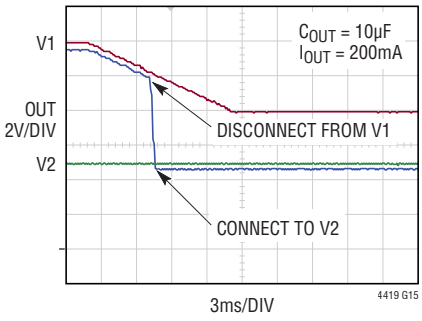
Switch R_{ON} vs Temperature



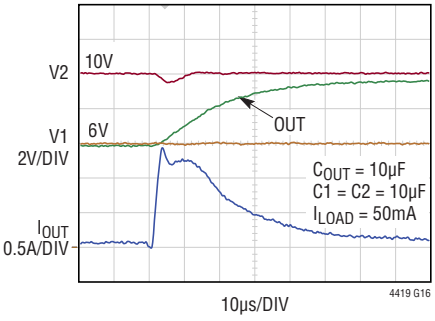
Freshness Seal Current vs V2 Voltage and Temperature



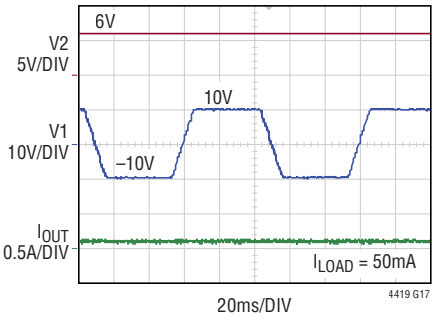
Switchover from a Higher to a Lower Voltage



Output Voltage and Current Waveforms During Switchover



V1 Reverse Voltage Blocking with V2 Powering OUT



PIN FUNCTIONS

ADJ: Adjustable V1 Switchover Threshold Input. ADJ is the noninverting input to the switchover threshold comparator. If V1 ≥ 1.55V and ADJ ≥ 1.097V for at least 64ms, OUT is switched internally to the primary V1 input. When the ADJ input voltage is lower than 1.047V, OUT is switched internally to V2, if V2 ≥ 1.55V. Otherwise, OUT stays unpowered. Tie ADJ via a resistive divider to V1 to set the V1 to V2 switchover voltage. Do not leave open.

CMP1: Auxiliary Comparator 1 Monitor Input. CMP1 is the noninverting input to an auxiliary comparator. The inverting input is internally connected to a 0.387V reference. Connect CMP1 to GND when it is not used.

CMP2: Auxiliary Comparator 2 Monitor Input. CMP2 is the noninverting input to a second auxiliary comparator. The inverting input is internally connected to a 0.387V reference. Connect CMP2 to GND when it is not used.

CMPOUT1: Auxiliary Comparator 1 Output. This open-drain comparator output is pulled low when CMP1 is below 0.387V and during power-up, otherwise it is released. Once released, connecting a resistor between CMPOUT1 and a desired supply voltage up to 18V causes this pin to be pulled high. Leave open if unused.

CMPOUT2: Auxiliary Comparator 2 Output. This open-drain comparator output is pulled low when CMP2 is below 0.387V and during power-up, otherwise it is released. Once released, connecting a resistor between CMPOUT1 and a desired supply voltage up to 18V causes this pin to be pulled high. Leave open if unused.

Exposed Pad: For best thermal performance, solder exposed pad to a large PCB area.

GND: Device Ground.

NC: No Connection. Not internally connected.

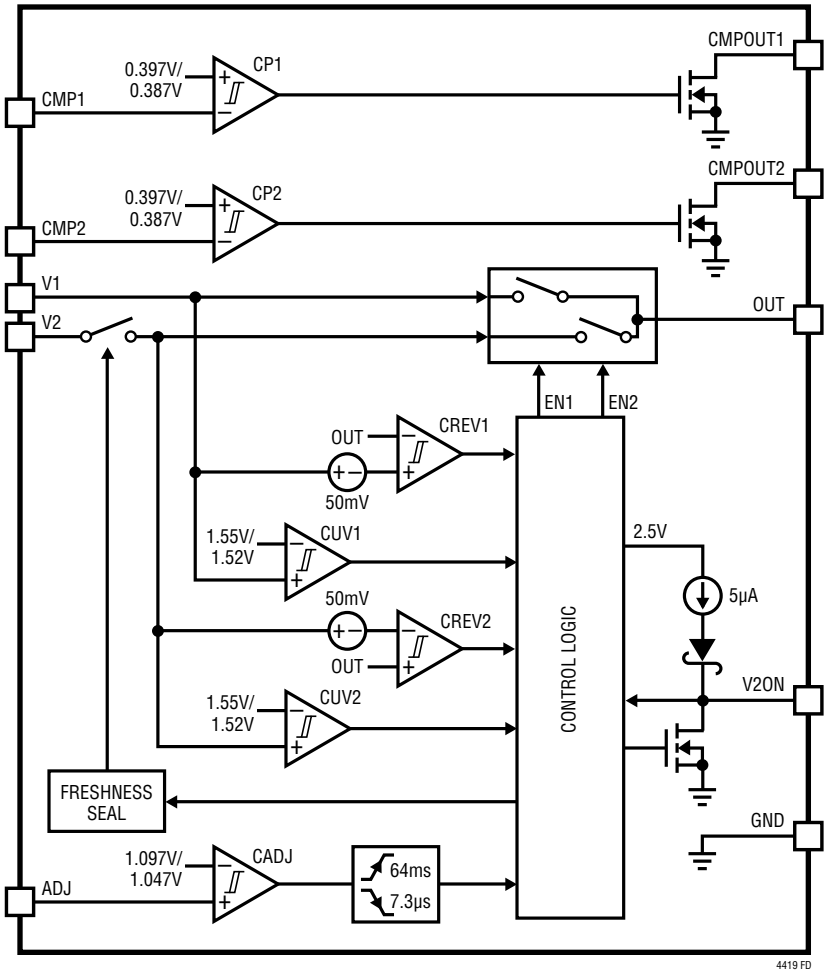
OUT: Output Voltage Supply. OUT is a prioritized voltage output that is either connected to V1, V2 or is unpowered as indicated in Table 1 of the Applications Information section. Additionally, OUT must be at least 50mV below the input supply for a connection to that supply to be activated. Bypass with a capacitor of 1µF or greater. See Applications Information section for bypass capacitor recommendations.

V1: Primary Power Supply. OUT is internally switched to V1 if V1 ≥ 1.55V and ADJ ≥ 1.097V. When in freshness seal mode, applying V1 ≥ 1.55V and ADJ ≥ 1.097V for 32ms disables freshness seal. Bypass with 1µF or greater. Tie to GND if unused.

V2: Backup Power Supply. V2 is valid if its voltage is ≥1.55V. OUT is internally switched to V2 if ADJ < 1.047V or V1 < 1.55V, provided V2 is valid. Refer to Table 1 of the Applications Information section. Bypass with 1µF or greater. Tie to GND if unused.

V2ON: V2 Connected Status. V2ON is an output that is driven high with a 5µA pull-up when the V2 to OUT power path is active. Otherwise it is driven low. Connect a resistor between OUT or V2 and this pin to provide additional pull-up. As this pin is used to enable freshness seal, do not force low or connect a pull-down resistor to this pin. Leave open if unused.

FUNCTIONAL DIAGRAM



OPERATION

The Functional Diagram shows the major blocks of the LTC4419. The LTC4419 is a PowerPath prioritizer that switches output OUT between primary (V1) and backup (V2) sources depending on their validity and priority with V1 having the highest priority. If neither supply is valid, OUT stays unpowered. A resistive divider between V1, ADJ and GND and comparators CUV1 and CADJ are used to monitor V1's voltage to establish validity. V1 is valid if V1 ≥ 1.55V and ADJ ≥ 1.097V for 64ms after V1 rises above 1.55V. Otherwise V1 is invalid. V2 is valid if its voltage as monitored by comparator CUV2 is ≥1.55V. Otherwise, it is invalid. Switchover threshold is independent of relative V1 and V2 voltages, permitting V1 to be lower or higher than V2 when V1 powers OUT and vice versa.

Power connection to the output is made by enhancing back-to-back internal P-channel MOSFETs. Current passed by the MOSFETs is limited to typically 1.1A if OUT is greater than 1V. Otherwise it is limited to 250mA. When switching from V1 to V2, the V1 to OUT power path is first disabled and comparator CREV2 is enabled. After the OUT voltage drops 50mV below V2, as detected by CREV2, OUT is then connected to V2. V2ON pulls high after switchover. This break-before-make strategy prevents OUT from backfeeding V2. Switchover back to V1 occurs in a similar manner once V1 has been revalidated. V2ON pulls low if the V2 power path is disabled and during initial power-up when V1 or V2 is first applied.

The LTC4419 blocks reverse voltages up to –15V when a reverse condition occurs on an inactive channel. The LTC4419 also disables a channel if the corresponding input supply falls below 1.52V. A small ~3µA current is drawn from either the prioritized input supply or the highest input supply if both input supplies are below 1.55V. Very little current (~320nA) is drawn from the unused supply.

The LTC4419 provides two additional comparators, CP1 and CP2, whose open-drain outputs pull low when CMP1 and CMP2 pin voltages fall below 0.387V and during initial power-up. These comparators can be used to monitor supplies to provide early power failure warning and other useful information.

The LTC4419 can be put into a V2 freshness seal mode to prevent battery discharge during storage or shipment. The Applications Information section lists the steps to engage and disengage V2 freshness seal.

APPLICATIONS INFORMATION

The LTC4419 is a low quiescent current 2-channel prioritizer that powers both its internal circuitry and its output OUT from a prioritized valid input supply. Unlike an ideal diode-OR, the LTC4419 does not draw current from the highest supply as long as any one supply is greater than 1.8V. Table 1 lists the input supply from which the LTC4419 draws its internal quiescent current I_{CC} and the supply to which OUT is connected after input supplies have been qualified.

Table 1. OUT and LTC4419 I_{CC} Power Table

INPUT VOLTAGES			OUT CONNECTION	I_{CC} SOURCE
V1 > 1.55V	ADJ > 1.097V	V2 > 1.55V		
Y†	Y†	X	V1	V1
X	N	Y	V2	V2
Y	N	N	Hi-Z	V1
N	X	Y	V2	V2
N	X	N	Hi-Z	V_{MAX}*

Note: X = Don't Care.
*V_{MAX} = Higher of V1 and V2. †For 64ms.

A typical battery backup application is shown in Figure 1. V1 is powered by a 2-cell Li-ion battery pack whose safe discharge limit is between 5.6V and 6V. V2 is powered by a 9V alkaline hold-up battery which is completely discharged when its voltage drops to 6V. In order to protect the 2-cell Li-ion battery on V1, switchover threshold is set to ~5.6V. After switchover to V2, the Li-ion battery primarily supplies only divider R1-R3's current, as the LTC4419 draws only a small standby current from V1. Monitor inputs CMP1 and CMP2 are configured to provide V1 and V2 undervoltage

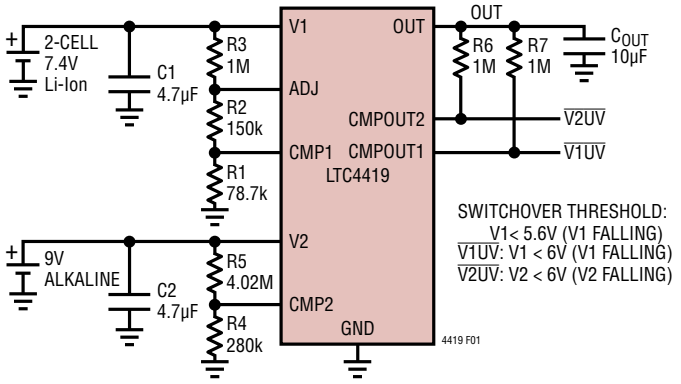


Figure 1. The LTC4419 Protecting a 2-Cell Li-Ion Battery Pack on V1 from Discharge Below Its Safe Minimum Voltage

warnings. Outputs $\overline{V1UV}$ and $\overline{V2UV}$ are driven low when V1 and V2 voltages fall below 6V. Relevant equations used to calculate these component values are discussed in the following subsections.

Setting the Switchover Threshold

Several factors affect switchover voltage and should be taken into account when calculating resistor values. These include resistor tolerance, 1.5% ADJ comparator threshold error, divider impedance and worst-case ADJ pin leakage. These factors also apply to resistive dividers connected to monitor inputs CMP1 and CMP2. Referring to Figure 1 and the Electrical Characteristics table, the typical V1 switchover threshold is:

$$V_{SW1} = \frac{V_{THA}}{R1+R2} \bullet (R1+R2+R3) \quad (1)$$

Typical V1 undervoltage threshold is:

$$V_{V1UV} = \frac{V_{THC}}{R1} \bullet (R1+R2+R3) \quad (2)$$

and typical V2 undervoltage threshold is:

$$V_{V2UV} = \frac{V_{THC}}{R4} \bullet (R4+R5) \quad (3)$$

Equations 1-3 assume ADJ and CMP pin leakages are negligible. To account for pin leakage, equations 1-3 must be modified by an $I_{LEAK} \bullet R_{EQ}$ term, where equivalent resistance, R_{EQ}, must be calculated on a case-by-case basis. Worst-case component values and reference voltage tolerances must be used to calculate the maximum and minimum threshold voltages. For example, to calculate minimum falling switchover threshold voltage, $V_{SW1(MIN)}$, use $V_{THA(MIN)}$, $(R2 + R1)_{(MAX)}$, and $R3_{(MIN)}$ in equation 1.

Selecting Output Capacitor, C_{OUT}

C_{OUT} can be selected to control either output voltage droop during switchover or output rising slew rate during initial power-up or when switching to a higher supply.

In general, output droop, ΔV_{OUT}, can be calculated by:

$$\Delta V_{OUT} = \frac{t_{NOV} \bullet I_{OUT}}{C_{OUT}} \quad (4)$$

APPLICATIONS INFORMATION

where I_{OUT} is the current supplied by C_{OUT} during non-overlap or "dead" time t_{NOV}. Choosing:

$$C_{OUT} \geq \frac{t_{NOV} \bullet I_{OUT}}{\Delta V_{OUT}} \quad (5)$$

limits output droop to less than ΔV_{OUT}.

In order to estimate t_{NOV} and I_{OUT}, first consider a scenario where power supplies are present on both V1 and V2, and their voltages are changing slowly compared to the ADJ comparator propagation delay t_{PDA}. In such cases, I_{OUT} is I_{LOAD} and t_{NOV} is t_{SWITCH}. C_{OUT} can be sized according to equation 5 with $I_{OUT} = I_{LOAD(MAX)}$ and $t_{NOV} = t_{SWITCH(MAX)}$ to limit maximum output droop when switching to a higher supply. When switching to a lower supply, switchover is initiated only after OUT falls V_{REV} below the supply that is being switched in. In such cases, total output droop is $\Delta V_{OUT} + V_{REV}$.

Next consider a scenario where the input power source powering OUT is unplugged. OUT back-feeds circuitry connected to the input supply pin. Both input and output droop at the same rate. Referring to Figure 1, assume the battery on V1 is unplugged when OUT is connected to V1. I_{OUT} is the sum of I_{LOAD} and the reverse current I_{BACK}, which in this example is I_{R3}. As OUT and V1, since the two are connected, droop below the ADJ threshold, switchover occurs to V2 with a dead time:

$$t_{NOV} = t_{PDA} + t_{SWITCH} \quad (6)$$

where t_{PDA} is an overdrive dependent ADJ comparator delay. As an approximation, use t_{PDA} from the Electrical Characteristics table to estimate t_{NOV}. Use this t_{NOV} and:

$$I_{OUT} = (I_{BACK} + I_{LOAD}) \quad (7)$$

in equation 5 to size C_{OUT}:

$$C_{OUT} \geq \frac{(t_{PDA} + t_{SWITCH}) \bullet I_{OUT}}{\Delta V_{OUT}} \quad (8)$$

Refer to Figure 2 for a more accurate estimate of t_{PDA} versus dV_{OUT}/dt. If ADJ is filtered with capacitor, its discharge time via divider R1-R3 increases t_{PDA}. This results in a higher output droop than estimated by equation 8.

In order to limit output rising slew rate dV_{OUT}/dt, size:

$$C_{OUT} \geq \frac{I_{LIM}}{\frac{dV_{OUT}}{dt}} \quad (9)$$

as the LTC4419 limits OUT charging current to I_{LIM} until OUT approaches the input supply to within $I_{LIM} \bullet R_{ON}$, where R_{ON} is the channel switch resistance. Refer to the Thermal Protection and Maximum C_{OUT} section to determine maximum allowed C_{OUT}.

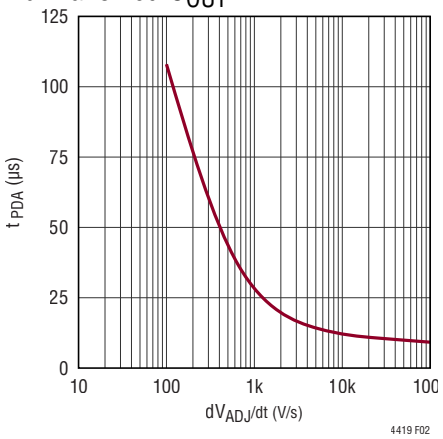


Figure 2. ADJ Comparator Propagation Delay as a Function of Slew Rate; t_{PDA} vs dV_{ADJ}/dt

Inductive Effects

Parasitic inductance and resistance can impact circuit performance by causing overshoot and undershoot of input and output voltages depending on the scenario. Parasitic inductance in the power path causes positive-going overshoot on the input and a negative-going undershoot on the output when the LTC4419 turns off. Another cause of positive input overshoot is R-L-C tank ringing during hot plug of an input supply. Input overshoot is most pronounced when the total resistance of the input tank is low. Care must be taken to ensure overvoltage transients do not exceed the absolute maximum ratings of the LTC4419. Additionally, parasitic resistance and inductance can cause input undershoot during power path turn-on. If severe enough, undershoot can temporarily invalidate a supply and cause repeated power up cycles ("motorboating") or unwanted switchover between sources.

APPLICATIONS INFORMATION

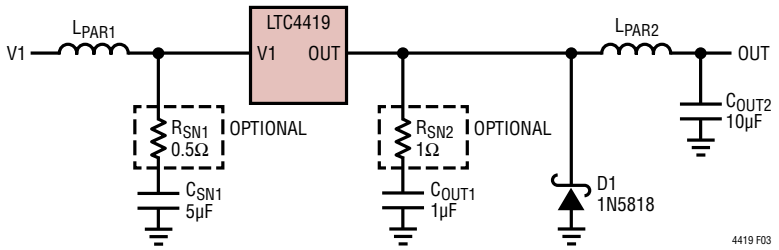


Figure 3. Recommended Inductive Transient Suppression Circuitry

The first step to avoid these issues is to minimize parasitic inductance and resistance in the power path. Guidelines are given in the layout section for minimizing parasitic inductance on the printed circuit board (PCB). External to the PCB, twist the power and ground wires together to minimize inductance.

Second, use a bypass capacitor at the input to limit input voltage overshoot during LTC4419 power path turn off. A few micro farads is sufficient for most applications. When hot plugging supplies with large parasitic inductances, it is possible for the R-L-C tank to ring to more than twice the nominal supply voltage. Wall adapters and batteries typically have enough loss (i.e. series resistance) to prevent ringing of this magnitude. However, if this is a problem, snub input capacitor C_{SN1} with resistor R_{SN1}, typically 0.5Ω. Place this network close to the supply pin.

Third, if an input capacitor is not permissible, use a TVS (such as SMAJ16CA) in applications when supply pin transients can exceed 24V. Use a bidirectional TVS in applications requiring reverse input protection. Note that a TVS does not address droop and motorboating, which are solved only by input bypassing.

During normal operation, the LTC4419 limits power path current to < 1.6A and internal circuitry prevents OUT from ringing below ground during power path turn off. This is also true for output shorts when the short is close to the LTC4419's OUT pin. However, if the output is shorted through a long wire, current in the wire inductance (L_{PAR2} in Figure 3) builds up due to the discharge of C_{OUT1} and can be much higher than 1.6A. This current causes the OUT pin to ring below its –0.3V absolute maximum rating once C_{OUT1} has been fully discharged. For this special case, split the output capacitor between C_{OUT1} and C_{OUT2} and make C_{OUT1} small. Snub C_{OUT1} with resistor R_{SN2} to damp R-L-C ringing if required. Size C_{OUT2} to obtain the required total output capacitance. Also add a diode between OUT and ground close to the LTC4419 to clamp negative ringing if the OUT pin rings below –0.3V.

Increasing CMP1 and CMP2 Hysteresis

In some applications, built-in CMP1 hysteresis may be insufficient. In such cases, CMP1 hysteresis can be increased as shown in Figure 4. Hysteresis at the monitored input V_{MON} with R8 present and assuming R9 << R8 is given by:

$$V_{HYST} = V_{HYSTC} \bullet \frac{R3}{R1||R3||R8} + V_{PU} \bullet \frac{R3}{R8} \quad (10)$$

where V_{HYSTC} and V_{THC} are found in the Electrical Characteristics table and are typically 10mV and 0.387V respectively. Account for supply V_{PU} and resistor R8 when calculating rising and falling thresholds of monitored input V_{MON}.

Supply Impedance and ADJ Comparator Hysteresis

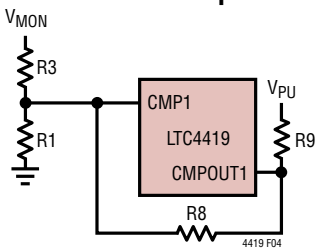


Figure 4. Increasing CMP1 Hysteresis

In some applications, V1 could be supplied by a battery pack with high ESR or through a long cable with appreciable series resistance. Load current, I_{OUT}, flowing through this resistance reduces the monitored V1 voltage by:

$$\Delta V1 = I_{OUT} \bullet R_{ESR} \quad (11)$$

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The drop can be as high as:

$$\Delta V1 = I_{LIM} \bullet R_{ESR} \quad (12)$$

when C_{OUT} is initially being charged. Voltage droop at the V1 pin can result in repeated switchover between V1 and V2 if built-in V1 (ADJ) hysteresis is insufficient.

In such cases, CMP1 can be used to set V1 hysteresis as shown in Figure 5. When V1 falls, ADJ and CMP2 are pulled low when CMP1 falls below V_{THC} and output CMPOUT2 activates hysteresis resistor R8. When switching from V1 to V2, current supplied by V1 will go to zero, resulting in a voltage increase on V1. Switchover back to V1 is prevented due to increased V1 hysteresis as determined by equation 10.

V1 droop is higher during the initial charging of C_{OUT}. Referring to Figure 5, to prevent repeated switchover when C_{OUT} is initially being charged, add input capacitor C1. Ideally, if V1 is greater than switchover threshold V_{SW1} by ΔV, size:

$$C1 \geq \frac{V_{SW1} \bullet C_{OUT} \bullet \left(1 - \frac{\Delta V}{2 \bullet I_{LIM} \bullet R_{ESR}}\right)}{\Delta V} \quad (13)$$

to ensure no switchover occurs when C_{OUT} is initially being charged. If the resulting C1 value causes large inrush current, is physically too big or requires a large snubber resistor when V1 is plugged in (refer to the Typical Applications section), select C1 to be as high a value as the application can tolerate.

A filter capacitor C_{ADJ} can also be added to ADJ to ride through the initial output charge up time. C_{ADJ} should be minimized as it slows ADJ response, resulting in a larger output droop when the input supply powering V1 is either unplugged or drops quickly.

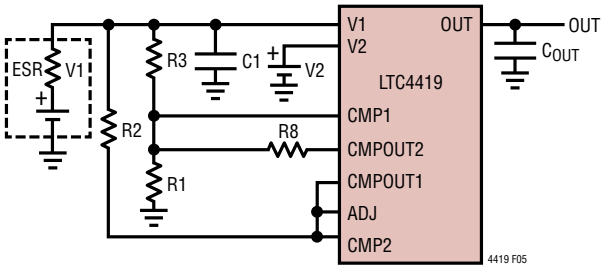


Figure 5. Increasing Supply Hysteresis in High ESR Applications

Input Shorts and Supply Brown-Out

The LTC4419 temporarily turns off its active power path during input shorts or brown-out conditions if the input supply falls below OUT by 0.7V. If the primary input supply becomes invalid, switchover to the backup supply occurs. The power path is reactivated when the input recovers to within 0.7V of the output.

Figure 6 shows the response of the LTC4419 to a brown-out and recovery on V1 where switchover to V2 does not occur as V1 stays above 1.8V. When V1 falls, OUT gets disconnected from V1 and is slowly discharged by load resistance R_{OUT}. When V1 recovers, the power path is reactivated and OUT tracks V1. In Figure 7, when V1 falls, OUT gets disconnected from V1 as V1 drops below the

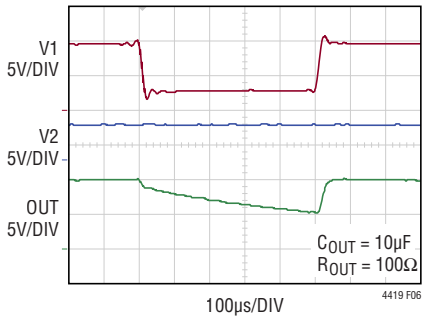


Figure 6. Voltage Waveforms During a Brown-Out on V1 that Does Not Result in a Switchover to V2. Switchover Threshold = 1.8V

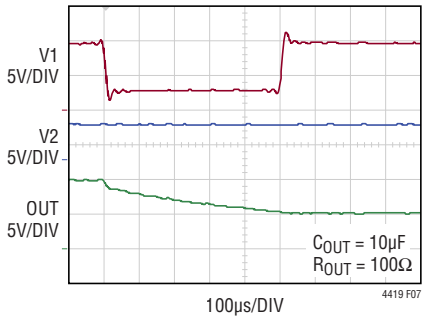


Figure 7. Voltage Waveforms When a Brown-Out on V1 Results in Switchover to V2. Switchover Threshold = 3V

APPLICATIONS INFORMATION

switch-over threshold. When V1 recovers, it needs to be qualified for 64ms before it is reconnected to OUT. OUT gets discharged by R_{OUT} and is connected to V2 once its voltage is 50mV less than V2.

Reverse Voltage Blocking

The LTC4419 blocks reverse voltages on supply pins V1 and V2 up to –15V relative to GND and up to –39V relative to OUT. Transient voltage suppressors (TVS) connected to V1 and V2 must be bidirectional and capacitors connected to these pins must be rated to handle reverse voltages. A reverse voltage on V2 does not disrupt V1 operation and vice versa.

Freshness Seal

Freshness seal mode prevents V2 battery discharge by keeping V2 disconnected from OUT even if V1 is absent or invalid. Very little current is drawn from V2—typically just 120nA. The following sequence (refer to Figure 8) puts the LTC4419 in freshness seal mode:

1. Power up V2 while holding V1 low and wait for at least 10ms.
2. Drive V2ON below 50mV.
3. Power up V1 and ADJ for at least 94ms. Freshness seal is enabled.

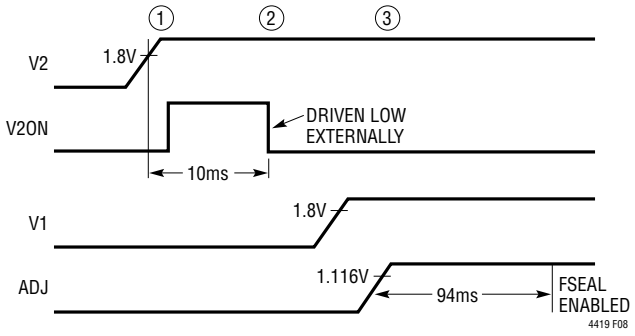


Figure 8. Freshness Seal Engage Procedure

Engage this mode if V2 is a backup battery either during storage or during shipment. Once freshness seal has been engaged, if V1 is disconnected, V2 stays disconnected from OUT. Freshness seal is automatically disabled the next time V1 is revalidated. Limit V2ON pin capacitance to less than 10nF in order to prevent freshness seal mode from accidentally being engaged.

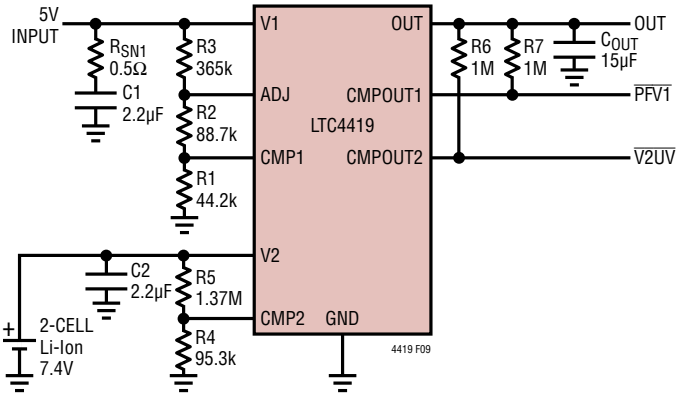


Figure 9. Design Example

Design Example

In Figure 9, the LTC4419 prioritizes between a 5V supply connected to V1 and a 7.4V 2-cell Li-Ion battery connected to V2. The system is designed to switch OUT to V2 when V1 drops below 4V, provide early power failure warning when V1 drops below 4.5V and low battery warning when the backup battery voltage drops below 6V. Maximum anticipated load current is 100mA and maximum allowed output droop is 100mV. Output rising slew rate is limited to <0.1V/µs and V1 and V2 input capacitors are limited to 10µF to avoid large inrush current. 1% tolerance resistors are used. ADJ and CMP pin leakages are ignored as their design impact is small.

First choose total resistive divider current to be ~10µA for V1 and ~5µA for V2. For the 5V supply, this results in:

$$R1+R2+R3=\frac{5V}{10\mu A}=500k\Omega \quad (14)$$

Since desired switchover threshold, V_{SW1}, and the total divider impedance are known, use equation 1 to first calculate R3. Using R3 and equation 2, calculate R1 and R2. Rewriting equation 1 results in:

$$(R1+R2)=\frac{V_{THA}\bullet(R1+R2+R3)}{V_{SW1}} \quad (15)$$

APPLICATIONS INFORMATION

Using (R1 + R2 + R3) = 500kΩ from equation 14, results in:

$$(R1+R2)=\frac{1.047V \bullet 500k\Omega}{4V}=130.9k\Omega \quad (16)$$

$$R3 \sim (500k\Omega - 130.9k\Omega) = 369.1k\Omega \quad (17)$$

Using the nearest 1% resistor value yields R3 = 365kΩ.

Rearranging equation 2 results in

$$R1=\frac{V_{THC} \bullet (R2+R2+R3)}{V_{\overline{PFV1}}} \quad (18)$$

$$R1=\frac{0.387V}{4.5V} \bullet (500k\Omega) \quad (19)$$

Solving equations 16 and 19 results in R1 = 43.3kΩ and R2 = 87.6kΩ. Using the nearest 1% resistors results in R2 = 88.7kΩ. Recalculating equation 1 using calculated R2 and R3 values and using standard 1% resistor values close to 43.3kΩ for R1 results in R1 = 44.2kΩ.

A similar procedure is used to calculate R4 and R5 using equation 3 and total divider current. The design equations are shown below:

$$R4+R5=\frac{7.4V}{5\mu A}=1.48M\Omega \quad (20)$$

as desired current in the divider is 5µA.

Rewriting equation 3 neglecting pin leakage and assuming R5 >> R4 results in:

$$R4=\frac{V_{THC} \bullet (R4+R5)}{V_{V2UV}} \quad (21)$$

$$R4=\frac{0.387V \bullet 1.48M\Omega}{6V} \quad (22)$$

Solving 20 and 22 results in R4 = 96.2kΩ and R5 = 1.38MΩ. Choosing the nearest 1% resistor results in R4 = 95.3kΩ and R5 = 1.37MΩ.

C_{OUT} affects both OUT droop during switchover as determined by equation 4 and OUT rising slew rate as determined by equation 9. Calculate minimum C_{OUT} required to meet desired output droop and slew rate specifications using equations 8 and 9 and size C_{OUT} to be the larger of the two values.

C_{OUT} required to limit OUT droop to < 100mV is given by equation 8:

$$C_{OUT} \geq \frac{(t_{PDA}+t_{SWITCH}) \bullet I_{LOAD}}{100mV} \quad (23)$$

$$C_{OUT} \geq \frac{(7.3\mu s+2.5\mu s) \bullet 0.1A}{100mV}=9.8\mu F \quad (24)$$

C_{OUT} required to limit OUT slew rate to < 0.1V/µs is given by equation 9:

$$C_{OUT} \geq \frac{I_{LIM}}{0.1V/\mu s}=11\mu F \quad (25)$$

Choose a C_{OUT} capacitor whose minimum value is 11µF accounting for voltage and temperature coefficients. Do this for other capacitors as well. Assuming correct PCB layout, choose C1 to be 2.2µF, which is ~ 1/5th of C_{OUT} to suppress inductive transients. Also snub C1 with a 0.5Ω resistor to prevent ringing.

Layout Consideration

Make power and ground traces as wide as possible. Place bypass capacitors, snubbers and TVS devices as close to the pin as possible to reduce power path resistance and parasitic inductance. These result in smaller overvoltage transients and improved overvoltage protection. Place resistive dividers close to the pins to improve noise immunity. Use a 4-layer board if possible with layer 2 as dedicated GND and solder the exposed pad to a large PCB GND trace for better heat dissipation. A partial layout for a 2-Layer PCB is shown in Figure 10.

APPLICATIONS INFORMATION

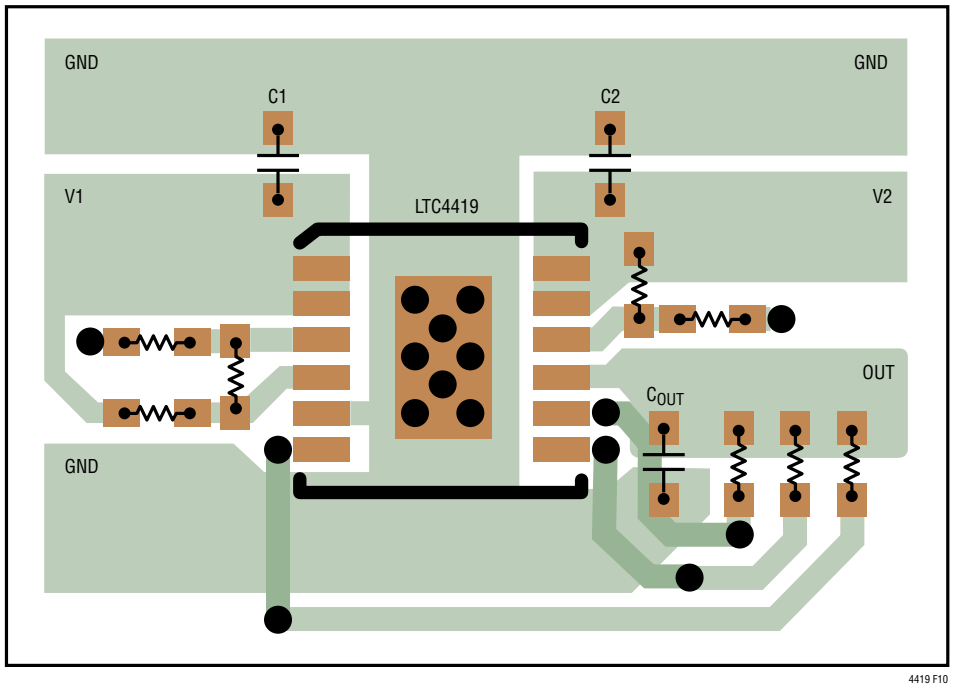


Figure 10. Recommended 12-Lead MSE Layout for a 2-Layer PCB

Thermal Protection and Maximum C_{OUT}

Depending on the difference between input and output voltages, the LTC4419's internal power dissipation can be high when operating in current limit mode. This usually occurs when a large C_{OUT} is being charged either during initial power up or when OUT switches over to a higher supply. The situation is made worse if a DC load is present on OUT, as this reduces the current available to charge C_{OUT}. In such cases, self heating can cause power path turn-off due to activation of the thermal protection circuitry. The power path is reactivated when die temperature drops to a safe value. This process can repeat indefinitely if C_{OUT} is discharged fully by load current I_{OUT} in the interval when the power path is off.

Maximum allowed C_{OUT} to prevent activation of the thermal protection circuit depends on several factors such as input supply and output voltages, starting ambient temperature, heat dissipation in the PCB and DC output current. Choose $C_{OUT} < 500\mu F$ if possible. If a larger C_{OUT} is necessary, use Figure 11 to choose C_{OUT}. Follow PCB layout guidelines to improve heat dissipation.

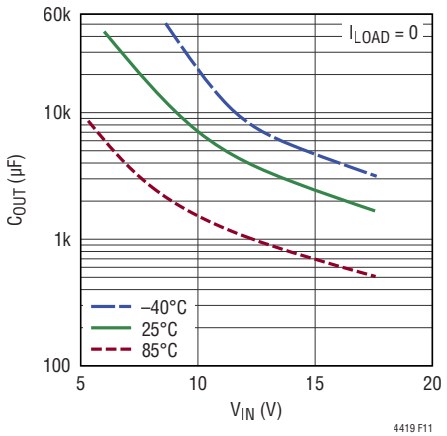
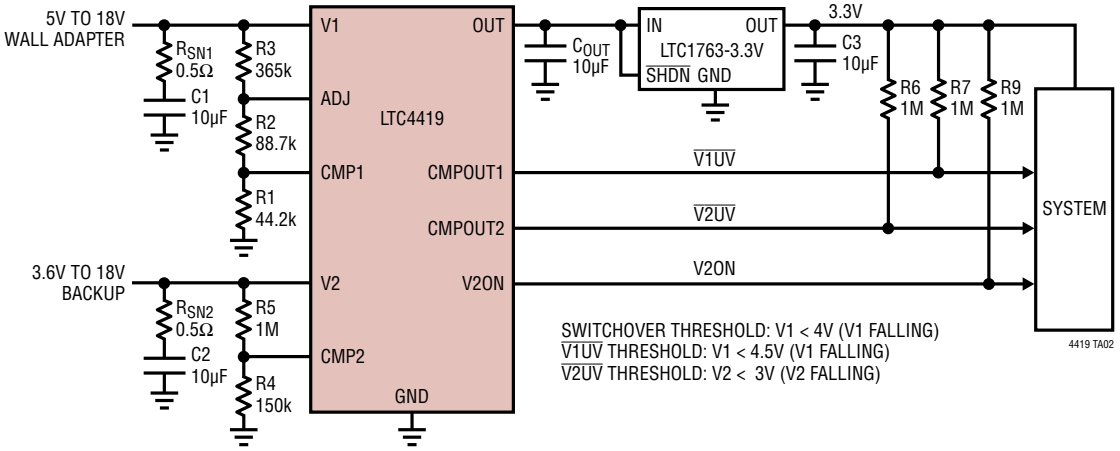


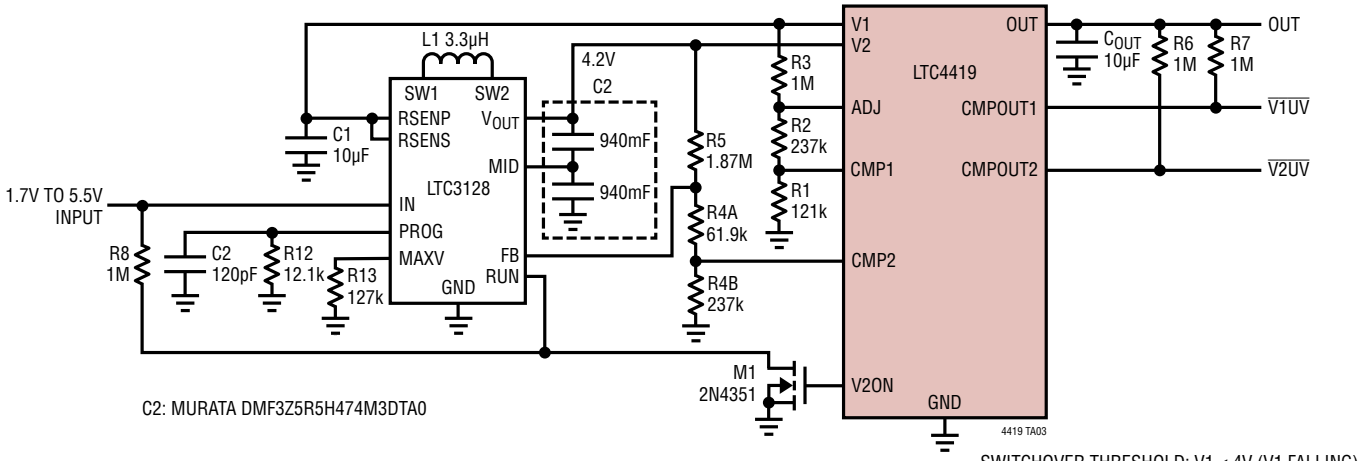
Figure 11. Maximum Allowed C_{OUT} vs Input Voltage for Different T_A

TYPICAL APPLICATIONS

Battery Backup with Interface to Low Voltage Logic

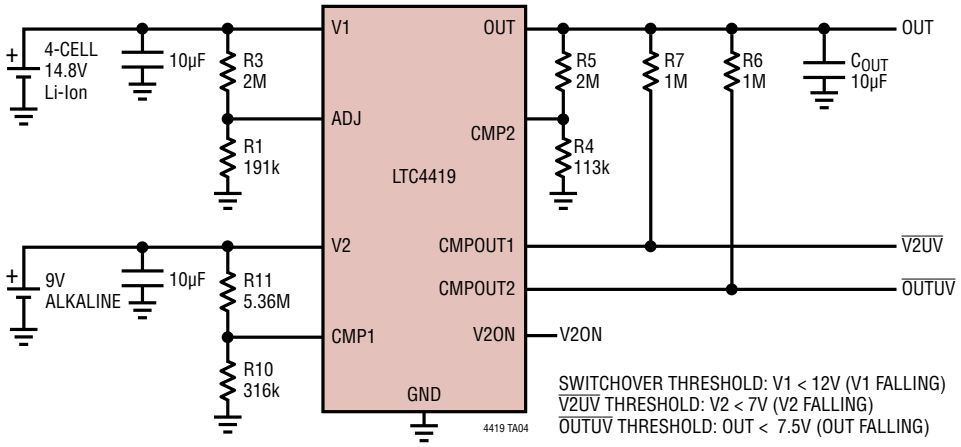


SuperCap Backup with SuperCap Charging

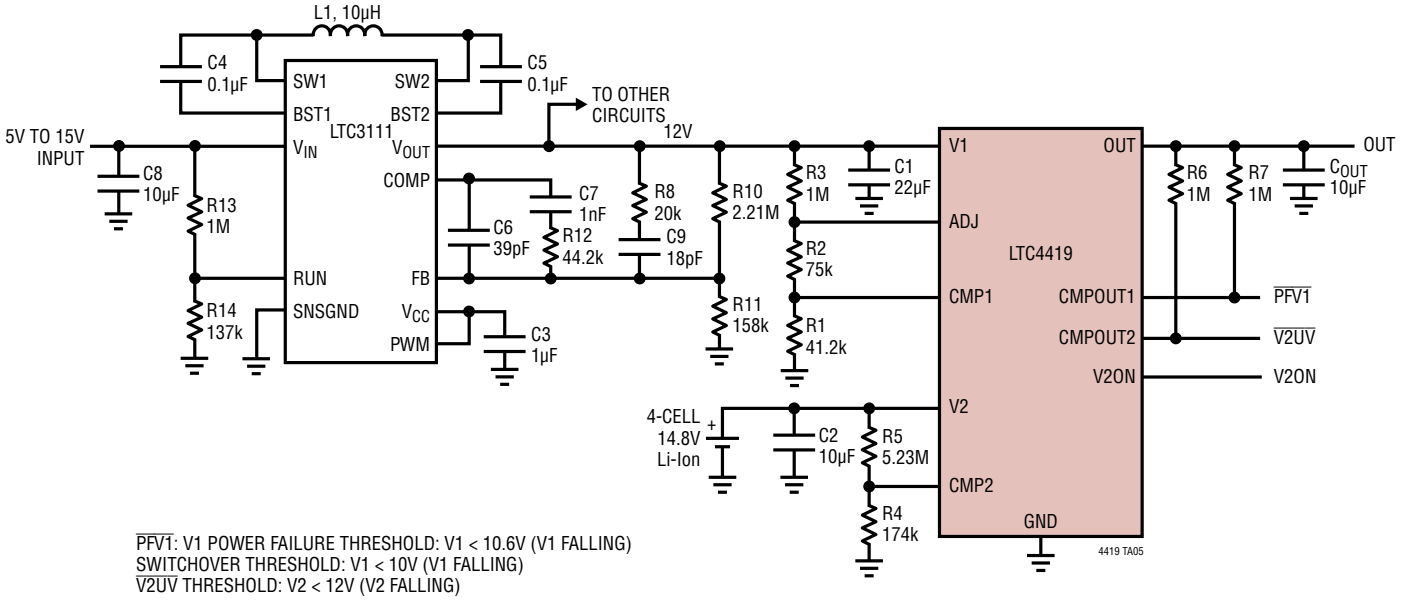


TYPICAL APPLICATIONS

Triple Supply Monitor with Primary Battery Pack Protection



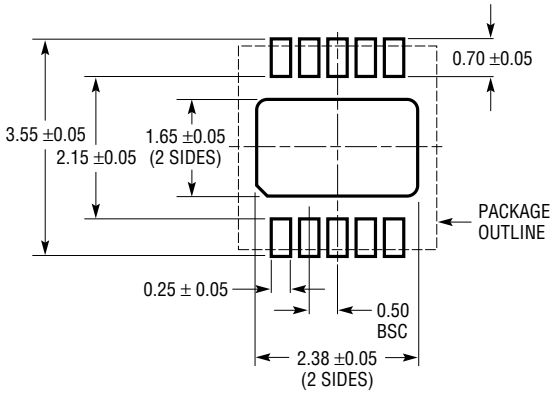
Early Power Failure Warning with Low Battery Indication



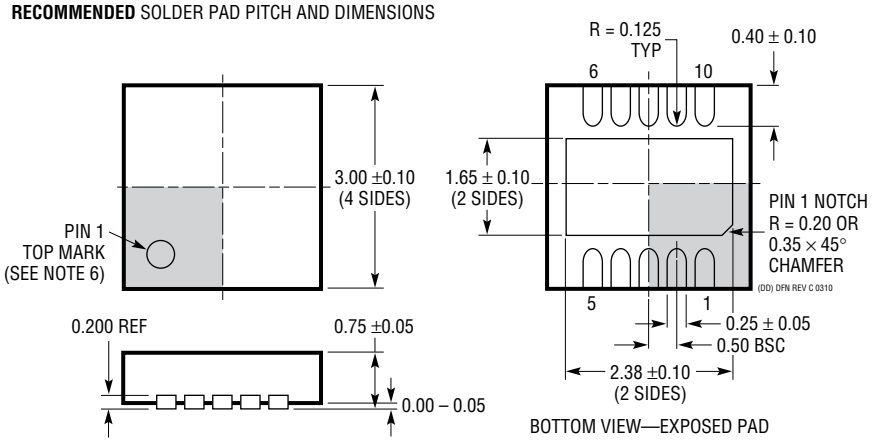
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4419#packaging for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



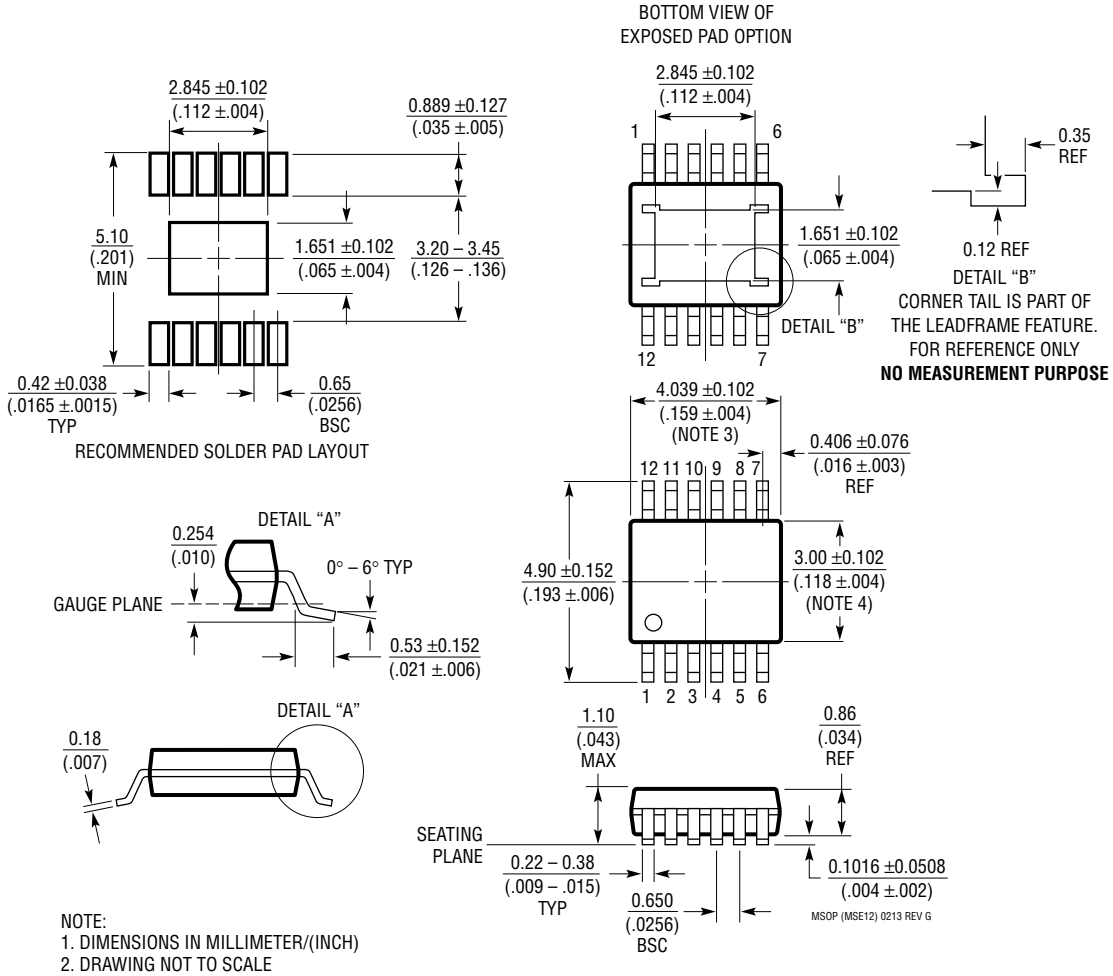
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4419#packaging for the most recent package drawings.

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)

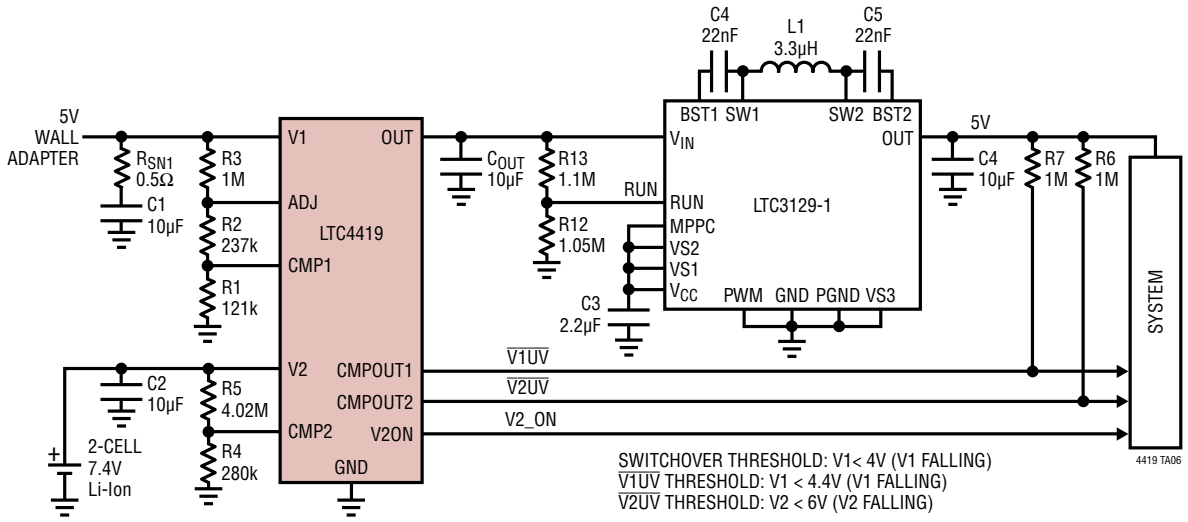


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

High Efficiency Backup



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1763	500mA, Low Noise Micropower LDO Regulators	V_{IN}: 1.8V to 20V, 12-DFN, SO-8 Packages
LTC2952	Pushbutton PowerPath Controller with Supervisor	V_{IN}: 2.7V to 28V, On/Off Timers, ±8kV HBM ESD, TSSOP-20 and QFN-20 Packages
LTC3103	15V, 300mA Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V-15V, DFN-10 and MSE-10 Packages
LTC3129/LTC3129-1	15V, 200mA Synchronous Buck-Boost DC/DC Converter with 1.3µA Quiescent Current	V_{IN}: 1.92V to 15V, QFN-16 and MSE-16 Packages
LTC3388-1/LTC3388-3	20V, 50mA High Efficiency Nanopower Step-Down Regulator	V_{IN}: 2.7V to 20V, DFN-10 and MSE-10 Packages
LTC4411	2.6A Low Loss Ideal Diode in ThinSOT™	Internal 2.6A P-channel, 2.6V to 5.5V, I_Q = 40µA, SOT-23 Package
LTC4412	36V Low Loss PowerPath Controller in ThinSOT	2.5V to 36V, P-channel, I_Q = 11µA, SOT-23 Package
LTC4415	Dual 4A Ideal Diodes with Adjustable Current Limit	Dual Internal P-channel, 1.7V to 5.5V, MSOP-16 and DFN-16 Packages
LTC4416	36V Low Loss Dual PowerPath Controller for Large PFETs	3.6V to 36V, 35µA per I_Q Supply, MSOP-10 Package
LTC4417	3-Channel Prioritized PowerPath Controller	Triple P-Channel Controller, 2.5V to 36V, SSOP-24 and QFN-24 Packages
LTC4355	Positive High Voltage Ideal Diode-OR with Supply and Fuse Monitors	Dual N-channel, 9V to 80V, SO-16, MSOP-16 and DFN-14 Packages
LTC4359	Ideal Diode Controller with Reverse Input Protection	N-channel, 4V to 80V, MSOP-8 and DFN-6 Packages

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