SONY

CXG1091TN

SP4T GSM Dualband Antenna Switch 5V + Logic

For the availability of this product, please contact the sales office.

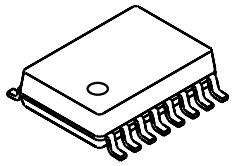
Description

The SP4T + logic is a high power antenna switch MMIC for use in dualband GSM handsets.

One Antenna can be routed to either of the 2 Tx or 2 Rx ports. It operates from 3 CMOS control lines (Tx ON/OFF and GSM900/1800 and Standby).

The Sony's J-FET process is used for low insertion loss.

16 pin TSSOP (Plastic)



Features

- 3 CMOS compatible control lines
- 34dBm power handling at 5.0V (GSM900)
- Low second harmonic < – 30dBm at 34dBm
- Small package size: 16-pin TSSOP (3.9 × 4.1mm)

Applications

Dualband handsets using combinations of GSM900/GSM1800/GSM1900 and DECT

Structure

GaAs J-FET MMIC

Truth Table

On Pass	Band select	Tx (H)/Rx (L)	Standby
Ant.-Tx1 GSM900	H	H	H
Ant.-Tx2 GSM1800	L	H	H
Ant.-Rx1 GSM900/1800	L	L	H
Ant.-Rx2 GSM900/1800	H	L	H
OFF	—	—	L

Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

E99758A9Y-PS

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Ant-Tx1, Tx2	*1		0.5	0.75	dB
			*2		0.6	0.85	dB
		Ant-Rx1, Rx2	*3		0.55	0.75	dB
			*4		0.7	0.9	dB
Isolation	ISO.	Ant-Tx1, Tx2	*1	20	25		dB
			*2	17	20		dB
		Ant-Rx1, Rx2	*3	24	28		dB
			*4	20	24		dB
VSWR	VSWR				1.2		
Harmonics **Note)**	2fo	Ant-Tx1, Tx2	*1, *2			–30	dBm
	3fo		*1, *2			–30	dBm
P_{1dB} compression input power	P_{1dB}	Ant-Tx1, Tx2	*1, *2		36		dBm
Switching speed	TSW				1		µs
Control current	I_{CTL}				100		µA
Supply current	I_{DD}		STBY = H		0.5	1	mA
Leakage current	I_{IK}		STBY = L			50	µA

*1 Pin = 34dBm, 880 to 915MHz, V_{DD} = 5.0V

*2 Pin = 32dBm, 1710 to 1785MHz, V_{DD} = 5.0V

*3 Pin = 10dBm, 925 to 960MHz

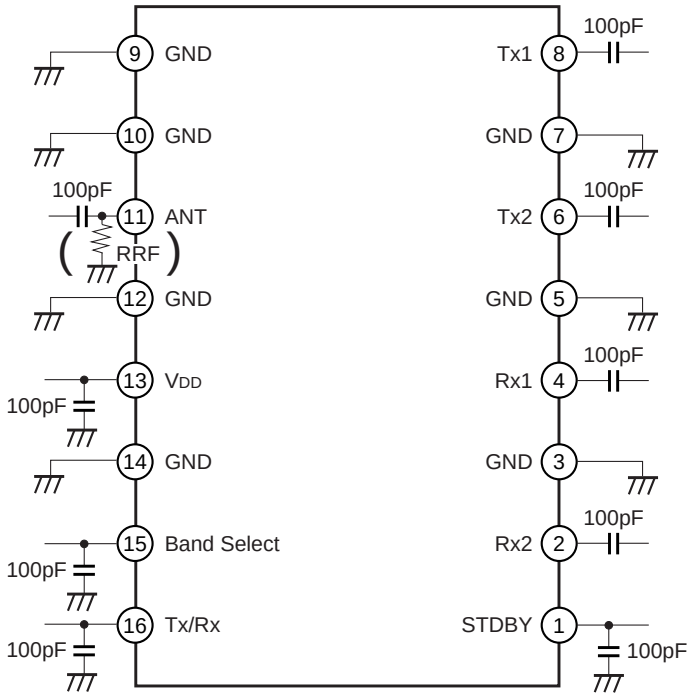
*4 Pin = 10dBm, 1805 to 1880MHz

Note) Harmonics measured with Tx inputs harmonically matched.

CMOS Logic Values (Ta = 25°C)

Logic	Min.	Typ.	Max.
High	2.4V	3.0V	
Low		0.0V	0.8V

Recommended Circuit

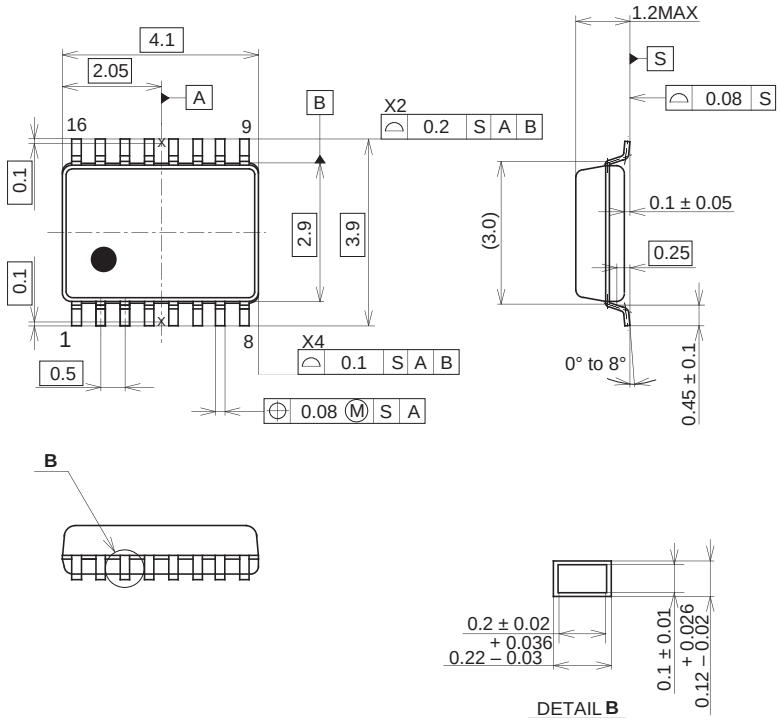


PCB Layout Recommendations

- As indicated in the diagram AC coupling capacitors are necessary to the Ant, Tx1, Tx2, Rx1, Rx2 pins.
- Ground plane should be included under the device and all ground pins connected to this.
- RRF (68kΩ) is used to be stabilized the electrical characteristics at high power signal input.

Package Outline Unit: mm

16PIN TSSOP(PLASTIC)



SONY CODE	TSSOP-16P-L01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g