

# ESD234-B1-W0201

## Protection device

TVS (transient voltage suppressor)

Bi-directional, 5.5 V, 56 pF, 0201, RoHS and halogen free compliant

## Feature list

- ESD/transient protection according to:
  - IEC61000-4-2 (ESD):  $\pm 19$  kV (air/contact discharge)
  - IEC61000-4-4 (EFT):  $\pm 2$  kV/  $\pm 40$  A (5/50 ns)
  - IEC61000-4-5 (Surge):  $\pm 7$  A (8/20  $\mu$ s)
- Bi-directional working voltage up to:  $V_{RWM} = \pm 5.5$  V
- Line capacitance:  $C_L = 56$  pF (typical) at  $f = 1$  MHz
- Clamping voltage:  $V_{CL} = 12.5$  V (typical) at  $I_{TLP} = 16$  A with  $R_{DYN} = 0.15 \Omega$  (typical)
- Very low reverse current:  $I_R < 1$  nA (typical)
- Small form factor SMD size 0201, low profile (0.58 mm x 0.28 mm x 0.15 mm) [3]
- Bi-directional, symmetric I/V characteristic for optimized design/assembly, recommendations for PCB assembly see [2]



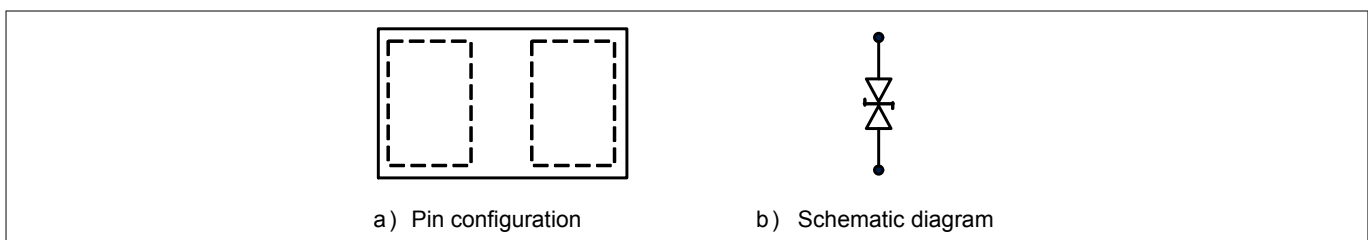
## Potential applications

- ESD protection of highly susceptible IC/ASICs in audio, headset, human digital interfaces

## Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

## Device information



**Figure 1** Pin configuration and schematic diagram

**Table 1** Part information

| Type            | Package | Configuration          | Marking code    |
|-----------------|---------|------------------------|-----------------|
| ESD234-B1-W0201 | WLL-2-1 | 1 line, bi-directional | Y <sup>1)</sup> |

<sup>1</sup> The device has no marking on the device top. The marking code is on pad side.

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**Maximum ratings**

# 1 Maximum ratings

Note:  $T_A = 25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

| Parameter                        | Symbol              | Values     | Unit |
|----------------------------------|---------------------|------------|------|
| Reverse working voltage          | $V_{RWM}$           | $\pm 5.5$  | V    |
| ESD discharge <sup>1)</sup>      | $V_{ESD}$ (contact) | $\pm 19$   | kV   |
|                                  | $V_{ESD}$ (air)     | $\pm 19$   |      |
| Peak pulse power <sup>2)</sup>   | $P_{PK}$            | 84         | W    |
| Peak pulse current <sup>2)</sup> | $I_{PP}$            | $\pm 7$    | A    |
| Operating temperature range      | $T_{OP}$            | -55 to 125 | °C   |
| Storage temperature              | $T_{stg}$           | -65 to 150 | °C   |

**Attention:** Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.

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<sup>1</sup>  $V_{ESD}$  according to IEC61000-4-2 ( $R = 330\ \Omega$ ,  $C = 150\text{ pF}$  discharge network)

<sup>2</sup> Stress pulse: 8/20 $\mu$ s current waveform according to IEC61000-4-5

Electrical characteristics

## 2 Electrical characteristics

Note:  $T_A = 25^\circ\text{C}$ , unless otherwise specified. Device is electrically symmetrical.

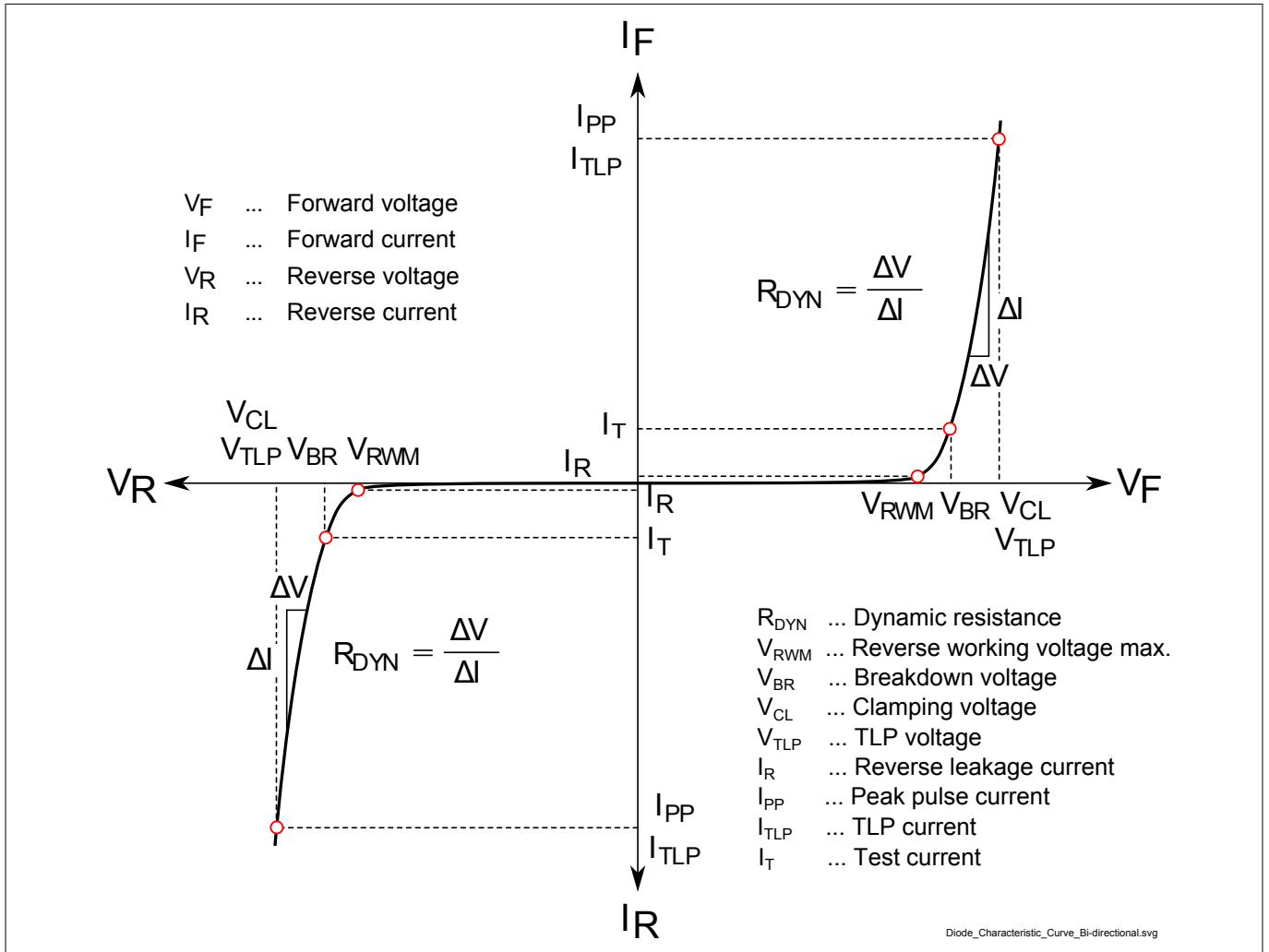


Figure 2 Definitions of electrical characteristics

**Electrical characteristics**

**Table 3 DC characteristics**

| Parameter         | Symbol   | Values |      |      | Unit | Note or test condition |
|-------------------|----------|--------|------|------|------|------------------------|
|                   |          | Min.   | Typ. | Max. |      |                        |
| Breakdown voltage | $V_{BR}$ | 7.5    | 8.6  | 9.7  | V    | $I_T = 1 \text{ mA}$   |
| Reverse current   | $I_R$    | –      | 1    | 100  | nA   | $V_R = 5.5 \text{ V}$  |

**Table 4 AC characteristics**

| Parameter        | Symbol | Values |      |      | Unit | Note or test condition                               |
|------------------|--------|--------|------|------|------|--|
|                  |        | Min.   | Typ. | Max. |      |  |
| Line capacitance | $C_L$  | 45     | 56   | 67   | pF   | $V_R = 0 \text{ V}, f = 1 \text{ MHz}$ <sup>1)</sup> |
|                  |        | –      | 56   | –    |      | $V_R = 0 \text{ V}, f = 1 \text{ GHz}$               |

**Table 5 ESD and Surge characteristics**

| Parameter                        | Symbol    | Values |      |      | Unit     | Note or test condition                         |
|----------------------------------|-----------|--------|------|------|----------|--|
|                                  |           | Min.   | Typ. | Max. |          |  |
| Clamping voltage <sup>2)</sup>   | $V_{CL}$  | –      | 9.5  | –    | V        | $I_{TLP} = 1 \text{ A}, t_p = 100 \text{ ns}$  |
|                                  |           | –      | 12.5 | –    |          | $I_{TLP} = 16 \text{ A}, t_p = 100 \text{ ns}$ |
|                                  |           | –      | 14.5 | –    |          | $I_{TLP} = 30 \text{ A}, t_p = 100 \text{ ns}$ |
| Clamping voltage <sup>3)</sup>   |           | –      | 9.5  | –    |          | $I_{PP} = 1 \text{ A}, t_p = 8/20 \mu\text{s}$ |
|                                  |           | –      | 10.5 | –    |          | $I_{PP} = 3 \text{ A}, t_p = 8/20 \mu\text{s}$ |
|                                  |           | –      | 12   | –    |          | $I_{PP} = 7 \text{ A}, t_p = 8/20 \mu\text{s}$ |
| Dynamic resistance <sup>2)</sup> | $R_{DYN}$ | –      | 0.15 |      | $\Omega$ | $t_p = 100 \text{ ns}$                         |

<sup>1</sup> Verified by design

<sup>2</sup> Please refer to Application Note AN210 [1]. TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 0.6 \text{ ns}$ .

<sup>3</sup> Stress pulse: 8/20 $\mu\text{s}$  current waveform according to IEC61000-4-5

Typical characteristic diagrams

### 3 Typical characteristic diagrams

Note:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

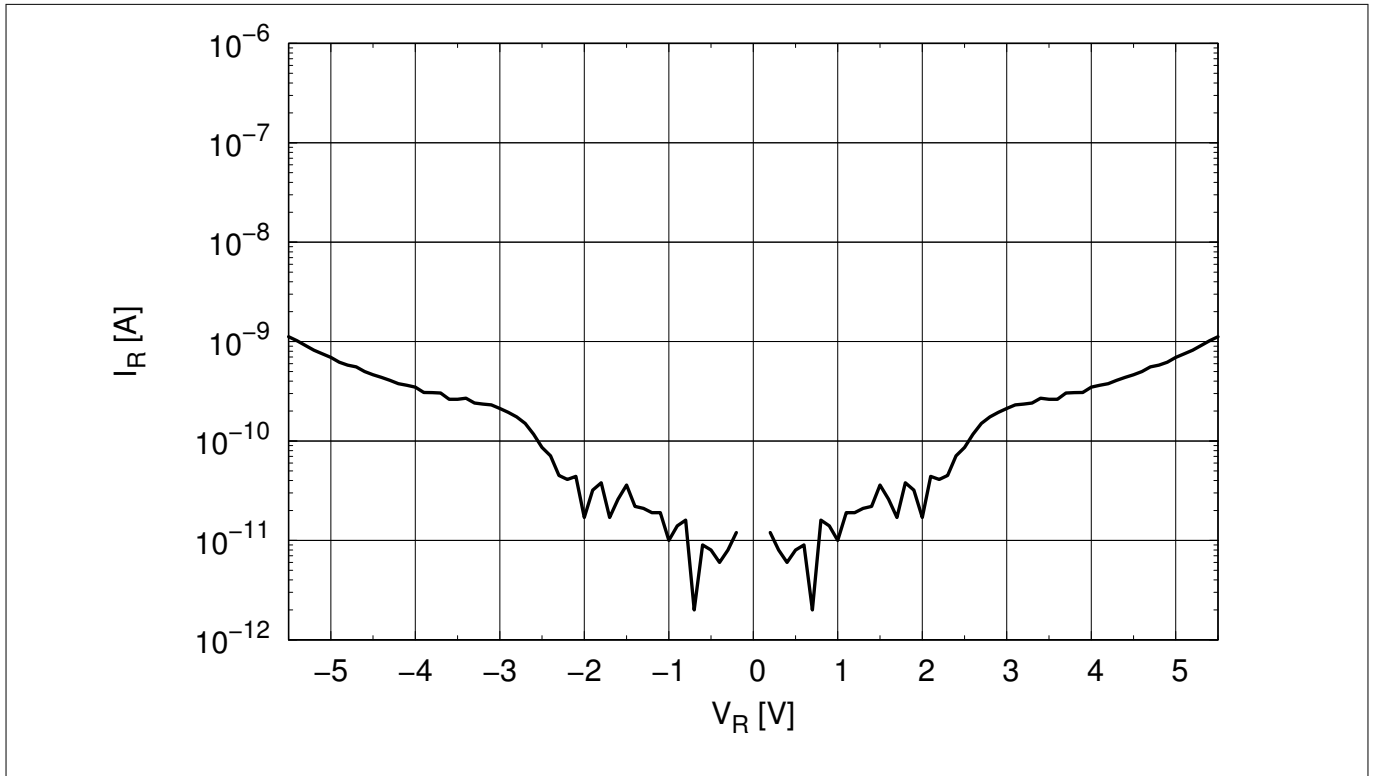


Figure 3 Reverse leakage current:  $I_R = f(V_R)$

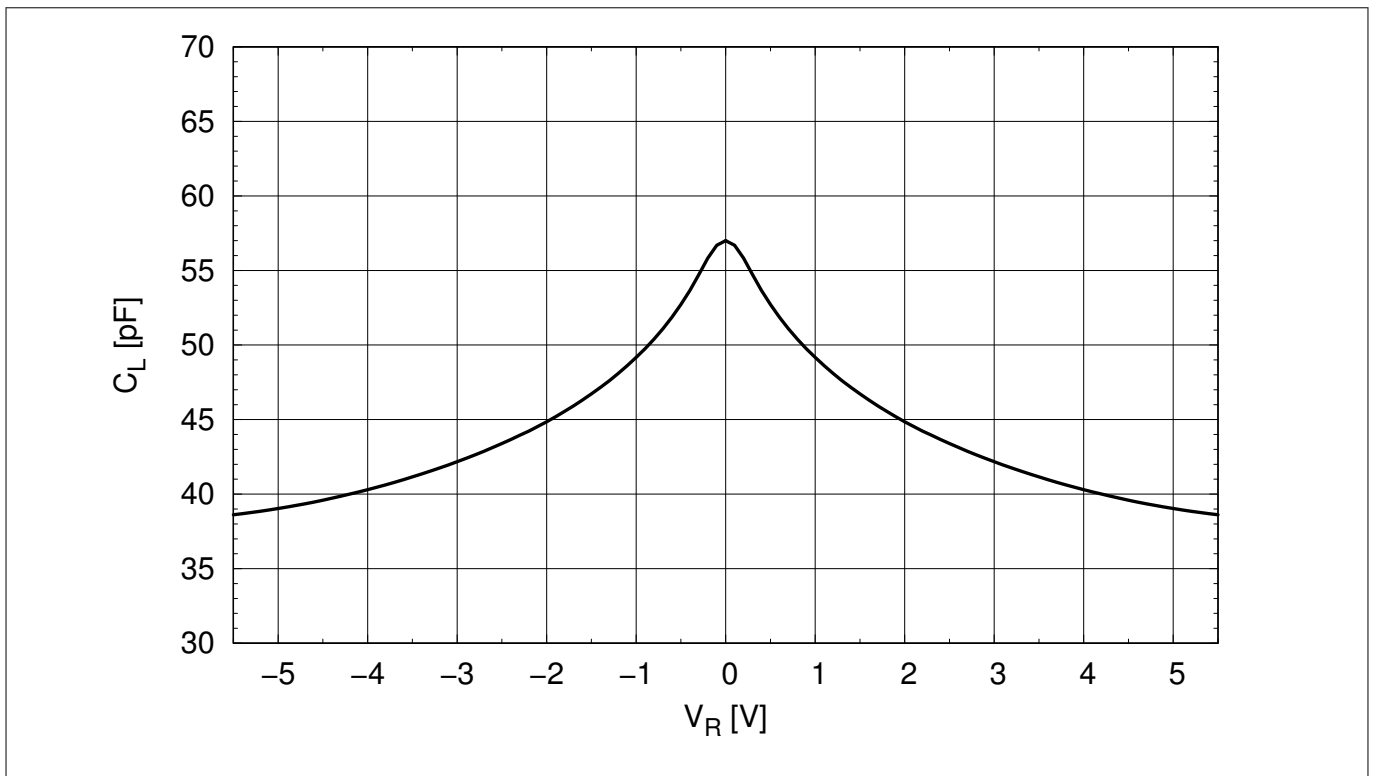


Figure 4 Line capacitance:  $C_L = f(V_R)$ ,  $f = 1\text{ MHz}$

Typical characteristic diagrams

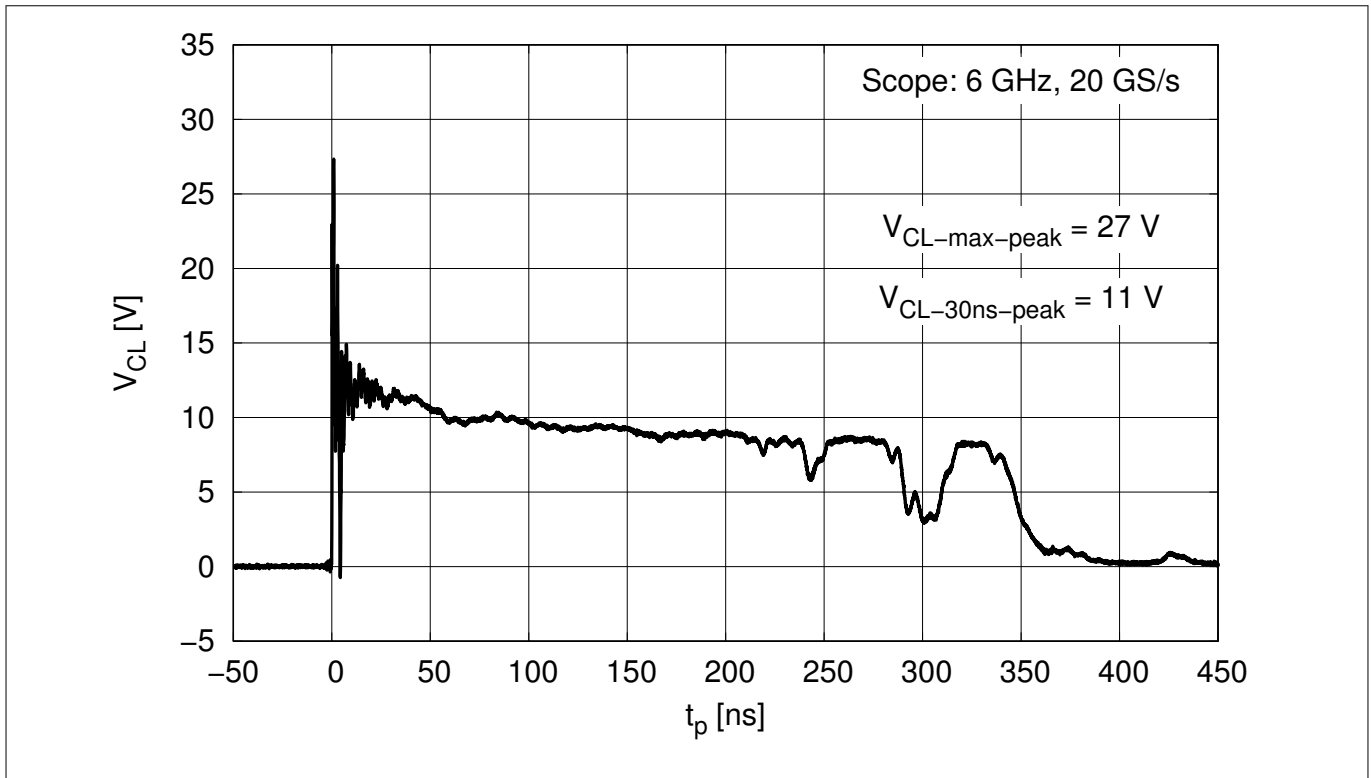


Figure 5 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV positive pulse (according to IEC61000-4-2)

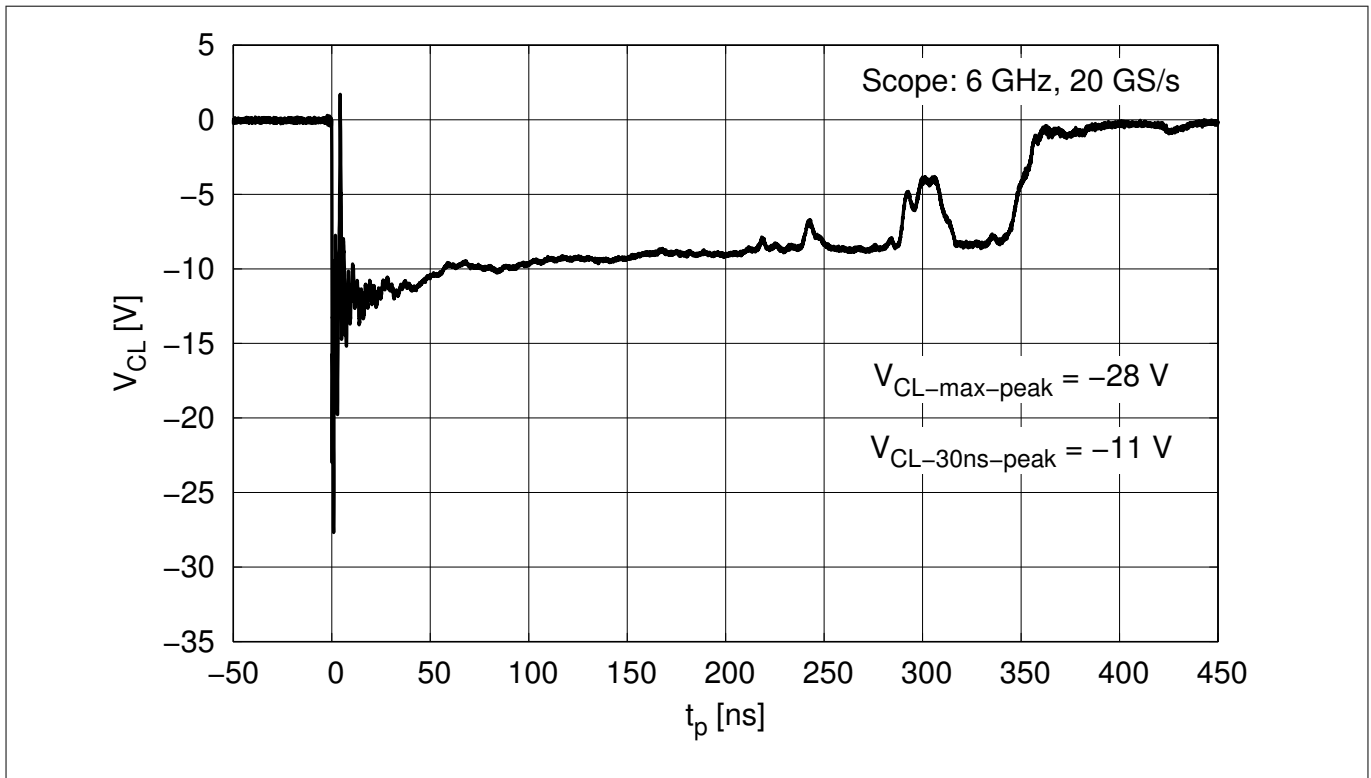


Figure 6 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV negative pulse (according to IEC61000-4-2)

Typical characteristic diagrams

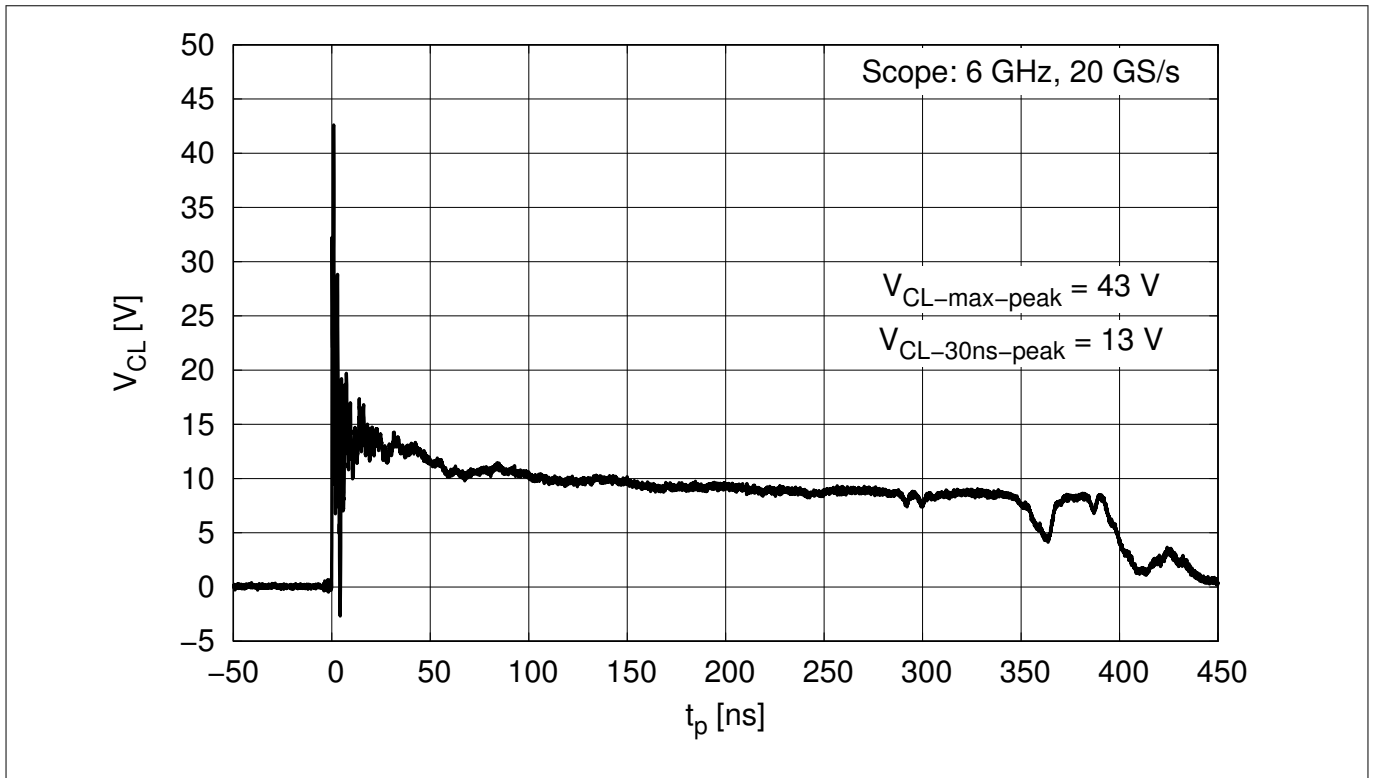


Figure 7 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV positive pulse (according to IEC61000-4-2)

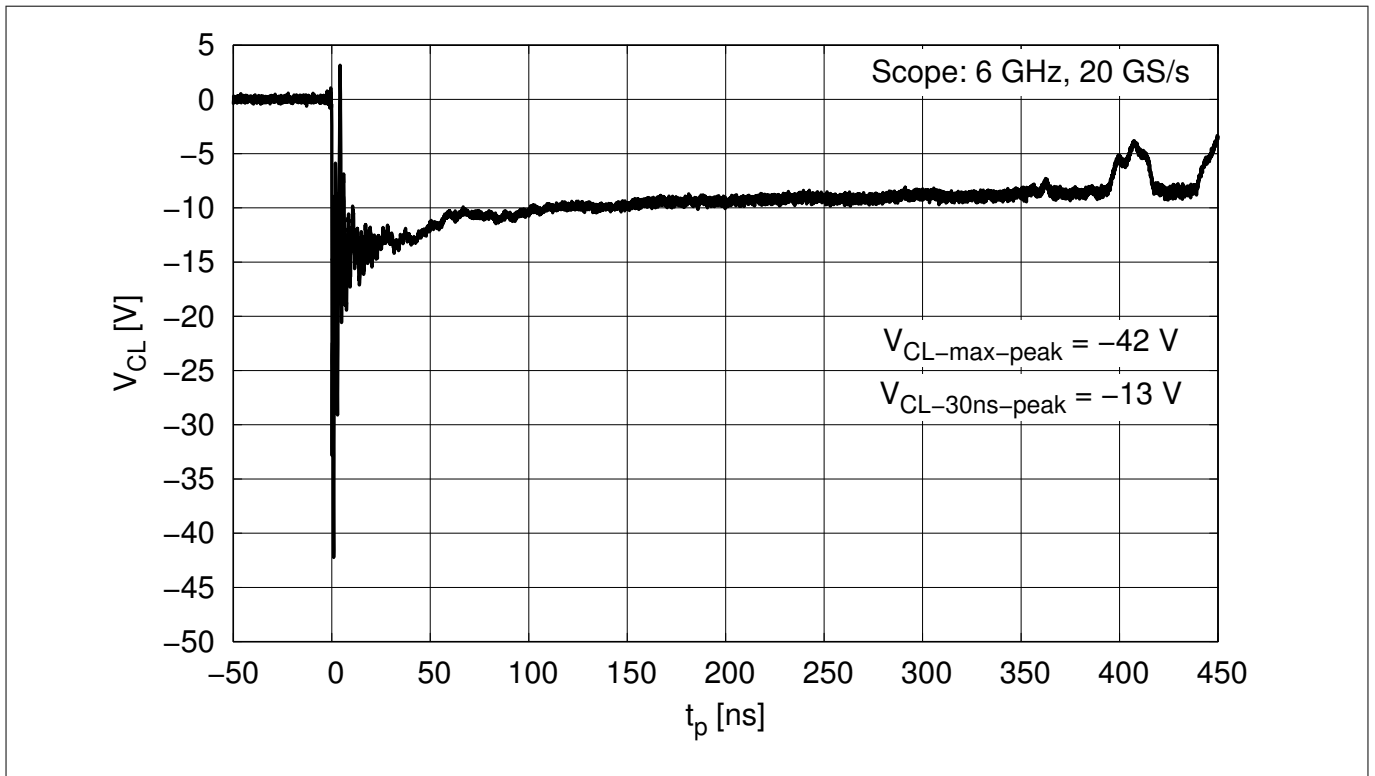


Figure 8 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV negative pulse (according to IEC61000-4-2)



Typical characteristic diagrams

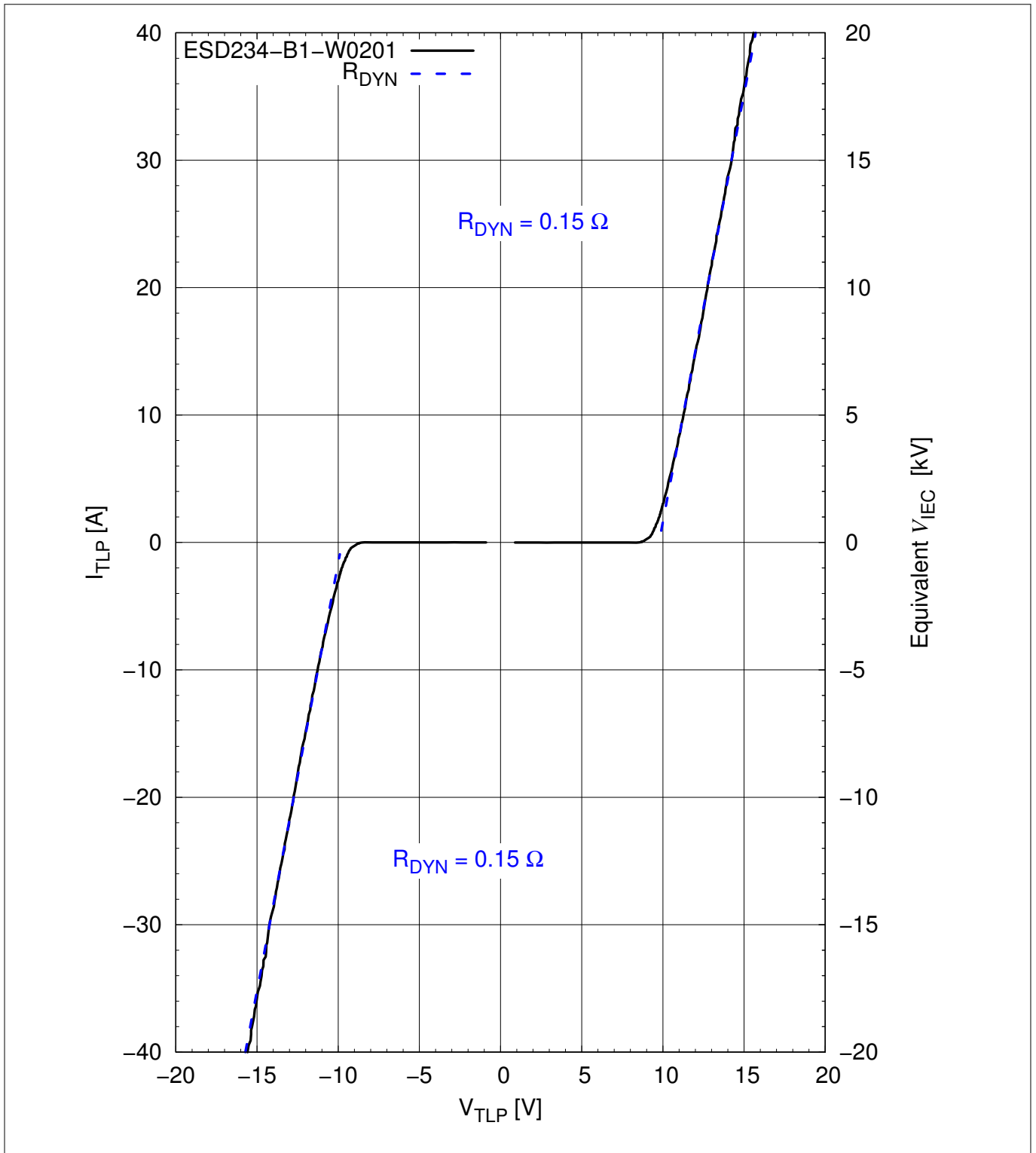


Figure 9 Clamping voltage (TLP):  $I_{TLP} = f(V_{TLP})$  [1]

Typical characteristic diagrams

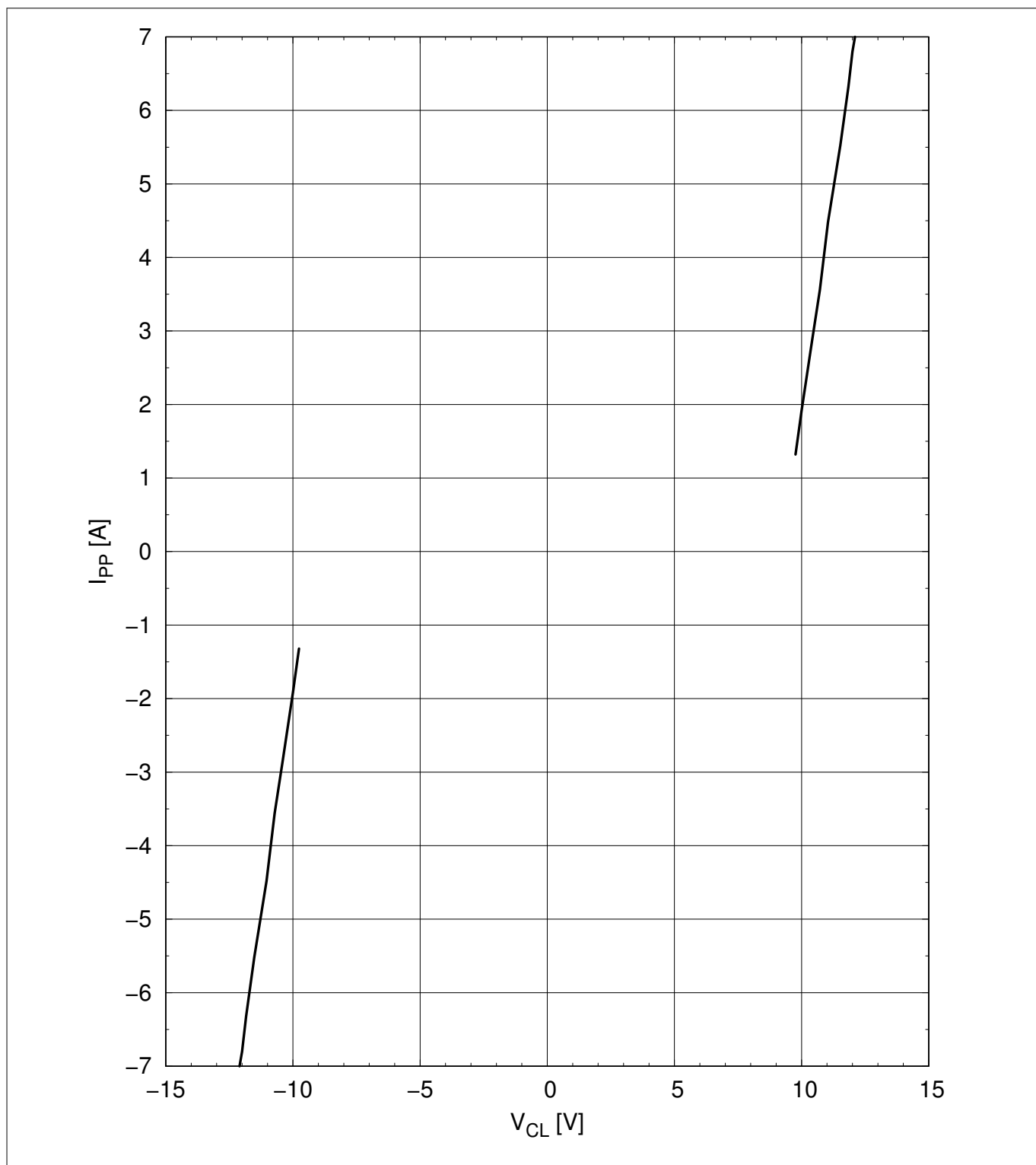


Figure 10 Clamping voltage (Surge):  $I_{PP} = f(V_{CL})$  according to IEC61000-4-5 [1]

Typical characteristic diagrams

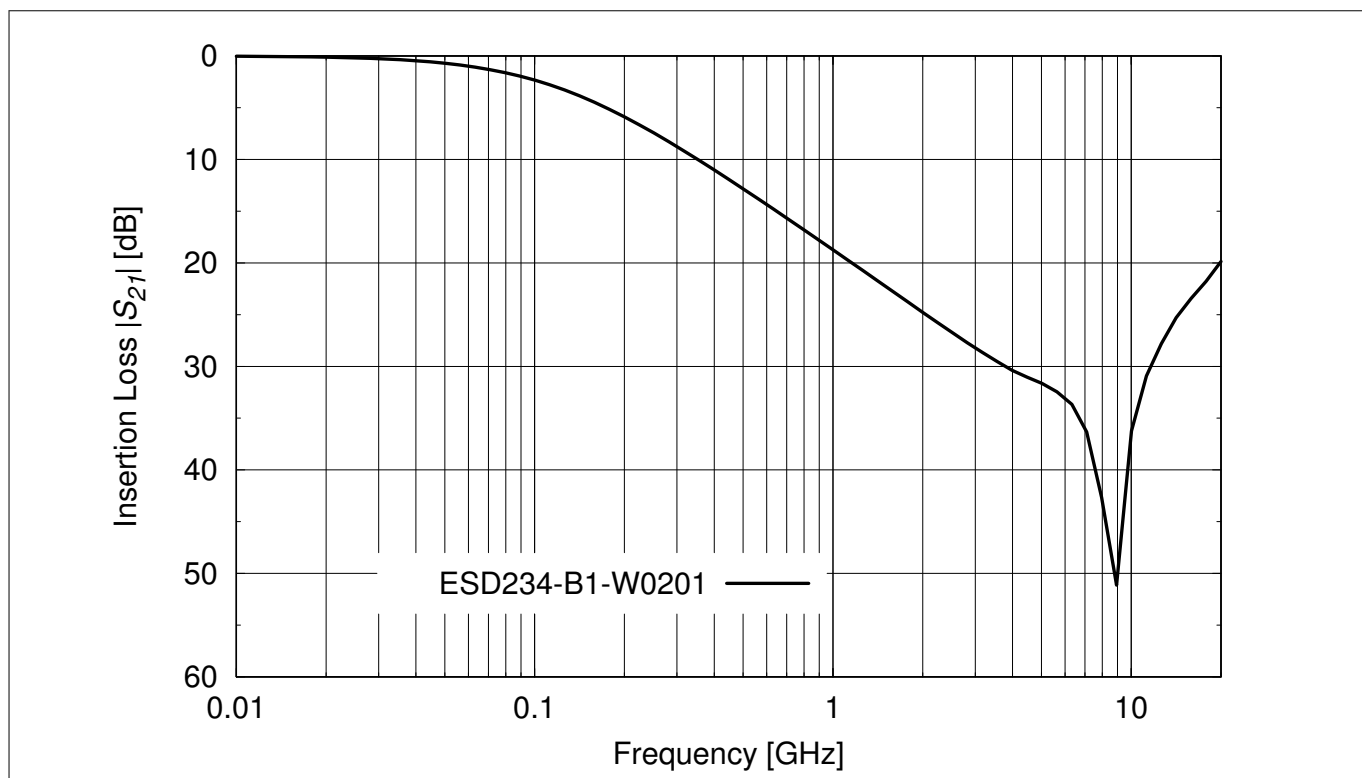


Figure 11 Insertion loss versus frequency in a 50  $\Omega$  system

Package information

## 4 Package information

### 4.1 WLL-2-1 package

Note: All dimensions in mm

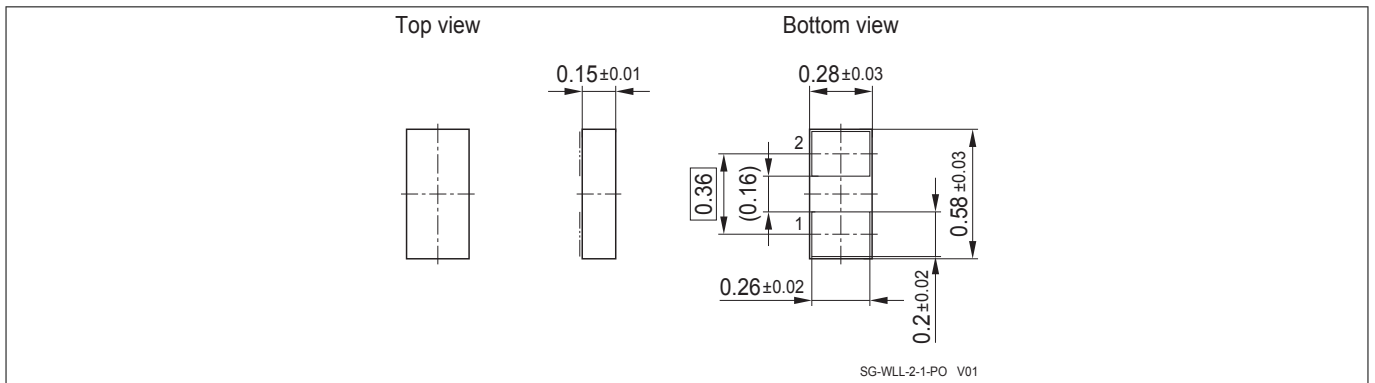


Figure 12 WLL-2-1 package outline

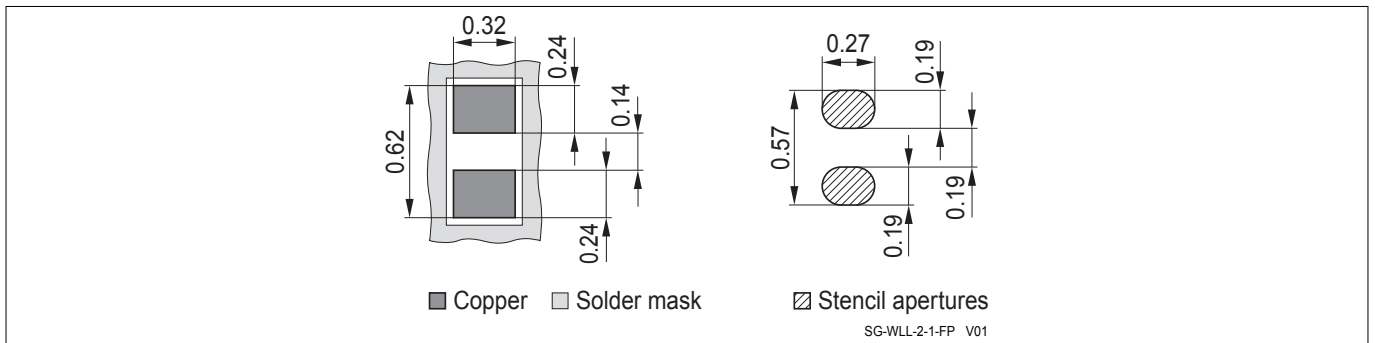


Figure 13 WLL-2-1 footprint

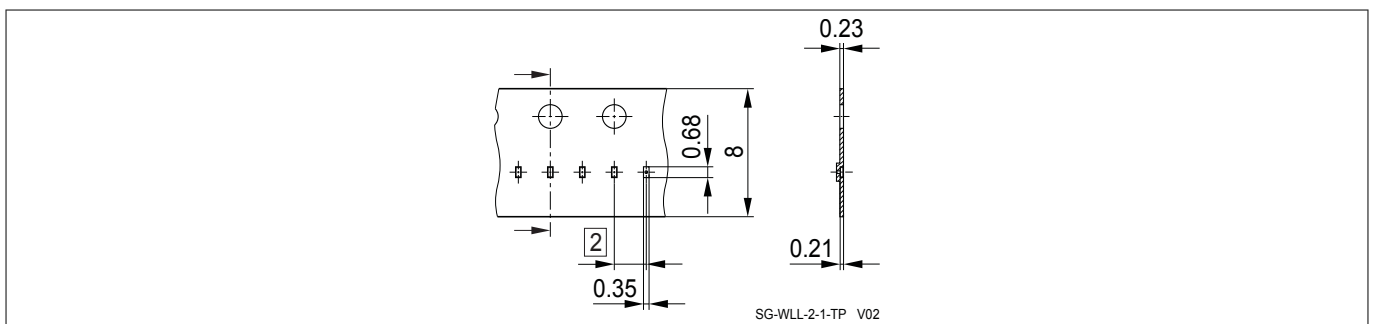


Figure 14 WLL-2-1 packing

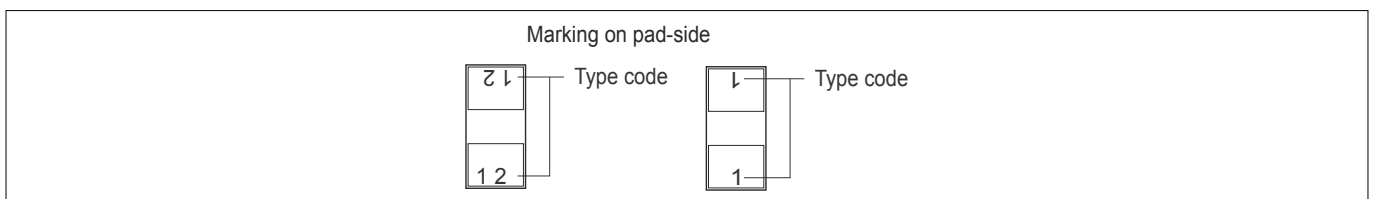


Figure 15 WLL-2-1 marking example (marking code see [Device information](#))

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References

## 5 References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for Printed Circuit Board Assembly of Infineon WLL Packages  
[http://www.infineon.com/Packageinformation\\_WLL](http://www.infineon.com/Packageinformation_WLL)
- [3] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost

## Revision history

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**Revision history: Rev.0.9, 2018-04-17**

| Page or Item             | Subjects (major changes since previous revision)  |
|--------------------------|---|
| Revision 1.0, 2018-09-06 |   |
|                          | Maximum ratings and electrical parameters updated |
|                          | Insertion loss diagram added                      |
|                          |   |

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**Edition 2018-09-06**

**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

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