

N-channel 60 V, 0.021 Ω typ., 7 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet - preliminary data

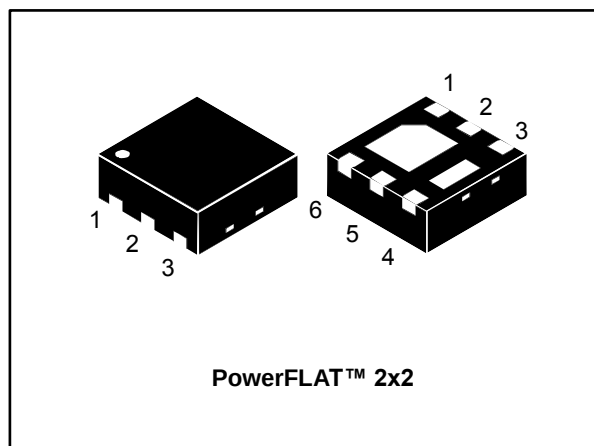
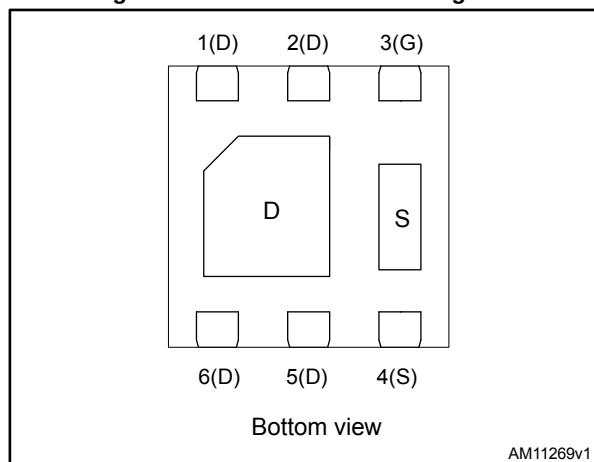


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL7N6F7	60 V	0.025 Ω	7 A

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL7N6F7	ST7N	PowerFLAT™ 2x2	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	7	A
I_D	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	4.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	2.4	W
T_J	Operating junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature		

Notes:

⁽¹⁾Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	52	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ sec.}$

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.5\text{ A}$		0.021	0.025	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	450	-	pF
C_{oss}	Output capacitance		-	210	-	pF
C_{rss}	Reverse transfer capacitance		-	22	-	pF
Q_g	Total gate charge	$V_{DD} = 48\text{ V}$, $I_D = 7\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 3: "Test circuit for gate charge behavior")	-	8	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$, $I_D = 3.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2: "Test circuit for resistive load switching times")	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 7: Source-drain diode

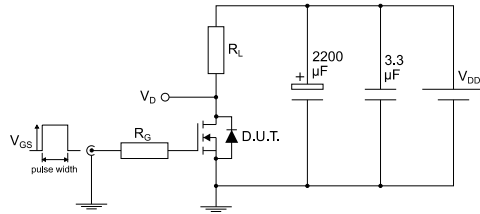
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_D = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 48\text{ V}$ (see Figure 4: "Test circuit for inductive load switching and diode recovery times")	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		nC
I_{RRM}	Reverse recovery current		-	TBD		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

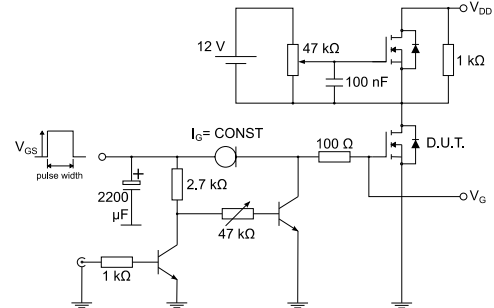
3 Test circuits

Figure 2: Test circuit for resistive load switching times



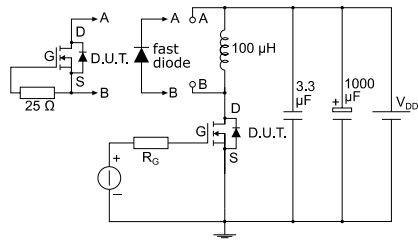
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Figure 3: Test circuit for gate charge behavior



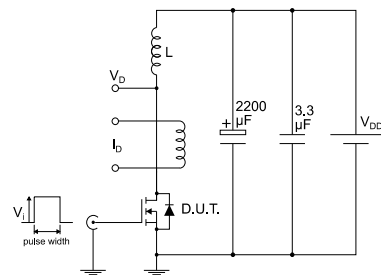
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Figure 4: Test circuit for inductive load switching and diode recovery times



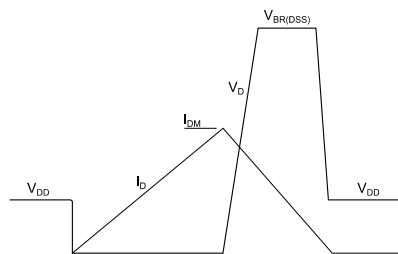
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Figure 5: Unclamped inductive load test circuit



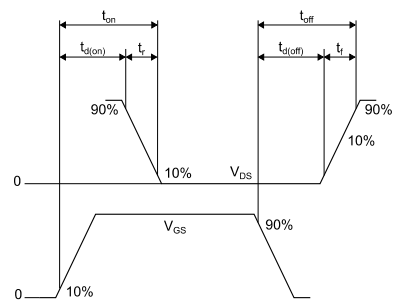
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Figure 6: Unclamped inductive waveform



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Figure 7: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT 2x2 package information

Figure 8: PowerFLAT™ 2x2 package outline

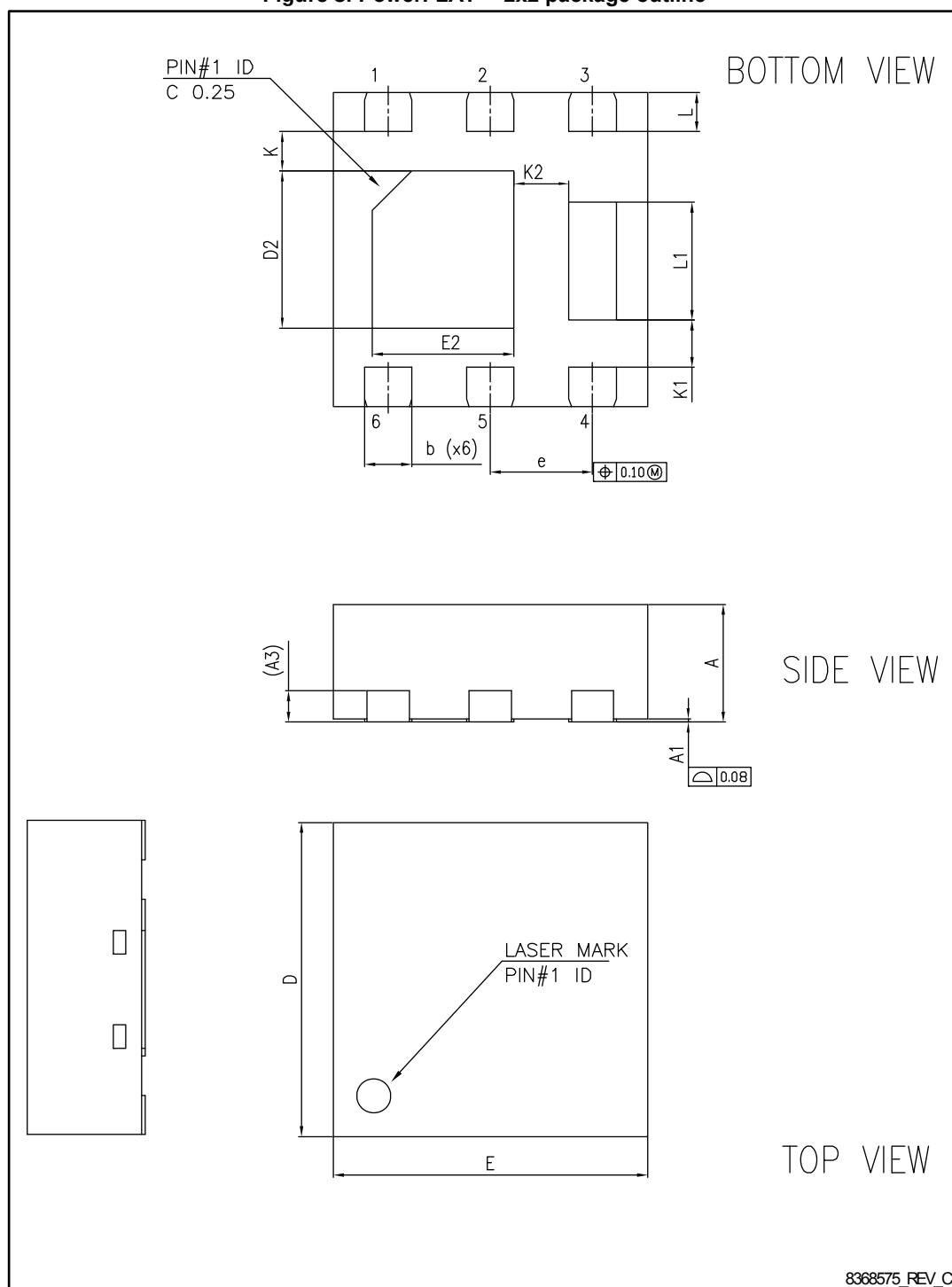
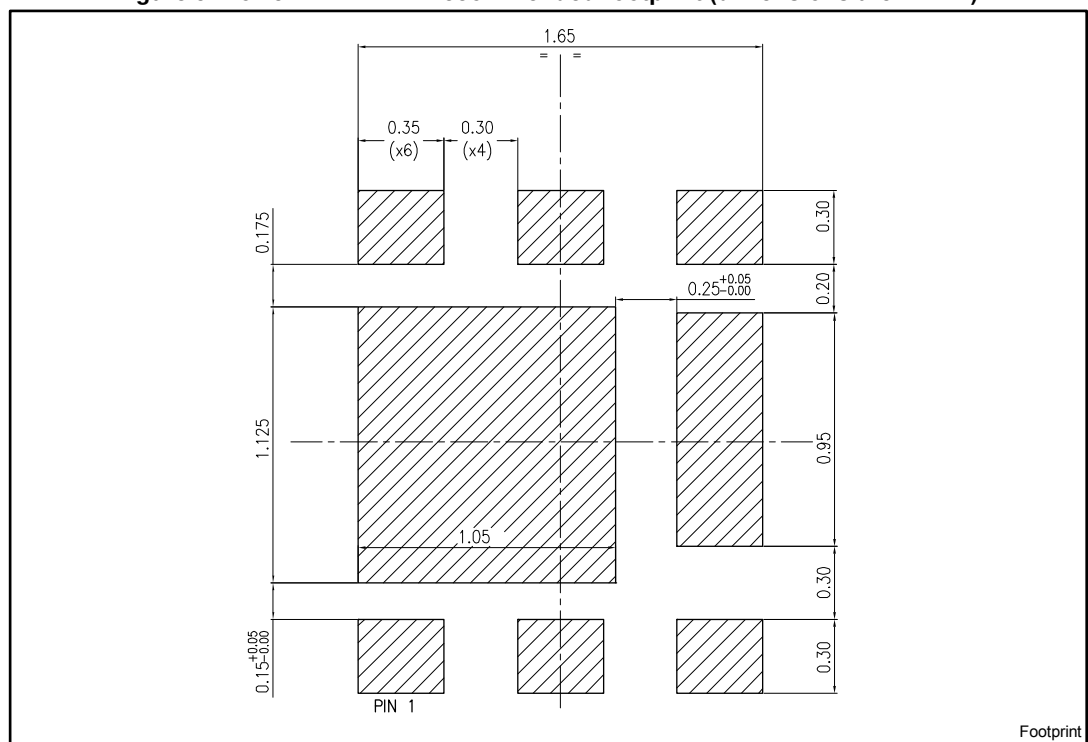


Table 8: PowerFLAT™ 2x2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 9: PowerFLAT™ 2x2 recommended footprint (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
27-Aug-2015	1	First release.

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