DLPC3436 Display Controller

1 Features

- DLP230NP (.23 1080p) DMD Display Controller
  - Supports Input Resolutions Up to 1080p
  - Low-Power DMD Interface With Interface Training
- Input Frame Rates Up to 240 Hz (60 Hz at 1080p Resolution)
- 24-Bit, Input Pixel Interface Support:
  - Parallel Interface Protocol
  - Pixel Clock up to 150 MHz
  - Multiple Input Pixel Data Format Options
- Pixel Data Processing Including:
  - IntelliBright™ Suite of Image Processing Algorithms
    - Content Adaptive Illumination Control
    - Local Area Brightness Boost
  - Color Coordinate Adjustment
  - Active Power Management Processing
- External Flash Support
- Embedded Frame Memory (eDRAM)
- System Features:
  - I^2C Control of Device Configuration
  - Programmable LED Current Control
  - One Frame Latency

2 Applications

- DLP Signage
- Mobile Projector
- Mobile Smart TV
- Smart Speaker
- Virtual / Augmented Reality Headsets & Glasses
- Mobile Accessory
- Smart home displays
- Pico projectors

3 Description

The DLPC3436 digital controller, a component of the DLP230NP (.23 1080p) chipset, supports reliable operation of the DLP230NP digital micromirror device (DMD). The DLP230NP chipset enables small form factor, low power, and high resolution 1080p displays.

Visit the *Getting Started with TI DLP® Pico™ Display Technology* page to learn more about the DLP230NP chipset.

The DLP230NP chipset includes established resources to help the user accelerate the design cycle, which include production ready optical modules, optical modules manufactures, and design houses.

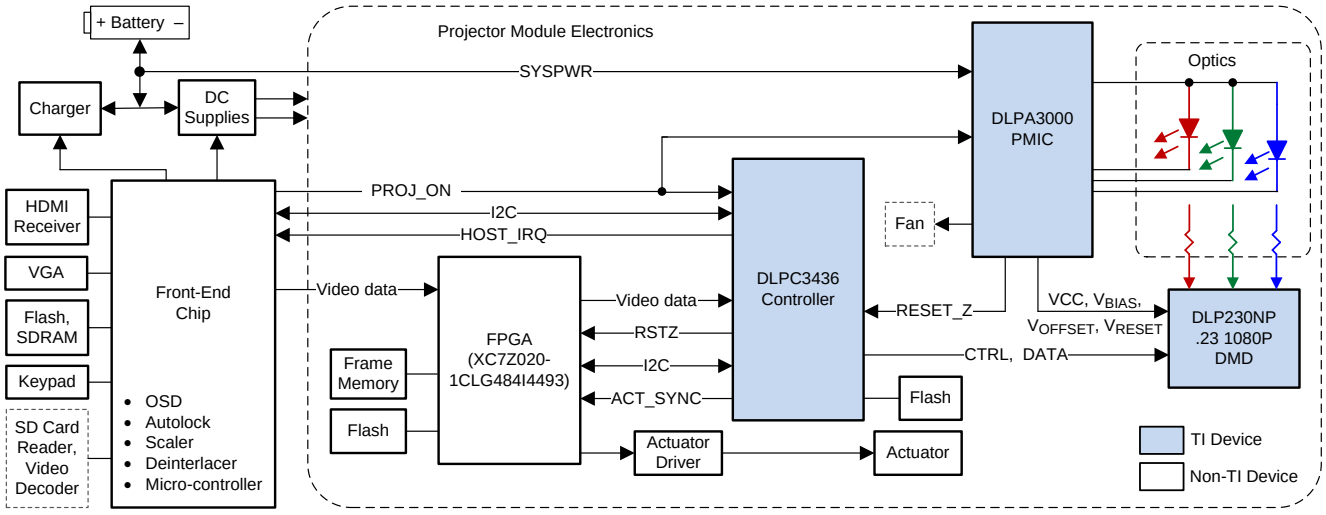
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC3436	NFBGA (176)	7.00 × 7.00 mm²

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

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4 Revision History

DATE	REVISION	NOTES
January 2019	*	Initial release.

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5 Device and Documentation Support

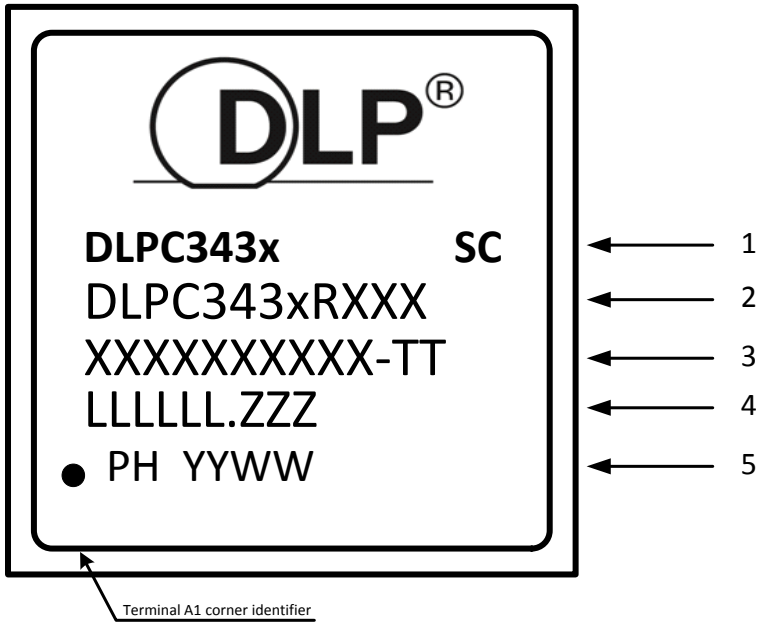
5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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5.1.2 Device Nomenclature

5.1.2.1 Device Markings



Marking Definitions:

Line 1:	DLP® Device Name: DLPC343x where**x** is a "6" for this device. SC: Solder ball composition e1: Indicates lead-free solder balls consisting of SnAgCu G8: Indicates lead-free solder balls consisting of tin-silver-copper (SnAgCu) with silver content less than or equal to 1.5% and that the mold compound meets TI's definition of green.
Line 2:	TI Part Number DLP® Device Name: DLPC343x = **x** is a "6" for this device. **R** corresponds to the TI device revision letter for example A, B or C **XXX** corresponds to the device package designator.
Line 3:	XXXXXXXXXX-TT Manufacturer Part Number
Line 4:	LLLLLL.ZZZ Foundry lot code for semiconductor wafers LLLLLL: Fab lot number ZZZ: Lot split number
Line 5:	PH YYWW ES : Package assembly information PH: Manufacturing site YYWW: Date code (YY = Year :: WW = Week)

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Device Support (continued)

NOTE

1. Engineering prototype samples are marked with an **X** suffix appended to the TI part number. For example, 2512737-0001X.

5.1.3 Video Timing Parameter Definitions

Active Lines Per Frame (ALPF) Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.

Active Pixels Per Line (APPL) Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.

Horizontal Back Porch (HBP) Blanking Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.

Horizontal Front Porch (HFP) Blanking Number of blank pixel clocks after the last active pixel but before Horizontal Sync.

Horizontal Sync (HS) Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.

Total Lines Per Frame (TLPF) Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).

Total Pixel Per Line (TPPL) Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).

Vertical Sync (VS) Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.

Vertical Back Porch (VBP) Blanking Number of blank lines after the leading edge of vertical sync but before the first active line.

Vertical Front Porch (VFP) Blanking Number of blank lines after the last active line but before the leading edge of vertical sync.

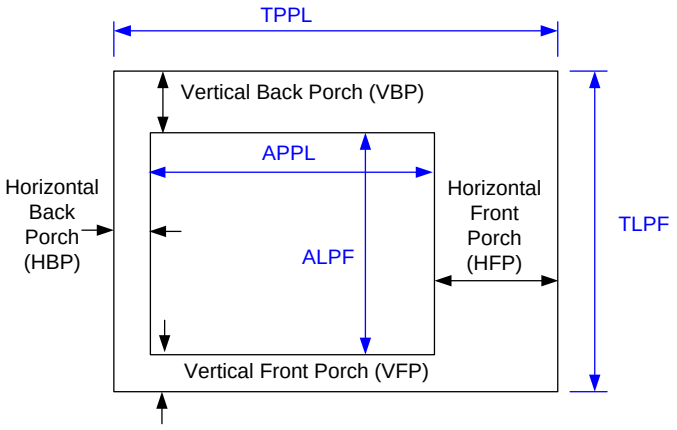


Figure 1. Timing Parameter Diagram

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5.2 Documentation Support

5.2.1 Related Documentation

The following table lists quick access links for associated parts of the DLP chipset:

Table 1. Chipset Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE
DLPA2000	Click here	Click here	Click here	Click here
DLPA2005	Click here	Click here	Click here	Click here
DLPA3000	Click here	Click here	Click here	Click here
DLP230NP	Click here	Click here	Click here	Click here

5.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

5.4 Trademarks

IntelliBright, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

5.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

5.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC3436CZVB	PREVIEW	NFBGA	ZVB	176	260	TBD	Call TI	Call TI			
XDLPC3436CZVB	ACTIVE	NFBGA	ZVB	176	260	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

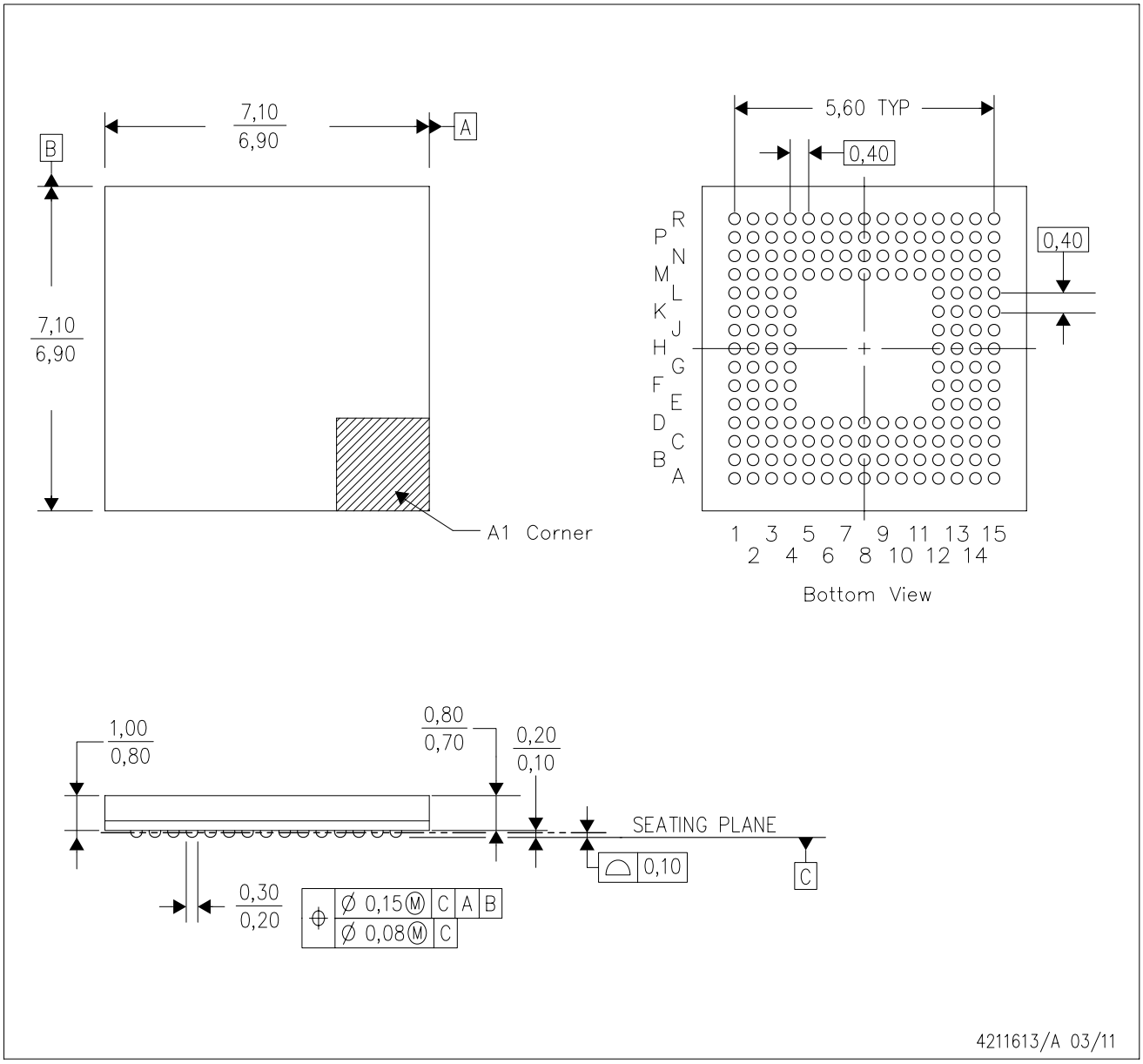
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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ZVB (S–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

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