符合 Qi (WPC v1.2) 标准的 bq51013B 高度集成式无线接收器电源

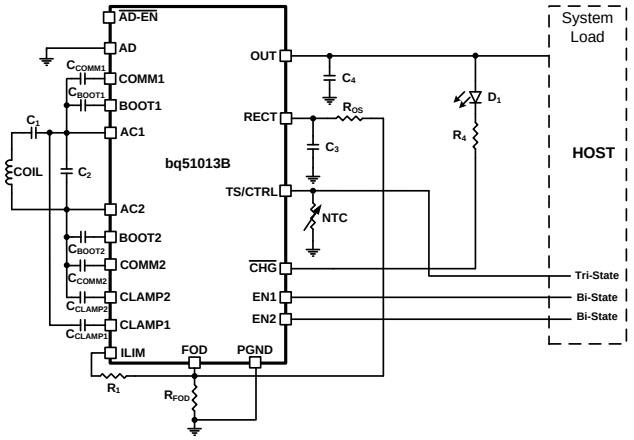
1 特性

- 集成式无线电源接收器解决方案
  - 93% 的整体峰值交流/直流转换效率
  - 完全同步整流器
  - 符合 WPC v1.2 标准的通信控制
  - 输出电压调节
  - 仅在 Rx 线圈和输出之间需要 IC
- 符合无线电源联盟 (WPC) v1.2 标准（启用 FOD）的高精度电流检测
- 动态整流器控制，可改进负载瞬态响应
- 可在宽泛的输出电源范围内优化性能的动态效率调节
- 针对稳健通信的自适应通信限制
- 支持 20V 最高输入电压
- 低功率耗散整流器过压钳位 (V_{OVP} = 15V)
- 热关断
- 用于温度监控、充电完成和故障主机控制的多功能 NTC 和控制引脚

2 应用

- 符合 WPC v1.2 标准的接收器
- 手机和智能电话
- 耳机
- 数码摄像机
- 便携式媒体播放器
- 手持设备

简化原理图



3 说明

bq51013B 器件是灵活的高级单芯片次级侧器件，适用于便携式 应用 中的无线电力传输，可提供高达 5W 的功率。bq51013B 器件在集成符合无线电源联盟 (WPC) Qi v1.2 通信协议所需的数字控制的同时提供接收器 (RX) 交流/直流电源转换和调节。bq51013B 与 bq50012A 初级侧控制器（或其他 Qi 发送器）相结合，可为无线电源解决方案实现一款完整的非接触式电力传输系统。使用 Qi v1.2 协议，在次级侧与初级侧之间建立全局反馈，从而控制电力传输过程。

bq51013B 集成了一个低电阻同步整流器、低压降稳压器、数字控制以及精确电压和电流回路，可确保高效率和低功率耗散。

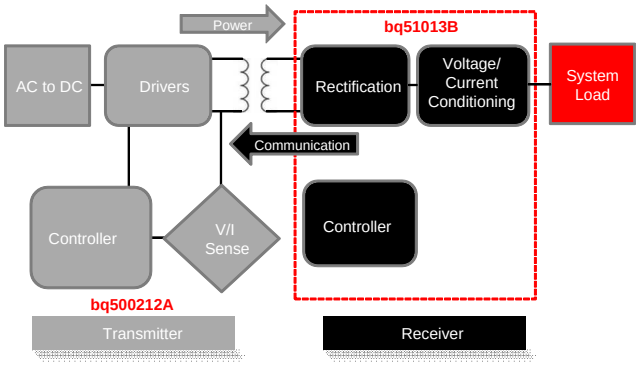
bq51013B 还包括一个数字控制器，用于计算移动设备接收的电量（不超过 WPC v1.2 标准设定的限值）。然后，控制器将该信息传输至发送器 (TX)，以便 TX 能够确定磁性界面内是否存在异物以及是否需要提升磁场内的安全级别。该异物检测 (FOD) 方法属于 WPC v1.2 规范中要求的一部分。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
bq51013B	VQFN (20)	4.50mm x 3.50mm
	DSBGA (28)	3.00mm x 1.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

无线电源系统概述



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (August 2015) to Revision C **Page**

- 通篇将“WPC v1.1”更改成了“WPC v1.2” ... 1
- Deleted the *Device Comparison Table* ... 4

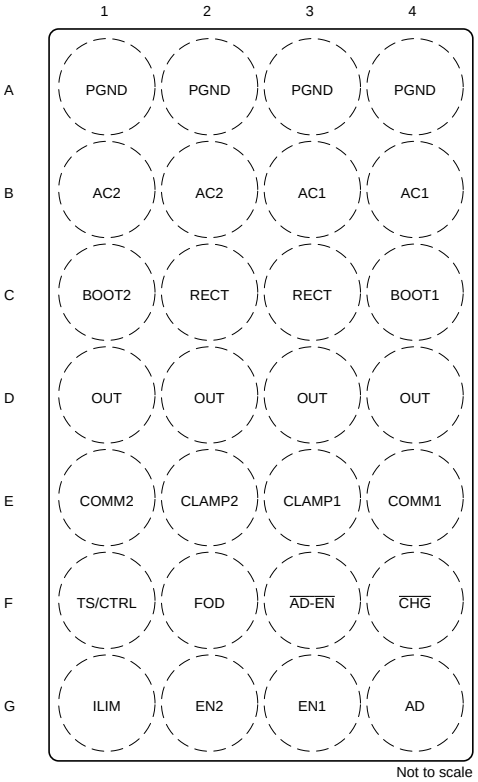
Changes from Revision A (October 2013) to Revision B **Page**

- 已添加 添加了 *ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- Added V_{AD} for clarity ... 6
- Changed UVLO to V_{UVLO} for clarity ... 6
- Added $V_{HYS-UVLO}$ for clarity ... 6
- Added $V_{HYS-OVP}$ for clarity ... 6
- Added $V_{COLD-Hyst}$ for clarity ... 7
- Added $V_{HOT-Hyst}$ for clarity ... 7
- Changed V_{CTRL} for clarity ... 7
- Changed T_{J-SD} and T_{J-Hys} for clarity ... 7
- Added $V_{AD-Pres}$ and $V_{AD-PresH}$ for clarity ... 8
- Changed to $V_{AD-Diff}$ for clarity ... 8
- Added I_{OUT-SR} and $I_{OUT-SRH}$ for clarity ... 8
- Changed Conditons for correct EPT packet ... 18
- Added state [0 1] for clarity ... 24

Changes from Original (March 2013) to Revision A **Page**

5 Pin Configuration and Functions

YFP Package
28-Pin DSBGA
Top View



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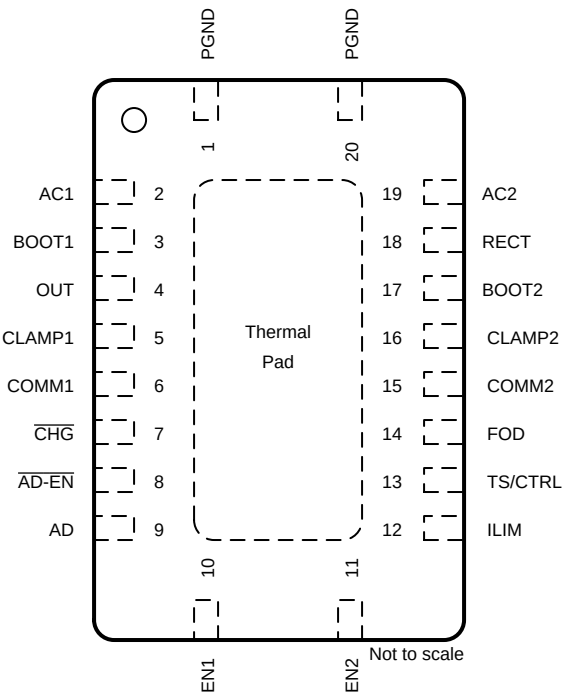
RHL Package
20-Pin VQFN
Top View



Not to scale

The exposed thermal pad should be connected to ground.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	YFP	RHL		
AC1	B3, B4	2	I	AC input from receiver coil.
AC2	B1, B2	19	I	
AD	G4	9	I	If AD functionality is used, connect this pin to the wired adapter input. When $V_{AD-Pres}$ is applied to this pin wireless charging is disabled and $\overline{AD\_EN}$ is driven low. Connect a 1-µF capacitor from AD to PGND. If unused, the capacitor is not required and AD should be connected directly to PGND.
$\overline{AD-EN}$	F3	8	O	Push-pull driver for external PFET when wired charging is active. Float if not used.
BOOT1	C4	3	O	Bootstrap capacitors for driving the high-side FETs of the synchronous rectifier. Connect a 10-nF ceramic capacitor from BOOT1 to AC1 and from BOOT2 to AC2.
BOOT2	C1	17	O	
$\overline{CHG}$	F4	7	O	Open-drain output – active when OUT is enabled. Float or tie to PGND if unused.
CLAMP2	E2	16	O	Open-drain FETs which are used for a non-power dissipative overvoltage AC clamp protection. When the RECT voltage goes above 15 V, both switches will be turned on and the capacitors will act as a low impedance to protect the device from damage. If used, capacitors are used to connect CLAMP1 to AC1 and CLAMP2 to AC2. Recommended connections are 0.47-µF capacitors.
CLAMP1	E3	5	O	
COMM1	E4	6	O	Open-drain outputs used to communicate with primary by varying reflected impedance. Connect a capacitor from COMM1 to AC1 and a capacitor from COMM2 to AC2 for capacitive load modulation. For resistive modulation connect COMM1 and COMM2 to RECT through a single resistor. See *Communication Modulator* for more information.
COMM2	E1	15	O	
EN1	G3	10	I	Inputs that allow user to enable and disable wireless and wired charging <EN1 EN2>: <00> Wireless charging is enabled unless AD voltage > V_{AD_Pres}. <01> Dynamic communication current limit disabled. <10> $\overline{AD-EN}$ pulled low, wireless charging disabled. <11> Wired and wireless charging disabled.
EN2	G2	11	I	

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	YFP	RHL		
FOD	F2	14	I	Input for the rectified power measurement. See *WPC v1.2 Compliance – Foreign Object Detection* for details.
ILIM	G1	12	I/O	Programming pin for the over current limit. The total resistance from ILIM to GND (R_{ILIM}) sets the current limit. The schematic shown in Figure 38 illustrates the R_{ILIM} as R_1 + R_{FOD}. Details can be found in *Electrical Characteristics* and Figure 38.
OUT	D1, D2, D3, D4	4	O	Output pin, delivers power to the load.
PGND	A1, A2, A3, A4	1, 20		Power ground
RECT	C2, C3	18	O	Filter capacitor for the internal synchronous rectifier. Connect a ceramic capacitor to PGND. Depending on the power levels, the value may be 4.7 μF to 22 μF.
TS/CTRL	F1	13	I	Dual function pin: Temperature Sense (TS) and Control (CTRL) pin functionality. For the TS functionality connect TS/CTRL to ground through a Negative Temperature Coefficient (NTC) resistor. If an NTC function is not desired, connect to PGND with a 10-kΩ resistor. See *Temperature Sense Resistor Network (TS)* for more details. For the CTRL functionality pull below $V_{CTRL-Low}$ or pull above $V_{CTRL-High}$ to send an End Power Transfer Packet. See Table 4 for more details.
—	—	PAD	—	The exposed thermal pad should be connected to ground (PGND)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Input voltage	AC1, AC2	–0.8	20	V
	RECT, COMM1, COMM2, OUT, $\overline{CHG}$, CLAMP1, CLAMP2	–0.3	20	
	AD, $\overline{AD\text{-}EN}$	–0.3	30	
	BOOT1, BOOT2	–0.3	26	
	EN1, EN2, FOD, TS/CTRL, ILIM	–0.3	7	
Input current	AC1, AC2		2	A(RMS)
Output current	OUT		1.5	A
Output sink current	$\overline{CHG}$		15	mA
	COMM1, COMM2		1	A
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) All voltages are with respect to the VSS terminal, unless otherwise noted.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{RECT}	Voltage	RECT	4	10	V
I_{RECT}	Current through internal rectifier	RECT		1.5	A
I_{OUT}	Output current	OUT		1.5	A
V_{AD}	Adapter voltage	AD		15	V
I_{AD-EN}	Sink current	$\overline{\text{AD-EN}}$		1	mA
I_{COMM}	COMMx sink current	COMM1, COMM2		500	mA
T_J	Junction temperature		0	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		bq51013B		UNIT
		RHL (VQFN)	YFP (DSBGA)	
		20 PiNS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.7	58.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.5	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	9.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.5	8.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range, –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Undervoltage lockout	V_{RECT}: 0 V → 3 V	2.5	2.7	2.8	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{RECT}: 3 V → 2 V		250		mV
$V_{RECT-OVP}$	Input overvoltage threshold	V_{RECT}: 5 V → 16 V	14.5	15	15.5	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{RECT}: 16 V → 5 V		150		mV
$V_{RECT-Th1}$	Dynamic V_{RECT} Threshold 1	I_{LOAD} < 0.1 x I_{IMAX} (I_{LOAD} rising)		7.08		V
$V_{RECT-Th2}$	Dynamic V_{RECT} Threshold 2	0.1 x I_{IMAX} < I_{LOAD} < 0.2 x I_{IMAX} (I_{LOAD} rising)		6.28		V
$V_{RECT-Th3}$	Dynamic V_{RECT} Threshold 3	0.2 x I_{IMAX} < I_{LOAD} < 0.4 x I_{IMAX} (I_{LOAD} rising)		5.53		V
$V_{RECT-Th4}$	Dynamic V_{RECT} Threshold 4	I_{LOAD} > 0.4 x I_{IMAX} (I_{LOAD} rising)		5.11		V
$V_{RECT-Track}$	V_{RECT} TRACKING	In current limit, voltage above V_{OUT}		V_{OUT}+0.25		V
I_{LOAD}	I_{LOAD} Hysteresis for dynamic V_{RECT} thresholds as a % of I_{ILIM}	I_{LOAD} falling		4%		
$V_{RECT-DPM}$	Rectifier undervoltage protection, restricts I_{OUT} at $V_{RECT-DPM}$		3	3.1	3.2	V
$V_{RECT-REV}$	Rectifier reverse voltage protection at the output	$V_{RECT-REV}$ = V_{OUT} - V_{RECT}, V_{OUT} = 10 V		8	9	V
QUIESCENT CURRENT						
I_{RECT}	Active chip quiescent current consumption from RECT	I_{LOAD} = 0 mA, 0°C ≤ T_J ≤ 85°C		8	10	mA
		I_{LOAD} = 300 mA, 0°C ≤ T_J ≤ 85°C		2	3	mA
I_{OUT}	Quiescent current at the output when wireless power is disabled (Standby)	V_{OUT} = 5 V, 0°C ≤ T_J ≤ 85°C		20	35	µA

Electrical Characteristics (continued)

over operating free-air temperature range, –40°C to 125°C (unless otherwise noted)

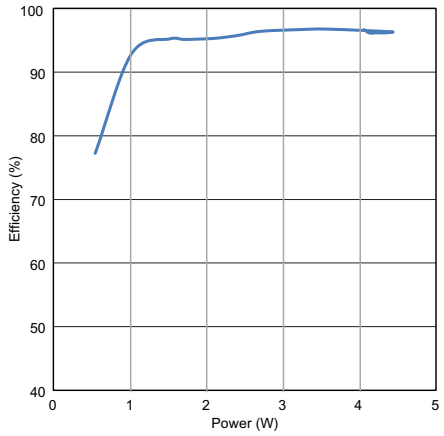
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM} SHORT CIRCUIT						
$R_{ILIM-SHORT}$	Highest value of ILIM resistance to ground (R_{ILIM}) considered a fault (short). Monitored for I_{OUT} > 100 mA	R_{ILIM}: 200 Ω → 50 Ω. I_{OUT} latches off, cycle power to reset			120	Ω
$t_{DGL-Short}$	Deglitch time transition from ILIM short to I_{OUT} disable			1		ms
$I_{ILIM\_SHORT,OK}$	$I_{LIM-SHORT,OK}$ enables the ILIM short comparator when I_{OUT} is greater than this value	I_{LOAD}: 0 mA → 200 mA	116	145	165	mA
$I_{ILIM\_SHORT,OK\ HYST}$	Hysteresis for $I_{LIM-SHORT,OK}$ comparator	I_{LOAD}: 0 mA → 200 mA		30		mA
I_{OUT}	Maximum output current limit, C_L	Maximum I_{LOAD} that will be delivered for 1 ms when I_{LIM} is shorted			2.45	A
OUTPUT						
$V_{OUT-REG}$	Regulated output voltage	I_{LOAD} = 1000 mA	4.95	5.00	5.04	V
		I_{LOAD} = 10 mA	4.96	5.01	5.06	
K_{ILIM}	Current programming factor for hardware protection	$R_{ILIM} = K_{ILIM} / I_{ILIM}$, where I_{ILIM} is the hardware current limit. I_{OUT} = 1 A	303	314	321	AΩ
K_{IMAX}	Current programming factor for the nominal operating current	$I_{IMAX} = K_{IMAX} / R_{ILIM}$ where I_{MAX} is the maximum normal operating current. I_{OUT} = 1 A		262		AΩ
I_{OUT}	Current limit programming range				1500	mA
I_{COMM}	Current limit during WPC communication	I_{OUT} > 300 mA		I_{OUT} + 50		mA
		I_{OUT} < 300 mA	330	381	426	mA
t_{HOLD}	Hold off time for the communication current limit during start-up			1		s
TS / CTRL FUNCTIONALITY						
$V_{TS-Bias}$	Internal TS Bias Voltage (V_{TS} is the voltage at the TS/CTRL pin, $V_{TS-Bias}$ is thet internal bias voltage)	$I_{TS-Bias}$ < 100 µA (periodically driven see $t_{TS/CTRL}$)	2	2.2	2.4	V
V_{COLD}	Rising threshold	$V_{TS-Bias}$: 50% → 60%	56.5	58.7	60.8	$\%V_{TS-Bias}$
$V_{COLD-Hyst}$	Falling hysteresis	$V_{TS-Bias}$: 60% → 50%		2		$\%V_{TS-Bias}$
V_{HOT}	Falling threshold	$V_{TS-Bias}$: 20% → 15%	18.5	19.6	20.7	$\%V_{TS-Bias}$
$V_{HOT-Hyst}$	Rising hysteresis	$V_{TS-Bias}$: 15% → 20%		3		$\%V_{TS-Bias}$
$V_{CTRL-High}$	Voltage on CTRL pin for a high		0.2		5	V
$V_{CTRL-Low}$	Voltage on CTRL pin for a low		0		0.05	mV
$t_{TS/CTRL-Meas}$	Time period of TS/CTRL measurements (when $V_{TS-Bias}$ is being driven internally)	Synchronous to the communication period		24		ms
$t_{TS-Deglitch}$	Deglitch time for all TS comparators			10		ms
R_{TS}	Pullup resistor for the NTC network. Pulled up to $V_{TB-Bias}$		18	20	22	kΩ
THERMAL PROTECTION						
T_{J-SD}	Thermal shutdown temperature			155		°C
T_{J-Hys}	Thermal shutdown hysteresis			20		°C
OUTPUT LOGIC LEVELS ON $\overline{CHG}$						
V_{OL}	Open-drain $\overline{CHG}$ pin	I_{SINK} = 5 mA			500	mV
I_{OFF}	$\overline{CHG}$ leakage current when disabled	$V_{\overline{CHG}}$ = 20 V			1	µA
COMM PIN						
$R_{DS(ON)}$	COMM1 and COMM2	V_{RECT} = 2.6 V		1.5		Ω

Electrical Characteristics (continued)

over operating free-air temperature range, –40°C to 125°C (unless otherwise noted)

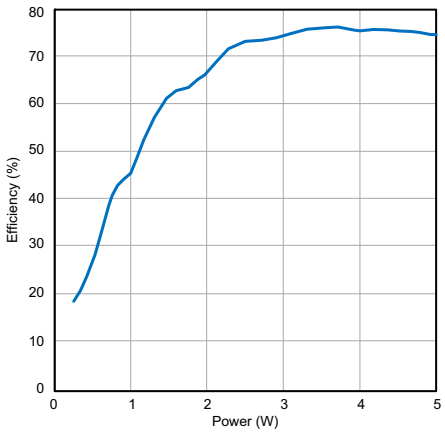
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{COMM}	Signaling frequency on COMM pin			2		kbps
I_{OFF}	COMMx pin leakage current	V_{COMM1} = 20 V, V_{COMM2} = 20 V			1	µA
CLAMP PIN						
$R_{DS(ON)}$	CLAMP1 and CLAMP2			0.8		Ω
ADAPTER ENABLE						
$V_{AD-Pres}$	V_{AD} Rising threshold voltage	V_{AD} 0 V → 5 V	3.5	3.6	3.8	V
$V_{AD-PresH}$	V_{AD} hysteresis	V_{AD} 5 V → 0 V		400		mV
I_{AD}	Input leakage current	V_{RECT} = 0 V, V_{AD} = 5 V			60	µA
R_{AD}	Pullup resistance from $\overline{\text{AD-EN}}$ to OUT when adapter mode is disabled and $V_{OUT} > V_{AD}$, EN-OUT	V_{AD} = 0 V, V_{OUT} = 5 V		200	350	Ω
$V_{AD-Diff}$	Voltage difference between V_{AD} and V $\overline{\text{AD-EN}}$ when adapter mode is enabled	V_{AD} = 5 V, 0°C ≤ T_J ≤ 85°C	3	4.5	5	V
SYNCHRONOUS RECTIFIER						
I_{OUT-SR}	I_{OUT} at which the synchronous rectifier enters half-synchronous mode, SYNC_EN	I_{LOAD} 200 mA → 0 mA	80	100	135	mA
$I_{OUT-SRH}$	Hysteresis for $I_{OUT,SR}$ (full-synchronous mode enabled)	I_{LOAD} 0 mA → 200 mA		30		mA
$V_{HS-DIODE}$	High-side diode drop when the rectifier is in half-synchronous mode	$I_{AC-VRECT}$ = 250 mA and T_J = 25°C		0.7		V
EN1 AND EN2						
V_{IL}	Input low threshold for EN1 and EN2				0.4	V
V_{IH}	Input high threshold for EN1 and EN2		1.3			V
R_{PD}	EN1 and EN2 pulldown resistance			200		kΩ
ADC (WPC RELATED MEASUREMENTS AND COEFFICIENTS)						
IOUT SENSE	Accuracy of the current sense over the load range	IOUT = 750 mA - 1000 mA	–1.5%	0%	0.9%	

6.6 Typical Characteristics



Input: RX AC power Output: RX RECT power
Efficiency: Output Power / Input Power

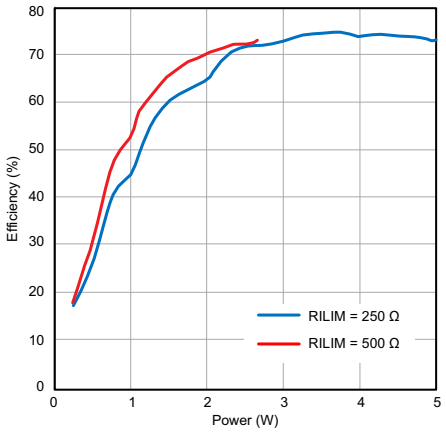
Figure 1. Rectifier Efficiency



Input: TX DC power Output: RX RECT power
Efficiency: Output Power / Input Power

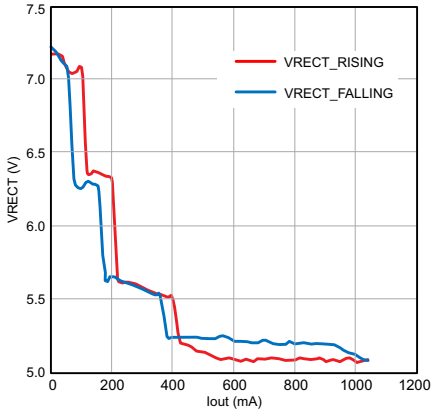
Figure 2. System Efficiency From DC Input to DC Output

Typical Characteristics (continued)



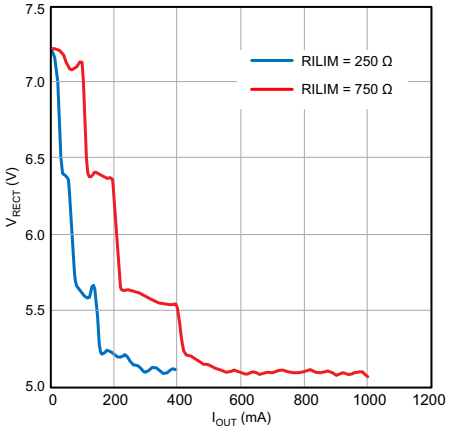
Input: TX DC power Output: RX RECT power
Plot: Output Power / Input Power

Figure 3. Light Load System Efficiency Improvement Due to Dynamic Efficiency Scaling Feature (1)



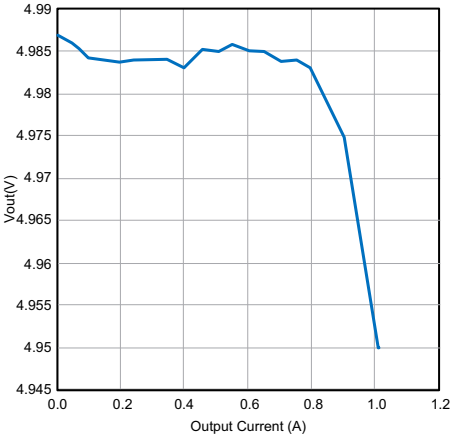
R_{ILIM} = 250 Ω

Figure 4. Impact of Load Current (I_{LOAD}) on Rectifier Voltage (V_{RECT})



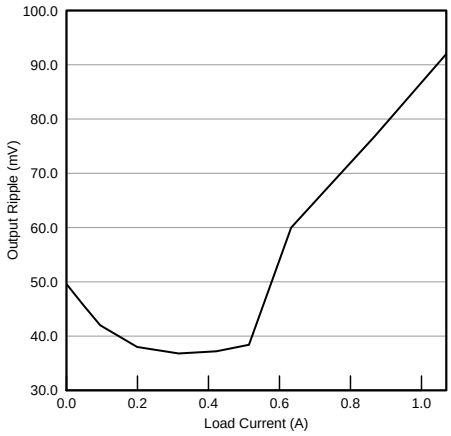
R_{ILIM} = 250 Ω and 750 Ω

Figure 5. Impact of Maximum Current setting (R_{ILIM}) on Rectifier Voltage (V_{RECT})



Maximum Current = 1 A

Figure 6. Impact of Load Current on Output Voltage



C_{OUT} = 1 µf Without Communication

Figure 7. Impact of Load Current on Output Ripple

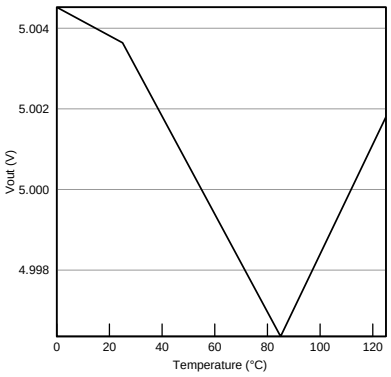


Figure 8. V_{OUT} vs Temperature

Typical Characteristics (continued)

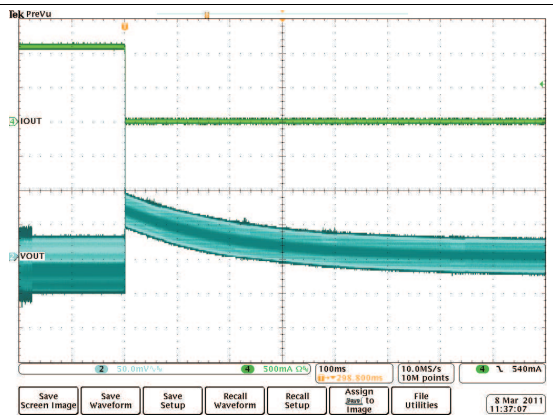


Figure 9. 1-A Instantaneous Load Dump (2)

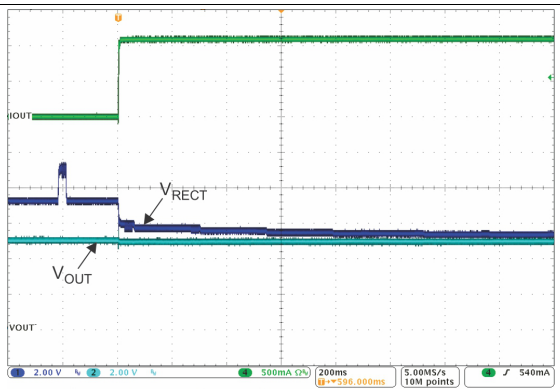


Figure 10. 1-A Load Step Full System Response

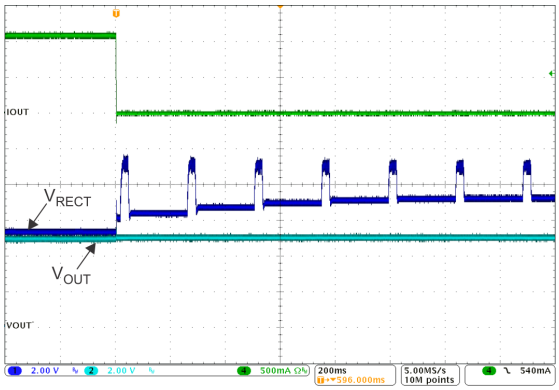


Figure 11. 1-A Load Dump Full System Response

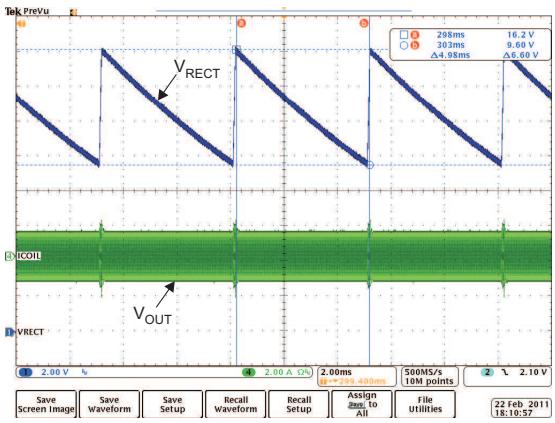


Figure 12. Rectifier Overvoltage Clamp (f_{op} = 110 kHz)

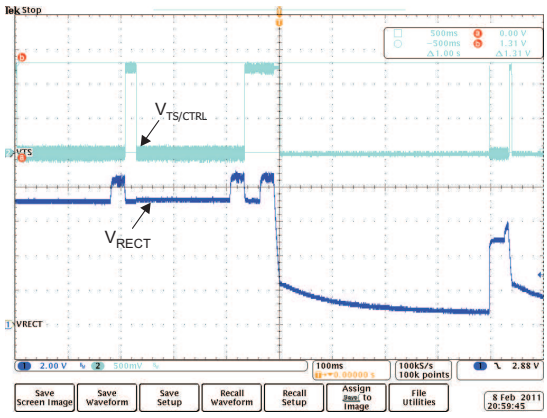


Figure 13. TS Fault

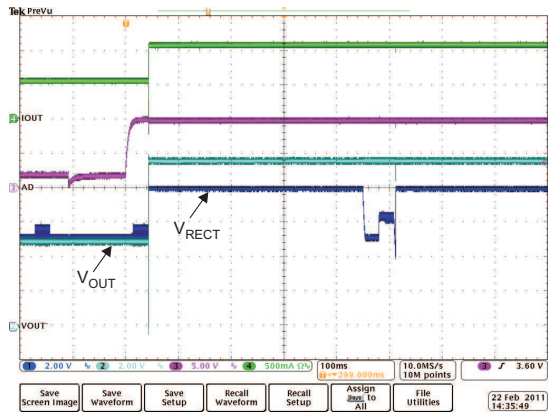


Figure 14. Adapter Insertion (V_{AD} = 10 V)

Typical Characteristics (continued)

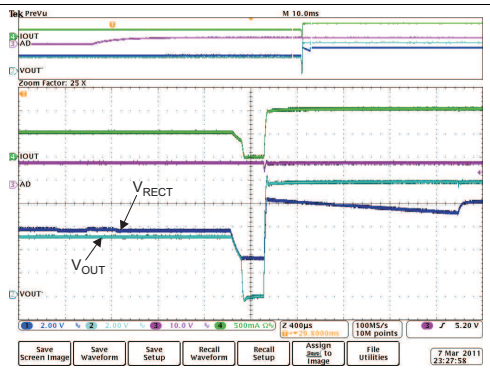


Figure 15. Adapter Insertion (V_{AD} = 10 V) Illustrating Break-Before-Make Operation

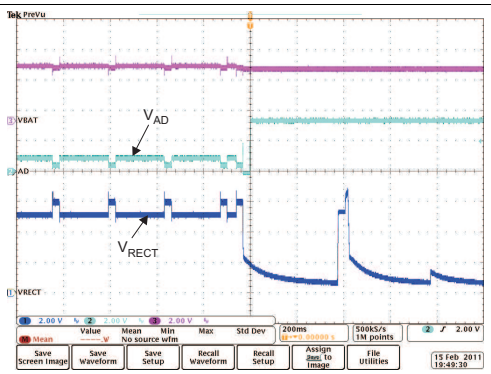


Figure 16. On-the-Go Enabled (V_{OTG} = 3.5 V) (3)

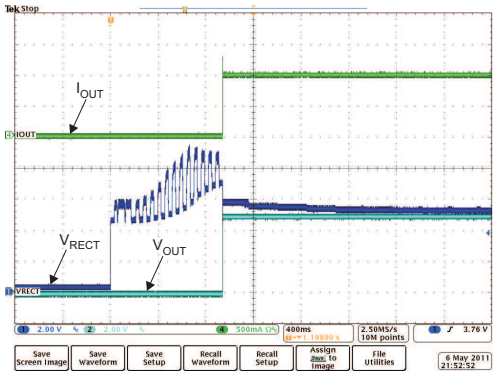


Figure 17. bq51013B Typical Start-Up With a 1-A System Load

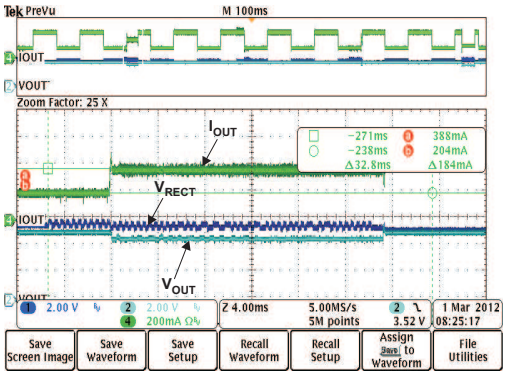


Figure 18. Adaptive Communication Limit Event Where the 400 mA Current Limit is Enabled (I_{OUT-DC} < 300 mA)

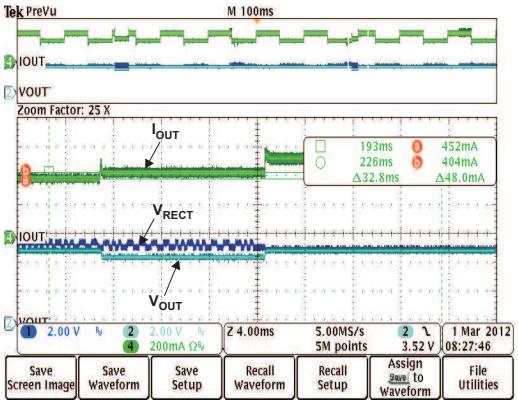


Figure 19. Adaptive Communication Limit Event Where the Current Limit is I_{OUT} + 50 mA (I_{OUT-DC} > 300 mA)

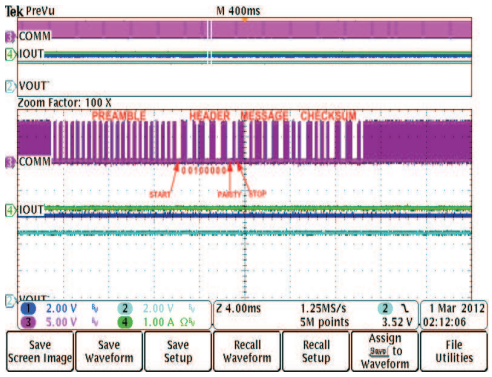


Figure 20. RX Communication Packet Structure

(1) Efficiency measured from DC input to the transmitter to DC output of the receiver. The bq500210EVM-689 TX was used for these measurements. Measurement subject to change if an alternate TX is used.

(2) Total droop experienced at the output is dependent on receiver coil design. The output impedance must be low enough at that particular operating frequency in order to not collapse the rectifier below 5 V.

(3) On-the-go mode is enabled by driving EN1 high. In this test, the external PMOS is connected between the output of the bq51013B device and the AD pin; therefore, any voltage source on the output is supplied to the AD pin.

7 Detailed Description

7.1 Overview

A wireless system consists of a charging pad (transmitter, TX or primary) and the secondary-side equipment (receiver, RX or secondary). There is a coil in the charging pad and in the secondary equipment which are magnetically coupled to each other when the secondary is placed on the primary. Power is then transferred from the transmitter to the receiver through coupled inductors (effectively an air-core transformer). Controlling the amount of power transferred is achieved by sending feedback (error signal) communication to the primary (to increase or decrease power).

The receiver communicates with the transmitter by changing the load seen by the transmitter. This load variation results in a change in the transmitter coil current, which is measured and interpreted by a processor in the charging pad. The communication is digital; packets are transferred from the receiver to the transmitter. Differential bi-phase encoding is used for the packets. The bit rate is 2-kbps.

Various types of communication packets have been defined. These include identification and authentication packets, error packets, control packets, end power packets, and power usage packets.

The transmitter coil stays powered off most of the time. It occasionally wakes up to see if a receiver is present. When a receiver authenticates itself to the transmitter, the transmitter will remain powered on. The receiver maintains full control over the power transfer using communication packets.

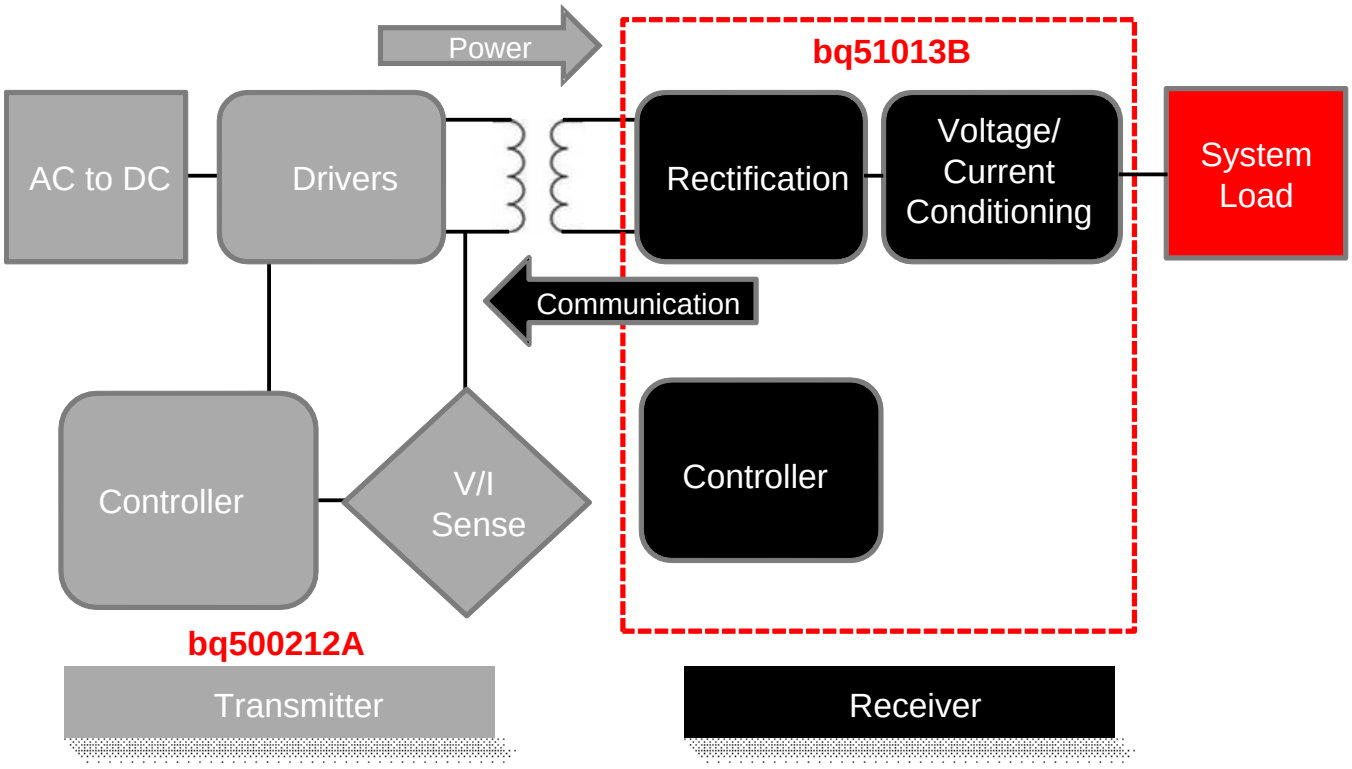
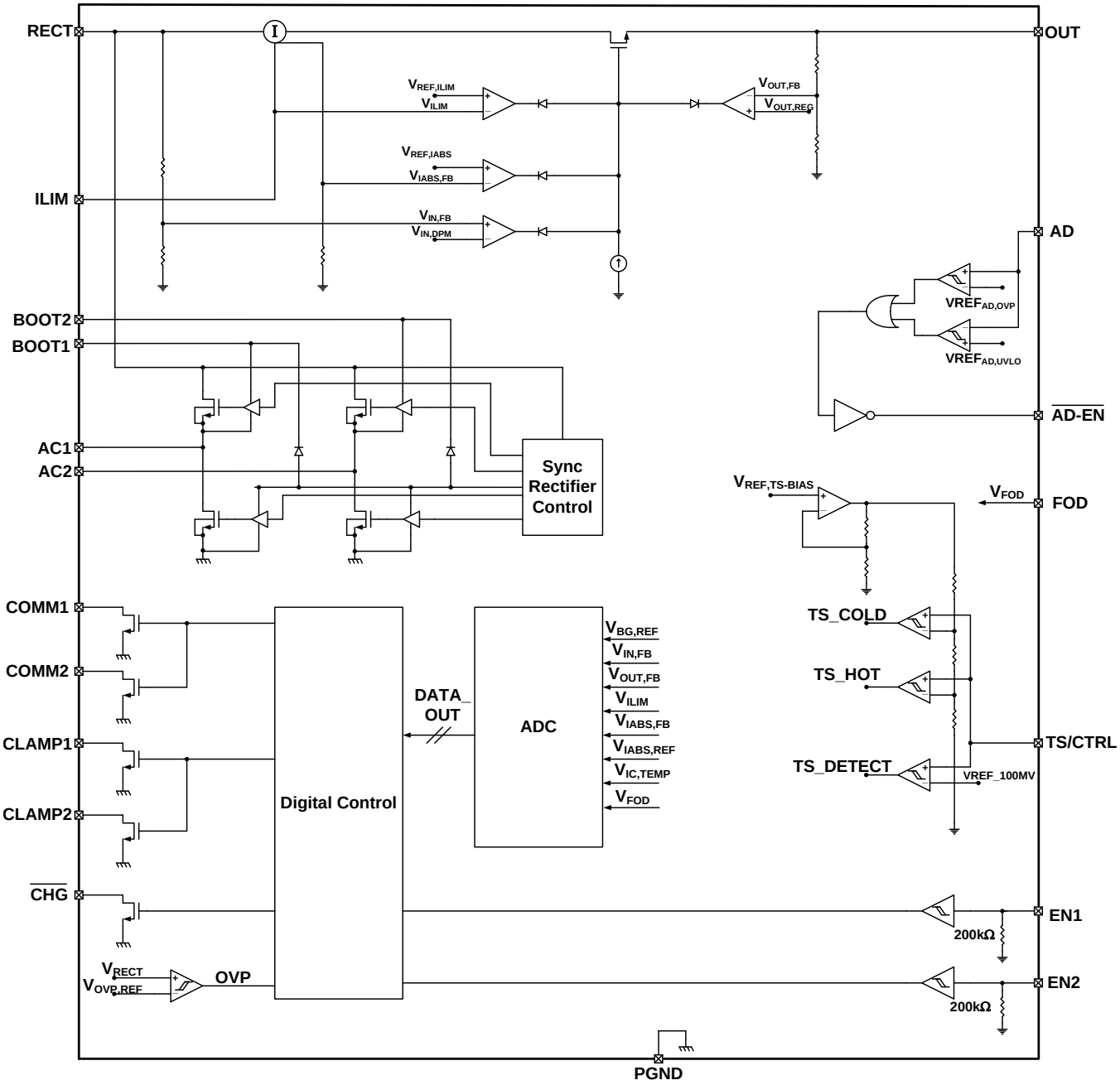


Figure 21. WPC Wireless Power System Indicating the Functional Integration of the bq51013B

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Details of a Qi Wireless Power System and bq51013 Power Transfer Flow Diagrams

The bq51013B integrates a fully compliant WPC v1.2 communication algorithm in order to streamline receiver designs (no extra software development required). Other unique algorithms such as Dynamic Rectifier Control are also integrated to provide best-in-class system performance. This section provides a high level overview of these features by illustrating the wireless power transfer flow diagram from start-up to active operation.

Feature Description (continued)

During start-up operation, the wireless power receiver must comply with proper handshaking to be granted a power contract from the TX. The TX will initiate the handshake by providing an extended digital ping. If an RX is present on the TX surface, the RX will then provide the signal strength, configuration and identification packets to the TX (see volume 1 of the WPC specification for details on each packet). These are the first three packets sent to the TX. The only exception is if there is a true shutdown condition on the EN1/EN2, AD, or TS/CTRL pins where the RX will shut down the TX immediately. See Table 4 for details. Once the TX has successfully received the signal strength, configuration and identification packets, the RX will be granted a power contract and is then allowed to control the operating point of the power transfer. With the use of the bq51013B Dynamic Rectifier Control algorithm, the RX will inform the TX to adjust the rectifier voltage above 7 V prior to enabling the output supply. This method enhances the transient performance during system start-up. See Figure 22 for the start-up flow diagram details.

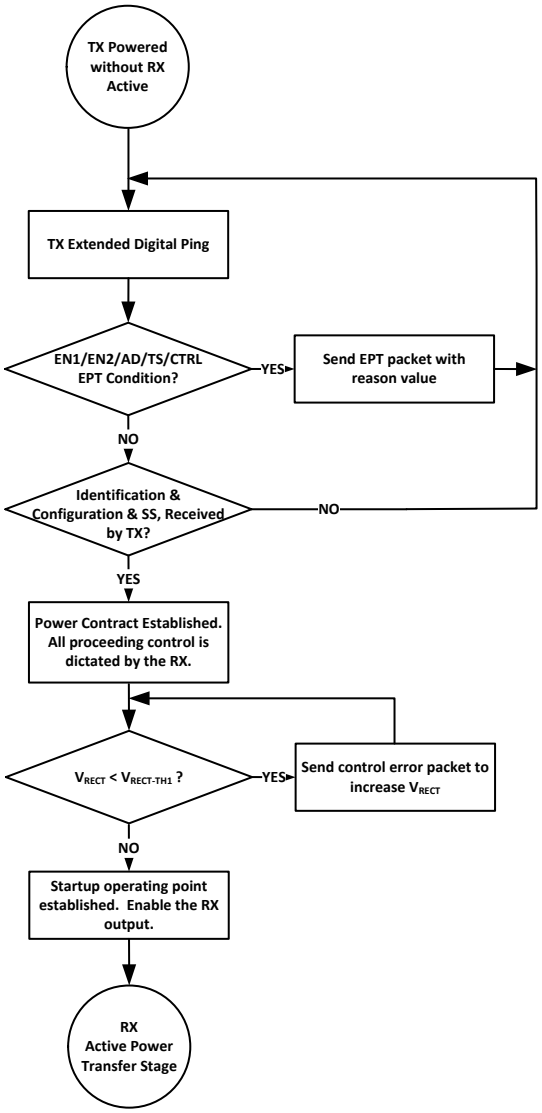


Figure 22. Wireless Power Start-Up Flow Diagram

Once the start-up procedure has been established, the RX will enter the active power transfer stage. This is considered the “main loop” of operation. The Dynamic Rectifier Control algorithm will determine the rectifier voltage target based on a percentage of the maximum output current level setting (set by K_{IMAX} and the ILIM resistance to GND). The RX will send control error packets in order to converge on these targets. As the output current changes, the rectifier voltage target will dynamically change. The feedback loop of the WPC system is

Feature Description (continued)

relatively slow where it can take up to 90 ms to converge on a new rectifier voltage target. It should be understood that the instantaneous transient response of the system is open loop and dependent on the RX coil output impedance at that operating point. More details on this will be covered in the section Receiver Coil Load-Line Analysis. The “main loop” will also determine if any conditions in Table 4 are true in order to discontinue power transfer. See Figure 23 which illustrates the active power transfer loop.

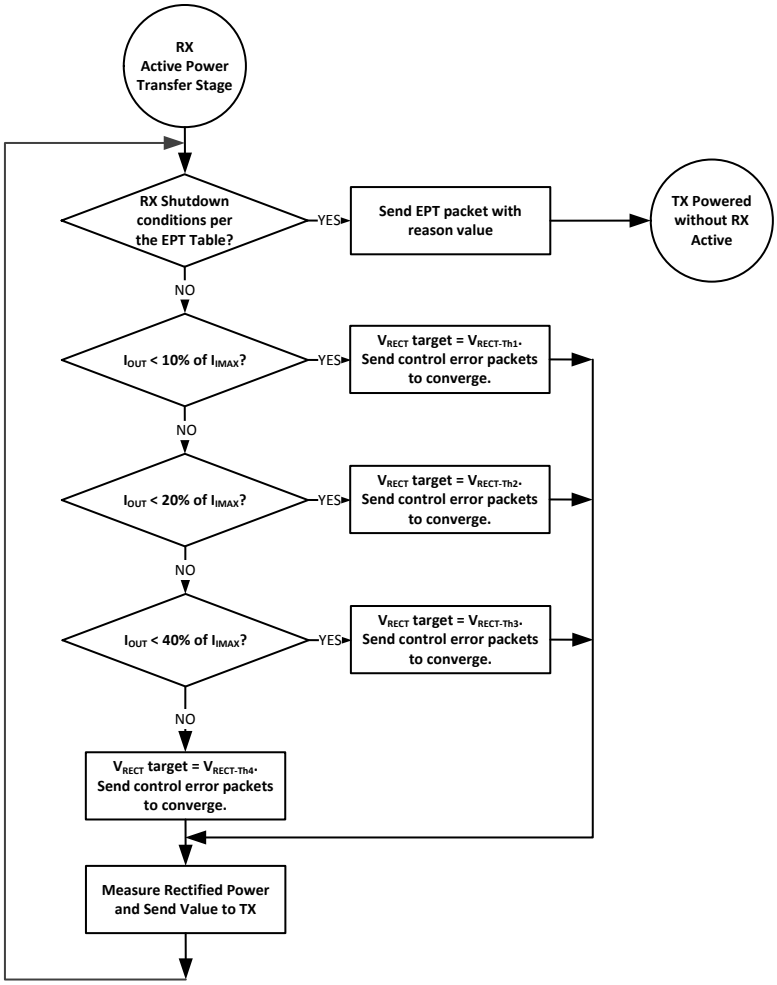


Figure 23. Active Power Transfer Flow Diagram

Another requirement of the WPC v1.2 specification is to send the measured received power. This task is enabled on the device by measuring the voltage on the FOD pin which is proportional to the output current and can be scaled based on the choice of the resitor to ground on the FOD pin.

7.3.2 Dynamic Rectifier Control

The Dynamic Rectifier Control algorithm offers the end system designer optimal transient response for a given maximum output current setting. This is achieved by providing enough voltage headroom across the internal regulator at light loads in order to maintain regulation during a load transient. The WPC system has a relatively slow global feedback loop where it can take more than 90 ms to converge on a new rectifier voltage target. Therefore, the transient response is dependent on the loosely coupled transformers output impedance profile. The Dynamic Rectifier Control allows for a 2 V change in rectified voltage before the transient response will be observed at the output of the internal regulator (output of the bq51013B). A 1-A application allows up to a 1.5-Ω output impedance. The Dynamic Rectifier Control behavior is illustrated in Figure 4 where R_{ILIM} is set to 220 Ω.

Feature Description (continued)

7.3.3 Dynamic Efficiency Scaling

The Dynamic Efficiency Scaling feature allows for the loss characteristics of the bq51013B to be scaled based on the maximum expected output power in the end application. This effectively optimizes the efficiency for each application. This feature is achieved by scaling the loss of the internal LDO based on a percentage of the maximum output current. Note that the maximum output current is set by the K_{IMAX} term and the R_{ILIM} resistance (where $R_{ILIM} = K_{IMAX} / I_{MAX}$). The flow diagram shown in Figure 23 illustrates how the rectifier is dynamically controlled (*Dynamic Rectifier Control*) based on a fixed percentage of the I_{MAX} setting. Table 1 summarizes how the rectifier behavior is dynamically adjusted based on two different R_{ILIM} settings.

Table 1. Dynamic Efficiency Scaling

OUTPUT CURRENT PERCENTAGE	R_{ILIM} = 500 Ω I_{MAX} = 0.5 A	R_{ILIM} = 220 Ω I_{MAX} = 1.14 A	V_{RECT}
0 to 10%	0 A to 0.05 A	0 A to 0.114 A	7.08 V
10 to 20%	0.05 A to 0.1 A	0.114 A to 0.227 A	6.28 V
20 to 40%	0.1 A to 0.2 A	0.227 A to 0.454 A	5.53 V
>40%	> 0.2 A	> 0.454 A	5.11 V

Figure 5 illustrates the shift in the *Dynamic Rectifier Control* behavior based on the two different R_{ILIM} settings. With the rectifier voltage (V_{RECT}) being the input to the internal LDO, this adjustment in the *Dynamic Rectifier Control* thresholds will dynamically adjust the power dissipation across the LDO where:

$$P_{DIS} = \left(V_{RECT} - V_{OUT}\right) \times I_{OUT} \quad (1)$$

Figure 3 illustrates how the system efficiency is improved due to the *Dynamic Efficiency Scaling* feature. Note that this feature balances efficiency with optimal system transient response.

7.3.4 R_{ILIM} Calculations

The bq51013B includes a means of providing hardware overcurrent protection by means of an analog current regulation loop. The hardware current limit provides an extra level of safety by clamping the maximum allowable output current (current compliance). The R_{ILIM} resistor size also sets the thresholds for the dynamic rectifier levels and thus providing efficiency tuning per each application's maximum system current. The calculation for the total R_{ILIM} resistance is as follows:

$$R_{ILIM} = \frac{K_{IMAX}}{I_{MAX}}$$

$$I_{ILIM} = 1.2 \times I_{MAX} = \frac{K_{ILIM}}{R_{ILIM}}$$

$$R_{ILIM} = R_1 + R_{FOD} \quad (2)$$

where

- I_{MAX} is the expected maximum output current during normal operation.
- I_{ILIM} is the hardware over current limit.

When referring to the application diagram shown in Figure 38, R_{ILIM} is the sum of R_{FOD} and R_1 (the total resistance from the ILIM pin to GND).

7.3.5 Input Overvoltage

If the input voltage suddenly increases in potential (for example, due to a change in position of the equipment on the charging pad), the voltage-control loop inside the bq51013B becomes active, and prevents the output from going beyond $V_{OUT-REG}$. The receiver then starts sending back error packets to the transmitter every 30 ms until the input voltage comes back to the $V_{RECT-REG}$ target, and then maintains the error communication every 250 ms.

If the input voltage increases in potential beyond $V_{RECT-OVP}$, the device switches off the LDO and communicates to the primary to bring the voltage back to $V_{RECT-REG}$. In addition, a proprietary voltage protection circuit is activated by means of C_{CLAMP1} and C_{CLAMP2} that protects the device from voltages beyond the maximum rating of the device.

7.3.6 Adapter Enable Functionality and EN1/EN2 Control

Figure 43 is an example application that shows the bq51013B used as a wireless power receiver that can power mutliplex between wired or wireless power for the down-system electronics. In the default operating mode, pins EN1 and EN2 are low, which activates the adapter enable functionality. In this mode, if an adapter is not present the AD pin will be low, and $\overline{\text{AD-EN}}$ pin will be pulled to the higher of the OUT and AD pins so that the PMOS between OUT and AD will be turned off. If an adapter is plugged in and the voltage at the AD pin goes above $V_{\overline{\text{AD-EN}}}$, then wireless charging is disabled and the $\overline{\text{AD-EN}}$ pin will be pulled approximately V_{AD} below the AD pin to connect AD to the secondary charger. The difference between AD and $\overline{\text{AD-EN}}$ is regulated to a maximum of $V_{AD-Diff}$ to ensure the V_{GS} of the external PMOS is protected.

The EN1 and EN2 pins include internal pulldown resistors (R_{PD}), so that if these pins are not connected bq51013B defaults to $\overline{\text{AD-EN}}$ control mode. However, these pins can be pulled high to enable other operating modes as described in Table 2:

Table 2. Adapter Enable Functionality

EN1	EN2	RESULT
0	0	Adapter control enabled. If adapter is present then secondary charger is powered by adapter, otherwise wireless charging is enabled when wireless power is available. Communication current limit is enabled.
0	1	Disables communication current limit.
1	0	$\overline{\text{AD-EN}}$ is pulled low, whether or not adapter voltage is present. This feature can be used for USB OTG applications.
1	1	Adapter and wireless charging are disabled, power will not be delivered by the OUT pin in this mode.

Table 3. EN1/EN2 Control

EN1	EN2	WIRELESS POWER	WIRED POWER	OTG MODE	ADAPTIVE COMMUNICATION LIMIT	EPT
0	0	Enabled	Priority(1)	Disabled	Enabled	Not Sent to TX
0	1	Priority(1)	Enabled	Disabled	Disabled	Not Sent to TX
1	0	Disabled	Enabled	Enabled(2)	N/A	No Response
1	1	Disabled	Disabled	Disabled	N/A	Termination

(1) If both wired and wireless power are present, wired or wireless is given priority based on EN2.
(2) Allows for a boost-back supply to be driven from the output terminal of the RX to the adapter port through the external back-to-back PMOS FET.

As described in Table 3, when EN1 is low, both wired and wireless power are useable. If both are present, priority is set between wired and wireless by EN2. When EN1 is high, wireless power is disabled and wired power functionality is set by EN2. When EN1 is high but EN2 is low, wired power is enabled if present. Additionally, USB OTG mode is active. In USB OTG mode, a charger connected to the OUT pin can power the AD pin. Note that EN1 must be pulled high from an active source (microcontroller). Finally, pulling both EN1 and EN2 high disables both wired and wireless charging.

NOTE

It is required to connect a back-to-back PMOS between AD and OUT so that voltage is blocked in both directions. Also, when AD mode is enabled no load can be pulled from the RECT pin as this could cause an internal device overvoltage in bq51013B.

7.3.7 End Power Transfer Packet (WPC Header 0x02)

The WPC allows for a special command for the receiver to terminate power transfer from the transmitter termed End Power Transfer (EPT) packet. Table 4 specifies the v1.2 reasons column and their corresponding data field value. The condition column corresponds to the methodology used by bq51013B to send equivalent message.

Table 4. End Power Transfer Packet

MESSAGE	VALUE	CONDITION
Unknown	0x00	AD > $V_{AD-Pres}$, or <EN1 EN2> = <10>, or TS/CTRL > $V_{CTRL-High}$, or TS > V_{COLD}
Charge Complete	0x01	<EN1 EN2> = <11>
Internal Fault	0x02	T_J > 150°C or R_{ILIM} < 100 Ω
Overtemperature	0x03	TS < V_{HOT}, or TS/CTRL < $V_{CTRL-Low}$
Overvoltage	0x04	V_{RECT} target does not converge
Overcurrent	0x05	Not sent
Battery Failure	0x06	Not sent
Reconfigure	0x07	Not sent
No Response	0x08	Not sent

7.3.8 Status Outputs

The bq51013B has one status output, $\overline{CHG}$. This output is an open-drain NMOS device that is rated to 20 V. The open-drain FET connected to the $\overline{CHG}$ pin will be turned on whenever the output of the power supply is enabled. The output of the power supply will not be enabled if the $V_{RECT-REG}$ does not converge at the no-load target voltage.

7.3.9 WPC Communication Scheme

The WPC communication uses a modulation technique termed “back-scatter modulation” where the receiver coil is dynamically loaded in order to provide amplitude modulation of the transmitter's coil voltage and current. This scheme is possible due to the fundamental behavior between two loosely coupled inductors (here between the TX and RX coils). This type of modulation can be accomplished by switching in and out a resistor at the output of the rectifier, or by switching in and out a capacitor across the AC1/AC2 net. Figure 24 shows how to implement resistive modulation.

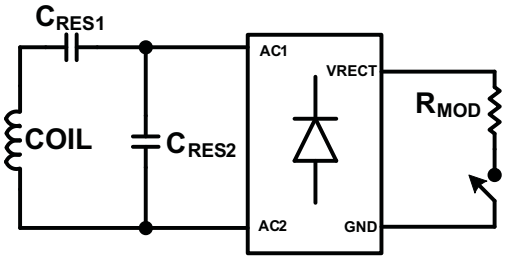


Figure 24. Resistive Modulation

Figure 25 shows how to implement capacitive modulation.

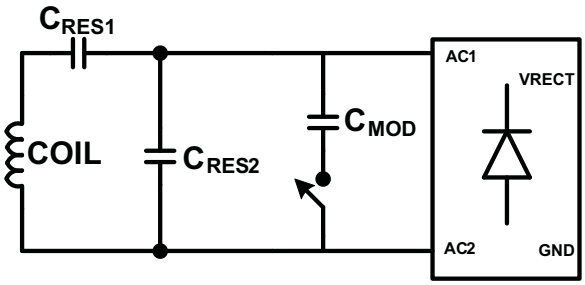


Figure 25. Capacitive Modulation

The amplitude change in the TX coil voltage or current can be detected by the transmitter's decoder. The resulting signal observed by the TX is shown in Figure 26.

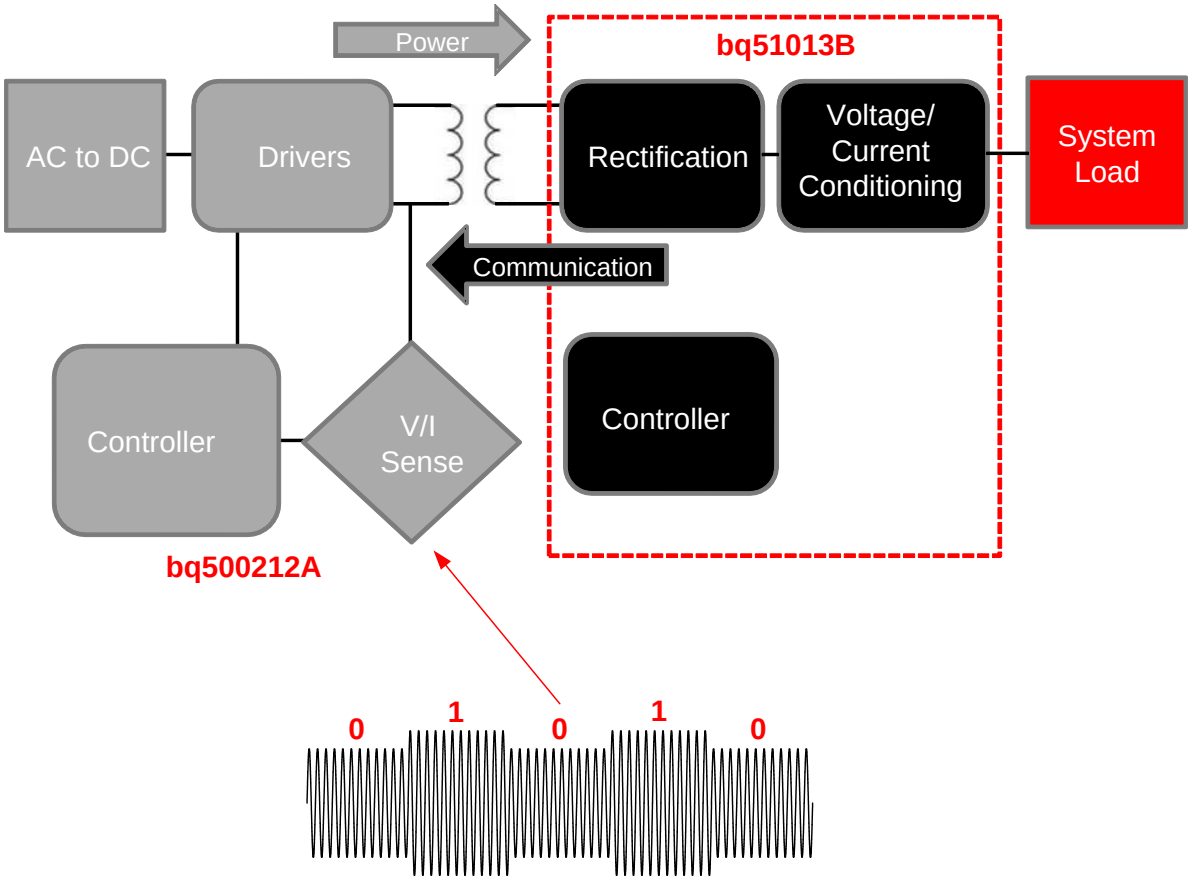


Figure 26. TX Coil Voltage/Current

The WPC protocol uses a differential bi-phase encoding scheme to modulate the data bits onto the TX coil voltage/current. Each data bit is aligned at a full period of 0.5 ms (t_{CLK}) or 2 kHz. An encoded ONE results in two transitions during the bit period and an encoded ZERO results in a single transition. See Figure 27 for an example of the differential bi-phase encoding.

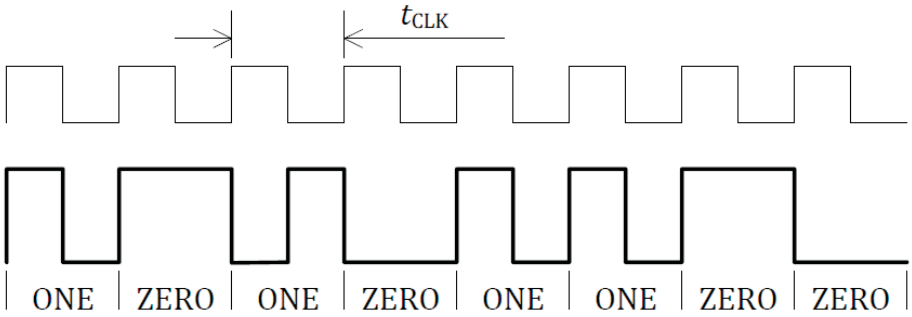


Figure 27. Differential Bi-Phase Encoding Scheme (WPC Volume 1: Low Power, Part 1 Interface Definition)

The bits are sent LSB first and use an 11-bit asynchronous serial format for each portion of the packet. This includes one start bit, n-data bytes, a parity bit, and a single stop bit. The start bit is always ZERO and the parity bit is odd. The stop bit is always ONE. Figure 28 shows the details of the asynchronous serial format.

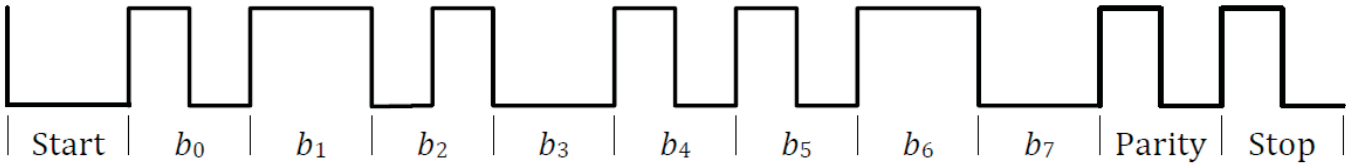


Figure 28. Asynchronous Serial Formatting (WPC Volume 1: Low Power, Part 1 Interface Definition)

Each packet format is organized as shown in Figure 29.

Figure 29. Packet Format (WPC Volume 1: Low Power, Part 1 Interface Definition)

Figure 20 shows an example waveform of the receiver sending a rectified power packet (header 0x04).

7.3.10 Communication Modulator

The bq51013B device provides two identical, integrated communication FETs which are connected to the pins COMM1 and COMM2. These FETs are used for modulating the secondary load current which allows the bq51013B to communicate error control and configuration information to the transmitter. Figure 30 shows how the COMMx pins can be used for resistive load modulation. Each COMMx pin can handle at most a 24-Ω communication resistor. Therefore, if a COMMx resistor between 12 Ω and 24 Ω is required, COMM1 and COMM2 pins must be connected in parallel. The bq51013B device does not support a COMMx resistor less than 12 Ω.

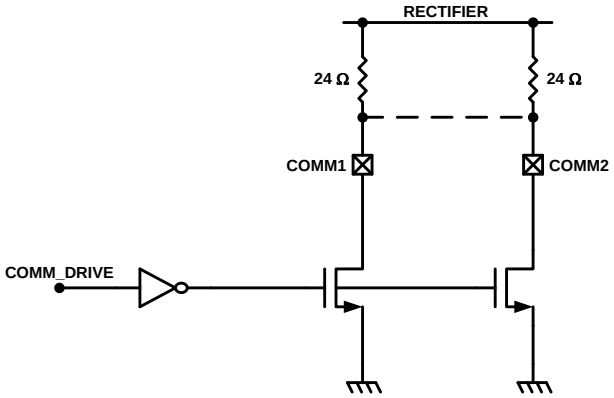


Figure 30. Resistive Load Modulation

In addition to resistive load modulation, the bq51013B is also capable of capacitive load modulation as shown in Figure 31. In this case, a capacitor is connected from COMM1 to AC1 and from COMM2 to AC2. When the COMMx switches are closed there is effectively a 22 nF capacitor connected between AC1 and AC2. Connecting a capacitor in between AC1 and AC2 modulates the impedance seen by the coil, which will be reflected in the primary as a change in current.

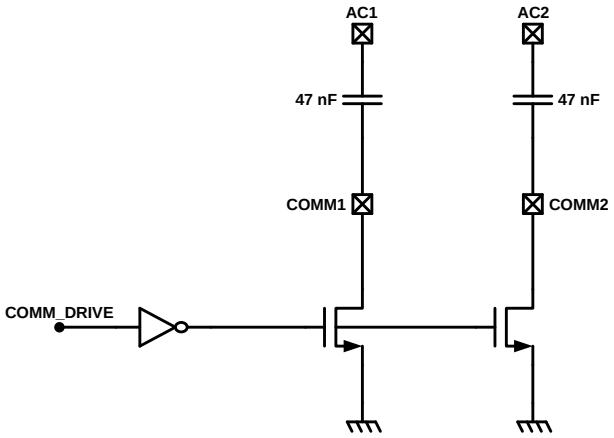


Figure 31. Capacitive Load Modulation

7.3.11 Adaptive Communication Limit

The Qi communication channel is established through backscatter modulation as described in the previous sections. This type of modulation takes advantage of the loosely coupled inductor relationship between the RX and TX coils. Essentially, the switching in-and-out of the communication capacitor or resistor adds a transient load to the RX coil in order to modulate the TX coil voltage and current waveform (amplitude modulation). The consequence of this technique is that a load transient (load current noise) from the mobile device has the same signature. To provide noise immunity to the communication channel, the output load transients must be isolated from the RX coil. The proprietary feature *Adaptive Communication Limit* achieves this by dynamically adjusting the current limit of the regulator. When the regulator is put in current limit, any load transients will be offloaded to the battery in the system.

Note that this requires the battery charger device to have input voltage regulation (weak adapter mode). The output of the RX appears as a weak supply if a transient occurs above the current limit of the regulator.

The Adaptive Communication Limit feature has two current limit modes and is detailed in Table 5.

Table 5. Adaptive Communication Limit

I_{OUT}	COMMUNICATION CURRENT LIMIT
< 300 mA	Fixed 400 mA
> 300 mA	I_{OUT} + 50 mA

The first mode is illustrated in Figure 18. In this plot, an output load pulse of 300 mA is periodically introduced on a DC current level of 200 mA. Therefore, the 400 mA current limit is enabled. The pulses on V_{RECT} indicate that a communication packet event is occurring. When the output load pulse occurs, the regulator limits the pulse to a constant 400 mA and, therefore, preserves communication. Note that V_{OUT} drops to 4.5 V instead of GND. A charger device with an input voltage regulation set to 4.5 V allows this to occur by offloading the load transient support to the mobile device's battery.

The second mode is illustrated in Figure 19. In this plot, an output pulse of 200 mA is periodically introduced on a DC current level of 400 mA. Therefore, the tracking current mode (I_{OUT} + 50 mA) is enabled. In this mode, the bq51013B measures the active output current and sets the regulator's current limit 50 mA above this measurement. When the load pulse occurs during a communication packet event, the output current is regulated to 450 mA. As the communication packet event has finished the output load is allowed to increase. Note that during the time the regulator is in current limit V_{OUT} is reduced to 4.5 V and 5 V when not in current limit.

7.3.12 Synchronous Rectification

The bq51013B provides an integrated, self-driven synchronous rectifier that enables high-efficiency AC to DC power conversion. The rectifier consists of an all NMOS H-Bridge driver where the backgates of the diodes are configured to be the rectifier when the synchronous rectifier is disabled. During the initial start-up of the WPC system the synchronous rectifier is not enabled. At this operating point, the DC rectifier voltage is provided by the diode rectifier. Once V_{RECT} is greater than V_{UVLO}, half synchronous mode will be enabled until the load current surpasses I_{BAT-SR}. Above I_{BAT-SR} the full synchronous rectifier stays enabled until the load current drops back below the hysteresis level ($I_{BAT-SRH}$) where half-synchronous mode is enabled re-enabled.

7.3.13 Temperature Sense Resistor Network (TS)

bq51013B includes a ratiometric external temperature sense function. The temperature sense function has two ratiometric thresholds which represent a hot and cold condition. An external temperature sensor is recommended in order to provide safe operating conditions for the receiver product. This pin is best used for monitoring the surface that can be exposed to the end user (place the NTC resistor closest to where the user would physically contact the end product).

Figure 32 allows for any NTC resistor to be used with the given V_{HOT} and V_{COLD} thresholds.

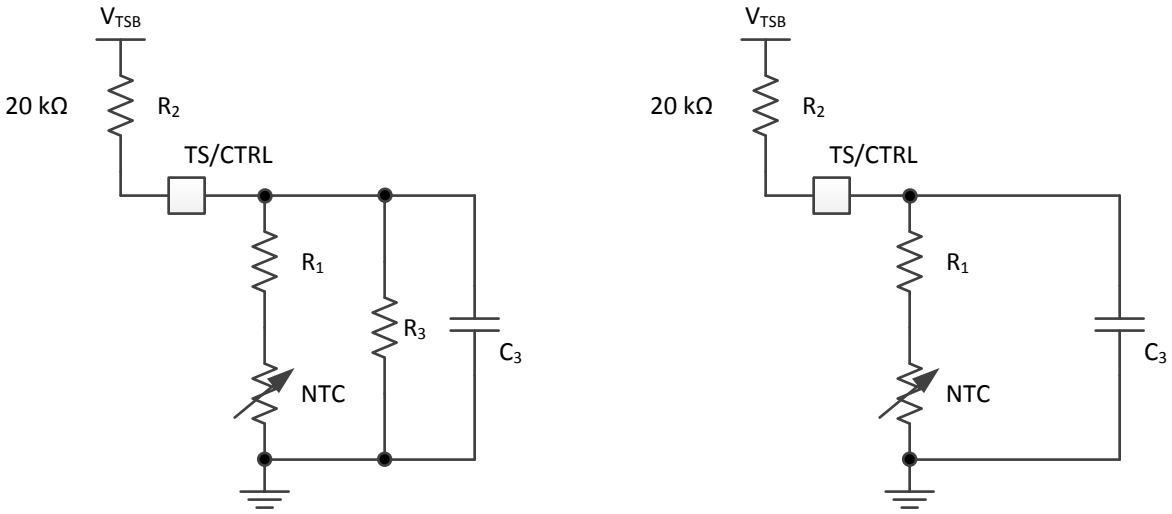


Figure 32. NTC Circuit Options For Safe Operation of the Wireless Receiver Power Supply

The resistors R_1 and R_3 can be solved by resolving the system of equations at the desired temperature thresholds. The two equations are:

$$\%V_{COLD} = \frac{\left(\frac{R_3\left(R_{NTC}|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}|_{TCOLD} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}|_{TCOLD} + R_1\right)}\right) + R2} \times 100$$

$$\%V_{HOT} = \frac{\left(\frac{R_3\left(R_{NTC}|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}|_{THOT} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}|_{THOT} + R_1\right)}\right) + R2} \times 100 \quad (3)$$

Where:

$$R_{NTC}\big|_{TCOLD} = R_O e^{\beta\left(1/T_{COLD} - 1/T_O\right)}$$

$$R_{NTC}\big|_{THOT} = R_O e^{\beta\left(1/T_{HOT} - 1/T_O\right)}$$

where

- T_{COLD} and T_{HOT} are the desired temperature thresholds in degrees Kelvin.
- R_O is the nominal resistance.
- β is the temperature coefficient of the NTC resistor. (4)

R_O is fixed at 20 kΩ. An example solution is provided:

- R1 = 4.23 kΩ
- R3 = 66.8 kΩ

where the chosen parameters are:

- $\%V_{HOT}$ = 19.6%
- $\%V_{COLD}$ = 58.7%
- T_{COLD} = –10°C
- T_{HOT} = 100°C
- β = 3380
- R_O = 10 kΩ

The plot of the percent V_{TSB} vs. temperature is shown in Figure 33:

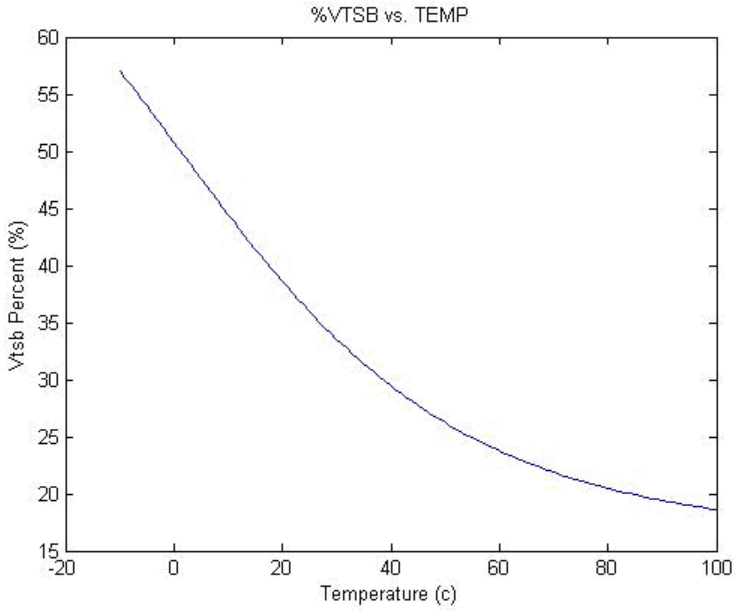


Figure 33. Example Solution for an NTC Resistor with R_O = 10 kΩ and β = 4500

Figure 34 illustrates the periodic biasing scheme used for measuring the TS state. An internal TS_READ signal enables the TS bias voltage ($V_{TS\text{-}Bias}$) for 24 ms. During this period, the TS comparators are read (with t_{TS} deglitch) and appropriate action is taken based on the temperature measurement. After this 24-ms period has elapsed, the TS_READ signal goes low, which causes the TS/CTRL pin to become high impedance. During the next 35 ms (priority packet period) or 235 ms (standard packet period), the TS voltage is monitored and compared to $V_{CTRL\text{-}HI}$. If the TS voltage is greater than $V_{CTRL\text{-}HI}$ then a secondary device is driving the TS/CTRL pin and a CTRL = '1' is detected.

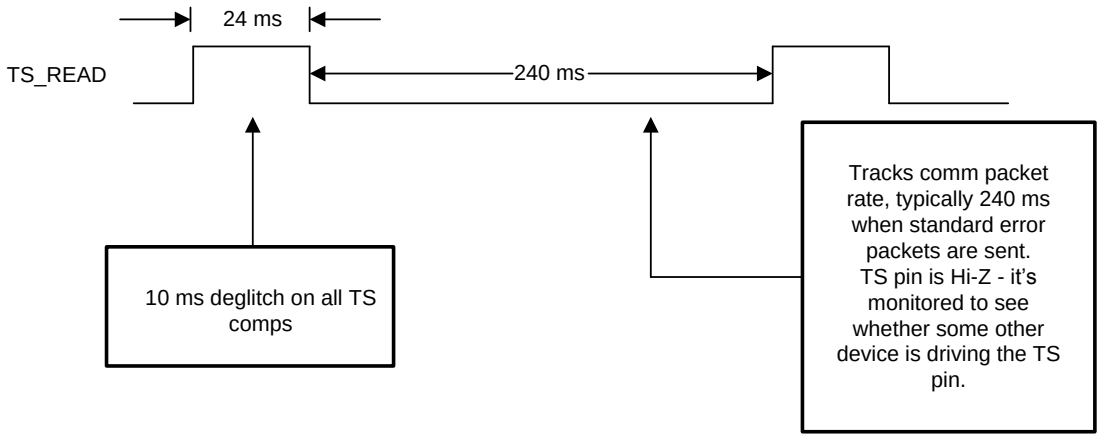


Figure 34. Timing Diagram For TS Detection Circuit

7.3.14 3-State Driver Recommendations for the TS/CTRL Pin

The TS/CTRL pin offers three functions with one 3-state driver interface:

- NTC temperature monitoring
- Fault indication
- Charge done indication

A 3-state driver can be implemented with the circuit in Figure 35 and the use of two GPIO connections. M3 and M4 and both resistors are external components.

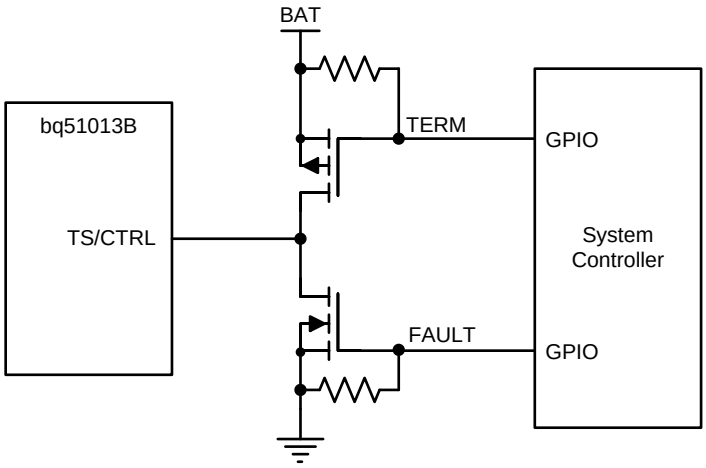


Figure 35. 3-State Driver For TS/CTRL

Note that the signals *TERM and FAULT* are given by two GPIOs. The truth table for this circuit is found in Table 6:

Table 6. Truth Table

TERM	FAULT	F (Result)
1	0	High Impedance (Normal Mode)
0	0	Charge Complete
1	1	System Fault
0	1	Turns on both the TERM FET and the FAULT FET, must not be used

The default setting is TERM = 1 and FAULT = 0. In this condition, the TS/CTRL net is high impedance (Hi-Z) and; therefore, the NTC is function is allowed to operate. When the TS/CTRL pin is pulled to GND (below $V_{CTRL-Low}$) by setting FAULT = 1 (TERM = 1), the RX is shut down with the indication of a fault. When the TS/CTRL pin is pulled to the battery (above $V_{CTRL-High}$) by setting TERM = 0 (FAULT = 0), the RX is shut down with the indication of a charge complete condition. Therefore, the host controller can indicate whether the RX is system is turning off due to a fault or due to a charge complete condition. Note that the condition where both the TERM FET and the FAULT FET are on (TERM = 0 and FAULT = 1) would short BAT to ground and must not happen.

If a 3-state GPIO is available, that GPIO could be tied directly to TS/CTRL. Normal operation would be high impedance.

7.3.15 Thermal Protection

The bq51013B includes a thermal shutdown protection. If the die temperature reaches T_{J-SD}, the LDO is shut off to prevent any further power dissipation. In this case bq51013B will send an EPT message of internal fault (0x02). Once the temperature falls T_{J-Hys} below T_{J-SD}, operation can continue.

7.3.16 WPC v1.2 Compliance – Foreign Object Detection

The bq51013B is a WPC v1.2 compatible device. In order to enable a Power Transmitter to monitor the power loss across the interface as one of the possible methods to limit the temperature rise of Foreign Objects, the bq51013B reports its Received Power to the Power Transmitter. The Received Power equals the power that is available from the output of the Power Receiver plus any power that is lost in producing that output power (the power loss in the Secondary Coil and series resonant capacitor, the power loss in the Shielding of the Power Receiver, the power loss in the rectifier). In the WPC1.2 specification, foreign object detection (FOD) is enforced. This means the bq51013B will send received power information with known accuracy to the transmitter.

WPC v1.2 defines Received Power as “the average amount of power that the Power Receiver receives through its Interface Surface, in the time window indicated in the Configuration Packet”.

To receive certification as a WPC v1.2 receiver, the Device Under Test (DUT) is tested on a Reference Transmitter whose transmitted power is calibrated, the receiver must send a received power such that:

$$0 > (TX\ PWR)_{REF} - (RX\ PWR\ out)_{DUT} > -375\ mW \quad (5)$$

This 375-mW bias ensures that system will remain interoperable.

WPC v1.2 Transmitter is tested to see if it can detect reference Foreign Objects with a Reference receiver.

WPC v1.2 Specification will allow much more accurate sensing of Foreign Objects.

7.3.17 Receiver Coil Load-Line Analysis

When choosing a receiver coil, TI recommends analyzing the transformer characteristics between the primary coil and receiver coil through load-line analysis. This will capture two important conditions in the WPC system:

- Operating point characteristics in the closed loop of the WPC system.
- Instantaneous transient response prior to the convergence of the new operating point.

An example test configuration for conducting this analysis is shown in Figure 36:

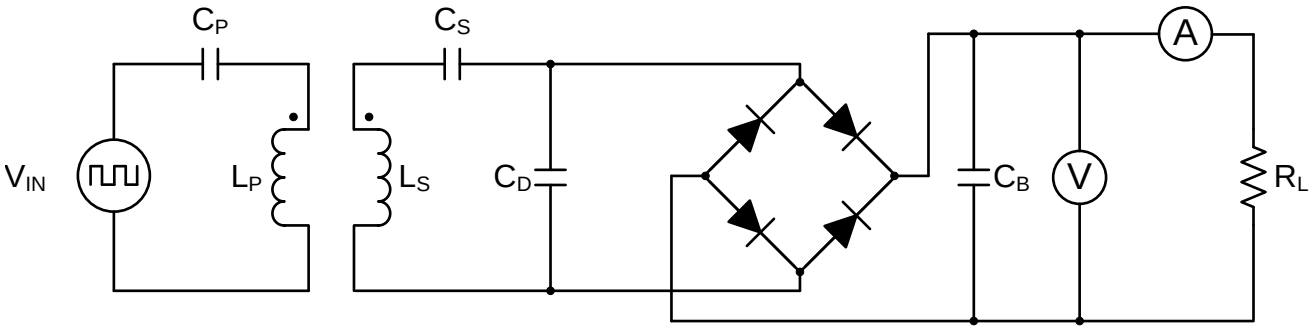


Figure 36. Load-Line Analysis Test Bench

Where:

- V_{IN} is a square-wave power source that should have a peak-to-peak operation of 19 V.
- C_P is the primary series resonant capacitor (for example, 100 nF for Type A1 coil).
- L_P is the primary coil of interest (such as, Type A1).
- L_S is the secondary coil of interest.
- C_S is the series resonant capacitor chosen for the receiver coil under test.
- C_D is the parallel resonant capacitor chosen for the receiver coil under test.
- C_B is the bulk capacitor of the diode bridge (voltage rating should be at least 25 V and capacitance value of at least 10 µF)
- V is a Kelvin connected voltage meter
- A is a series ammeter
- R_L is the load of interest

TI recommends that the diode bridge be constructed of Schottky diodes.

The test procedure is as follows

- Supply a 19-V AC signal to L_P starting at a frequency of 210 kHz
- Measure the resulting rectified voltage from no load to the expected full load
- Repeat the above steps for lower frequencies (stopping at 110 kHz)

An example load-line analysis is shown in Figure 37:

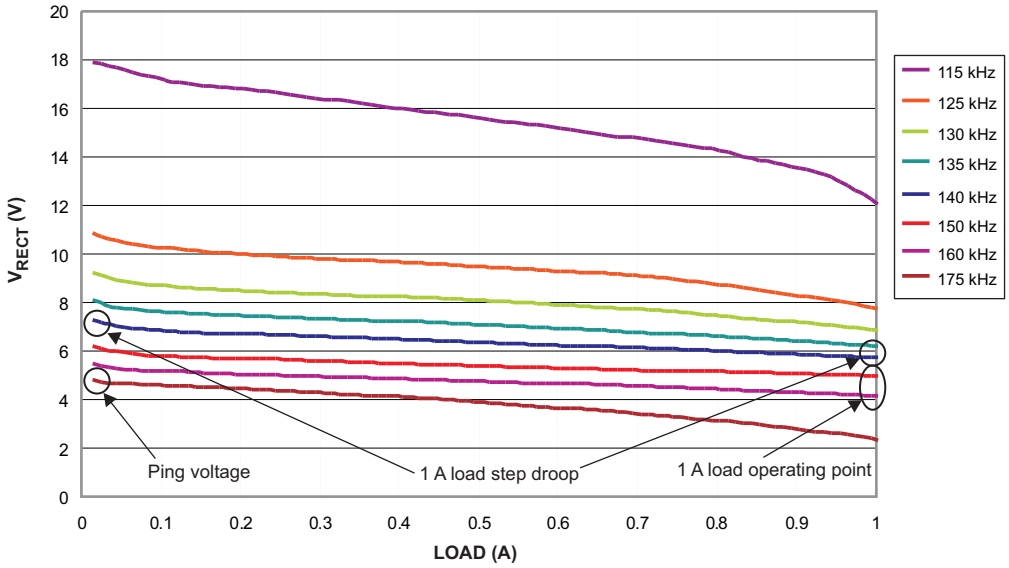


Figure 37. Example Load-Line Results

What Figure 37 conveys about the operating point is that a specific load and rectifier target condition consequently results in a specific operating frequency (for the type A1 TX). For example, at 1 A the dynamic rectifier target is 5.15 V. Therefore, the operating frequency will be from 150 kHz to 160 kHz in the above example. This is an acceptable operating point. If the operating point ever falls outside the WPC frequency range (110 kHz – 205 kHz), the system will never converge and will become unstable.

In regards to transient analysis, there are two major points of interest:

- Rectifier voltage at the ping frequency (175 kHz).
- Rectifier voltage droop from no load to full load at the constant operating point.

In this example, the ping voltage will be approximately 5 V. This is above the UVLO of the bq51013B and, therefore, start-up in the WPC system can be ensured. If the voltage is near or below the UVLO at this frequency, then start-up in the WPC system may not occur.

If the maximum load step is 1 A, the droop in this example will be approximately 1 V (using the 140 kHz load-line). To analyze the droop, locate the load-line that starts at 7 V at no-load. Follow this load-line to the maximum load expected and take the difference between the 7-V no-load voltage and the full-load voltage at that constant frequency. Ensure that the full-load voltage at this constant frequency is above 5 V. If it descends below 5 V, the output of the power supply will also droop to this level. This type of transient response analysis is necessary due to the slow feedback response of the WPC system. This simulates the step response prior to the WPC system adjusting the operating point.

NOTE

Coupling between the primary and secondary coils will worsen with misalignment of the secondary coil. Therefore, it is recommended to re-analyze the load-lines at multiple misalignments to determine where, in planar space, the receiver will discontinue operation.

See Table 7 for recommended RX coils.

7.4 Device Functional Modes

The operational modes of the bq51013B are described in the *Feature Description*. The bq51013B has several functional modes. Start-up refers to the initial power transfer and communication between the receiver (bq51013B circuit) and the transmitter. Power transfer refers to any time that the TX and RX are communicating and power is being delivered from the TX to the RX. Power transfer termination occurs when the RX is removed from the TX, power is removed from the TX, or the RX requests power transfer termination.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq51013B is a fully integrated wireless power receiver in a single device. The device complies with the WPC v1.2 specifications for a wireless power receiver. When paired with a WPC v1.2 compliant transmitter, it can provide up to 5 W of power. There are several tools available for the design of the system. These tools may be obtained by checking the product page at www.ti.com/product/bq51013B.

8.2 Typical Applications

8.2.1 bq51013B Wireless Power Receiver Used as a Power Supply

The following application discussion covers the requirements for setting up the bq51013B in a Qi-compliant system for use as a power supply.

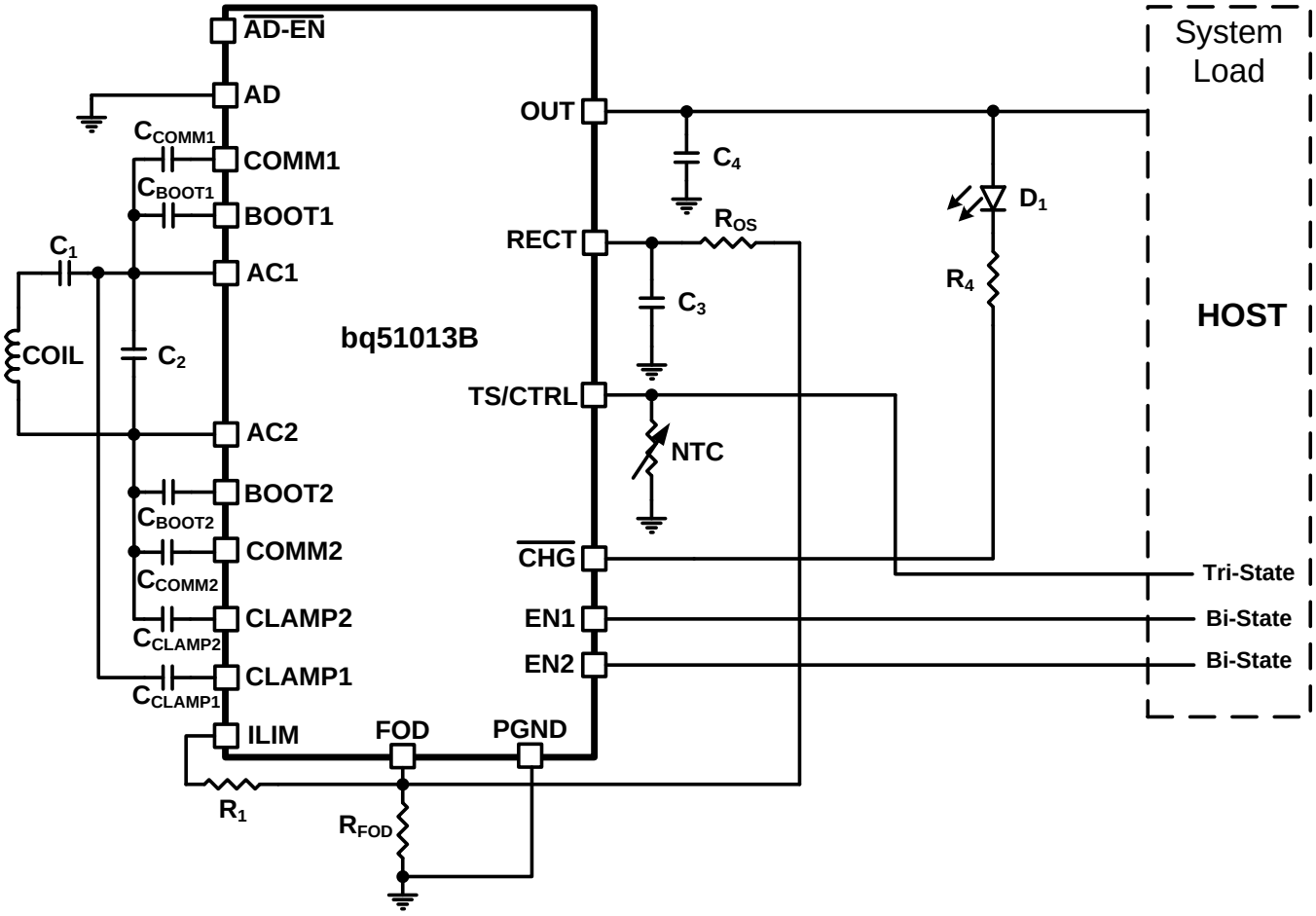


Figure 38. bq51013B Used as a Wireless Power Receiver and Power Supply for System Loads

Typical Applications (continued)

8.2.1.1 Design Requirements

This application is for a system that has varying loads from less than 100 mA up to 1 A. It must work with any Qi-certified transmitter. There is no requirement for any external thermal measurements. An LED indication is required to indicate an active power supply. Each of the components from the application drawing will be examined.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Using The bq51013b as a Wireless Power Supply: (See Figure 38)

Figure 43 is the schematic of a system which uses the bq51013B as a power supply while power multiplexing the wired (adapter) port.

When the system shown in Figure 38 is placed on the charging pad, the receiver coil is inductively coupled to the magnetic flux generated by the coil in the charging pad which consequently induces a voltage in the receiver coil. The internal synchronous rectifier feeds this voltage to the RECT pin which has the filter capacitor C3.

The bq51013B identifies and authenticates itself to the primary using the COMM pins by switching on and off the COMM FETs and hence switching in and out C_{COMM}. If the authentication is successful, the transmitter will remain powered on. The bq51013B measures the voltage at the RECT pin, calculates the difference between the actual voltage and the desired voltage $V_{RECT-REG}$, (threshold 1 at no load) and sends back error packets to the primary. (Dynamic V_{RECT} Thresholds are shown in the *Electrical Characteristics* table.) This process goes on until the input voltage settles at $V_{RECT-REG}$. During a load transient, the dynamic rectifier algorithm will set the targets specified by $V_{RECT-REG}$ thresholds 1, 2, 3, and 4. This algorithm is termed Dynamic Rectifier Control and is used to enhance the transient response of the power supply.

During power up, the LDO is held off until the $V_{RECT-REG}$ threshold 1 converges. The voltage control loop ensures that the output voltage is maintained at $V_{OUT-REG}$ to power the system. The bq51013B meanwhile continues to monitor the input voltage, and maintains sending error packets to the primary every 250 ms. If a large overshoot occurs, the feedback to the primary speeds up to every 32 ms in order to converge on an operating point in less time.

8.2.1.2.2 Series and Parallel Resonant Capacitor Selection

Shown in Figure 38, the capacitors C1 (series) and C2 (parallel) make up the dual resonant circuit with the receiver coil. These two capacitors must be sized correctly per the WPC v1.2 specification. Figure 39 illustrates the equivalent circuit of the dual resonant circuit:

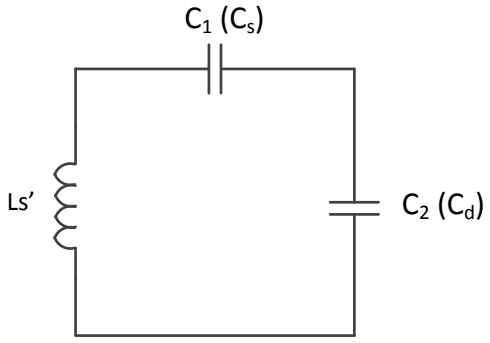


Figure 39. Dual Resonant Circuit With the Receiver Coil

The Power Receiver Design Requirements in Volume 1 of the WPC v1.2 specification highlights in detail the sizing requirements. To summarize, the receiver designer will be required to take inductance measurements with a standard test fixture as shown in Figure 40:

Typical Applications (continued)

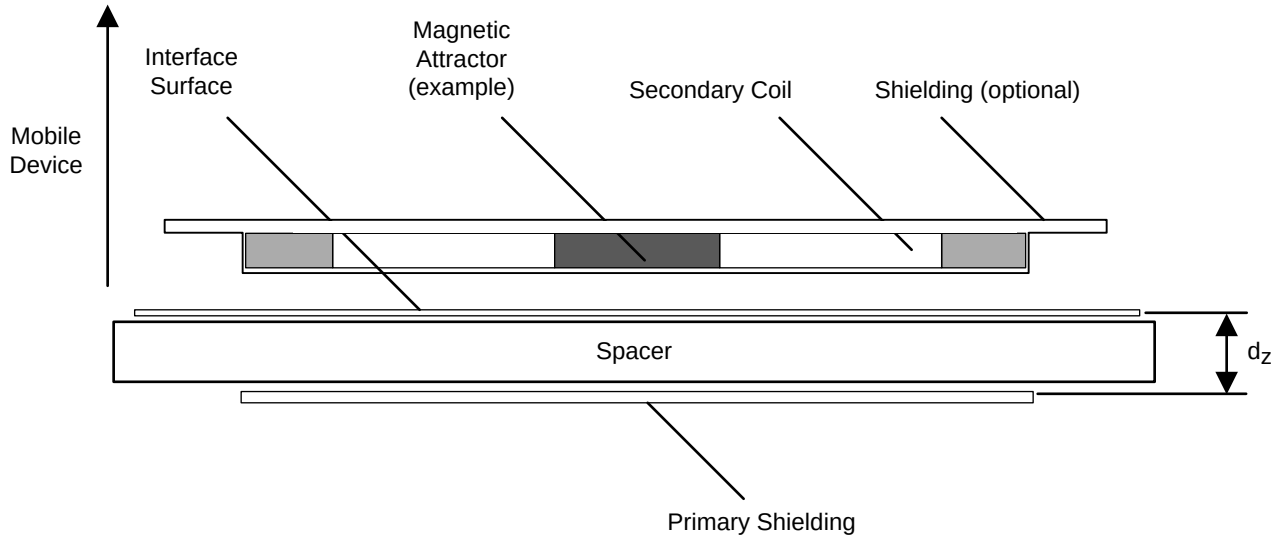


Figure 40. WPC V1.2 Receiver Coil Test Fixture For the Inductance Measurement Ls' (Copied From System Description Wireless Power Transfer, Volume 1: Low Power, Part 1 Interface Definition, Version 1.1)

The primary shield is to be 50 mm × 50 mm × 1 mm of Ferrite material PC44 from TDK Corp. The gap d_Z is to be 3.4 mm. The receiver coil, as it will be placed in the final system (for example, the back cover and battery must be included if the system calls for this), is to be placed on top of this surface and the inductance is to be measured at 1-V RMS and a frequency of 100 kHz. This measurement is termed Ls'. The same measurement is to be repeated without the test fixture shown in Figure 40. This measurement is termed Ls or the free-space inductance. Each capacitor can then be calculated using Equation 6:

$$C_1 = \left[\left(f_S \times 2\pi \right)^2 \times L_S' \right]^{-1}$$

$$C_2 = \left[\left(f_D \times 2\pi \right)^2 \times L_S - \frac{1}{C_1} \right]^{-1}$$

where

- f_S is 100 kHz +5/-10%.
- f_D is 1 MHz ±10%. (6)

C_1 must be chosen first prior to calculating C_2.

The quality factor must be greater than 77 and can be determined by Equation 7:

$$Q = \frac{2\pi \cdot f_D \cdot L_S}{R}$$

where

- R is the DC resistance of the receiver coil. (7)

All other constants are defined above.

Typical Applications (continued)

For this application, the selected coil inductance, Ls, is 11 µH and the Ls' is 16 µH with a DC resistance of 191 mΩ. Using Equation 6, the C1 resolves to 158.3 nF (with a range of 144 nF to 175 nF). For an optimum solution of 3 capacitors in parallel, the chosen capacitors are 68 nF, 47 nF, and 39 nF for a total of 154 nF, well within the desired range. Using the same equation (and the chosen value for C_1), C_2 resolves to 2.3 nF. This is easily met with capacitors of 2.2 nF and 100 pF. The C_1 and C_2 capacitors must have a minimum voltage rating of 25 V. Solving for the quality factor (Q in Equation 7), gives a value of over 500.

Table 7 lists the recommended RX coils.

Table 7. Recommended RX Coils

MANUFACTURER	PART NUMBER	DIMENSIONS	Ls	Ls'	OUTPUT CURRENT RANGE	APPLICATION
Dexerials	NSTC4832T7346-16B	32 mm × 48 mm	10.9 µH	15.6 µH(1)	50 mA - 1000 mA	General 5-V Power Supply
Mingstar	312-00015	28 mm × 14 mm	36.3 µH	43.7 µH(1)	50 mA - 1000 mA	General 5-V Power Supply
NuCurrent	NC-01-R37L02O-25250R53	25 mm (round)	10.9 µH	14.1 µH(1)	50 mA - 1000 mA	General 5-V Power Supply
TDK	WR483265-15F5-G	48 mm × 32 mm	13.2 µH	18.8 µH(1)	50 mA - 1000 mA	General 5-V Power Supply
Vishay	IWAS-4832FF-50	48mm × 32 mm	10.9 µH	15.8 µH(2)	50 mA - 1000 mA	General 5-V Power Supply

(1) Ls' measurements conducted with a standard battery behind the RX coil assembly. This measurement is subject to change based on different battery sizes, placements, and casing material.
(2) Battery not present behind the RX coil assembly. Subject to drop in inductance depending on the placement of the battery.

TI recommends that all inductance measurements are repeated in the designers specific system as there are many influence on the final measurements.

8.2.1.2.3 COMM, CLAMP, and BOOT Capacitors

For most applications, the COMM, CLAMP, and BOOT capacitance values will be chosen to match the bq51013BEVM-764.

The BOOT capacitors are used to allow the internal rectifier FETs to turn on and off properly. These capacitors are from AC1 to BOOT1 and from AC2 to BOOT2 and must have a minimum 25-V rating. A 10-nF capacitor with a 25-V rating is chosen.

The CLAMP capacitors are used to aid in the clamping process to protect against overvoltage. These capacitors are from AC1 to CLAMP1 and from AC2 to CLAMP2 and must have a minimum 25-V rating. A 0.47-µF capacitor with a 25-V rating is chosen.

The COMM capacitors are used to facilitate the communication from the RX to the TX. This selection can vary a bit more than the BOOT and CLAMP capacitors. In general, a 22-nF capacitor is recommended. Based on the results of testing of the communication robustness in the final solution, a change to a 47-nF capacitor may be in order. The larger the capacitor the larger the deviation will be on the coil which sends a stronger signal to the TX. This also decreases the efficiency somewhat. In this case, a 22-nF capacitor with a 25-V rating is chosen.

8.2.1.2.4 Control Pins and $\overline{\text{CHG}}$

This section discusses the pins that control the functions of the bq51013B (AD, $\overline{\text{AD\_EN}}$, EN1, EN2, and TS/CTRL).

This solution uses wireless power exclusively. The AD pin is tied low to disable wired power interaction. The output pin $\overline{\text{AD\_EN}}$ is left floating.

EN1 and EN2 are tied to the system controller GPIO pins. This allows the system to control the wireless power transfer. Normal operation leaves EN1 and EN2 low or floating (GPIO low or high impedance). EN1 and EN2 have internal pulldown resistors. With both EN1 and EN2 low, wireless power is enabled and power can be transferred whenever the RX is on a suitable TX. The RX system controller can terminate power transfer and send an EPT 0x01 (Charge Complete) by setting EN1=EN2=1. The TX will terminate power when the EPT 0x01 is received. The TX will continue to test for power transfer, but will not engage until the RX requests power. For example, if the TX is the bq500212A, the TX will send digital pings approximately once per 5 seconds. During each ping, the bq51013B will resend the EPT 0x01. Between the pings, the bq500212A goes into low power

"Sleep" mode reducing power consumption. When the RX system controller determines it is time to resume power transfer (for example, the battery voltage is below its recharge threshold) the controller simply returns EN1 and EN2 to low (or float) states. The next ping of the bq500212A will power the bq51013B which will now communicate that it is time to transfer power. The TX and RX communication resumes and power transfer is reinitiated.

The TS/CTRL pin will be used as a temperature sensor (with the NTC) and maintain the ability to terminate power transfer through the system controller. In this case, the GPIO will be in high impedance for normal NTC (Temperature Sense) control.

The $\overline{CHG}$ pin is used to indicate power transfer. A 2.1-V forward bias LED is used for D_1 with a current limiting 1.5-kΩ series resistor. The LED and resistor are tied from OUT to PGND and D_1 will light during power transfer.

8.2.1.2.5 Current Limit and FOD

The current limit and foreign object detection functions are related. The current limit is set by R_1 + R_{FOD}. R_{FOD} and Ros are determined by FOD calibration. Default values of 20 kΩ for Ros and 196 Ω for R_{FOD} are used. The final values need to be determined based on the FOD calibration. The tool for FOD calibration can be found on the bq51013B web folder under "Tools & software". Good practice is to set the layout with 2 resistors for Ros and 2 for R_{FOD} to allow for precise values once the calibration is complete.

After setting R_{FOD}, R_1 can be calculated based on the desired current limit. The maximum current for this solution under normal operating conditions (I_{MAX}) is 1 A. Using Equation 2 to calculate the maximum current yields a value of 262 Ω for R_{ILIM}. With R_{FOD} set to 196 Ω the remaining resistance for R_1 is 66 Ω. This also sets the hardware current limit to 1.2 A to allow for temporary current surges without system performance concerns.

8.2.1.2.6 RECT and OUT Capacitance

RECT capacitance is used to smooth the AC to DC conversion and to prevent minor current transients from passing to OUT. For this 1-A I_{MAX}, select two 10-µF capacitors and one 0.1-µF capacitor. These should be rated to 16 V.

OUT capacitance is used to reduce any ripple from minor load transients. For this solution, a single 10-µF capacitor and a single 0.1-µF capacitor are used.

8.2.1.3 Application Curves

Figure 41 shows wireless power start-up when the RX is placed on the TX. In this case, the bq500212A is used as the transmitter. When the rectifier voltage stabilizes, the output is enabled and current is passed. In this case, the load is resistive generating 900 mA. The pulses on the RECT pin indicate communication packets being transferred from the RX to the TX.

Figure 42 shows a current transition. The plot shows a 1-A load removed then added again. Note the stability of V_{OUT}.

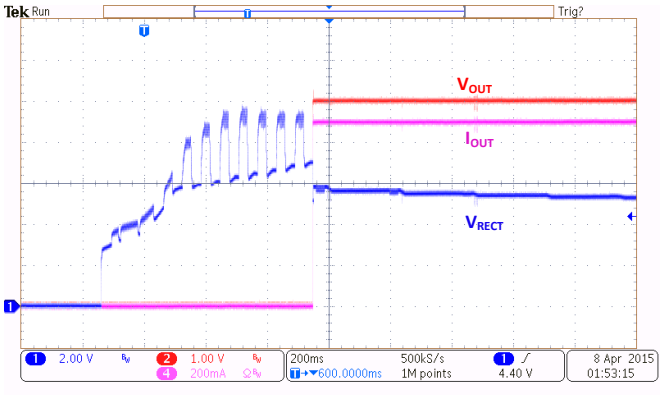


Figure 41. Start-Up With 900-mA Load

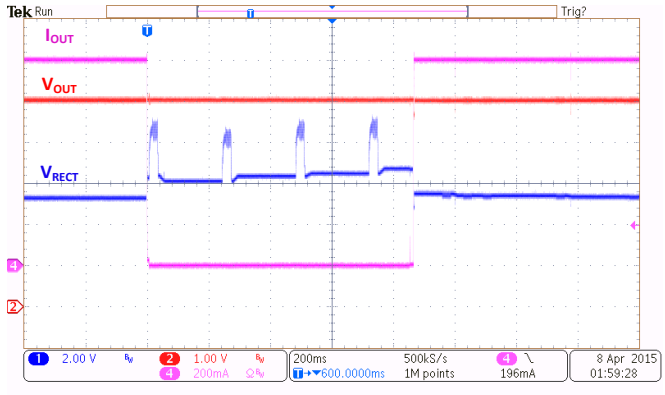


Figure 42. Load Transitions (1 A to 0 A to 1 A)

8.2.2 Dual Power Path: Wireless Power and DC Input

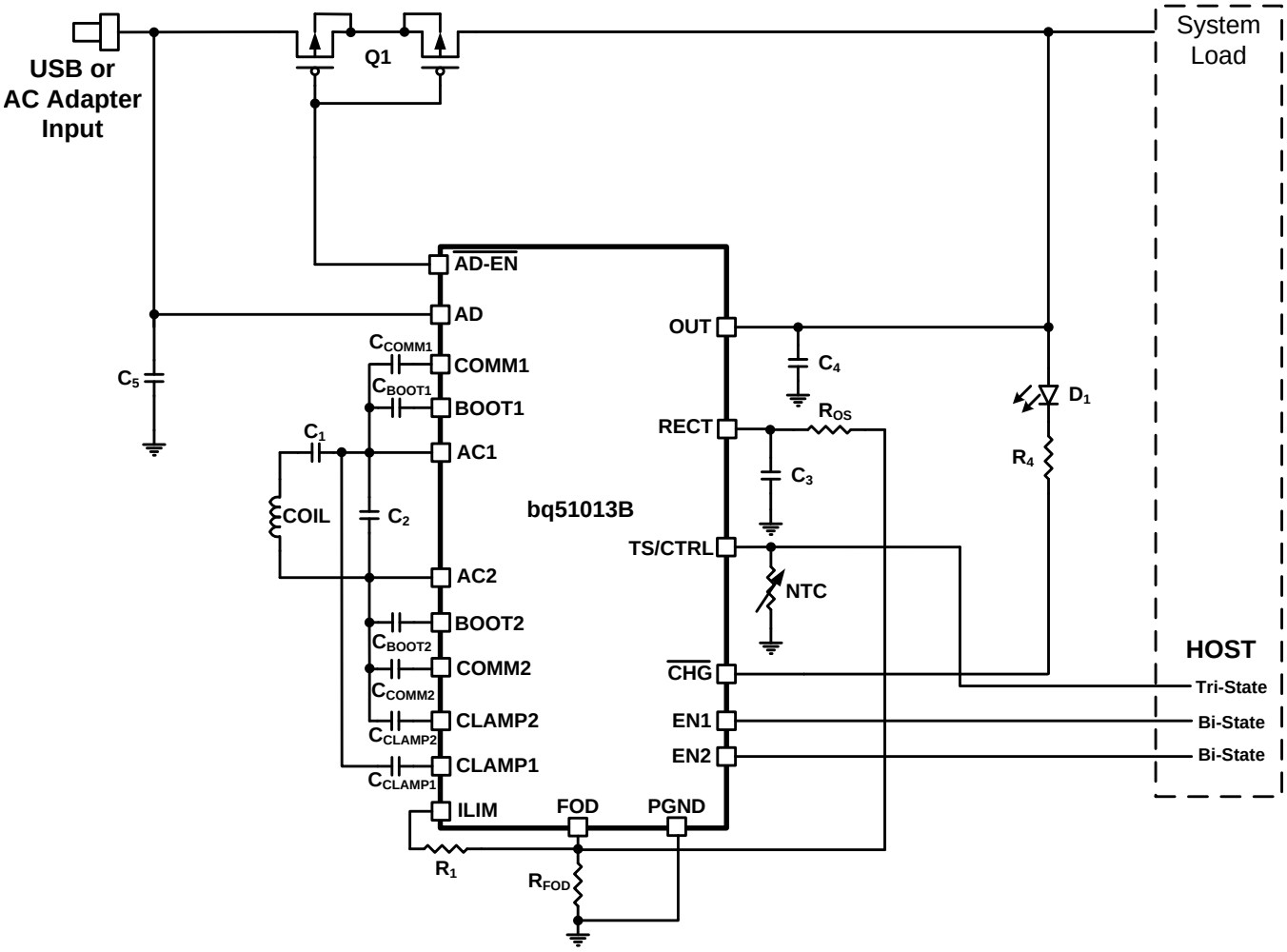


Figure 43. bq51013B Used as a Wireless Power Receiver and Power Supply for System Loads With Adapter Power-Path Multiplexing

8.2.2.1 Design Requirements

This solution adds the ability to disable wireless charging with the AD and $\overline{\text{AD\_EN}}$ pins. A DC supply (USB or AC Adapter with DC output) can also be used to power the subsystem. This can occur during wireless power transfer or without wireless power transfer. The system must allow power transfer without any back-flow or damage to the circuitry.

8.2.2.2 Detailed Design Procedure

The components chosen for the *bq51013B Wireless Power Receiver Used as a Power Supply* system are identical. Adding a blocking FET while using the bq51013B for control is the only addition to the circuitry.The AD pin will be tied to the DC input as a threshold detector. The $\overline{\text{AD\_EN}}$ pin will be used to enable or disable the blocking FET. The blocking FET must be chosen to handle the appropriate current level and the DC voltage level supplied from the input. In this example, the expectation is that the DC input will be 5 V with a maximum current of 1 A (same configuration as the wireless power supply). The CSD75207W15 is a good fit because it is a P-Channel, –20-V, 3.9-A FET pair in a 1.5-mm^2 WCSP.

The following scope plots show behavior under different conditions.

Figure 44 shows the transition from wireless power to wired power when power is added to the AD pin. V_{RECT} drops and there is a short time (I_{OUT} drops to zero) when neither source is providing power. When Q1 is enabled (through AD_EN) the output current turns back on. Note the RECT voltage after about 500 ms. This is the TX sending a ping to check to see if power is required. RECT returns to low after the bq51013B informs the TX it does not need power (without enabling the OUT pin). This timing is based on the TX (bq500212A used here).

Figure 45 shows the transition to wireless power when the AD voltage is removed. Note that after wired power is removed, the next ping from the (bq500212A) will energize the bq51013B. Once the rectifier voltage is stable the output will turn on.

Figure 46 shows a system placed onto the transmitter with AD already powered. The TX sends a ping which the RX responds to and informs the TX that no power is needed. The ping will continue with the timing based on the TX used.

Figure 47 shows the AD added when the RX is not on a TX. This indicates normal start-up without requirement of the TX.

8.2.2.3 Application Curves

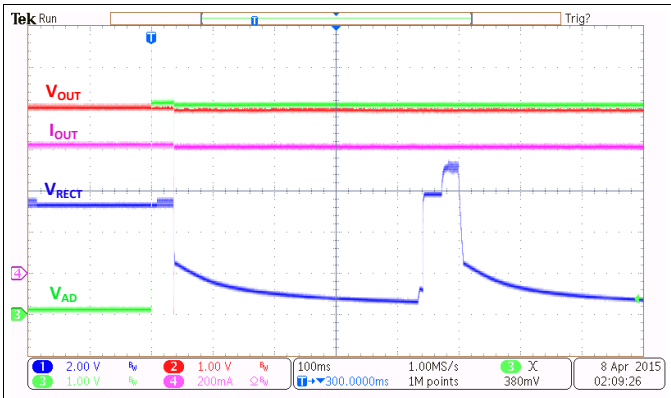


Figure 44. Transition Between Wireless Power and Wired Power (EN1 = EN2 = LOW)

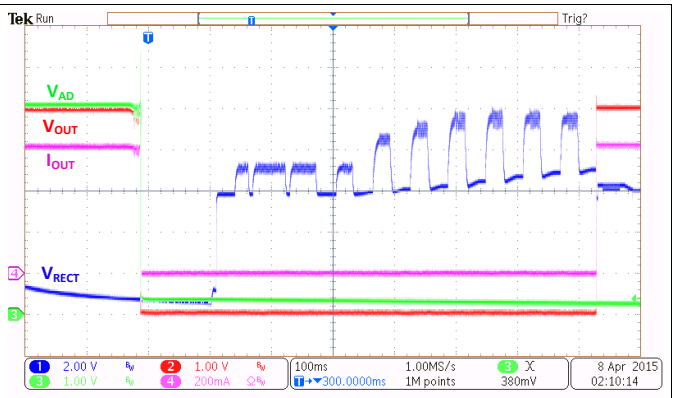


Figure 45. Transition Between Wired Power and Wireless Power (EN1 = EN2 = LOW)

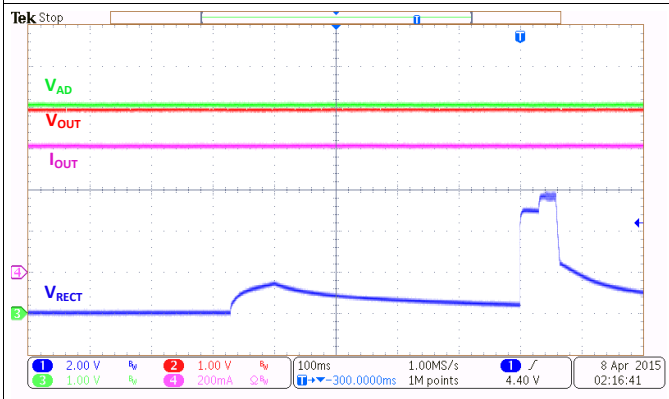


Figure 46. Wireless Power Start-Up With V_{AD} = 5 V (EN1 = EN2 = LOW)

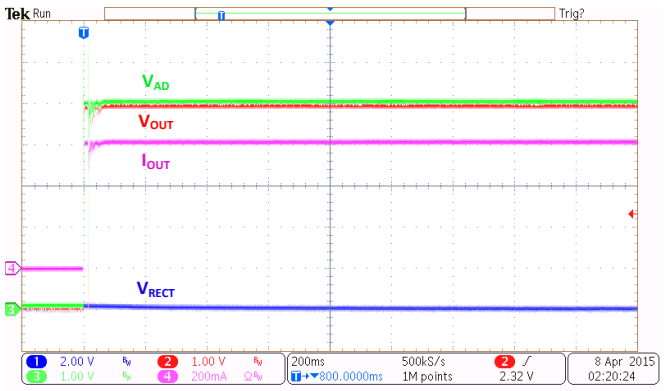


Figure 47. AD Power Start-Up With No Transmitter (EN1 = EN2 = LOW)

8.2.3 Wireless and Direct Charging of a Li-Ion Battery at 800 mA

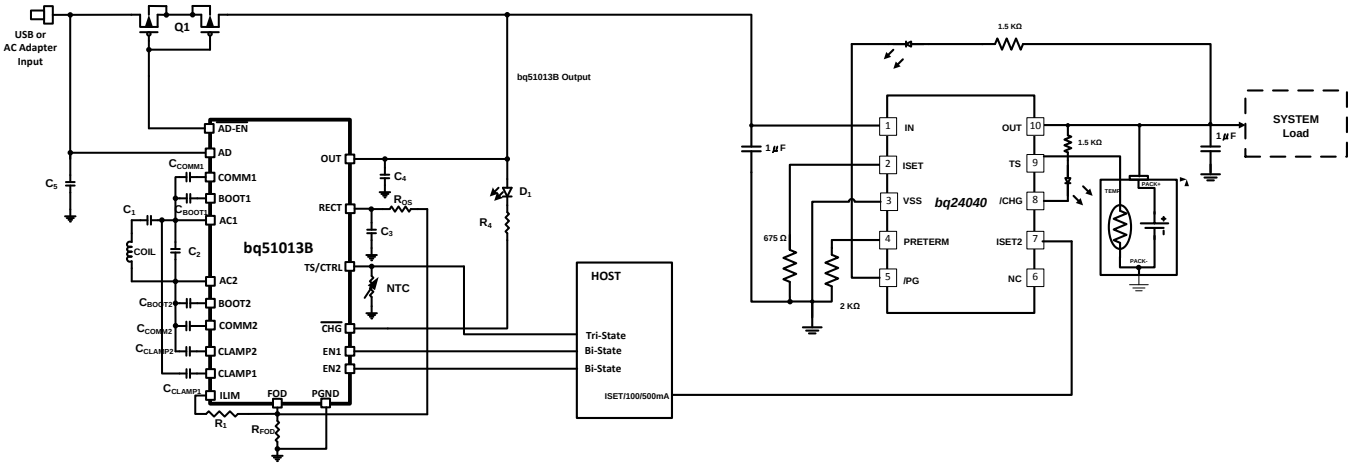


Figure 48. bq51013B Used as a Wireless Power Supply With Adapter Multiplexing for a Linear Charger

8.2.3.1 Design Requirements

The goal of this design is to charge a 3.7-V Li-Ion battery at 800 mA either wirelessly or with a direct USB wired input. This design will use the bq51013B wireless power supply and the bq24040 single-cell Li-Ion battery charger. A low resistance path has to be created between the output of bq51013B and the input of bq24040.

8.2.3.2 Detailed Design Procedure

The basic bq51013B design is identical to the *Dual Power Path: Wireless Power and DC Input*. The bq51013B OUT pin is tied to the output of Q1 and directly to the IN pin of the bq24040. No other changes to the bq51013B circuitry are required.

The bq24040 has a few parameters that need to be programmed for this charger to work properly. Ceramic decoupling capacitors are needed on the IN and OUT pins using the values shown in Figure 48. After evaluation during actual system operational conditions, the final values may be adjusted up or down. In high amplitude pulsed load applications, the IN and OUT capacitors will generally require larger values. The next step is setting up the fast charge current and pre-charge and termination current.

Program the Fast Charge Current, ISET: $R_{ISET} = [K_{ISET}/I_{OUT}] = [540\ A\Omega / 0.8\ A] = 675\ \Omega$.

Program the Termination Current, ITERM: $R_{PRE\text{-}TERM} = [K_{TERM}/\%_{OUT\text{-}FC}] = 200\ \Omega/\% \times 10\% = 2\ k\Omega$.

TS Function: To enable the temperature sense function, a 10-kΩ NTC thermistor (103AT) from TS to VSS should be placed in the battery pack. To disable the temperature sense function, use a fixed 10-kΩ resistor between TS and VSS.

Figure 49 shows start-up of the wireless system with the bq24040 charger when TX power is applied after the full RX system has been placed on the charging pad. Channel 1 (yellow) shows the initial power to the TX system. The RECT pin of the bq51013B is shown on Channel 3 (purple). The output of the bq24040 is shown on Channel 2 (blue). Battery current can be seen on Channel 4 (green).

Figure 50 shows a similar condition but in this case, the battery is not connected initially, so the battery detection routine can be observed. After the battery is connected to the charger, the charge current jumps to 800 mA and the output voltage becomes stable. Both the current out of the bq51013B (Channel 1, yellow) and the current out of the bq24040 (Channel 4, green) can be seen.

8.2.3.3 Application Curves

The following plots show the performance of the bq51013B + charger solution.

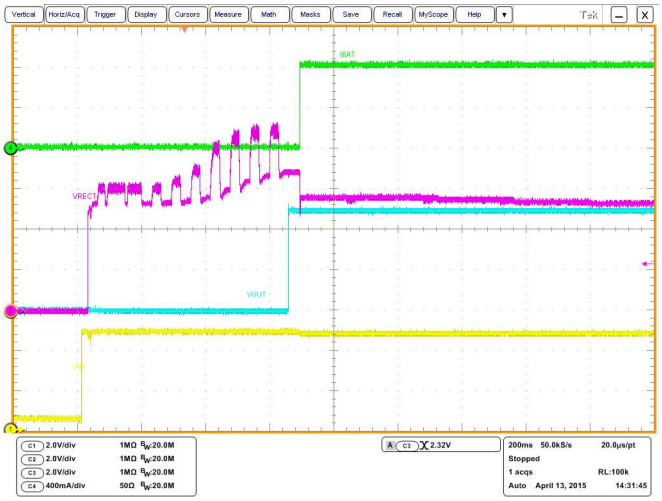


Figure 49. System Start-Up (200 ms / division)

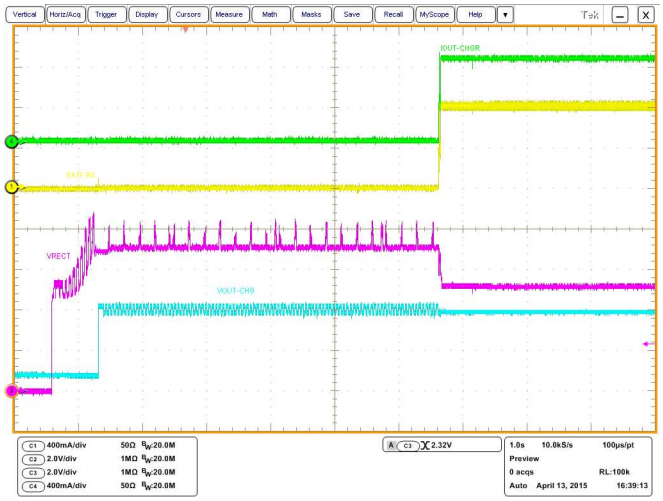


Figure 50. System Start-Up With Battery Inserted After Wireless Power is Enabled (1 s / division)

9 Power Supply Recommendations

The bq51013B requires a Qi-compatible transmitter as its power source.

10 Layout

10.1 Layout Guidelines

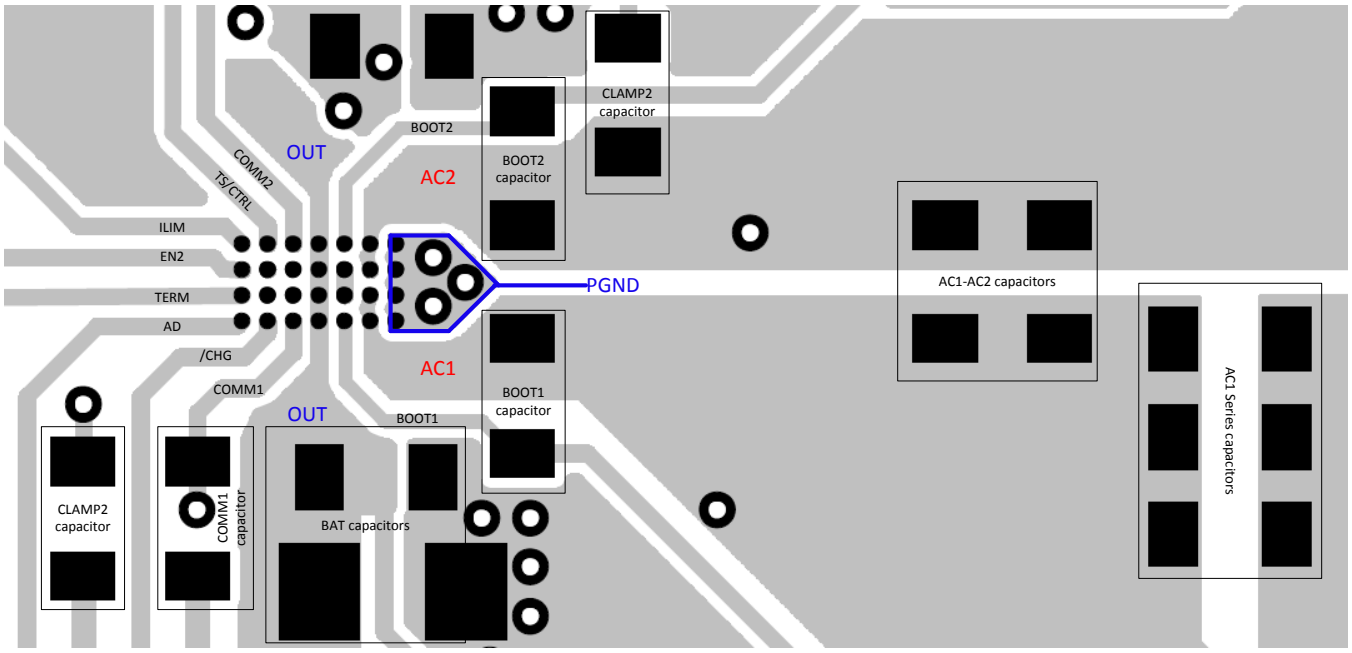
- Keep the trace resistance as low as possible on AC1, AC2, and BAT.
- Detection and resonant capacitors must be as close to the device as possible.
- COMM, CLAMP, and BOOT capacitors must be placed as close to the device as possible.
- Via interconnect on PGND net is critical for appropriate signal integrity and proper thermal performance.
- High frequency bypass capacitors must be placed close to RECT and OUT pins.
- ILIM and FOD resistors are important signal paths and the loops in those paths to PGND must be minimized.

  Signal and sensing traces are the most sensitive to noise; the sensing signal amplitudes are usually measured in mV, which is comparable to the noise amplitude. Make sure that these traces are not being interfered by the noisy and power traces. AC1, AC2, BOOT1, BOOT2, COMM1, and COMM2 are the main source of noise in the board. These traces should be shielded from other components in the board. It is usually preferred to have a ground copper area placed underneath these traces to provide additional shielding. Also, make sure they do not interfere with the signal and sensing traces. The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components).

  For a 1-A fast charge current application, the current rating for each net is as follows:

  - AC1 = AC2 = 1.2 A
  - OUT = 1 A
  - RECT = 100 mA (RMS)
  - COMMx = 300 mA
  - CLAMPx = 500 mA
  - All others can be rated for 10 mA or less

10.2 Layout Example



For the RHL package, the thermal pad should be connected to ground to help dissipate heat.

Figure 51. bq51013B Layout Schematic

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.1.2 开发支持

可以在 bq51013B 网络文件夹（位于工具和软件下）中找到用于异物检测 (FOD) 校准的工具。

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.3 商标

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11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，也不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ51013BRHLR	ACTIVE	VQFN	RHL	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51013B	Samples
BQ51013BRHLT	ACTIVE	VQFN	RHL	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51013B	Samples
BQ51013BYFPR	ACTIVE	DSBGA	YFP	28	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013B	Samples
BQ51013BYFPT	ACTIVE	DSBGA	YFP	28	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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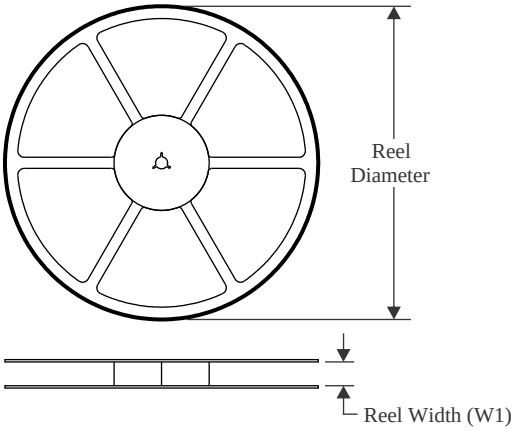
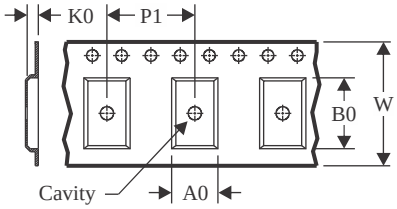
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

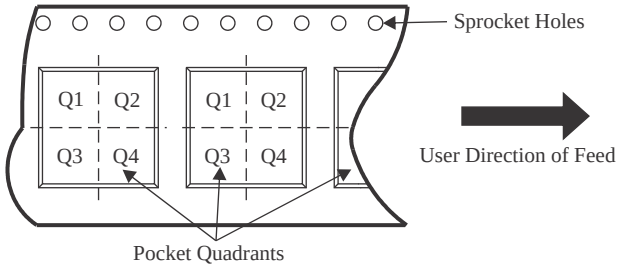


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

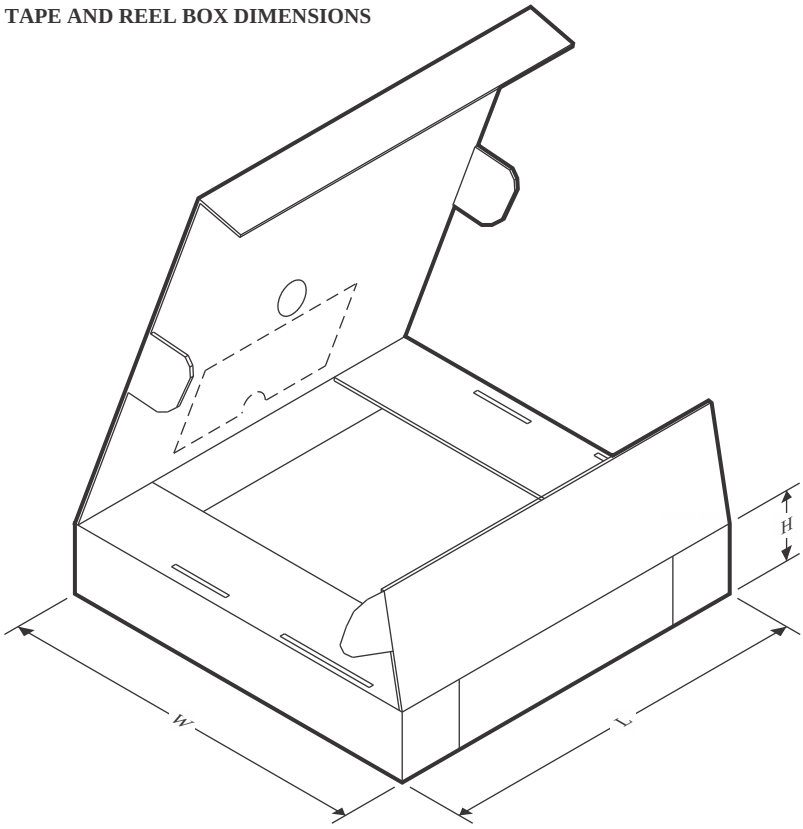
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ51013BRHLR	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51013BRHLT	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51013BYFPR	DSBGA	YFP	28	3000	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51013BYFPT	DSBGA	YFP	28	250	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

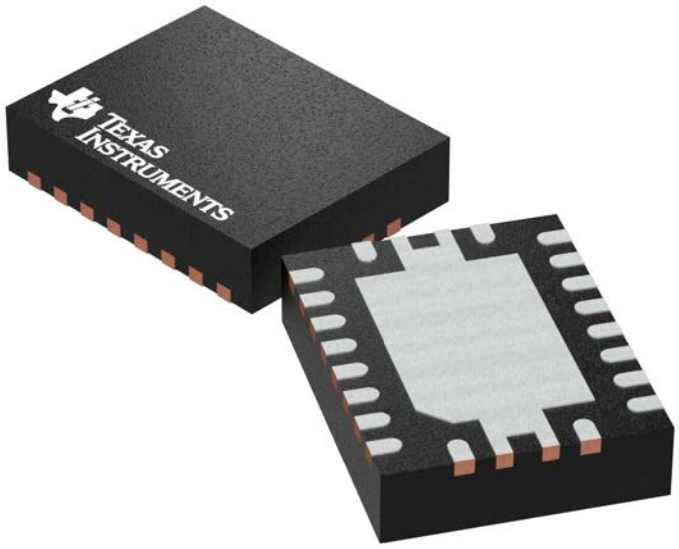
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ51013BRHLR	VQFN	RHL	20	3000	367.0	367.0	35.0
BQ51013BRHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ51013BYFPR	DSBGA	YFP	28	3000	182.0	182.0	20.0
BQ51013BYFPT	DSBGA	YFP	28	250	182.0	182.0	20.0

RHL 20

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

3.5 x 4.5 mm, 0.5 mm pitch



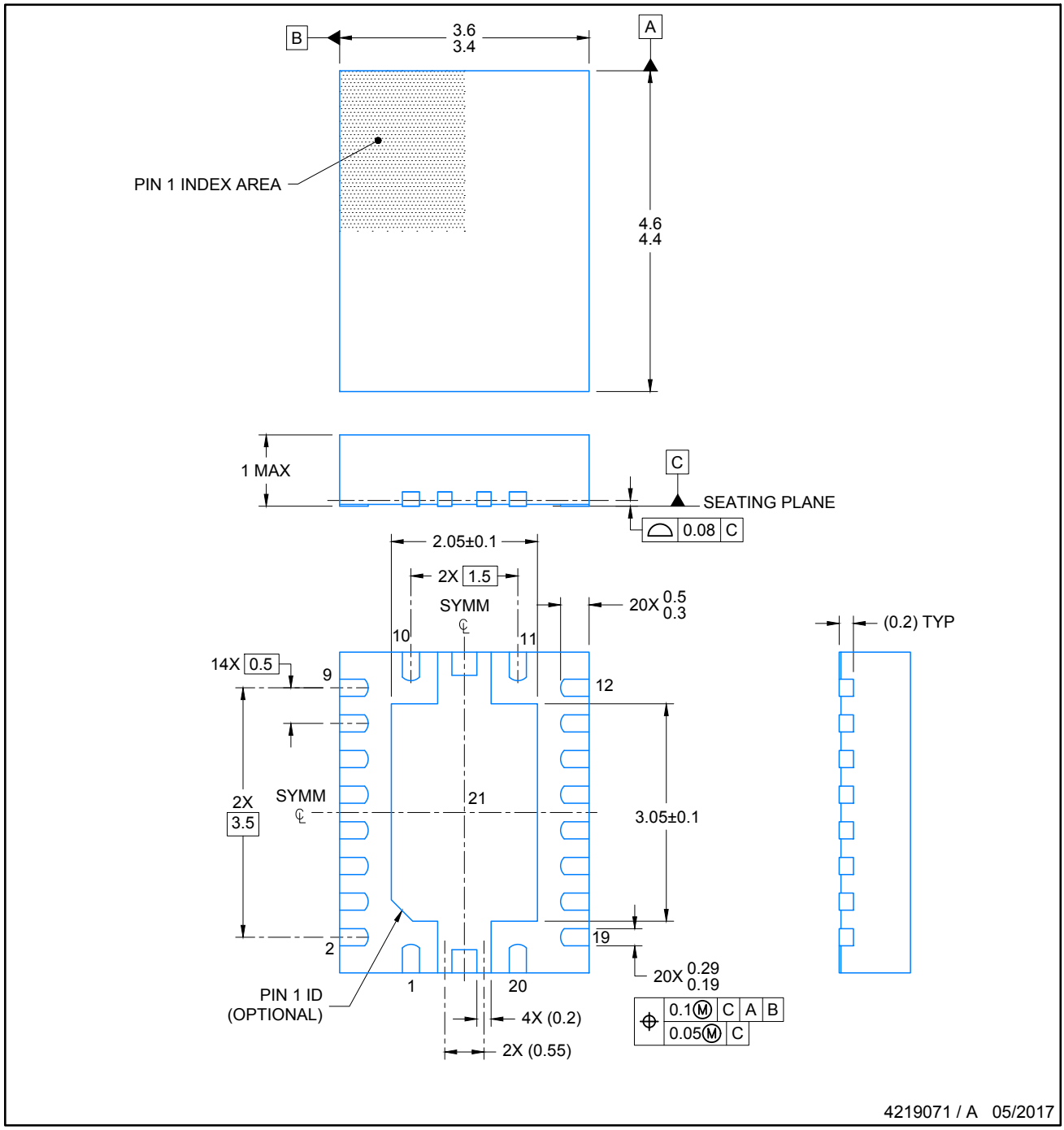
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RHL0020A

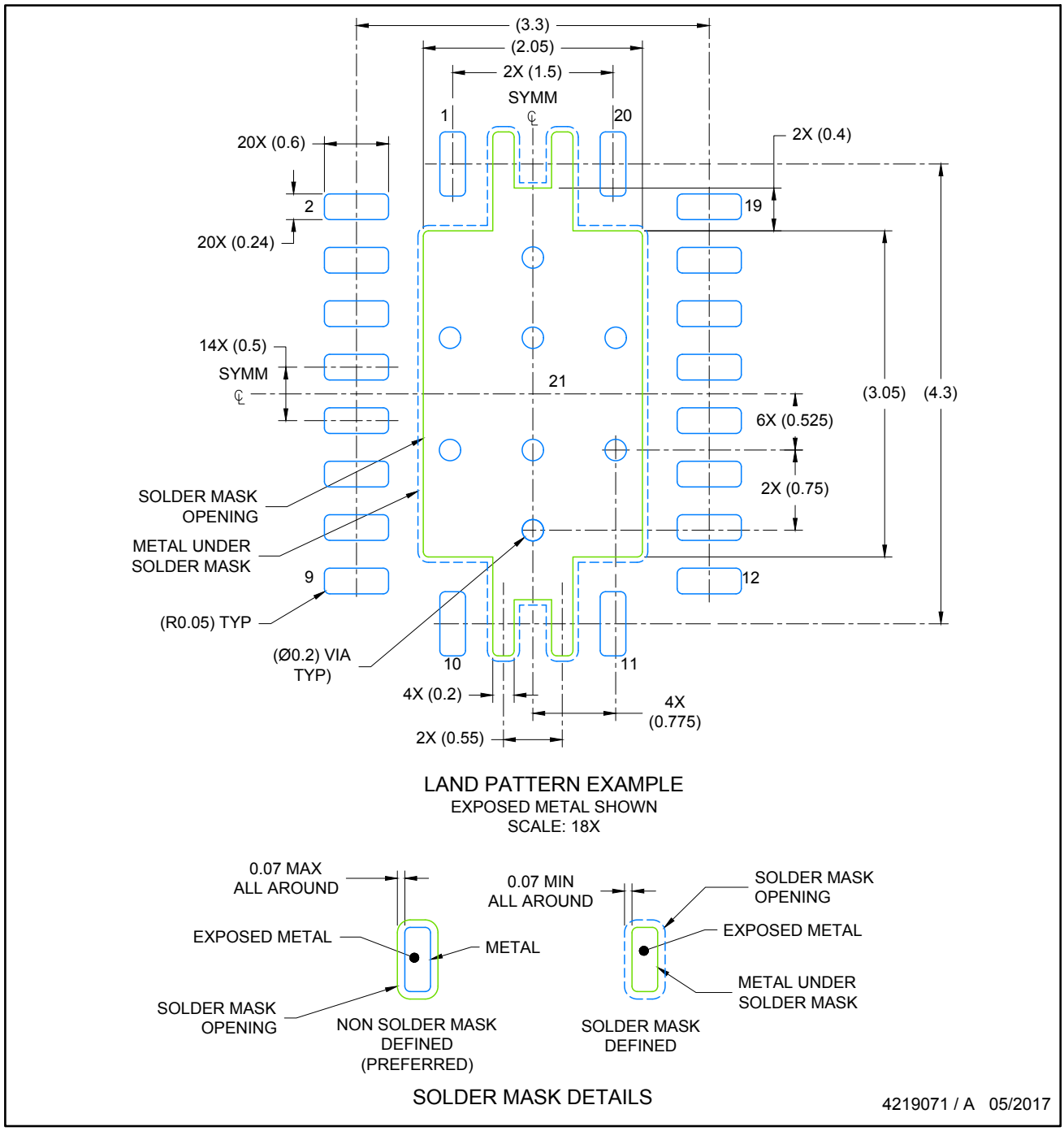
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

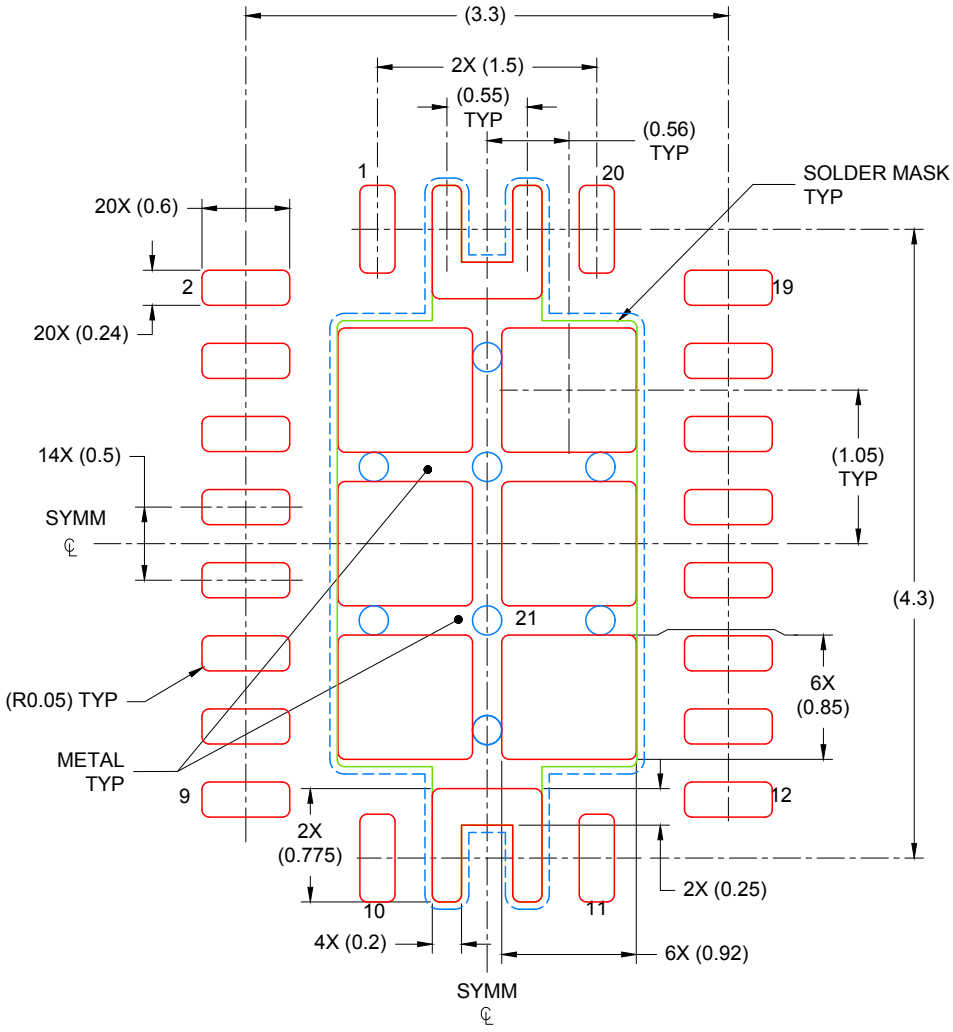


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to theri locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

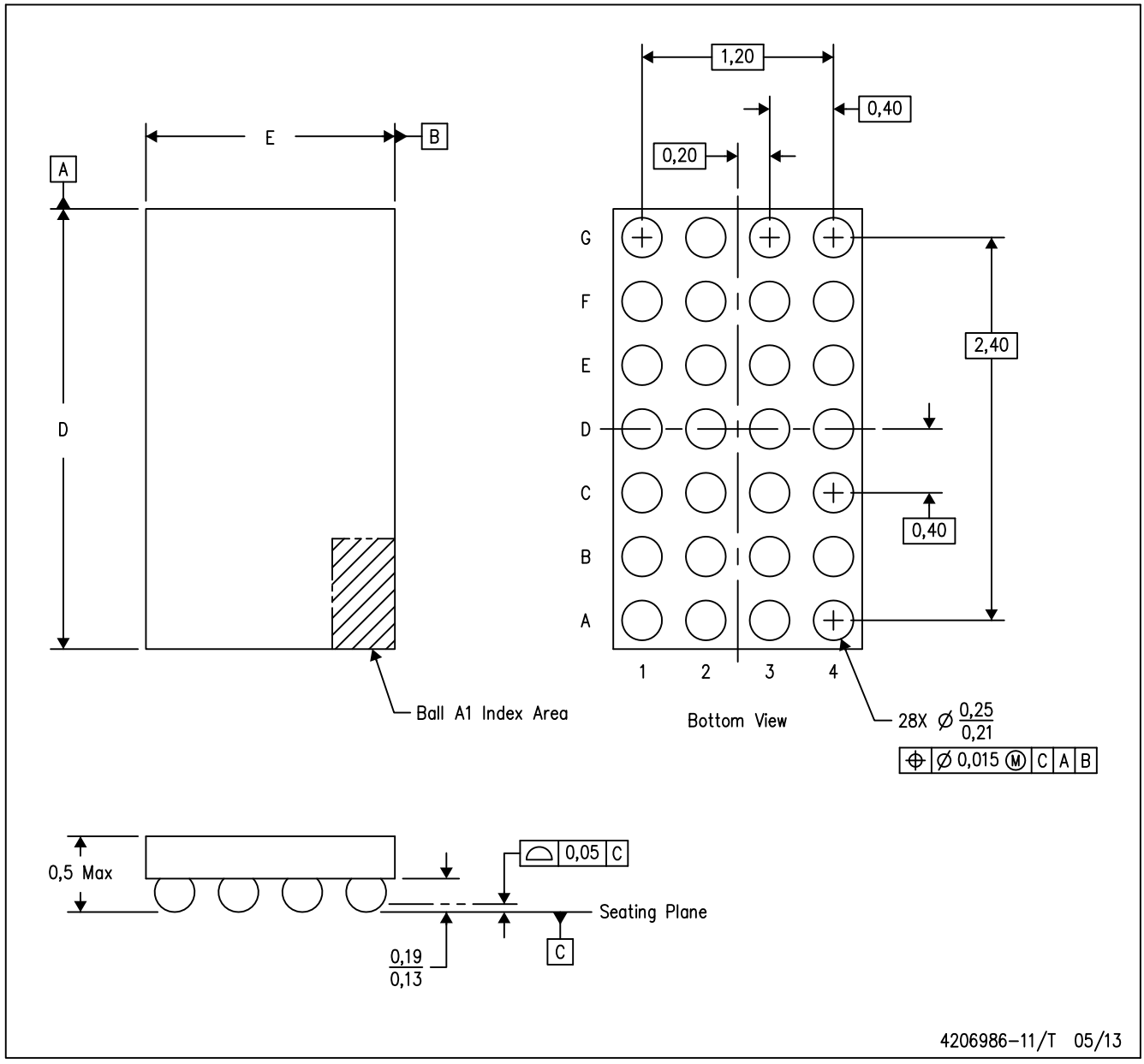
EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 20X

4219071 / A 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

YFP (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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