

- One Receiver and Sixteen Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
- Designed for Signaling Rates Up to 622 Mbps
- Enabling Logic Allows Separate Control of Each Bank of Four Channels or 2-Bit Selection of Any One of the Four Banks
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100 Ω Load
- Electrically Compatible With LVDS, PECL, LVPECL, LVTTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Termination Networks
- Propagation Delay Times <4.7 ns
- Output Skew is < 300 ps and Part-to-Part Skew <1.5 ns
- Total Power Dissipation Typically 470 mW With All Ports Enabled and at 200 MHz
- Driver Outputs or Receiver Input is High Impedance when Disabled or With $V_{CC} < 1.5$ V
- Bus-Pin ESD Protection Exceeds 12 kV
- Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch

description

The SN65LVDS116 is one differential line receiver connected to sixteen differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644, is a data signaling technique that offers the low-power, low-noise coupling, and switching speeds to transmit data at speeds up to 622 Mbps and relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device and signaling technique is for point-to-point or multidrop baseband data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of the signals repeated from the input. This is particularly advantageous in system clock distribution.

The SN65LVDS116 is characterised for operation from -40°C to 85°C .

DGG PACKAGE (TOP VIEW)

GND	1	64	A1Y
V _{CC}	2	63	A1Z
V _{CC}	3	62	A2Y
GND	4	61	A2Z
ENA	5	60	A3Y
ENA	6	59	A3Z
NC	7	58	A4Y
NC	8	57	A4Z
NC	9	56	B1Y
ENB	10	55	B1Z
ENB	11	54	B2Y
NC	12	53	B2Z
NC	13	52	B3Y
NC	14	51	B3Z
GND	15	50	B4Y
V _{CC}	16	49	B4Z
V _{CC}	17	48	C1Y
GND	18	47	C1Z
A	19	46	C2Y
B	20	45	C2Z
NC	21	44	C3Y
ENC	22	43	C3Z
ENC	23	42	C4Y
S0	24	41	C4Z
S1	25	40	D1Y
SM	26	39	D1Z
END	27	38	D2Y
END	28	37	D2Z
GND	29	36	D3Y
V _{CC}	30	35	D3Z
V _{CC}	31	34	D4Y
GND	32	33	D4Z



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**TEXAS
INSTRUMENTS**

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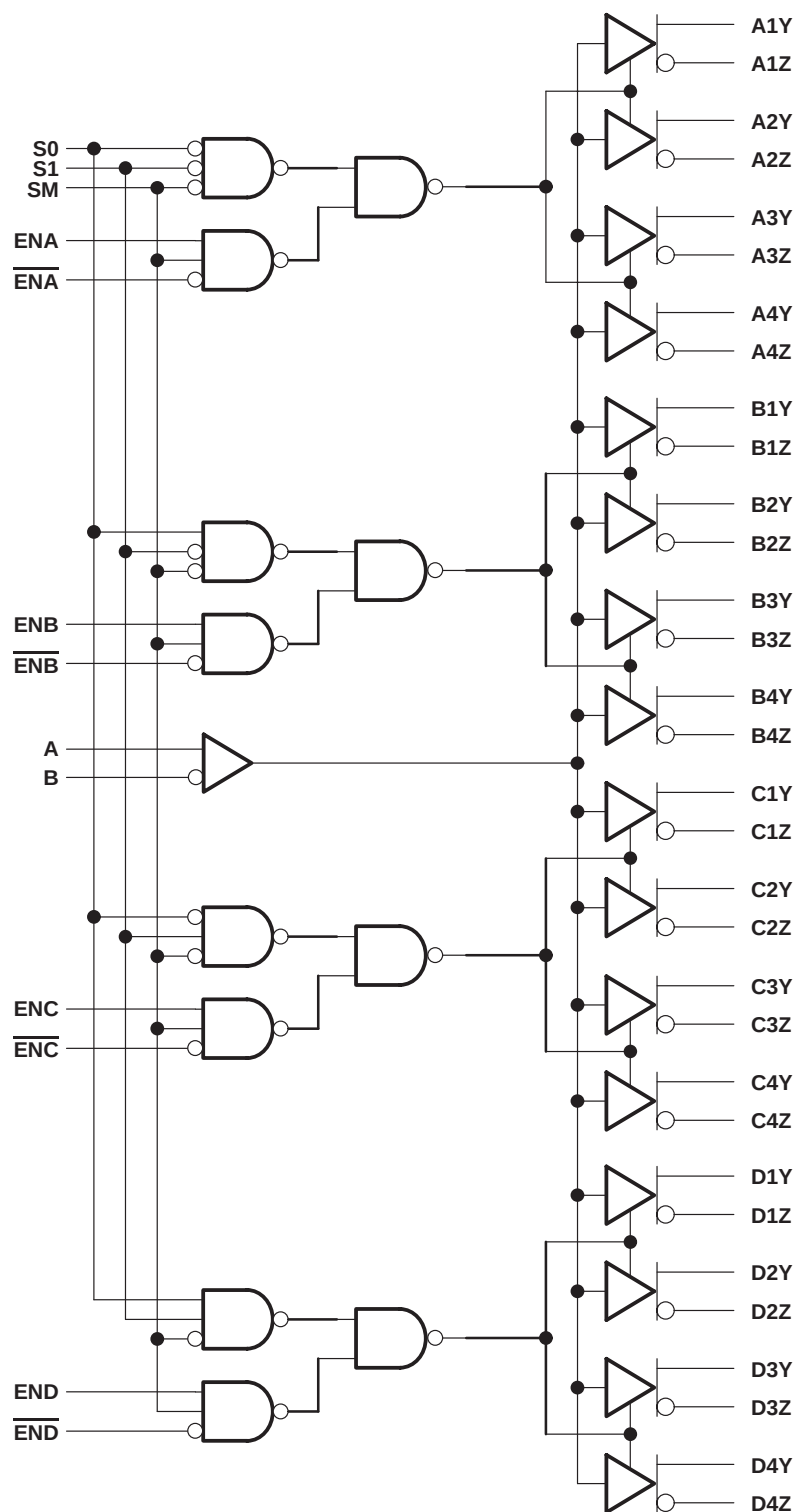
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logic diagram (positive logic)

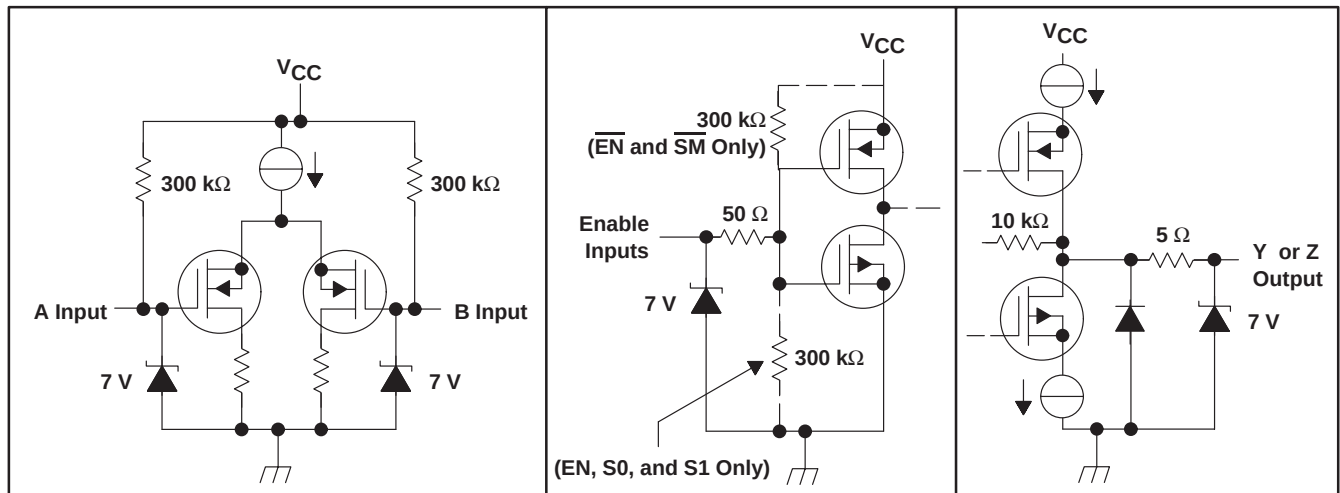


FUNCTION TABLE

INPUT						OUTPUT							
$V_{ID} = V_A - V_B$	SM	EN	$\overline{EN}$	S1	S0	AY	AZ	BY	BZ	CY	CZ	DY	DZ
X	H	L	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
$V_{ID} \geq 100 \text{ mV}$	H	H	L	X	X	H	L	H	L	H	L	H	L
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	H	H	L	X	X	?	?	?	?	?	?	?	?
$V_{ID} \leq -100 \text{ mV}$	H	H	L	X	X	L	H	L	H	L	H	L	H
X	H	X	H	X	X	Z	Z	Z	Z	Z	Z	Z	Z
$V_{ID} \geq 100 \text{ mV}$	L	X	X	L	L	H	L	Z	Z	Z	Z	Z	Z
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	L	X	X	L	L	?	?	Z	Z	Z	Z	Z	Z
$V_{ID} \leq -100 \text{ mV}$	L	X	X	L	L	L	H	Z	Z	Z	Z	Z	Z
$V_{ID} \geq 100 \text{ mV}$	L	X	X	L	H	Z	Z	H	L	Z	Z	Z	Z
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	L	X	X	L	H	Z	Z	?	?	Z	Z	Z	Z
$V_{ID} \leq -100 \text{ mV}$	L	X	X	L	H	Z	Z	L	H	Z	Z	Z	Z
$V_{ID} \geq 100 \text{ mV}$	L	X	X	H	L	Z	Z	Z	Z	H	L	Z	Z
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	L	X	X	H	L	Z	Z	Z	Z	?	?	Z	Z
$V_{ID} \leq -100 \text{ mV}$	L	X	X	H	L	Z	Z	Z	Z	L	H	Z	Z
$V_{ID} \geq 100 \text{ mV}$	L	X	X	H	H	Z	Z	Z	Z	Z	Z	H	L
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	L	X	X	H	H	Z	Z	Z	Z	Z	Z	?	?
$V_{ID} \leq -100 \text{ mV}$	L	X	X	H	H	Z	Z	Z	Z	Z	Z	L	H

H = high level, L = low level, Z = high impedance, ? = indeterminate

equivalent input and output schematic diagrams



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 4 V
Input voltage range, Enable inputs	–0.5 V to 6 V
A, B, Y or Z	–0.5 V to 4 V
Electrostatic discharge, Y, Z, and GND (see Note 2)	Class 3, A: 12 kV, B: 500 V
All pins	Class 3, A: 4 kV, B: 400 V
Continuous power dissipation	See Dissipation Rating Table
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DGG	2094 mW	16.7 mW/°C	1089 mW

[‡] This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $ V_{ID} $	0.1		3.6	V
Common-mode input voltage, V_{IC}	$\frac{ V_{ID} }{2}$		$2.4 - \frac{ V_{ID} }{2}$	V
			$V_{CC} - 0.8$	V
Operating free-air temperature, T_A	–40		85	°C



electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{ITH+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V _{ITH-}	Negative-going differential input voltage threshold		-100			
V _{OD}	Differential output voltage magnitude	R _L = 100Ω, V _{ID} = ±100 mV, See Figure 1 and Figure 2	247	340	454	mV
Δ V _{OD}	Change in differential output voltage magnitude between logic states		-50		50	
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states		-50		50	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage			50	150	
I _{CC}	Supply current	Enabled, R _L = 100Ω		84	115	mA
		Disabled		3.2	6	
I _I	Input current (A or B inputs) [‡]	V _I = 0 V	-2		-20	μA
		V _I = 2.4 V	-1.2			
I _{I(OFF)}	Power-off Input current (A or B inputs)	V _{CC} = 1.5 V, V _I = 2.4 V			20	μA
I _{IH}	High-level input current	ENx, S0, S1			20	μA
		ENx, SM			-20	
I _{IL}	Low-level input current	ENx, S0, S1			10	μA
		ENx, SM			-10	
I _{OS}	Short-circuit output current	V _{OY} or V _{OZ} = 0 V			±24	mA
		V _{OD} = 0 V			±12	
I _{OZ}	High-impedance output current	V _O = 0 V or V _{CC}			±1	μA
I _{O(OFF)}	Power-off output current	V _{CC} = 1.5 V, V _O = 3.6 V			±1	μA
C _{IN}	Input capacitance (A or B inputs)	V _I = 0.4 sin (4E6πt) + 0.5 V		5		pF
C _O	Output capacitance (Y or Z outputs)	V _I = 0.4 sin (4E6πt) + 0.5 V		9.4		

[†] All typical values are at 25°C and with a 3.3 V supply.

[‡] The non-algebraic convention, where the more positive (least negative) limit is designated minimum, is used in this data sheet for the input current (I_I) only.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	R _L = 100 Ω, C _L = 10 pF, See Figure 4	2.2	3.1	4.7	ns
t _{PHL}	Propagation delay time, high-to-low-level output		2.2	3.1	4.7	
t _r	Differential output signal rise time		0.3	0.8	1.2	ns
t _f	Differential output signal fall time		0.3	0.8	1.2	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH}) [‡]			140	500	ps
t _{sk(o)}	Output skew, channel-to-channel [§]			100	300	
t _{sk(pp)}	Part-to-part skew				1.5	ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		5.7	15	ns
t _{PZL}	Propagation delay time, high-impedance-to-low-level output			7.7	15	
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.2	15	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			3.2	15	ns

[†] All typical values are at 25°C and with a 3.3 V supply.

[‡] t_{sk(p)} is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.

[§] t_{sk(o)} is the magnitude of the time difference between the t_{PLH} or t_{PHL} measured at any two outputs.

^{||} t_{sk(pp)} is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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PARAMETER MEASUREMENT INFORMATION

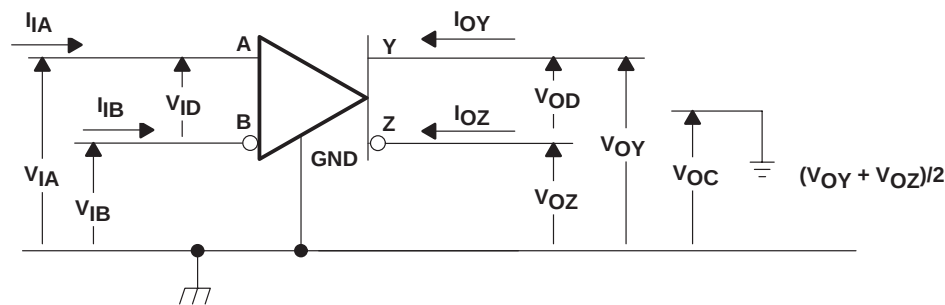


Figure 1. Voltage and Current Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE
VI _A	VI _B	VI _D	VI _C
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V

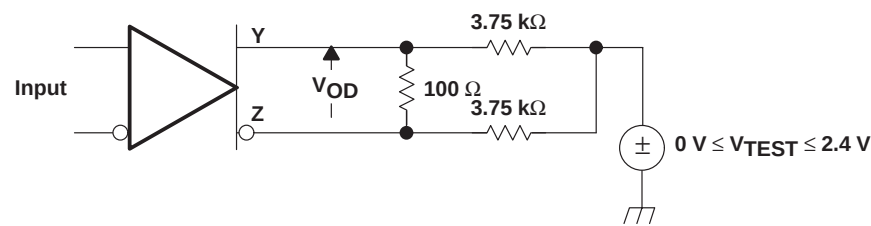
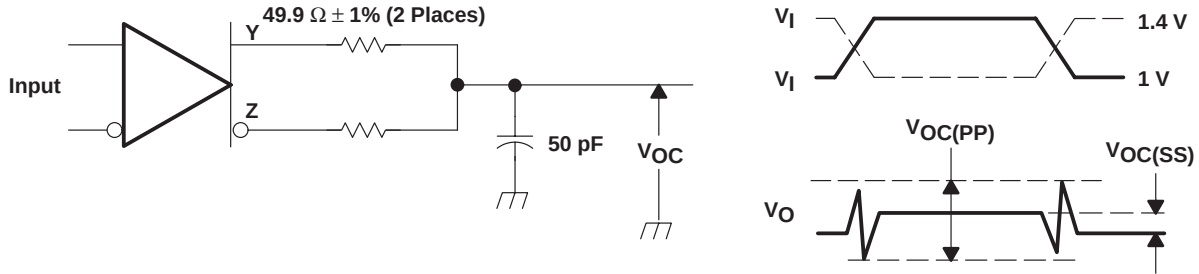


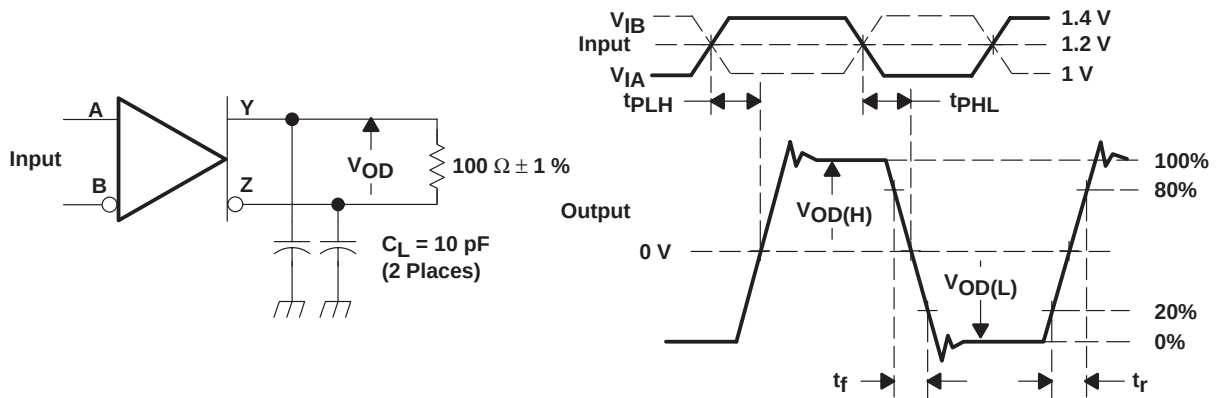
Figure 2. VOD Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, Pulsewidth = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, Pulsewidth = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

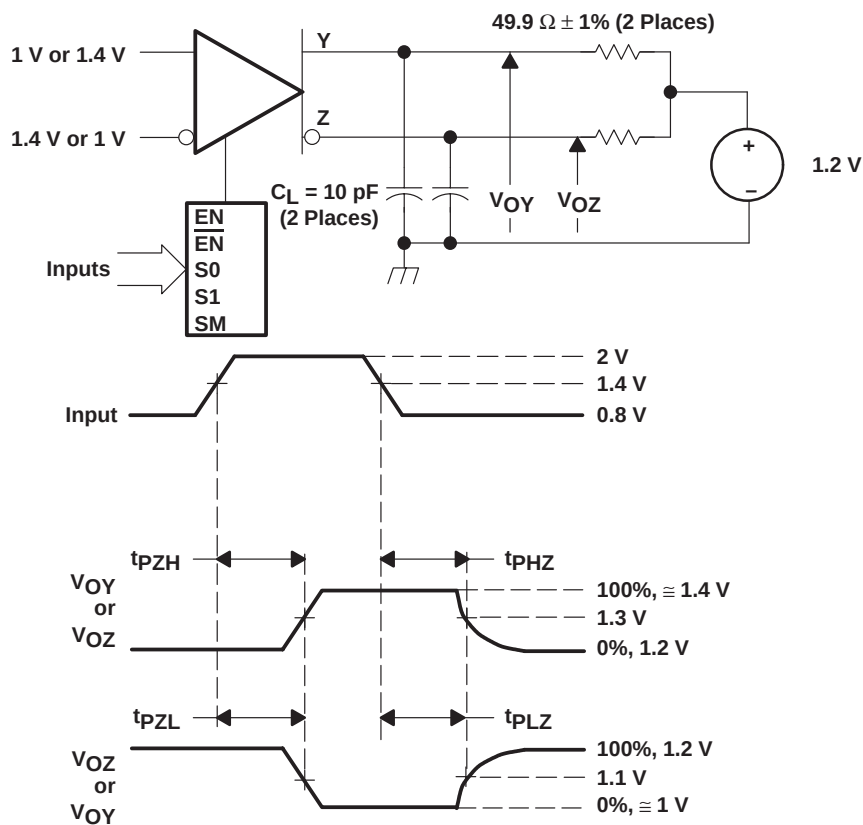
Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

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PARAMETER MEASUREMENT INFORMATION



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 0.5 Mpps, Pulswidth = $500 \pm 10 \text{ ns}$. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

TYPICAL CHARACTERISTICS

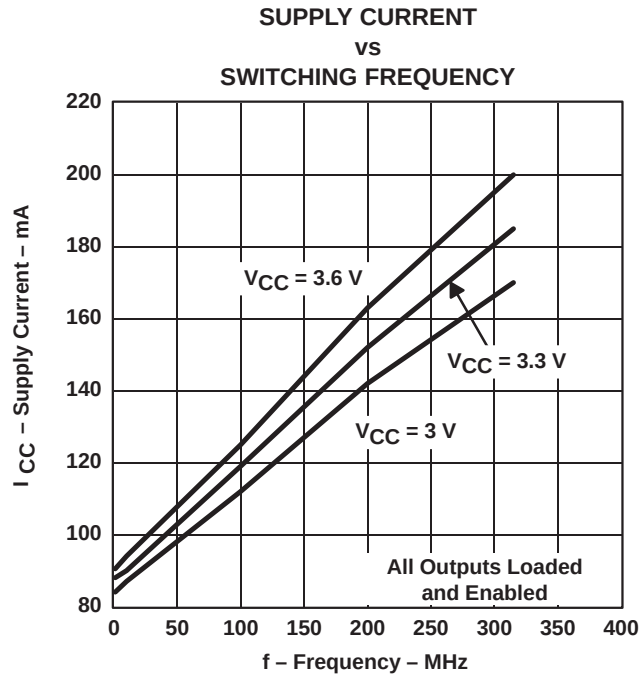


Figure 6

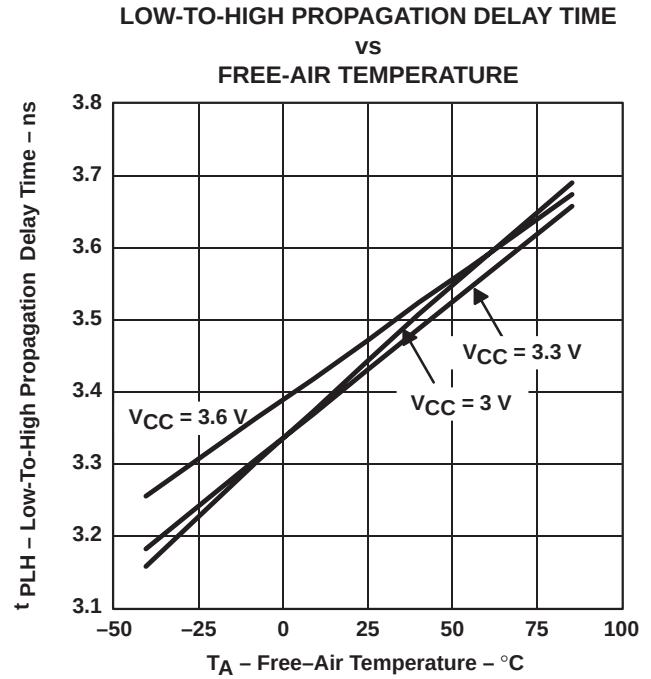


Figure 7

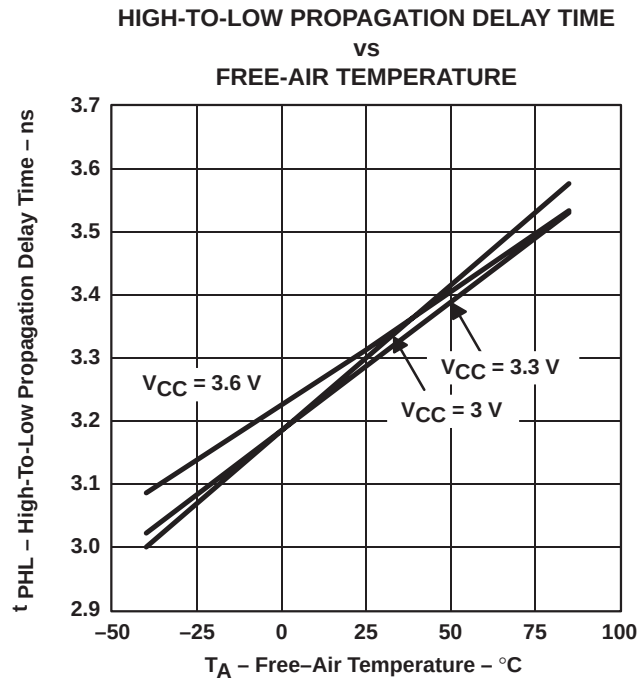


Figure 8

TYPICAL CHARACTERISTICS

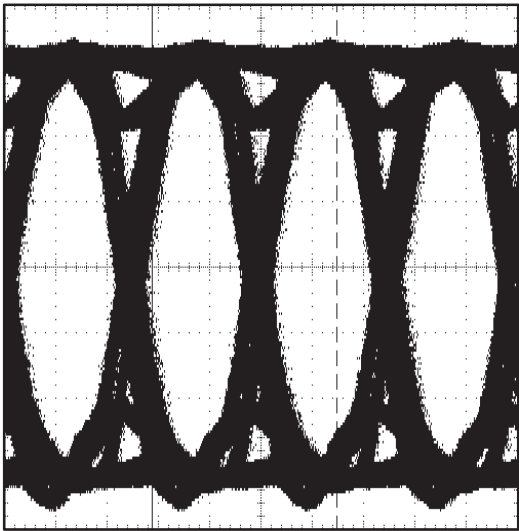


Figure 9. Typical Differential Eye Pattern at 400 Mbps

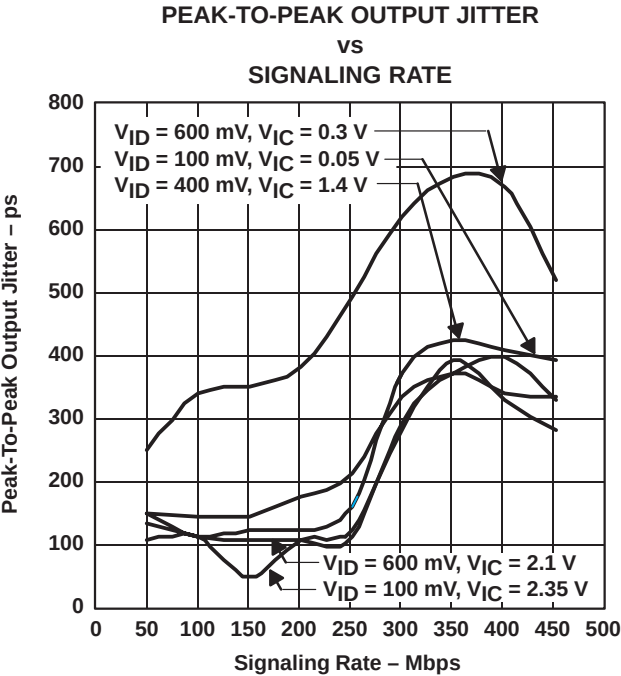


Figure 10. Typical Peak-To-Peak Output Jitter vs V_{ID} and V_{IC}

APPLICATION INFORMATION

An LVDS receiver can be used to receive various other types of logic signals. Figure 11 through Figure 19 show the termination circuits for SSTL, HSTL, GTL, BTL, LVPECL, PECL, CMOS, and TTL.

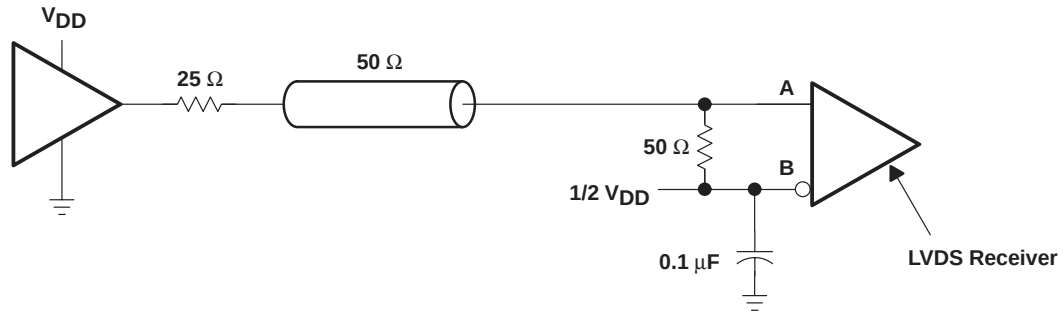


Figure 11. Stub-Series Terminated (SSTL) or High-Speed Transceiver Logic (HSTL)

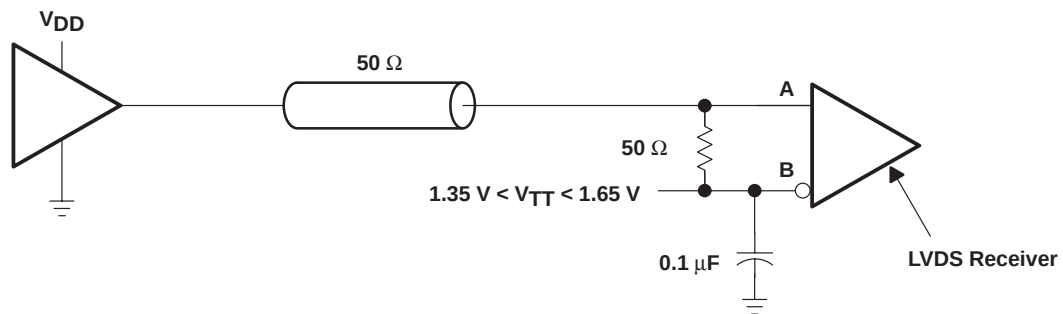


Figure 12. Center-Tap Termination (CTT)

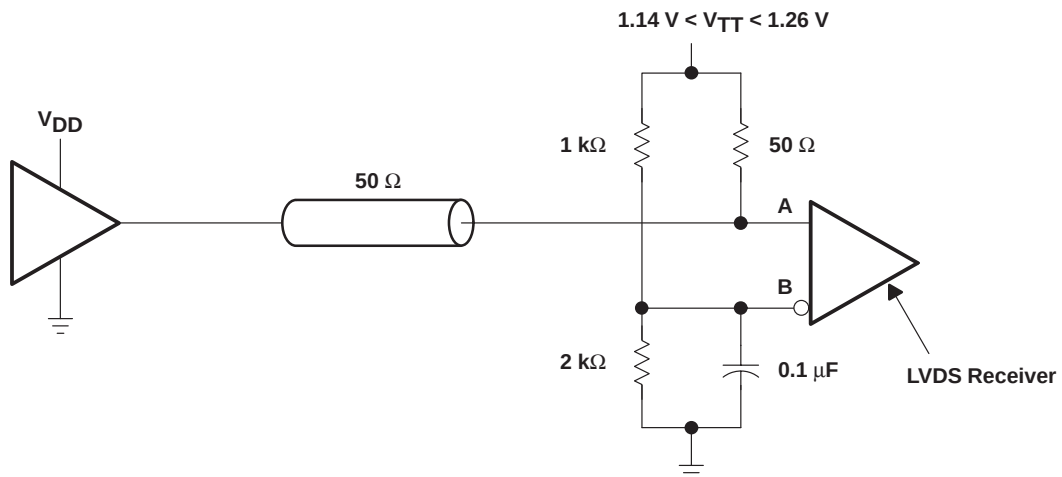


Figure 13. Gunning Transceiver Logic (GTL)

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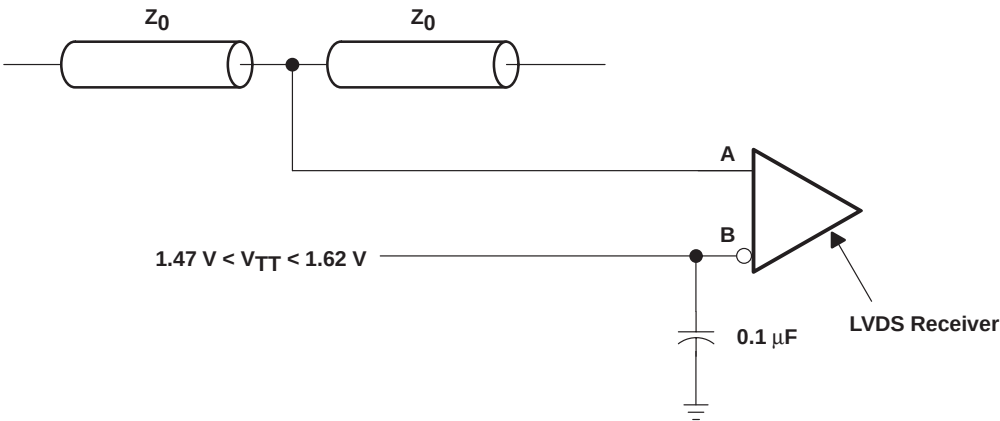


Figure 14. Backplane Transceiver Logic (BTL)

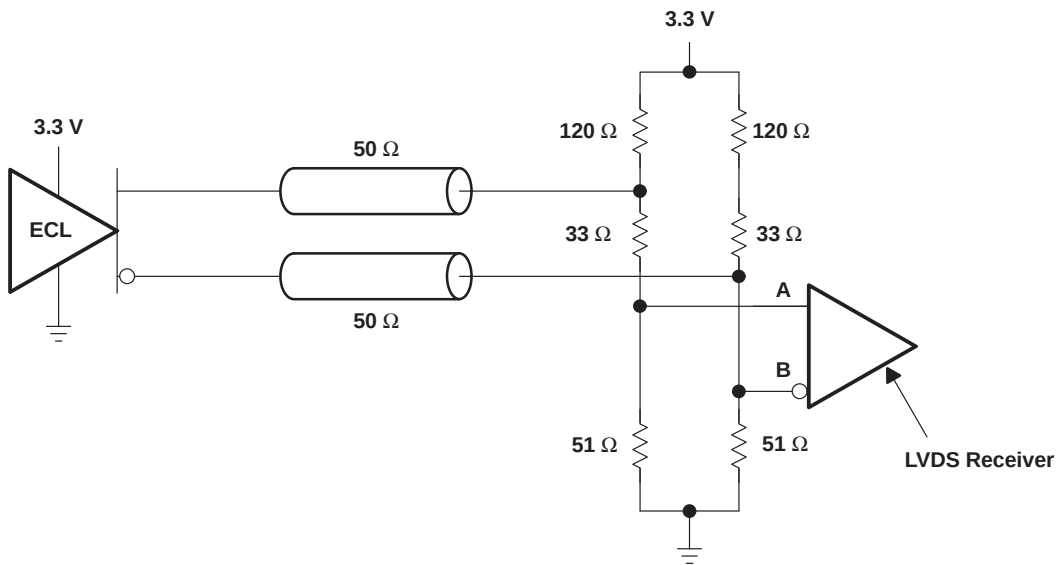


Figure 15. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

APPLICATION INFORMATION

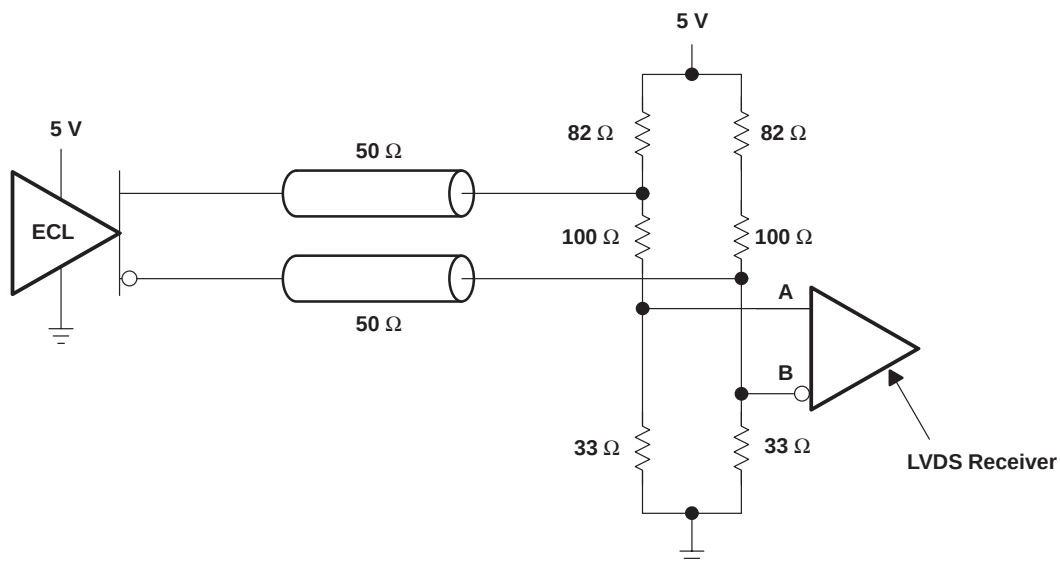


Figure 16. Positive Emitter-Coupled Logic (PECL)

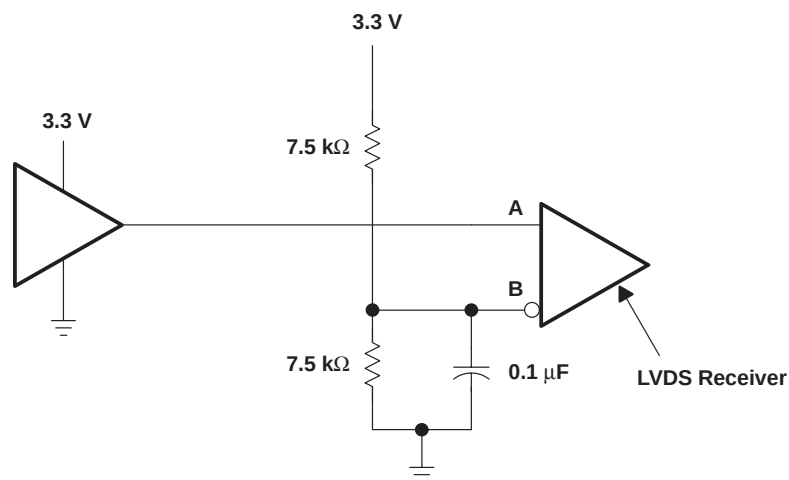


Figure 17. 3.3-V CMOS

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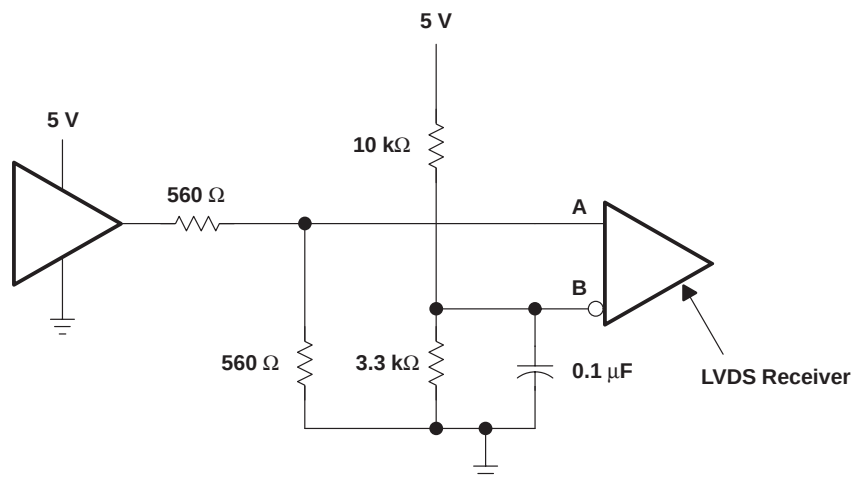


Figure 18. 5-V CMOS

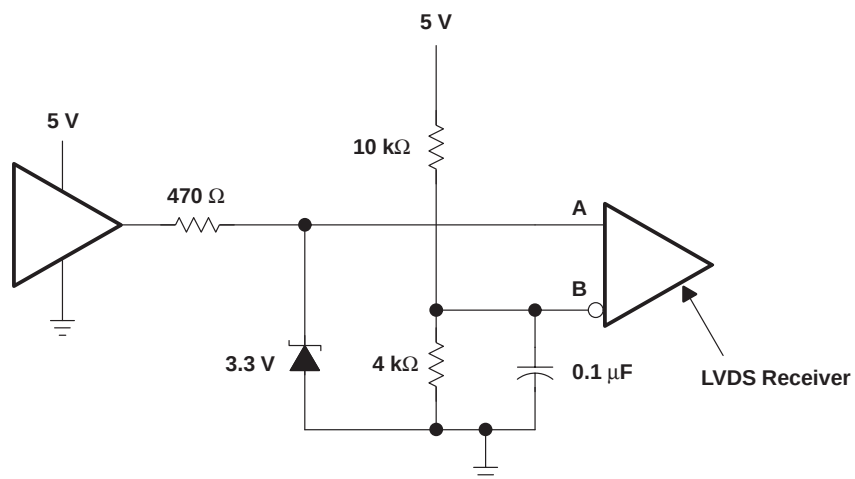


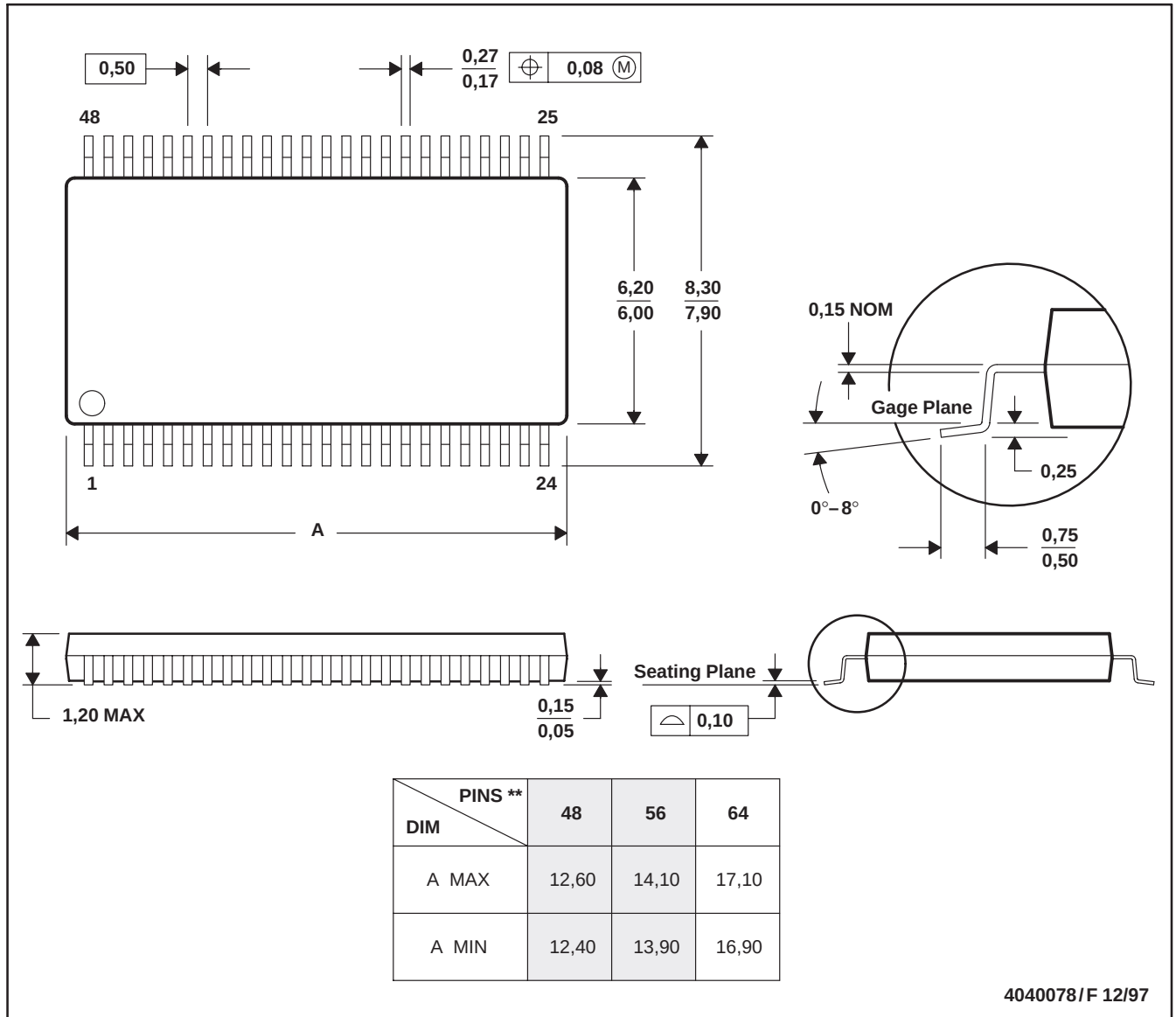
Figure 19. TTL

MECHANICAL DATA

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold protrusion not to exceed 0,15.
E. Falls within JEDEC MO-153

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