PRELIMINARY
Notice ; This is not a final specification.
some parametric limits are subject to change.

M62462FP

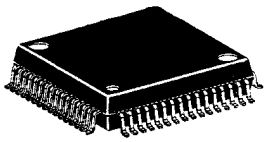
Dolby Pro Logic Surround Decoder

Description

The M62462FP is a Single Chip Dolby Pro Logic Surround Decoder.This LSI has all functions necessary for Dolby Pro Logic Surround.

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Outline



Outline 64P6N
0.8mm pich QFP
(14.0mm*14.0mm*2.8mm)

Features

- **Includes all functions necessary for Dolby Pro Logic Surround**
  - **-Adaptive Matrix**
  - **-Input Auto-Balance**
  - **-Noise Sequencer**
  - **-Center Mode Control ON/OFF, WIDE/NORMAL/PHANTOM**
  - **-Modified Dolby B type Noise Reduction**
  - **-4 channel (Lch/Rch/Cch/Sch) / 3 channel (Lch/Rch/Cch)**
  - **-Digital delay Delay time:15.4 to 51.2msec**
- **Cch/Sch Master Volume 0 to -84dB/1dB step**
- **3-lines MCU control**
- **Current control oscillation circuit for system clock**

System Configuration

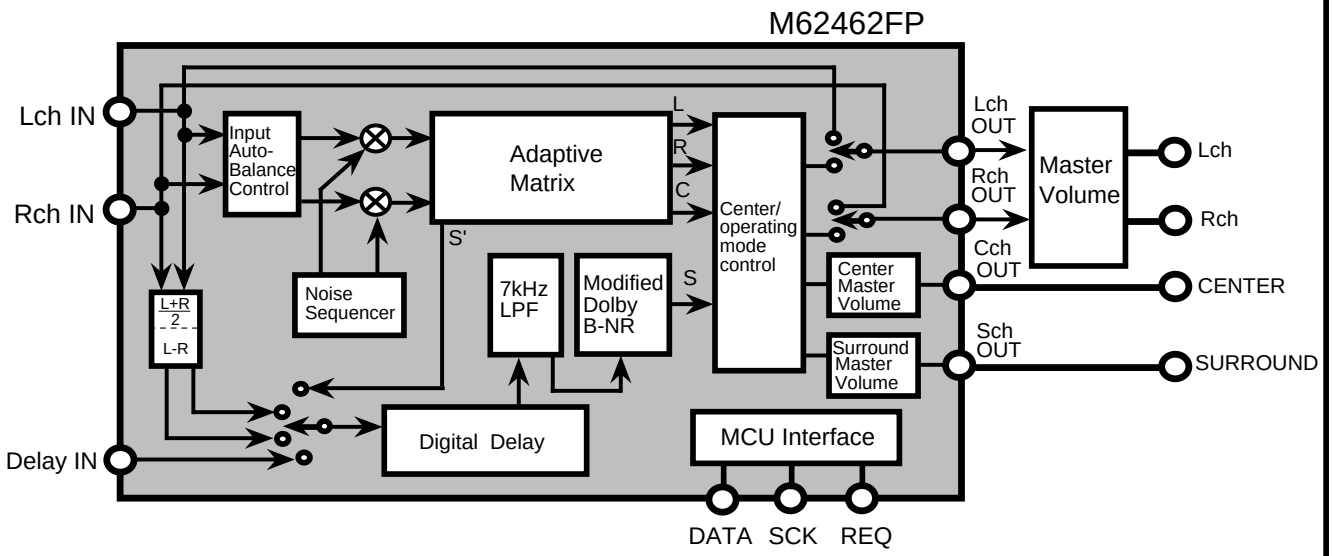


FIG.1 Pin Configuration

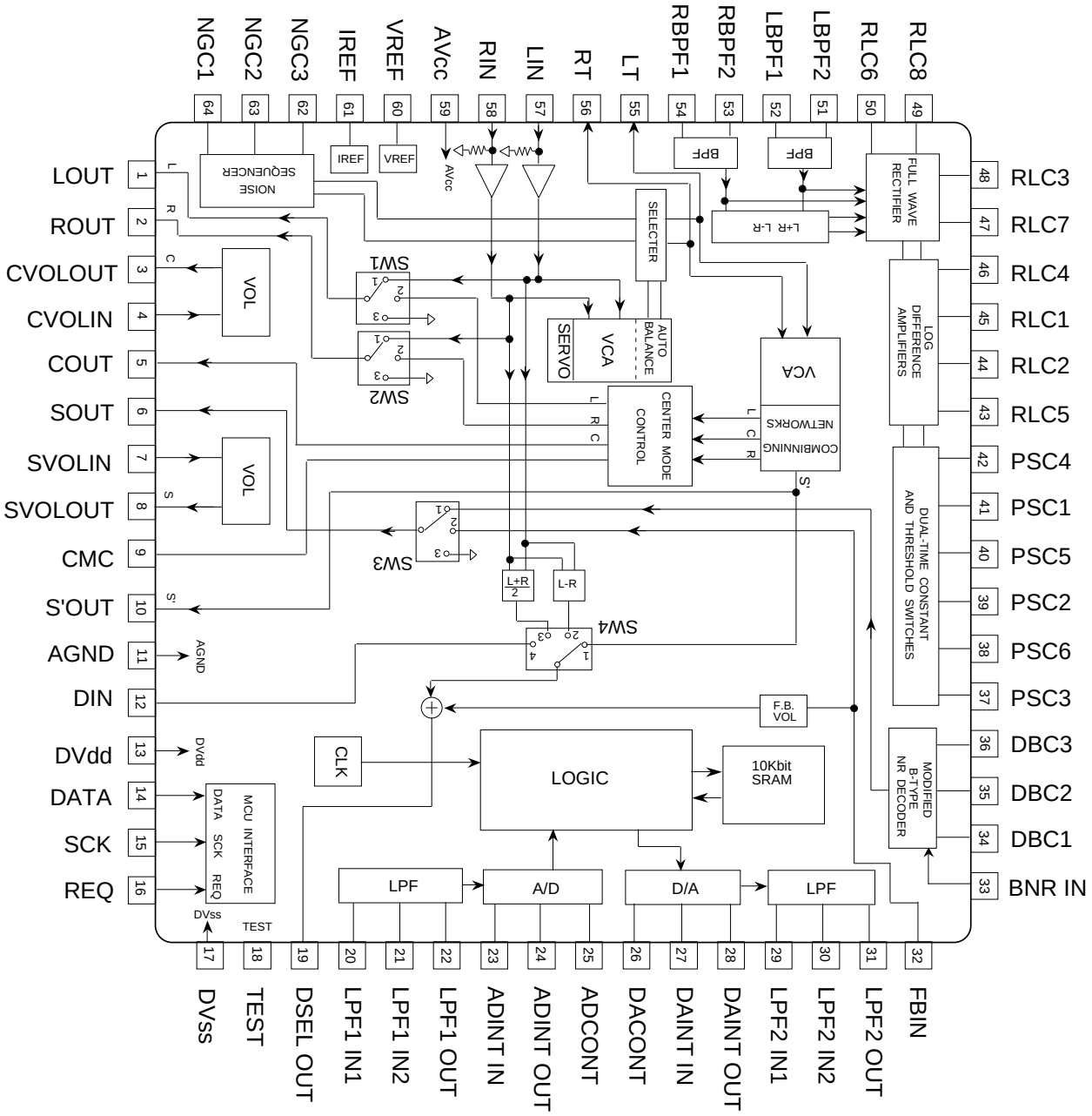
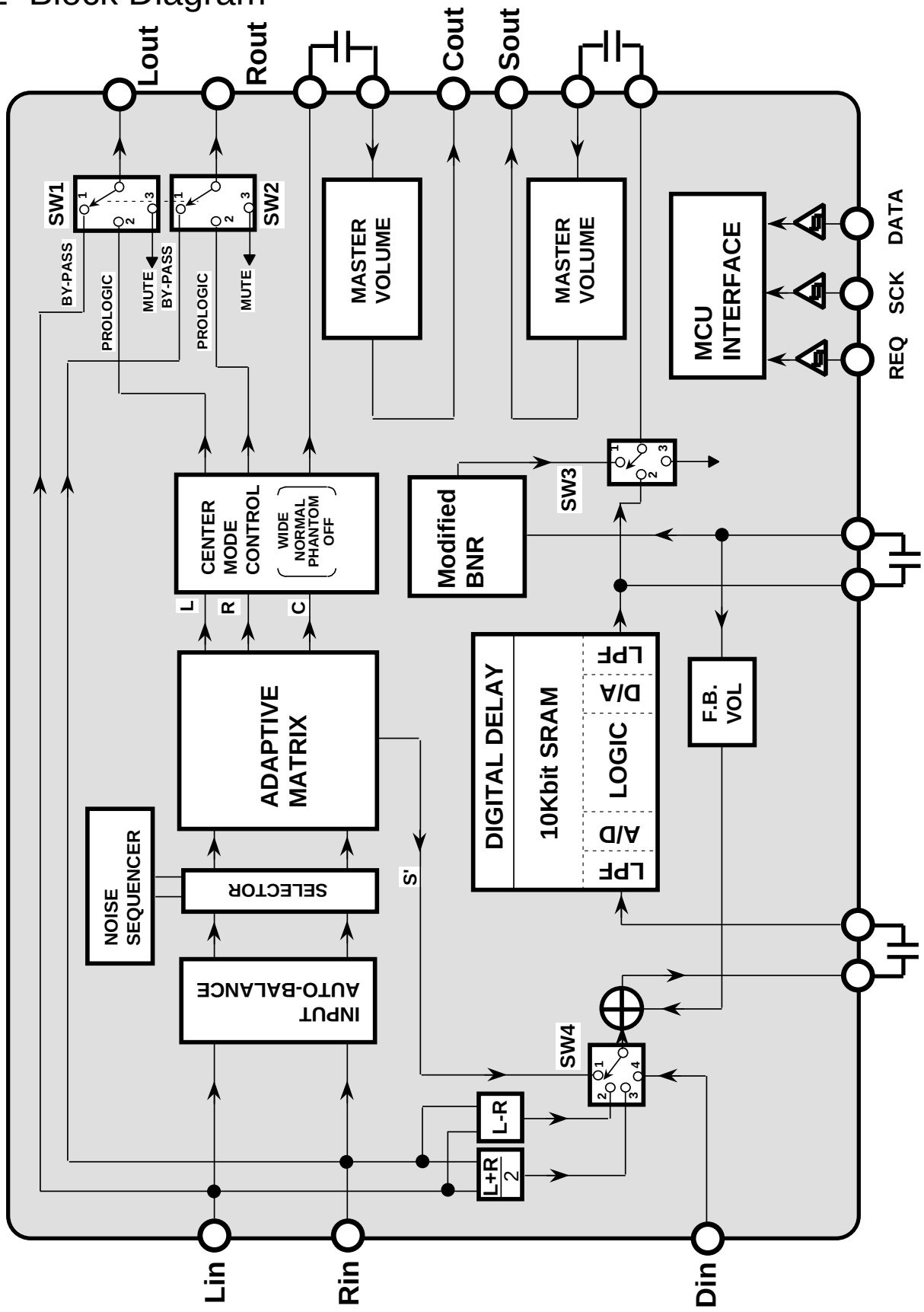


Fig.2 Block Diagram



7.FUNCTIONAL DESCRIPTION

FUNCTION		DESCRIPTION
1	Fundamental function for Dolby Pro Logic Surround Decoder	-Adaptive Matrix -Input Auto-Balance -Noise Sequencer -Center Mode Control ON/OFF WIDE/NORMAL/PHANTOM -Modified Dolby B type Noise Reduction -4ch(L,R,C,S), 3ch(L,R,C) Mode Switch
2	RAM for Digital Delay	10K-bit RAM
3	Surround Delay Time	15.4, 20.5, 25.6, 29.2msec (for Dolby Pro Logic Surround) 51.2msec (for Space Surround)
4	Circuit for Space Surround	Digital delay circuit can be used for Space Surround such as a Disco, Hall or Live.
5	Feedback Volume	Delay Signal Feedback Volume -3 to -21 dB/3dB step, and -∞
6	Cch/Sch Master Volume	0 to -84dB/1dB step, and -∞
7	Bypass Switch	Bypass the decode circuit
8	Output Mute	Mute the Lch and Rch output
9	MCU Interface	Controlled by 3-lines serial data from MCU Including the Chip Address (2 bit)
10	Current control oscillation circuit	Including the oscillation circuit without external parts.

9.ABSOLUTE MAXIMUM RATINGS

(Ta=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply Voltage		10.5	V
VDD			6.5	V
Topr	Operating Temperature		-20 to +75	°C
Tstg	Storage Temperature		-40 to +125	°C

10.RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Condition	Limits			Units
			Min	Typ	Max	
Vcc	Supply Voltage		8	9	10	V
VDD			4.5	5	5.5	V

11.ELECTRICAL CHARACTERISTICS

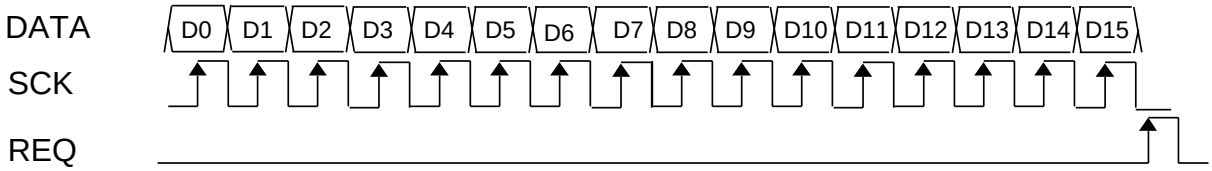
(Ta=25°C,Vcc=9V,V_{DD}=5V ,Cch volume=0dB,at C-OUT 0dBd=300mVrms,f=1kHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
Total						
Icc	Circuit current	No signal		25		mA
I_{DD}	Circuit current	No signal		25		mA
Vref	Reference voltage	No signal		4.0		V
Auto-Balance						
CPR	Capture range			±5		dB
CER	Error collection			±4		dB
Adaptive Matrix						
△VoL	Output level accuracy relative to Cch	L, R, S'ch output		0		dB
MR	Matrix rejection	L, R, C, S'ch output		40		dB
HRAM	Head room	L, R, C, S'output		17		dB
THDAM	Total harmonic distortion	L, R, C, S'ch output 4ch mode		0.05		%
SNAM	S/N ratio	Rg=0Ω,weighted CCIR/ARM 4ch mode		80		dB
Noise Sequencer						
Vno	Output noise level			-12.5		dB
△Vno	Noise level accuracy relative to Cch	L, R, S'ch output		0		dB
Modified B Noise Reduction (Sch Volume=0dB, 0dB reference is 300mVrms/100Hz at S-Out)						
VGNR	Gain between input and output	Vin=0dBd,f=100Hz		-9.2		dB
DEC1	Decode character 1	Vin=0dBd,f=1.0kHz		-0.1		dB
DEC2	Decode character 2	Vin=-15dBd,f=1.4kHz		-1.5		
DEC3	Decode character 3	Vin=-20dBd,f=1.4kHz		-3.4		
DEC4	Decode character 4	Vin=-40dBd,f=5.0kHz		-5.3		
THDNR	Total harmonic distortion	Vin=0dBd,f=1kHz		0.07		%
HRNR	Head room	THD=1%		17		dB
SNNR	S/N ratio	Rg=0Ω, weighted CCIR/ARM		78		dB
C,S ch Master Volume						
ATT_{max}	Maximum attenuator	ATT=-∞		-90		dB
VOLS	Volume step			1.0		dB
Digital Delay						
Gv	Gain between input and output			0		dB
THDD	Total harmonic distortion	Td=20msec,Vin=0dBd		0.3		%
No	Output noise voltage	Td=20msec,Vi=0Vrms,JIS-A		92		dBV
Line(at Dolby Pro Logic is off)						
THDLN	Total harmonic distortion	L,Rch output		0.002		%
SNLN	S/N ratio	L,Rch output		100		dB

12.SERIAL DATA CONTROL FORMAT

Data Input Format

DATA is read at the rising edge of SCK, and loaded last 16 bits at the rising edge of REQ.



D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
L	L	Mode Set		Pro Logic Mode	Center Mode		Sch Volume							Chip Address	
	H	Delay Time			Auto-Balance	set to "L"	Cch Volume								
H	L	Noise Sequencer			Space Surround Mode			Feedback Volume							
	H	Test Mode													

Control condition

	Control Mode	Contents
1	Mode Set	Normal Stereo / Dolby Pro Logic / Space Surround / Mute
2	Pro Logic Mode	4ch Pro Logic / 3ch stereo
3	Delay Time	15.4, 20.5, 25.6, 29.2, 51.2 msec
4	Noise Sequencer	ON / OFF Lch / Rch / Cch / Sch
5	Center Mode	Wide / Normal / Phantom / OFF
6	Auto-Balance	Input Auto-Balance ON / OFF
7	Space Surround Mode	Input to Delay L-R / (L+R)/2 / Din(External) BNR ON / OFF
8	Feedback Volume	-3 to -21dB / 3dB step and -∞
9	Cch/Sch Volume	0 to -84dB / 1dB step and -∞
10	Chip Address	Input data effecte or not

Set Conditions

Mode Setting (D0="L",D1="L")

D2	D3	Condition	Switch		
			SW1	SW2	SW4
L	L	Normal stereo (bypass)	1	1	4
L	H	Dolby Pro Logic Surround	2	2	1
H	L	Space surround	1	1	2to4
H	H	Output Mute	3	3	4

Pro Logic Mode Setting(D0="L",D1="L")

D4	Condition	SW3
L	4ch Pro Logic	1
H	3ch Stereo	3

Center Mode Setting (D0="L",D1="L")

D5	D6	Condition
L	L	Wide
L	H	Normal
H	L	Phantom
H	H	OFF

Delay Time Setting (D0="L,D1="H")

D2	D3	D4	Condition	Sampling frequency
L	L	L	15.4msec	500kHz
L	L	H	20.5msec	500kHz
L	H	L	25.6msec	400kHz
L	H	H	29.2msec	333kHz
H	L	L	51.2msec	200kHz

Auto-Balance Setting (D0="L",D1="H")

D5	Condition
L	Auto-Balance OFF
H	Auto-Balance ON

Noise Sequencer (D0="H",D1="L")

D2	D3	D4	Condition	
L	-	-	Noise Sequencer OFF	
H	L	L	Noise Sequencer ON	Lch
	L	H		Rch
	H	L		Cch
	H	H		Sch

Space Surround Mode (D0="H",D1="L")

D5	D6	D7	Condition		Switch SW3	Switch SW4
L	L	-	Delay input	L-R	-	2
L	H	-		(L+R)/2	-	3
H	L	-		Din(External)	-	4
H	H	-				
-	-	L	BNR OFF		2	-
-	-	H	BNR ON		1	-

Feedback Volume

D8	D9	D10	Volume Level
L	L	L	-3dB
L	L	H	-6dB
L	H	L	-9dB
L	H	H	-12dB
H	L	L	-15dB
H	L	H	-18dB
H	H	L	-21dB
H	H	H	-∞

Chip Address

D14	D15	Data Read
L	H	Enable
Others		Unable

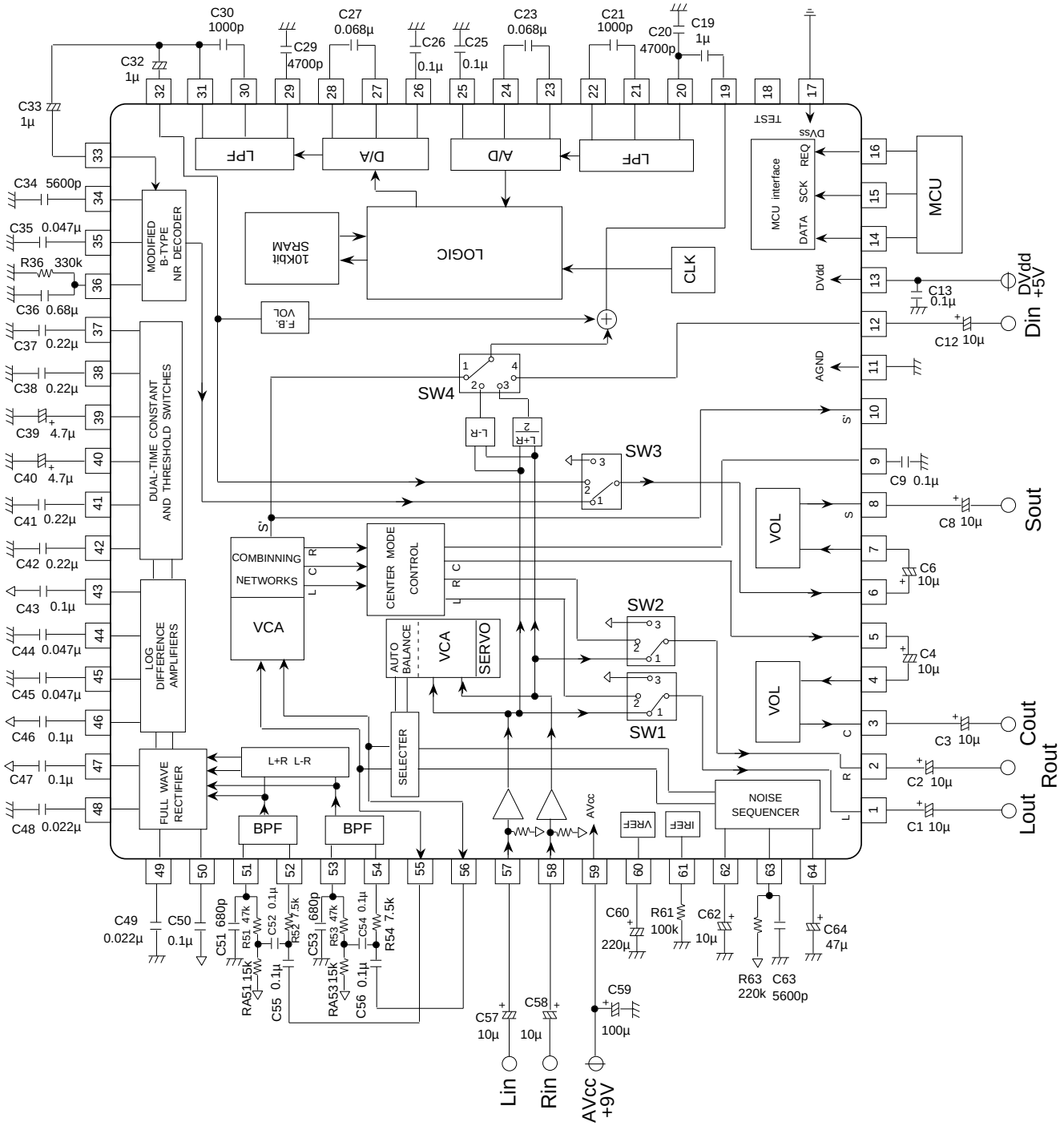
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Sch Volume Setting (D0="L",D1="L")
Cch Volume Setting (D0="L",D1="H")

Volume Level	D7	D8	D9	D10	D11
0 dB	L	L	L	L	L
-2 dB	L	L	L	L	H
-4 dB	L	L	L	H	L
-6 dB	L	L	L	H	H
-8 dB	L	L	H	L	L
-10 dB	L	L	H	L	H
-12 dB	L	L	H	H	L
-14 dB	L	L	H	H	H
-16 dB	L	H	L	L	L
-18 dB	L	H	L	L	H
-20 dB	L	H	L	H	L
-22 dB	L	H	L	H	H
-24 dB	L	H	H	L	L
-26 dB	L	H	H	L	H
-28 dB	L	H	H	H	L
-30 dB	L	H	H	H	H
-32 dB	H	L	L	L	L
-34 dB	H	L	L	L	H
-36 dB	H	L	L	H	L
-40 dB	H	L	L	H	H
-44 dB	H	L	H	L	L
-48 dB	H	L	H	L	H
-52 dB	H	L	H	H	L
-56 dB	H	L	H	H	H
-60 dB	H	H	L	L	L
-64 dB	H	H	L	L	H
-68 dB	H	H	L	H	L
-72 dB	H	H	L	H	H
-76 dB	H	H	H	L	L
-80 dB	H	H	H	L	H
-84 dB	H	H	H	H	L
- ∞	H	H	H	H	H

Volume Level	D12	D13
0 dB	L	L
-1 dB	L	H
-2 dB	H	L
-3 dB	H	H

13.APPLICATION EXAMPLE



14.EXTERNAL PARTS LIST

Parts No.	Values	Unit	Tol.	Parts No.	Values	Unit	Tol.
C1	10	µF		C50	0.1	µF	20%
C2	10	µF		C51	680	pF	5%
C3	10	µF		C52	0.1	µF	5%
C4	10	µF		C53	680	pF	5%
C6	10	µF		C54	0.1	µF	5%
C8	10	µF		C55	0.1	µF	5%
C9	0.1	µF	10%	C56	0.1	µF	5%
C12	10	µF		C57	10	µF	
C13	0.1	µF		C58	10	µF	
C19	1	µF		C59	100	µF	
C20	4700	pF	5%	C60	220	µF	
C21	1000	pF	5%	C62	10	µF	10%
C23	0.068	µF	5%	C63	6800	pF	5%
C25	0.1	µF	5%	C64	47	µF	
C26	0.1	µF	5%				
C27	0.068	µF	5%				
C29	4700	pF	5%				
C30	1000	pF	5%	R36	330	kΩ	10%
C32	1	µF		R51	47	kΩ	5%
C33	1	µF		RA51	15	kΩ	5%
C34	5600	pF	5%	R52	7.5	kΩ	5%
C35	0.047	µF	5%	R53	47	kΩ	5%
C36	0.68	µF	10%	RA53	15	kΩ	5%
C37	0.22	pF	10%	R54	7.5	kΩ	5%
C38	0.22	pF	10%	R61	100	kΩ	1%
C39	4.7	µF	20%	R63	220	kΩ	5%
C40	4.7	µF	20%				
C41	0.22	µF	10%				
C42	0.22	µF	10%				
C43	0.1	µF	20%				
C44	0.047	µF	5%				
C45	0.047	µF	5%				
C46	0.1	µF	20%				
C47	0.1	µF	20%				
C48	0.022	µF	5%				
C49	0.022	µF	5%				