MIC2166

Adaptive On-Time DC-DC Controller

Hyper Speed Control™ Family

General Description

The Micrel MIC2166 is a synchronous adaptive on-time buck controller targeting high-performance, cost-sensitive applications such as set-top boxes, gateways, routers, computing peripherals, and telecom/networking equipment.

The MIC2166 operates over a supply range of 4.5V to 28V. It has an internal linear regulator which provides a regulated 5V supply to power the internal control circuitry. MIC2166 operates at a constant 600kHz switching frequency and can be used to drive up to 25A of output current. The output voltage is adjustable from 0.8V to 5.5V.

A unique Hyper Speed Control™ architecture enables ultra-fast transient response while reducing the output capacitance and also makes High V_{IN}/Low V_{OUT} operation possible.

A UVLO feature is provided to ensure proper operation under power-sag conditions to prevent the external power MOSFET from over heating. Also, a soft-start feature is provided to reduce the inrush current. Short current sensing on the bottom MOSFET with hiccup mode current limiting ensures protection in case of an output short circuit. Further, the MIC2166 includes an EN pin to shut down the converter and a Power-Good (PGOOD) pin to allow simple sequencing.

The MIC2166 is available in a 10 pin MSOP ePad package with a junction operating temperature ranging from –40°C to +125°C. All support documentation can be found on Micrel's web site at: www.micrel.com.

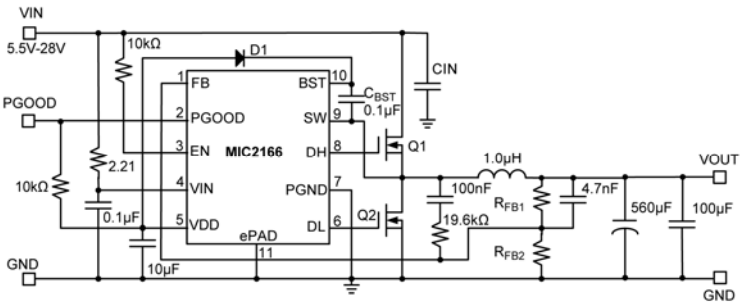
Features

- Hyper Speed Control™ architecture enables
  - High delta V operation (V_{IN}=28V and V_{OUT}=0.8V)
  - Small output capacitance
- Built-in 5V regulator for single-supply operation
- Any Capacitor™ stable
  - Zero ESR to high ESR
- Power-Good (PGOOD) output
- Input voltage range: 4.5V to 28V
- 5µA typical shutdown current
- 25A output current drive capability
- Adjustable output from 0.8V to 5.5V with ±1% FB accuracy
- 600kHz switching frequency
- Internal 5ms digital soft-start
- Thermal-shutdown and hiccup current-limit protection
- No external current-sense resistor required
- Safe start-up into pre-biased loads
- 10-pin MSOP ePad package
- –40°C to +125°C junction temperature range

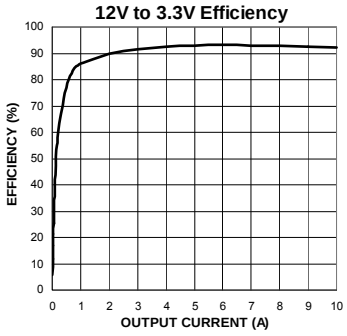
Applications

- Set-top box, gateways, routers and DSL modems
- Printers, scanners, graphic and video cards
- Servers, PCs and processor core supply
- Low-Voltage Distributed Power

Typical Application



MIC2166 Adjustable Output 600kHz Buck Converter

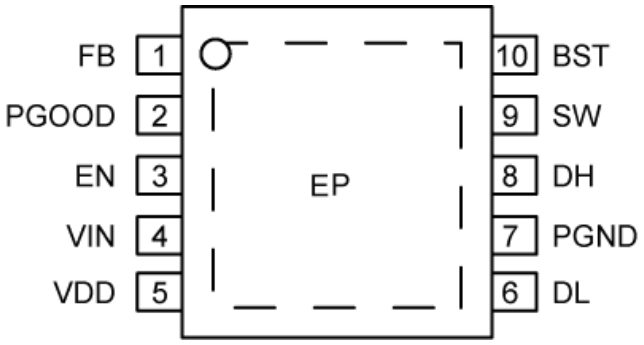


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Ordering Information

Part Number	Voltage	Switching Frequency	Junction Temperature Range	Package	Lead Finish
MIC2166YMME	Adjustable	600kHz	–40° to +125°C	10-pin ePad MSOP	Pb-Free

Pin Configuration



10-Pin ePad MSOP (MME)

Pin Description

Pin Number	Pin Name	Pin Function
1	FB	Feedback (Input): Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider the output an FB is used to set the desired output voltage.
2	PGOOD	Power Good (Output): Open Drain Output. The PGOOD pin is externally tied with a resistor to VDD. High output when V_{OUT}>90% nominal.
3	EN	Enable (Input): A logic level control of the output. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the off state, supply current of the device is greatly reduced (typically 5µA). The EN pin should not be left open. Connect to VIN if sequencing is not required.
4	VIN	Supply Voltage: Input voltage for the internal +5V linear regulator. The VIN operating voltage range is from 4.5V to 28V. A 0.1µF capacitor between VIN and the ground is required.
5	VDD	5V Internal Linear Regulator (Output): VDD is the external MOSFET gate drive supply voltage and an internal supply bus for the IC. VDD is created by internal LDO from VIN. When VIN <+5.5V, VDD Should be tied to VIN. A 2.2µF (minimum) ceramic capacitor from VDD to GND is recommended for clean operation.
6	DL	Low-Side Gate Drive (Output): High-current driver output for external low-side MOSFET. The DL driving voltage swings from ground to VDD.
7	PGND	Power Ground. PGND is the ground path for the MIC2166 buck converter power stage. The PGND pin connects to the sources of low-side N-Channel MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the Signal ground (GND) loop.
8	DH	High-Side Gate Drive (Output): High-current driver output for external high-side MOSFET. The DH driving voltage is floating on the switch node voltage (SW). It swings from ground-to-VDD minus the diode drop.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
9	SW	Switch Node (Input): High current output driver return. The SW pin connects directly to the switch node. Due to the high speed switching on this pin, the SW pin should be routed away from sensitive nodes. Current Sense (Input): SW pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF-time. The current sensing is necessary for short circuit protection. In order to sense the current accurately, connect the low-side MOSFET drain to SW using a Kelvin connection.
10	BST	Boost (Output): Bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the VDD pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the SW pin. Adding a small resistor at BST pin can slow down the turn-on time of high-side N-Channel MOSFETs.
EP	GND	Thermal Pad and Signal ground. GND is the ground path for VDD and the control circuitry. The loop for the signal ground should be separate from the power ground (PGND) loop.

Absolute Maximum Ratings[1]

V_{IN} to GND ..... –0.3V to +29V
V_{DD}, V_{FB}, V_{PGOOD} to GND ..... –0.3V to +6V
V_{BST} to V_{SW} ..... –0.3V to +6V
V_{BST} to GND ..... –0.3V to +35V
V_{EN} to GND ..... –0.3V to (V_{IN}+0.3V)
V_{DH} to V_{SW} ..... –0.3V to (V_{BST} + 0.3V)
V_{DL} to GND ..... –0.3V to (V_{DD} + 0.3V)
PGND to GND ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10sec) ..... 260°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... 4.5V to 28V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}
Junction Temperature (T_J) ..... –40°C to +125°C
Package Thermal Resistance [3]
MSOP-10L ePad (θ_{JA}) ..... 77°C/W
MSOP-10L ePad (θ_{JC}) ..... 10°C/W

Electrical Characteristics

V_{IN} = V_{EN}= 12V; V_{BST} – V_{SW} = 5V; T_J = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ 125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Input Supply					
Input Voltage Range (V_{IN})		**4.5**		**28**	V
Quiescent Supply Current	V_{FB} = 1.5V (non-switching)		950	**1500**	µA
Shutdown Current	V_{EN} = 0V		5	**10**	µA
VDD Supply					
VDD Output Voltage	V_{IN} = 7V to 28V, I_{DD} = 40mA	**4.8**	5.2	**5.4**	V
VDD UVLO Threshold	V_{DD} rising	**3.7**	4.2	**4.5**	V
VDD UVLO Hysteresis			400		mV
Dropout Voltage (V_{IN} - V_{DD})	I_{DD} = 25mA		380	**600**	mV
DC-DC Controller					
Output-Voltage Adjust Range (V_{OUT})		**0.8**		**5.5**	V
Reference					
Feedback Regulation Voltage	T_J = 25°C	0.792	0.8	0.808	V
	0°C ≤ T_J ≤ 85°C	**0.788**		**0.812**	V
	–40°C ≤ T_J ≤ 125°C	**0.784**		**0.816**	V
Load Regulation	I_{OUT} = 0A to 10A Depends on external components		0.25		%
Line Regulation	V_{IN} = 4.5V to 28V Depends on external components		0.25		%
FB Bias Current	V_{FB} = 0.8V		50	**500**	nA
Enable Control [5]					
Enable Logic Level High		**1.6**			V
Enable Logic Level Low				**0.6**	V
Enable Hysteresis			100		mV
Enable Bias Current	V_{EN} = 12V		6	**30**	µA

Electrical Characteristics (Continued)

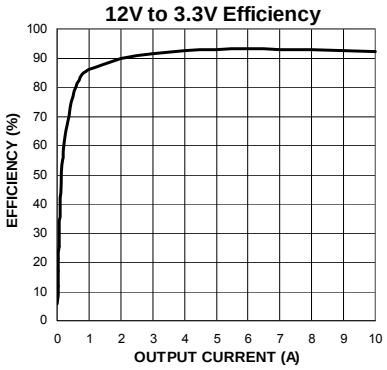
$V_{IN} = V_{EN}$= 12V; $V_{BST} – V_{SW}$ = 5V; T_J = 25°C, unless noted. Bold values indicate –40°C ≤ T_J ≤ 125°C.

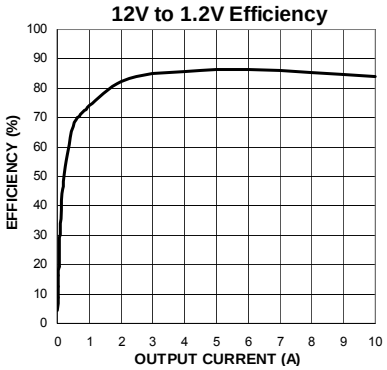
Parameter	Condition	Min	Typ	Max	Units
On Timer					
Switching Frequency		**450**	600	**750**	kHz
Minimum Off-Time		**200**	300	**400**	ns
Maximum Duty Cycle	Results from Switching Frequency and Minimum Off-Time		82		%
Minimum Duty Cycle	V_{FB} = 1.0V		0		%
Short Current Protection					
Current-Limit Threshold	V_{FB} = 0.79V	**98**	133	**182**	mV
Short-Circuit Current	V_{FB} = 0V	**24**	48	**72**	mV
FET Drives					
DH, DL Output Low Voltage	I_{SINK} = 10mA			**0.1**	V
DH, DL Output High Voltage	I_{SOURCE} = 10mA	**V_{DD} – 0.1V or V_{BST} – 0.1V**			V
DH On-Resistance	Pull Up, I_{SOURCE} = 20mA		2	**3**	Ω
	Pull Down, I_{SINK} = 20mA		1.5	**3**	Ω
DL On-Resistance	Pull Up, I_{SOURCE} = 20mA		2	**3**	Ω
	Pull Down, I_{SINK} = 20mA		1	**2**	Ω
SW, BST Leakage Current	$V_{SW} = V_{BST}$ = 0			**30**	µA
Power Good (PGOOD)					
PGOOD Threshold Voltage	Sweep V_{FB} from Low-to-High	**85**	90	**95**	$\%V_{OUT}$
PGOOD Hysteresis	Sweep V_{FB} from High-to-Low		6.0		$\%V_{OUT}$
PGOOD Delay Time	Sweep V_{FB} from Low-to-High		100		µs
PGOOD Low Voltage	$V_{FB} < 0.9 \times V_{NOM}$, I_{PGOOD} = 1mA		70	**200**	mV
Thermal Protection					
Over-temperature Shutdown	T_J Rising		160		°C
Over-temperature Shutdown Hysteresis			15		°C

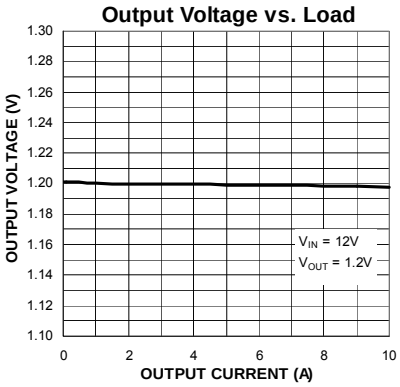
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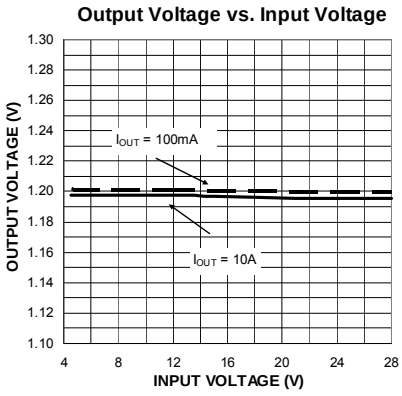
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
5. Enable pin should not be left open.

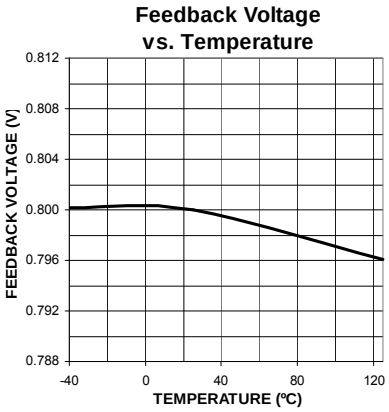
Typical Characteristics

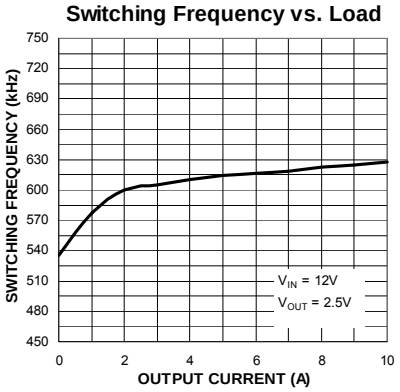


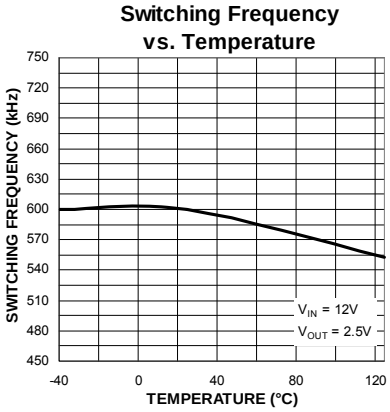


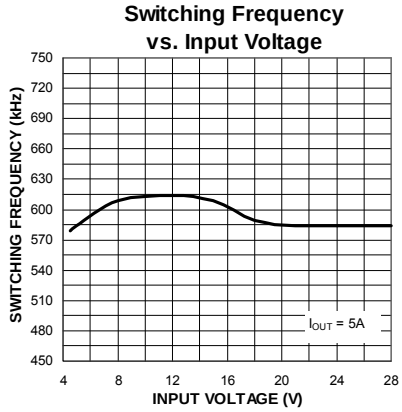


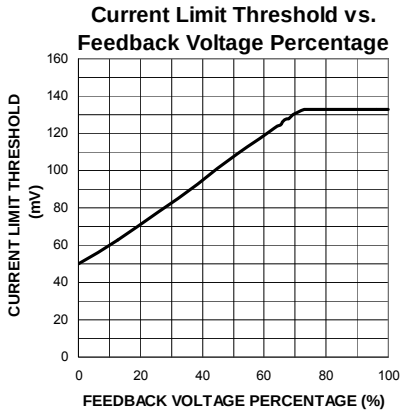




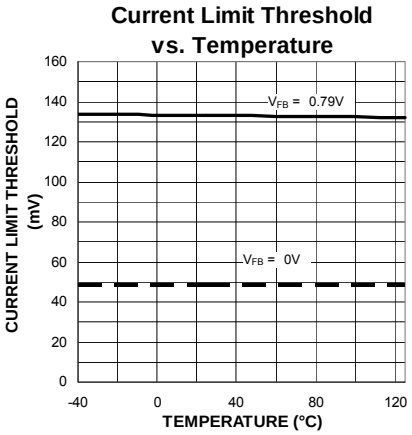


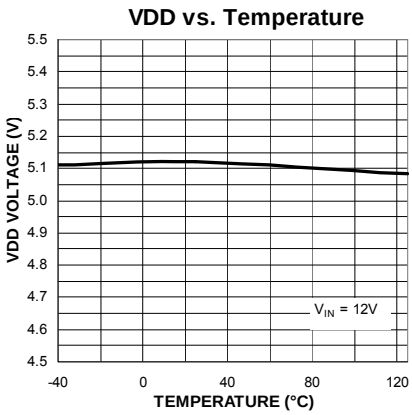


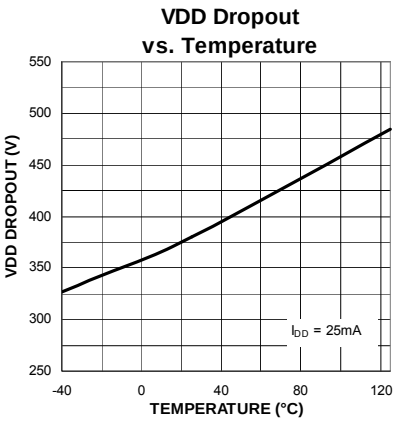


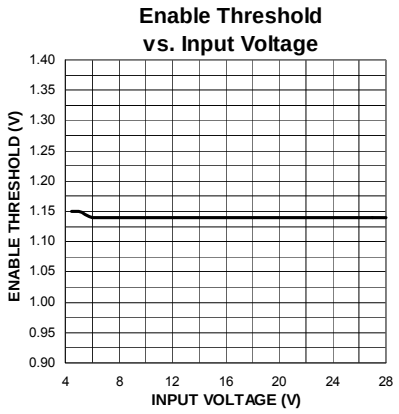


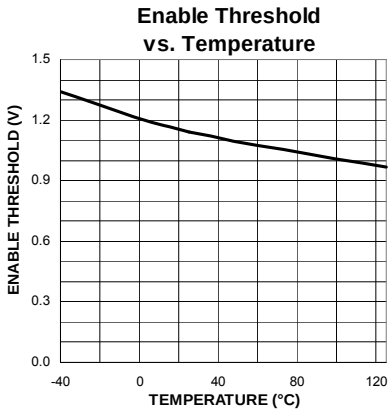
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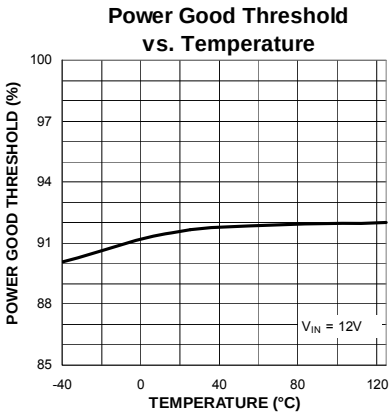


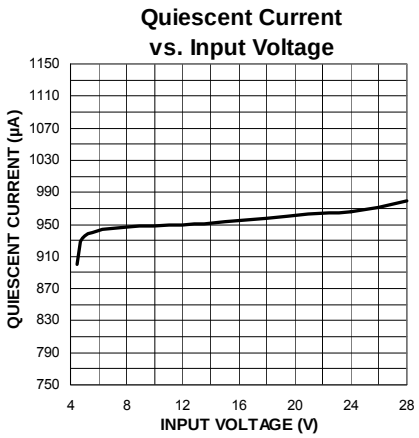


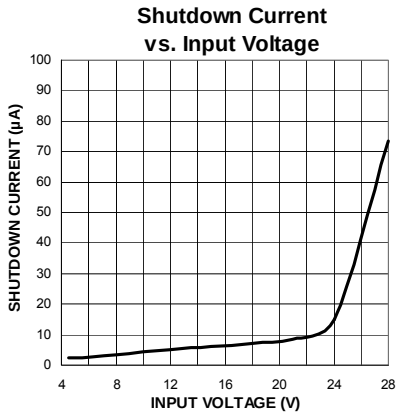


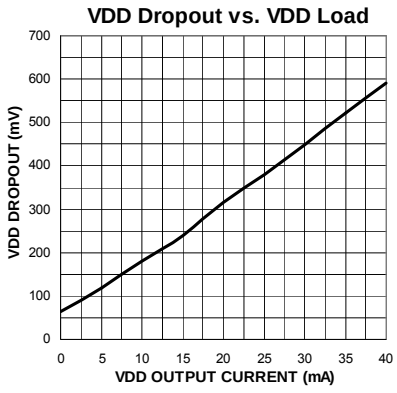






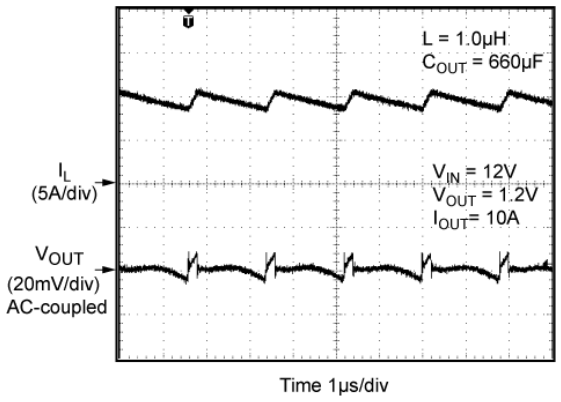




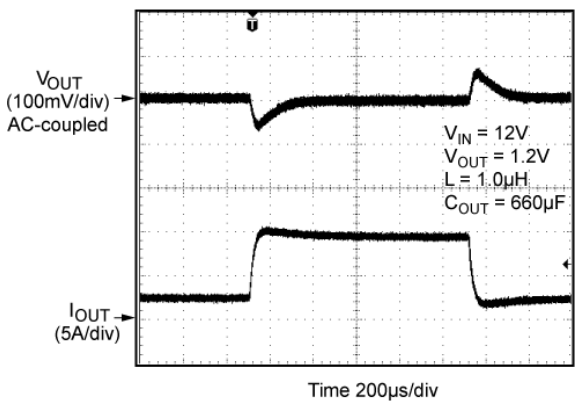


Functional Characteristics

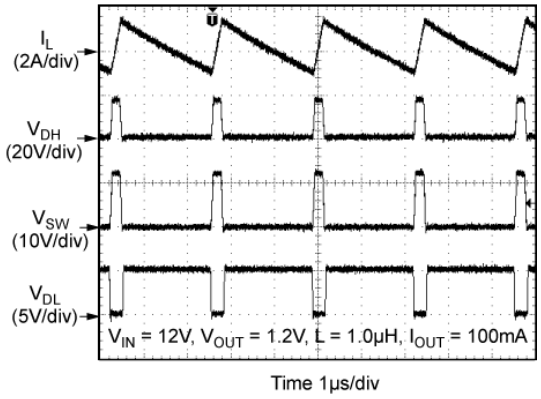
Output Voltage Ripple



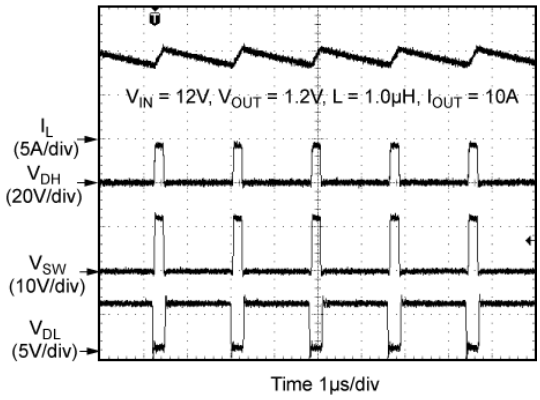
Load Transient (2.5A to 10A)



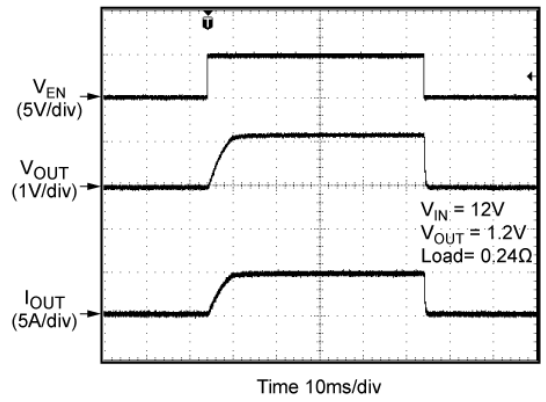
Switching Waveform (Light Load)



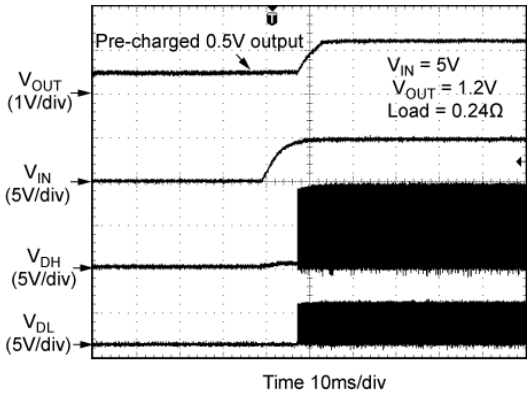
Switching Waveform (Heavy Load)



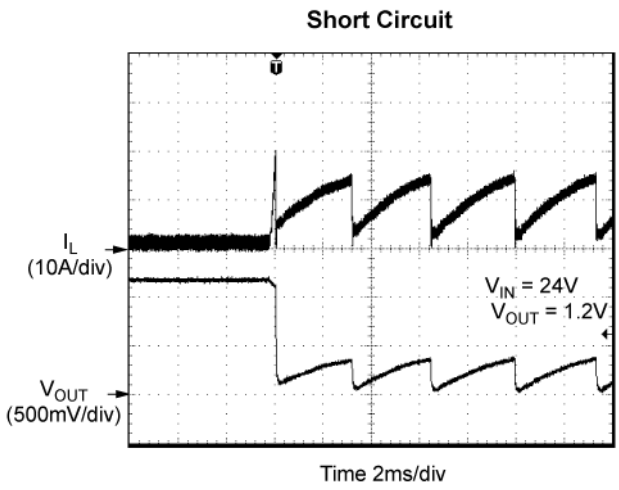
Power-Up/Power-Down

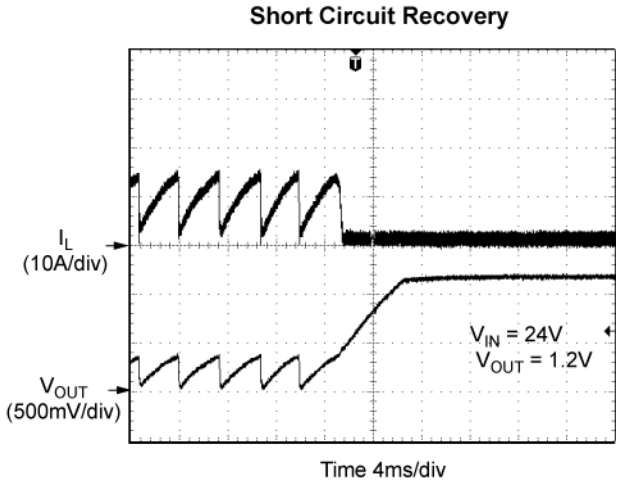


Start-Up with Prebias VOUT



Functional Characteristics (Continued)





Functional Diagram

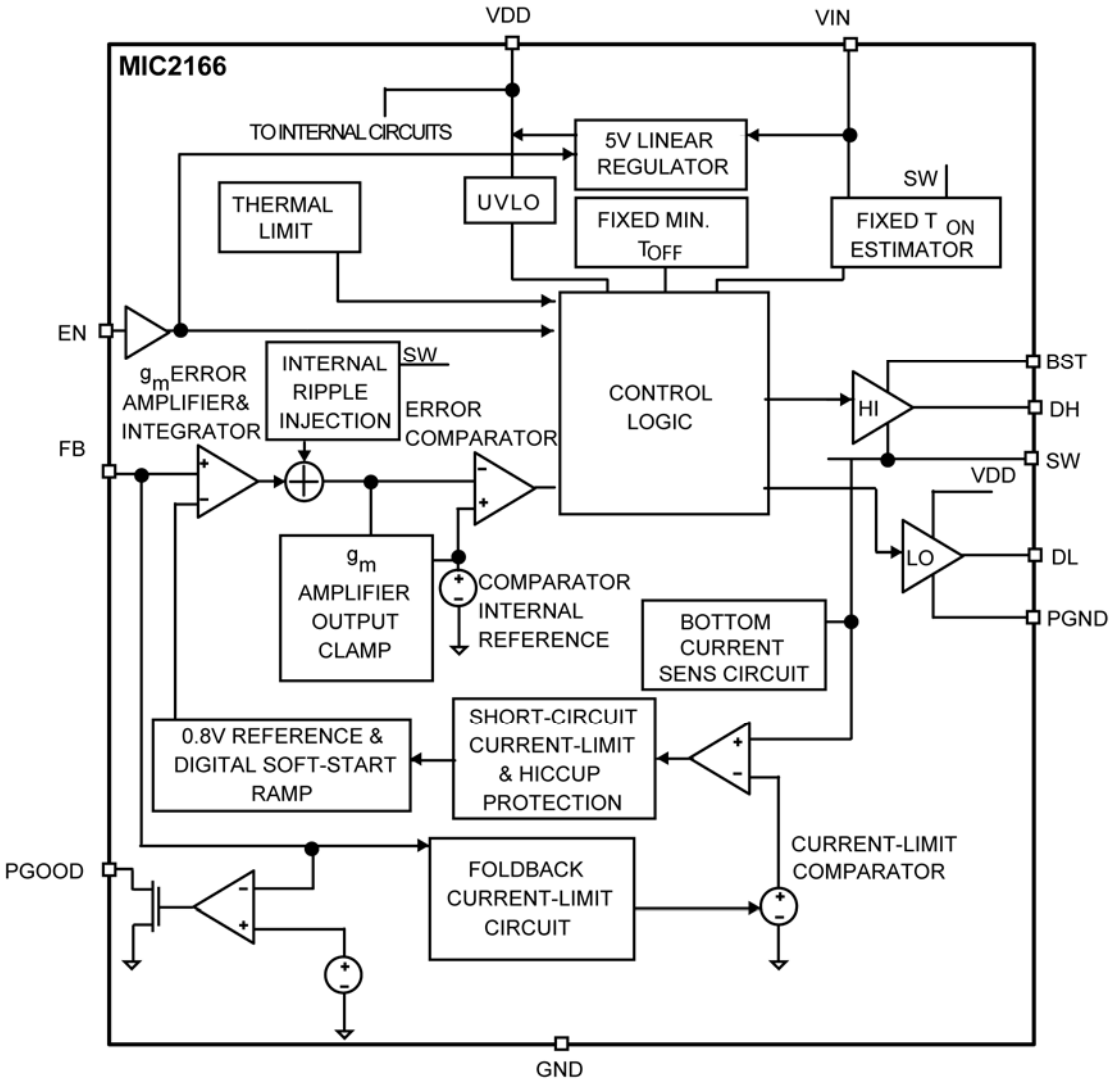


Figure 1. MIC2166 Block Diagram

Functional Description

The MIC2166 is an adaptive on-time buck controller built for low cost and high performance. Featuring an internal 5V linear regulator and Power-Good (PGOOD) output, it is designed for a wide input voltage range from 4.5V to 28V, high output power buck converters. An estimated ON-time method is used in the MIC2166 to obtain a constant switching frequency and to simplify the control compensation. Over-current protection is implemented without the use of an external sense resistor. It includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

Theory of Operation

The MIC2166 is an adaptive on-time buck controller. Figure 1 illustrates the block diagram for the control loop.

The output voltage variation will be sensed by the MIC2166 feedback pin FB via the voltage divider. The FB voltage V_{FB} is compared to a 0.8V reference voltage V_{REF} at the error comparator through a low gain transconductance (g_m) amplifier at switching frequency. This g_m amplifier improves the MIC2166 converter output voltage regulation. If the FB voltage V_{FB} decreases and the output of the g_m amplifier is below 0.8V, The error comparator will trigger the control logic and generate an ON-time period, in which DH pin is logic high and DL pin is logic low. The ON-time period length is predetermined by the "Fixed T_{ON} Estimator" circuitry:

$$T_{ON(estimated)} = \frac{V_{OUT}}{V_{IN} \times f_{sw}} \quad (1)$$

where V_{OUT} is the output voltage, V_{IN} is the power stage input voltage, and f_{SW} is the switching frequency (600kHz for MIC2166).

After an ON-time period, the MIC2166 goes into the OFF-time period, in which DH pin is logic low and DL pin is logic high. The OFF-time period length depends on V_{FB} in most cases. When V_{FB} decreases and the output of the g_m amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by V_{FB} is less than the minimum OFF time $T_{OFF(min)}$, which is about 300ns typical, then the MIC2166 control logic will apply the $T_{OFF(min)}$ instead. $T_{OFF(min)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET. The maximum duty-cycle is obtained from the 300ns $T_{OFF(min)}$:

$$D_{MAX} = \frac{T_S - T_{OFF(min)}}{T_S} = 1 - \frac{300ns}{T_S}$$

where $T_S = 1/f_{SW}$. It is not recommended to use MIC2166 with a OFF-time close to $T_{OFF(min)}$ during steady state operation. Also, as V_{OUT} increases, the internal ripple injection will increase and reduce the line regulation performance. Therefore, the maximum output voltage of the MIC2166 should be limited to 5.5V. Please refer to "Setting Output Voltage" subsection in "Application Information" for more details.

The estimated ON-time method results in a constant switching frequency in the MIC2166. The actual ON-time varies slightly with the different rising and falling times of the external MOSFETs. Therefore, the type of the external MOSFETs and the output load current will modify the actual ON-time and the switching frequency. Also, the minimum T_{ON} results in a lower switching frequency in high V_{IN} and low V_{OUT} applications, such as 24V to 1.0V. The minimum T_{ON} measured on the MIC2166 evaluation board is about 100ns. During the load transient, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop, the steady-state and load-transient scenarios are analyzed. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as V_{FB}. Figure 2 shows the MIC2166 control loop timing during steady-state operation. During steady-state, the g_m amplifier senses V_{FB} ripple, which is proportional to the output voltage (V_{OUT}) ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the estimation. The ending of OFF-time is controlled by V_{FB}. At the valley of V_{FB} ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

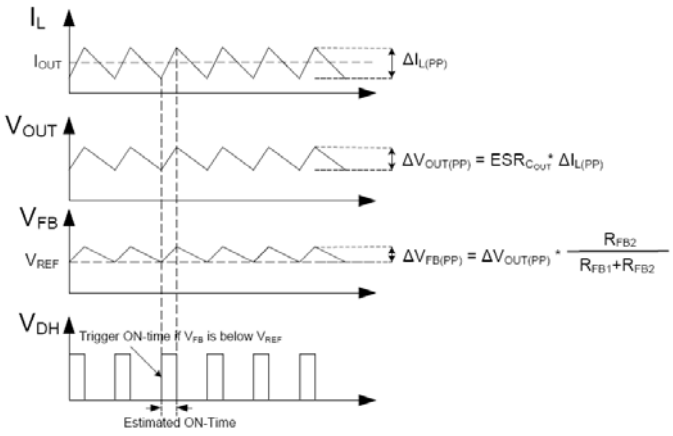


Figure 2. MIC2166 Control Loop Timing

Figure 3 shows the load transient operation of the MIC2166 converter. The output voltage drops due to the sudden load increase, which causes V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $T_{OFF(min)}$ is generated to charge C_{BST} since V_{FB} is still below V_{REF}. Then, the next ON-time period is triggered due to the low V_{FB}. Therefore, the switching frequency changes during the load transient. With the varying duty-cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC2166 converter.

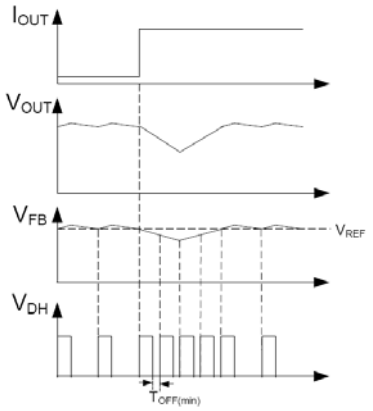


Figure 3. MIC2166 Load-Transient Response

Unlike in current-mode control, the MIC2166 uses the output voltage ripple, which is proportional to the inductor current ripple if the ESR of the output capacitor is large enough, to trigger an ON-time period. The predetermined ON-time makes MIC2166 control loop have the advantage of constant ON-time mode control and eliminates the need for slope compensation.

The MIC2166 has its own stability concern: V_{FB} ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended V_{FB} ripple is 20mV~100mV. If a low ESR output capacitor is selected, the V_{FB} ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the V_{OUT} ripple and the V_{FB} ripple are not in phase with the inductor current ripple if the ESR of the output capacitor is very low. Therefore, ripple injection is required for a low ESR output capacitor. Please refer to "Ripple Injection" subsection in "Application Information" for more details.

Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC2166 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 5ms. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{REF} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption.

Current Limit

The MIC2166 uses the $R_{DS(ON)}$ of the low-side power MOSFET to sense over-current conditions. This method will avoid adding cost, board space and power losses taken by discrete current sense resistors. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC2166 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage is compared with a current-limit threshold voltage V_{CL} after a blanking time of 150ns. If the sensed voltage is over V_{CL}, which is 133mV typical at 0.8V V_{FB}, then the MIC2166 turns off the high-side and low-side MOSFETs and a soft-start sequence is triggered. This mode of operation is called "hiccup mode" and its purpose is to protect the downstream load in case of a hard short. The current limit threshold V_{CL} has a back fold characteristic related to the FB voltage. Please refer to the "Typical Characteristics" for the curve of current limit threshold vs. FB voltage percentage. The circuit in Figure 4 illustrates the MIC2166 current limiting circuit.

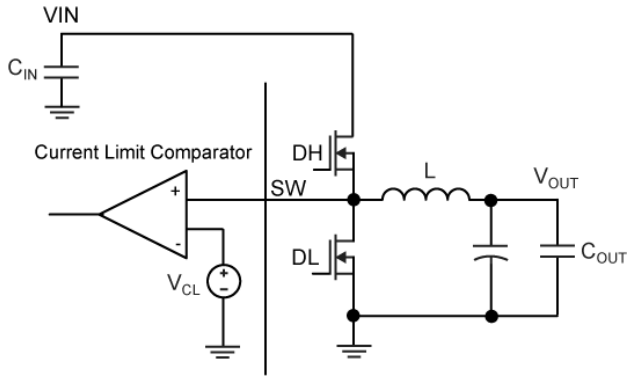


Figure 4. MIC2166 Current Limiting Circuit

Using the typical V_{CL} value of 133mV, the current limit value is roughly estimated as:

$$I_{CL} \approx \frac{133mV}{R_{DS(ON)}}$$

For designs where the current ripple is significant compared to the load current I_{OUT}, or for low duty-cycle operation, calculating the current limit I_{CL} should take into account that one is sensing the peak inductor current and that there is a blanking delay of approximately 150ns.

$$I_{CL} = \frac{133mV}{R_{DS(ON)}} + \frac{V_{OUT} \times t_{DLY}}{L} - \frac{\Delta I_{L(PP)}}{2} \quad (2)$$

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (1 - D)}{f_{SW} \times L} \quad (3)$$

where:

V_{OUT} = Output voltage

t_{DLY} = Current-limit blanking time, 150ns typical

$\Delta I_{L(PP)}$ = Inductor current ripple peak-to-peak value

D = Duty Cycle

f_{SW} = Switching frequency

The MOSFET $R_{DS(ON)}$ varies between 30% to 40% with temperature; therefore, it is recommended to add 50% margin to I_{CL} in the above equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect SW pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$.

MOSFET Gate Drive

The MIC2166 high-side drive circuit is designed to switch an N-Channel MOSFET. The typical application schematic shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reversed biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e., ΔBST = 10mA x 1.67µs/0.1µF = 167mV. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G at BST pin can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the internal linear regulator V_{DD}. The nominal low-side gate drive voltage is V_{DD} and the nominal high-side gate drive voltage is approximately $V_{DD} – V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. A dead-time of approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Application Information

MOSFET Selection

The MIC2166 controller works from an input voltage of 4.5V to 28V and has an internal 5V V_{DD} supply to provide power to turn the external N-Channel power MOSFETs for the high-side and low-side switches. For applications where V_{IN} < 5.5V, it is recommended to connect VDD-to-VIN to bypass the internal linear regulator. The external power MOSFETs should be logic-level MOSFETs, whose operation is specified at V_{GS} = 4.5V.

There are different criteria for choosing the high-side and low-side MOSFETs. These differences are more significant at lower duty cycles such as 24V to 1.2V conversion. In such an application, the high-side MOSFET is required to switch as quickly as possible to minimize transition losses, whereas the low-side MOSFET can switch slower, but must handle larger RMS currents. When the duty-cycle approaches 50%, the on-resistance of the high-side MOSFET starts to become critical.

It is important to note that the on-resistance of a MOSFET increases with increasing temperature. For a MOSFET with a 0.4%/°C thermal coefficient a 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 30% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and the value of current limit. Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2166 gate-drive circuit. At 600kHz switching frequency, the gate charge can be a significant source of power dissipation in the MIC2166. At light output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

$$I_{G[HS]}(avg) = Q_G \times f_{SW} \quad (4)$$

where:

$I_{G[HS]}$(avg) = Average High-Side (HS) MOSFET gate current

Q_G = Total gate charge for the high-side MOSFET taken from the manufacturer's data sheet for V_{GS} = V_{DD}.

f_{SW} = Switching Frequency

The low-side MOSFET is turned on and off at V_{DS} = 0V because an internal body diode or external freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at V_{DS} = 0 instead of gate charge.

For the Low-Side (LS) MOSFET:

$$I_{G[LS]}(avg) = C_{ISS} \times V_{GS} \times f_{SW} \quad (5)$$

Since the current from the gate drive comes from the V_{DD}, which is the output of the internal linear regulator power by V_{IN}, the power dissipated in the MIC2166 due to gate drive is:

$$P_{GATEDRIVE} = V_{IN} \times (I_{G[high\text{-}side]}(avg) + I_{G[low\text{-}side]}(avg)) \quad (6)$$

A convenient figure of merit for switching MOSFETs is the on-resistance times the total gate charge ($R_{DS(ON)}$ × Q_G). Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2166. Also, the $R_{DS(ON)}$ of the low-side MOSFET will determine the current limit value. Please refer to "Current Limit" subsection is "Functional Description" for more details.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage V_{IN}. A safety factor of 20% should be added to the V_{DS}(max) of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the MOSFETs is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{SW} = P_{CONDUCTION} + P_{AC} \quad (7)$$

$$P_{CONDUCTION} = I_{SW(RMS)}^{2} \times R_{DS(ON)} \quad (8)$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)} \quad (9)$$

where:

$R_{DS(ON)}$ = on-resistance of the MOSFET switch

D = Duty Cycle = V_{OUT} / V_{IN}

Making the assumption that the turn-on and turn-off transition times are equal; the transition times can be approximated by:

$$t_T = \frac{C_{ISS} \times V_{DD} + C_{OSS} \times V_{IN}}{I_G} \quad (10)$$

where:

C_{ISS} and C_{OSS} are measured at V_{DS} = 0

I_G = gate-drive current

The total high-side MOSFET switching loss is:

$$P_{AC} = (V_{IN} + V_D) \times I_{PK} \times t_T \times f_{SW} \quad (11)$$

where:

t_T = Switching transition time

V_D = Diode drop

f_{SW} = Switching Frequency

The high-side MOSFET switching losses increase with the switching frequency and the input voltage V_{IN}. The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by equation 12:

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{SW} \times 20\% \times I_{OUT(max)}} \quad (12)$$

where:

f_{SW} = switching frequency

20% = ratio of AC ripple current to DC output current

$V_{IN(max)}$ = maximum power stage input voltage

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{SW} \times L} \quad (13)$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(PK)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(PP)} \quad (14)$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

$$I_{L(RMS)} = \sqrt{I_{OUT(max)}^2 + \frac{\Delta I_{L(PP)}^2}{12}} \quad (15)$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high-frequency operation of the MIC2166 requires the use of ferrite materials for all but the most cost sensitive applications.

Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by the equation below:

$$P_{INDUCTORCu} = I_{L(RMS)}^2 \times R_{WINDING} \quad (16)$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

$$R_{WINDING} = R_{WINDING(20°C)} \times (1+ 0.0042 \times (T_H - T_{20°C})) \quad (17)$$

where:

T_H = temperature of wire under full load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

Output Capacitor Selection

The type of the output capacitor is usually determined by its ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitors are tantalum, low-ESR aluminum electrolytic, OS-CON, POSCAPS, and ceramic. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(pp)}}{\Delta I_{L(PP)}} \quad (18)$$

where:

$\Delta V_{OUT(PP)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated below:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2} \quad (19)$$

where:

C_{OUT} = output capacitance value

f_{SW} = switching frequency

As described in the "Theory of Operation" subsection in "Functional Description", MIC2166 requires at least 20mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator to behavior properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitor C_{OUT} should be much smaller than the ripple caused by the output capacitor ESR. If low ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough FB voltage ripples. Please refer to the "Ripple Injection" subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated below:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \quad (20)$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}^2 \times ESR_{C_{OUT}} \quad (21)$$

Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning on a "hot-plugging". A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend upon the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{C_{IN}} \quad (22)$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{C_{IN}(RMS)} \approx I_{OUT(max)} \times \sqrt{D \times (1 - D)} \quad (23)$$

The power dissipated in the input capacitor is:

$$P_{DISS(C_{IN})} = I_{C_{IN}(RMS)}^2 \times ESR_{C_{IN}} \quad (24)$$

External Schottky Diode (Optional)

An external freewheeling diode can be used to keep the inductor current flow continuous while both MOSFETs are turned off.

The diode conducts current during the dead-time. The dead-time prevents current from flowing unimpeded through both MOSFETs and is typically 30ns. The diode conducts twice during each switching cycle. Although the average current through this diode is small, the diode must be able to handle the peak current.

$$I_{D(avg)CM} = I_{OUT} \times 2 \times 30ns \times f_{SW} \quad (25)$$

The reverse voltage requirement of the diode is:

$$V_{DIODE(rrm)} = V_{IN}$$

The power dissipated by the Schottky diode is:

$$P_{DIODE} = I_{D(avg)} \times V_F \quad (26)$$

where, V_F = forward voltage at the peak diode current.

An external Schottky diode is recommended, even though the low-side MOSFET contains a parasitic body diode since the Schottky diode has much less forward voltage than the body diode. The external diode will improve efficiency and reduce the high frequency noise. If the MOSFET body diode is used, it must be rated to handle the peak and average current. The body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn-on.

An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and less power loss.

Snubber Design

A snubber is used to damp out high frequency ringing caused by parasitic inductance and capacitance in the buck converter circuit. Figure 5 shows a simplified schematic of the buck converter. Stray capacitance consists mostly of the two MOSFETs' output capacitance (C_{OSS}). The stray inductance consists mostly package inductance and trace inductance. The arrows show the resonant current path when the high side MOSFET turns on. This ringing causes stress on the semiconductors in the circuit as well as increased EMI.

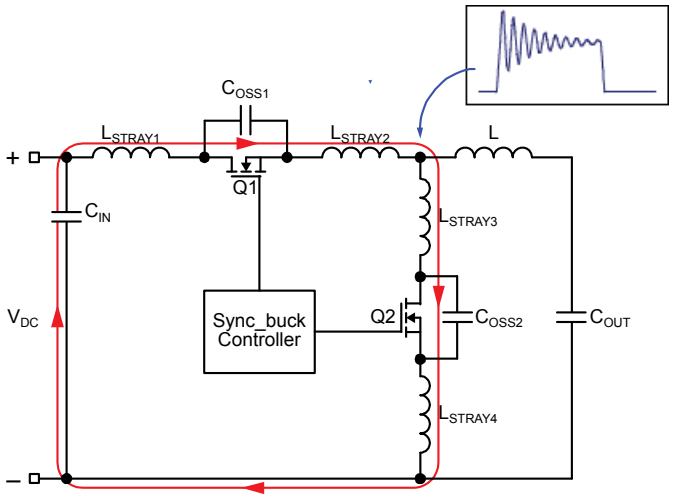


Figure 5. Output Parasitics

One method of reducing the ringing is to use a resistor and capacitor to lower the Q of the resonant circuit, as shown in Figure 6. Capacitor C_S is used to block DC and minimize the power dissipation in the resistor. This capacitor value should be between 2 and 10 times the parasitic capacitance of the MOSFET C_{OSS}. A capacitor that is too small will have high impedance and prevent the resistor from damping the ringing. A capacitor that is too large causes unnecessary power dissipation in the resistor, which lowers efficiency.

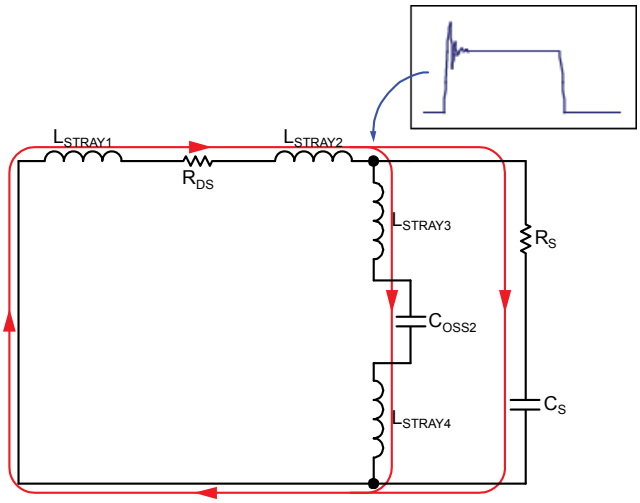


Figure 6. Snubber Circuit

The snubber components should be placed as close as possible to the low-side MOSFET and/or external Schottky diode since it contributes to most of the stray capacitance. Placing the snubber too far from the MOSFET or using a trace that is too long or thin will add inductance to the snubber and diminishes its effectiveness.

A proper snubber design requires that the parasitic inductance and capacitance be known. A method of determining these values and calculating the damping resistor value is outlined below:

1. Measure the ringing frequency at the switch node which is determined by parasitic L_P and C_P. Define this frequency as f_1.
2. Add a capacitor C_S (such as 2 times as big as the C_{OSS} of the FET) from the switch node to ground and measure the new ringing frequency. Define this new (lower) frequency as f_2. L_P and C_P can now be solved using the values of f_1, f_2 and C_S.
3. Add a resistor R_S in series with C_S to generate critical damping.

Step 1: First measure the ringing frequency on the switch node voltage when the high-side MOSFET turns on. This ringing is characterized by the equation:

$$f_1 = \frac{1}{2\pi\sqrt{L_P \times C_P}} \quad (27)$$

where C_P and L_P are the parasitic capacitance and inductance.

Step 2: Add a capacitor, C_S, in parallel with the synchronous MOSFET, Q2. The capacitor value should be approximately 2 times the C_{OSS} of Q2. Measure the frequency of the switch node ringing, f_2:

$$f_2 = \frac{1}{2\pi\sqrt{Lp \times (Cs + Cp)}} \quad (28)$$

Define f' as:

$$f' = \frac{f_1}{f_2}$$

Combining the equations for f_1, f_2 and f' to derive C_P, the parasitic capacitance:

$$C_P = \frac{C_S}{(f')^2 - 1} \quad (29)$$

L_P is solved by re-arranging the equation for f_1:

$$L_P = \frac{1}{(2\pi)^2 \times C_P \times (f_1)^2} \quad (30)$$

Step 3: Calculate the damping resistor.

Critical damping occurs at Q = 1:

$$Q = R_S \times \sqrt{\frac{C_P}{L_P}} = 1 \quad (31)$$

Solving for R_S:

$$R_S = \sqrt{\frac{L_P}{C_p}} \quad (32)$$

Figure 6 shows the snubber in the circuit and the damped switch node waveform. The snubber capacitor, C_S, is charged and discharged each switching cycle. The energy stored in C_S is dissipated by the snubber resistor, R_S, two times per switching period. This power is calculated in the equation below:

$$P_{SNUBBER} = f_{SW} \times C_S \times V_{IN}^2 \quad (33)$$

Ripple Injection

The V_{FB} ripple required for proper operation of the MIC2166 g_m amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10mV to 20mV, and the V_{FB} ripple is less than 20mV. If the V_{FB} ripple is so small that the g_m amplifier and error comparator cannot sense it, the MIC2166 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the V_{FB} ripple:

1. Enough ripple at V_{OUT} due to the large ESR of the output capacitors.

As shown in Figure 7a, the converter is stable without any ripple injection. The V_{FB} ripple is:

$$\Delta V_{FB(pp)} = \frac{R2}{R1+R2} \times \Delta V_{OUT} \quad (34)$$

where $\Delta V_{OUT} = ESR_{C_{OUT}} \cdot \Delta I_{L(PP)}$, $\Delta I_{L(PP)}$ is the peak-to-peak value of the inductor current ripple.

2. Inadequate ripple at V_{OUT} due to the small ESR of the output capacitors.

The output voltage ripple is fed into the FB pin through a feedforward capacitor C_{ff} in this situation, as shown in Figure 7b. The typical C_{ff} value is between 1nF and 100nF. With the feedforward capacitor, V_{FB} ripple is very close to the output voltage ripple:

$$\Delta V_{FB(pp)} \approx \Delta V_{OUT} \quad (35)$$

3. Virtually no ripple at V_{OUT} due to the very low ESR of the output capacitors.

In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{inj} and a capacitor C_{inj}, as shown in Figure 7c. The injected ripple is:

$$\Delta V_{FB(PP)} = V_{IN} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau} \quad (36)$$

$$K_{div} = \frac{R1//R2}{R_{inj} + R1//R2} \quad (37)$$

where:

V_{IN} = Power stage input voltage at VIN pin

D = Duty Cycle

f_{SW} = switching frequency

$\tau = (R1 // R2 // R_{inj}) \cdot C_{ff}$

In equations (36) and (37), it is assumed that the time constant associated with C_{ff} must be much greater than the switching period:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a C_{ff} of 1nF to 100nF can easily satisfy the large time constant consumption. Also, a 100nF injection capacitor C_{inj} is used in order to be considered as short for a wide range of the frequencies.

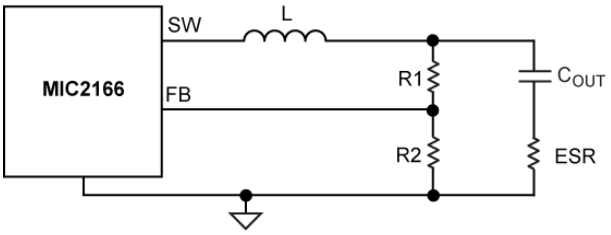


Figure 7a. $\frac{R2}{R1+R2} \times \Delta V_{OUT} > 20mV$

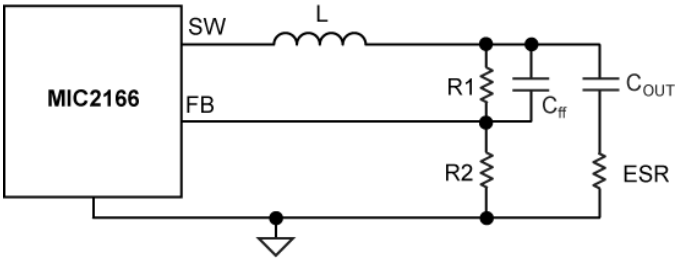


Figure 7b. $\frac{R2}{R1+R2} \times \Delta V_{OUT} < 20mV$ **and** $\Delta V_{OUT} > 20mV$

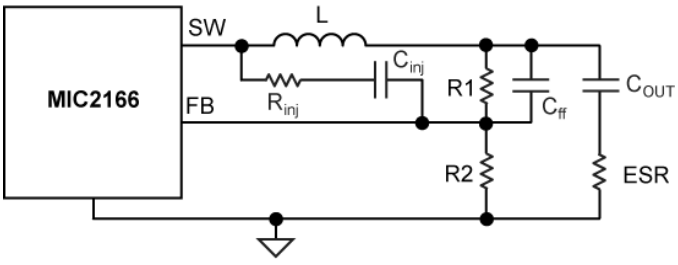


Figure 7c. $\Delta V_{OUT} < 20mV$

The process of sizing the ripple injection resistor and capacitors is:

Step 1. Select C_{ff} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{ff} is 1nF to 100nF if R1 and R2 are in kΩ range.

Step 2. Select R_{inj} according to the expected feedback voltage ripple. According to the equation (36):

$$K_{div} = \frac{\Delta V_{FB(PP)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)} \quad (38)$$

Then the value of Rinj is obtained as:

$$R_{inj} = (R1 // R2) \times (\frac{1}{K_{div}} - 1) \quad (39)$$

Step 3. Select C_{inj} as 100nF, which could be considered as short for a wide range of the frequencies.

Setting Output Voltage

The MIC2166 requires two resistors to set the output voltage, as shown in Figure 8.

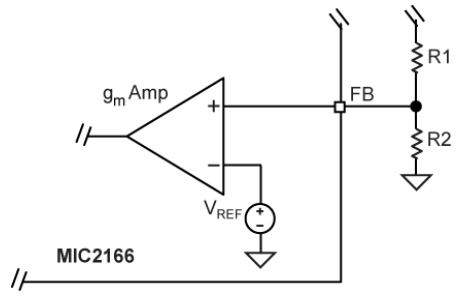


Figure 8. Voltage-Divider Configuration

The output voltage is determined by the equation:

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \quad (40)$$

where V_{REF} = 0.8V. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. The total voltage divider resistance R1+R2 is recommended to be 7.5kΩ. Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}} \quad (41)$$

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the MIC2166, as shown in Figure 10. The inverting input voltage V_{INJ} is clamped to 1.2V. As V_{OUT} is increased, the swing of V_{INJ} will be clamped. The clamped V_{INJ} reduces the line regulation because it is reflected back as a DC error on the FB terminal. Therefore, the maximum output voltage of the MIC2166 should be limited to 5.5V to avoid this problem.

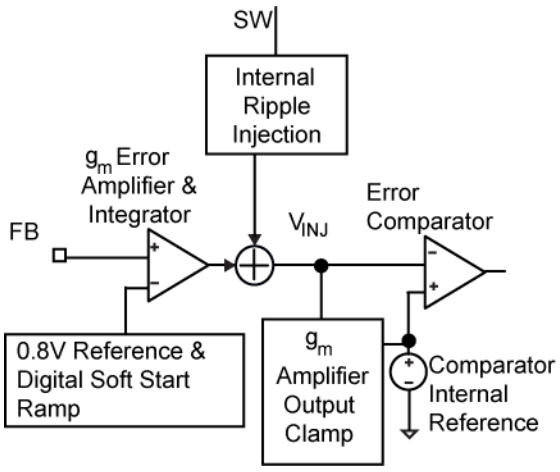


Figure 9. Internal Ripple Injection

PCB Layout Guidelines

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC2166 converter.

IC

- The 10µF ceramic capacitor, which connects to the VDD terminal, must be located next to the IC. The VDD terminal is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect the VDD and PGND pins.
- Place the IC and MOSFETs close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.
- The exposed pad (ePad) on the bottom of the IC must be connected to the ground through several vias.
- The feedback resistors should be placed close to the FB pin. The top feedback resistor should connect directly to the output node. Run this trace away from the switch node (SW).

Input Capacitor

- Place the VIN input capacitor next.
- Place the VIN input capacitors on the same side of the board and as close to the MOSFETs as possible.
- Keep both the VIN and PGND connections short.
- Place several vias to the ground plane close to the VIN input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The SW pin should be connected directly to the drain of the low-side MOSFET to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Schottky Diode

- Place the Schottky diode on the same side of the board as the MOSFETs and VIN input capacitor.
- The connection from the Schottky diode’s Anode to the input capacitors ground terminal must be as short as possible.
- The diode’s Cathode connection to the switch node (SW) must be keep as short as possible.

RC Snubber

- Place the RC snubber on the same side of the board and as close to the MOSFETs as possible.

MOSFETs

- Low-side MOSFET gate drive trace (DL pin to MOSFET gate pin) must be short and routed over a ground plane. The ground plane should be the connection between the MOSFET source and PGND.
- Chose a low-side MOSFET with a high C_{GS}/C_{GD} ratio and a low internal gate resistance to minimize the effect of dv/dt inducted turn-on.
- Do not put a resistor between the LSD output and the gate of the low-side MOSFET.
- Use a 4.5V V_{GS} rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET. MOSFETs that are rated for operation at less than 4.5V V_{GS} should not be used.

Evaluation Board Schematic

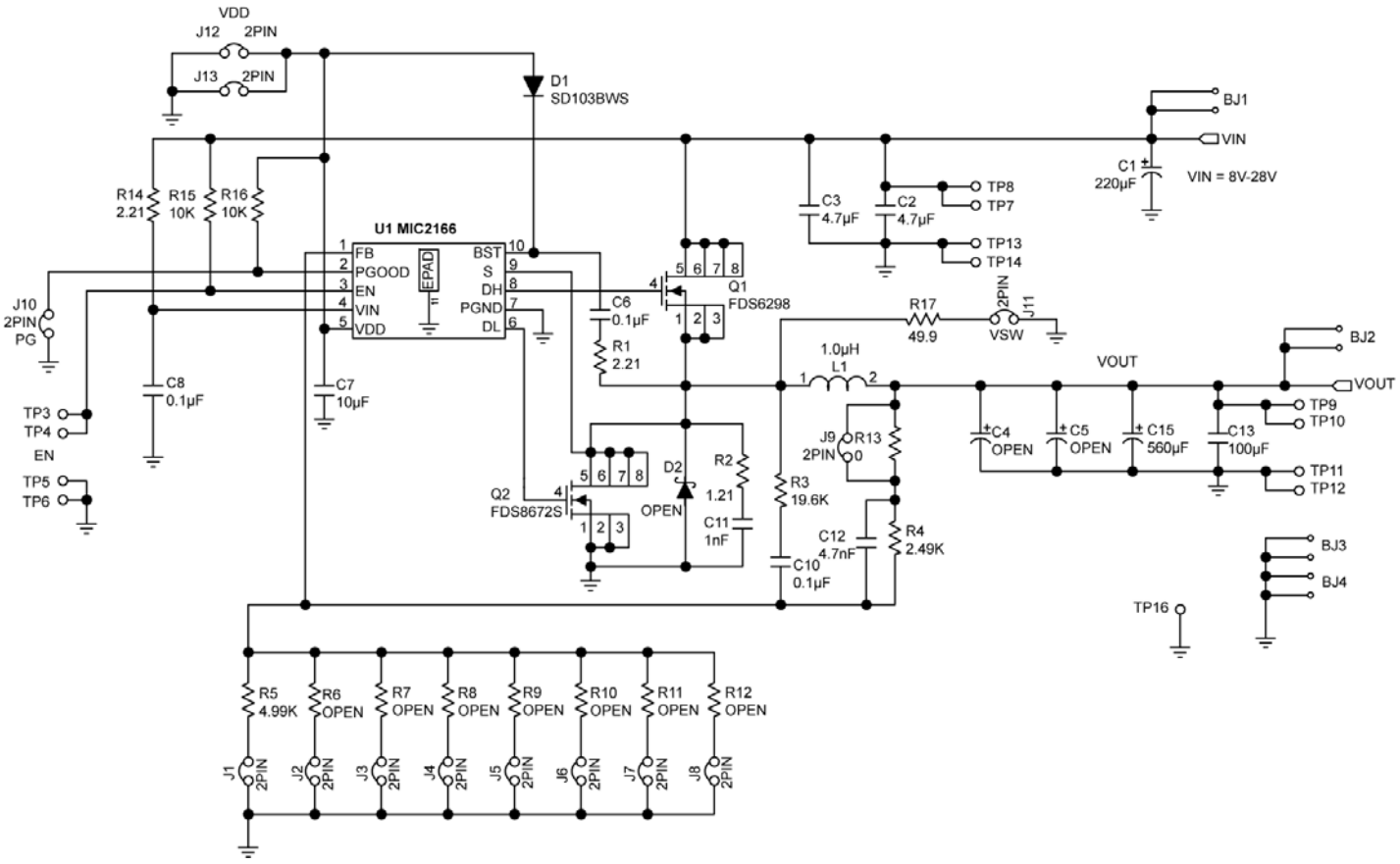


Figure 10. Schematic of MIC2166 8V-24V to 1.2V/10A Evaluation Board

Bill of Materials

Item	Part Name	Manufacturer	Description	Qty.
C1	B41125A7227M	EPCOS[1]	220µF Aluminum Capacitor, SMD, 35V	1
	222215095001E3	Vishay Dale[2]		
C2,C3	12105C475KAZ2A	AVX[3]	4.7µF Ceramic Capacitor, X7R, Size 1210, 50V	2
	GRM32ER71H475KA88L	Murata[4]		
C6,C8,C10	06035C104KAT2A	AVX[3]	0.1µF Ceramic Capacitor, X7R, Size 0603, 50V	3
	GRM188R71H104KA93D	MuRata[4]		
	C1608X7R1H104K	TDK[5]		
C7	0805ZD106KAT2A	AVX[3]	10µF Ceramic Capacitor, X5R, Size 0805, 10V	1
	GRM21BR61A106KE19L	MuRata[4]		
C11	06035C102KAT2A	AVX[3]	1nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H102KA01D	MuRata[4]		
	C1608X7R1H102K	TDK[5]		
C12	06035C472KAT2A	AVX[3]	4.7nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H472KA01D	MuRata[4]		
	C1608X7R1H472K	TDK[5]		
C13	12106D107MAT2A	AVX[3]	100µF Ceramic Capacitor, X5R, Size 1210, 6.3V	1
	GRM32ER60J107ME20L	MuRata[4]		
C15	6SEPC560MX	SANYO[6]	560µF OSCON Capacitor, 6.3V	1
D1	SD103BWS-7	Diodes Inc[7]	Small Signal Schottky Diode	1
	SD103BWS	Vishay Dale[2]		
L1	HCF1305-1R0-R	Cooper Bussmann[8]	1.0µH Inductor, 24A Saturation Current	1
Q1	FDS6298	Fairchild[9]	30V, 13A N-Channel MOSFET 12mΩ Rds(on) @ 4.5V	1
Q2	FDS8672S	Fairchild[9]	30V, 18A N-Channel MOSFET 7mΩ Rds(on) @ 4.5V	1

Notes:

1. EPCOS: www.epcos.com.
2. Vishay: www.vishay.com.
3. AVX: www.avx.com.
4. MuRata: www.murata.com.
5. TDK: www.tdk.com.
6. Sanyo: www.sanyo.com.
7. Diode Inc.: www.diodes.com.
8. Cooper Bussmann: www.cooperbussmann.com.
9. Fairchild: www.fairchildsemi.com.

Bill of Materials (Continued)

Item	Part Name	Manufacturer	Description	Qty.
R1,R14	CRCW06032R21FKEA	Vishay Dale[2]	2.21Ω Resistor, Size 0603, 1%	2
R2	CRCW08051R21FKEA	Vishay Dale[2]	1.21Ω Resistor, Size 0805, 1%	1
R3	CRCW060319K6FKEA	Vishay Dale[2]	19.6kΩ Resistor, Size 0603, 1%	1
R4	CRCW06032K49FKEA	Vishay Dale[2]	2.49kΩ Resistor, Size 0603, 1%	1
R5	CRCW06034K99FKEA	Vishay Dale[2]	4.99kΩ Resistor, Size 0603, 1%	1
R13*	CRCW06030000Z0EA	Vishay Dale[2]	0Ω Resistor, Size 0603, 1%	1
R15,R16	CRCW060310K0FKEA	Vishay Dale[2]	10kΩ Resistor, Size 0603, 1%	2
R17*	CRCW060349R9FKEA	Vishay Dale[2]	49.9Ω Resistor, Size 0603, 1%	1
U1	**MIC2166YMME**	**Micrel, Inc.[10]**	600kHz Buck Controller	1

*R13 and R17 are for test purpose only.

Notes (Continued):

10. Micrel, Inc: www.micrel.com.

PCB Layout Recommendations

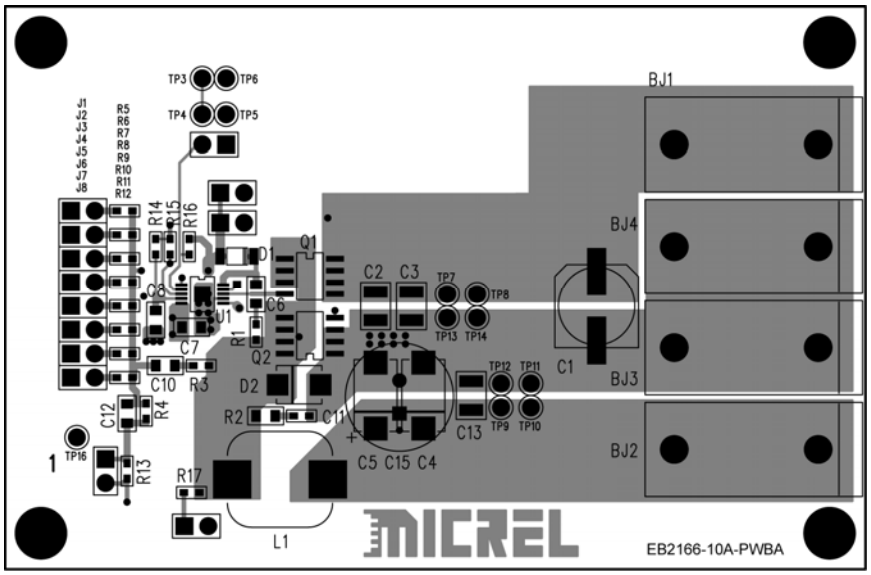


Figure 11. MIC2166 10A Evaluation Board Top Layer

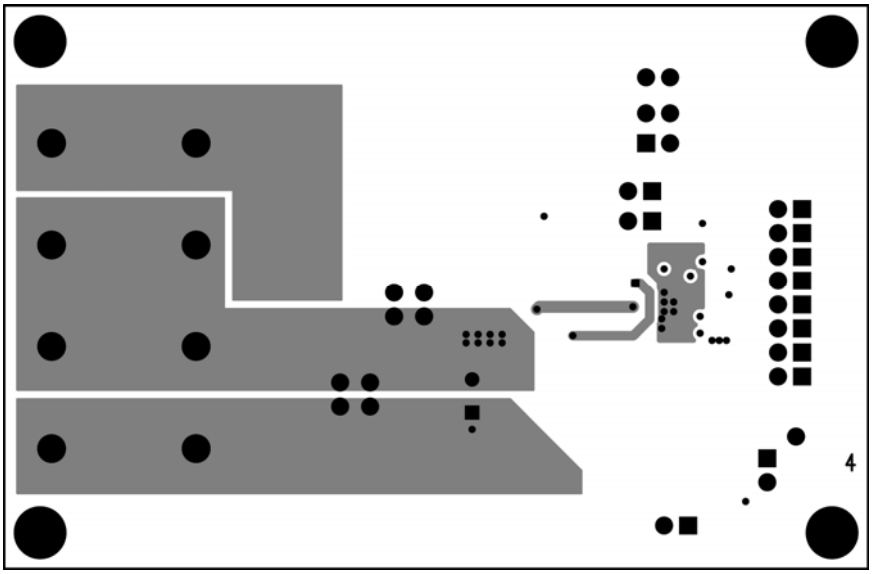


Figure 12. MIC2166 10A Evaluation Board Bottom Layer

PCB Layout Recommendations (Continued)

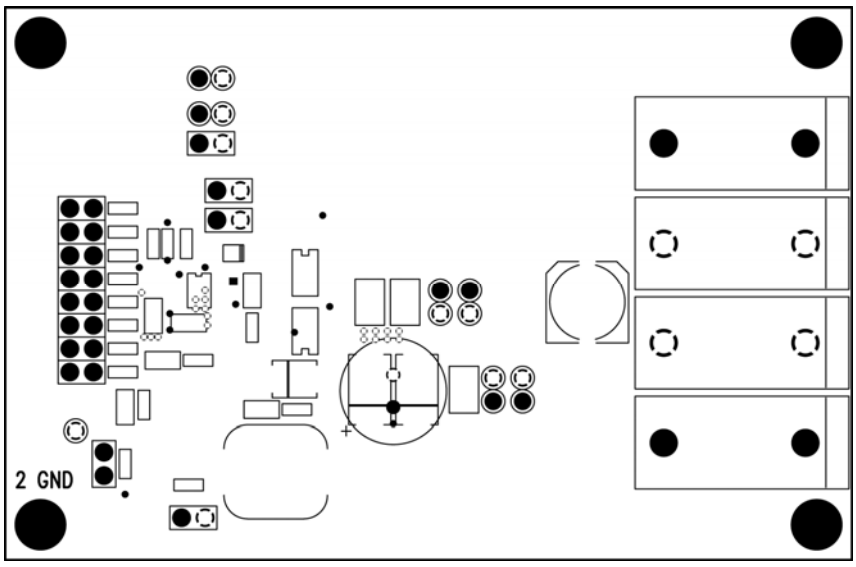


Figure 13. MIC2166 10A Evaluation Board Mid-Layer 1 (GND Plane)

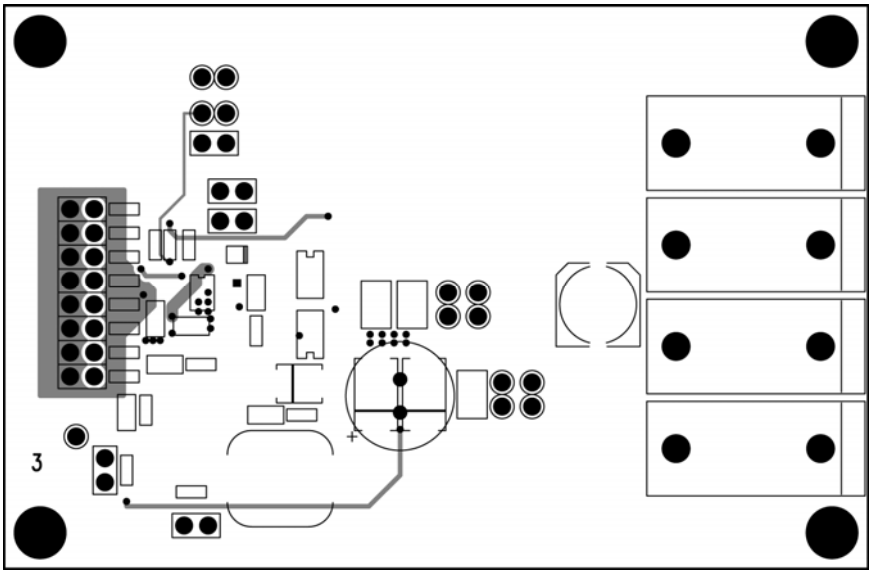
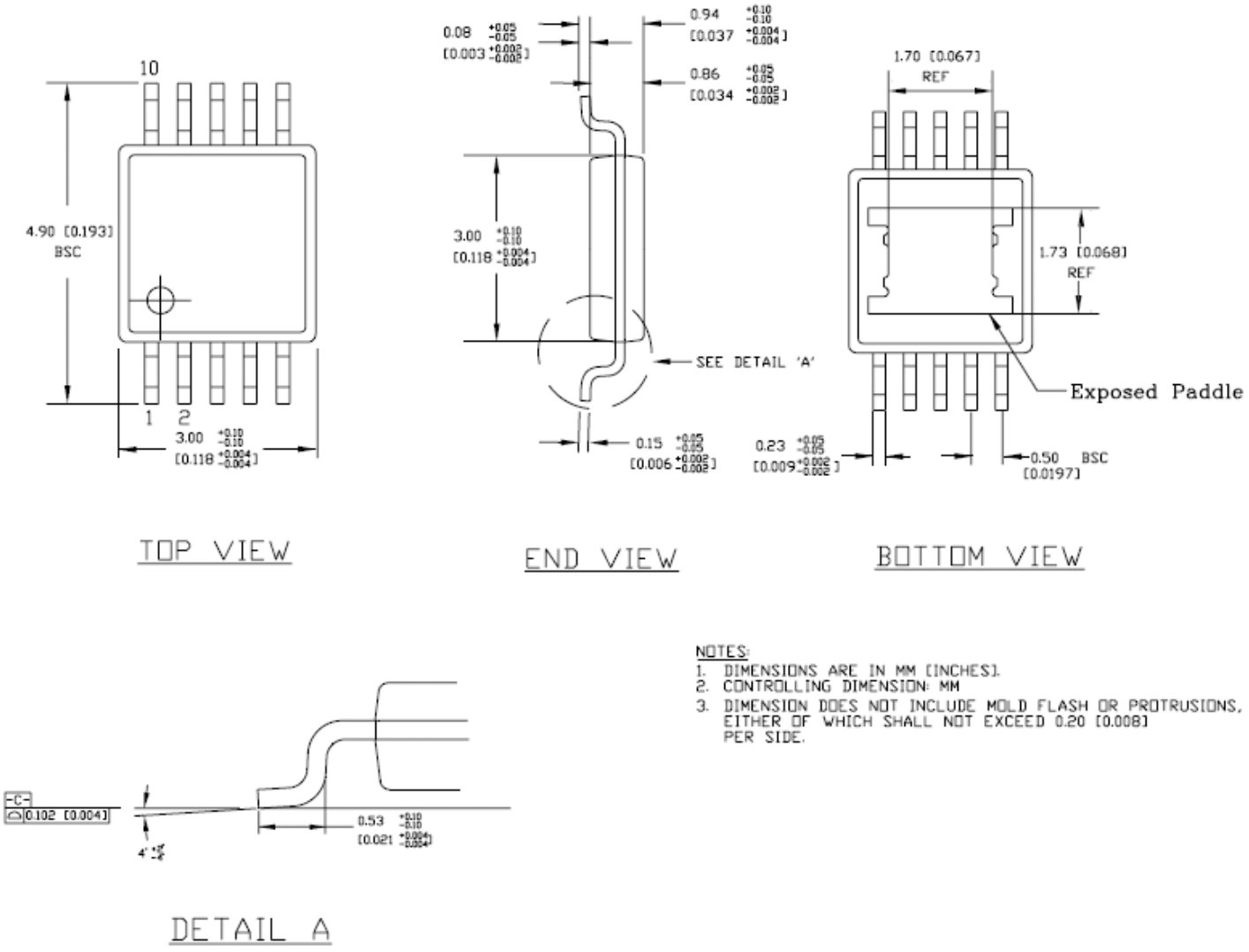


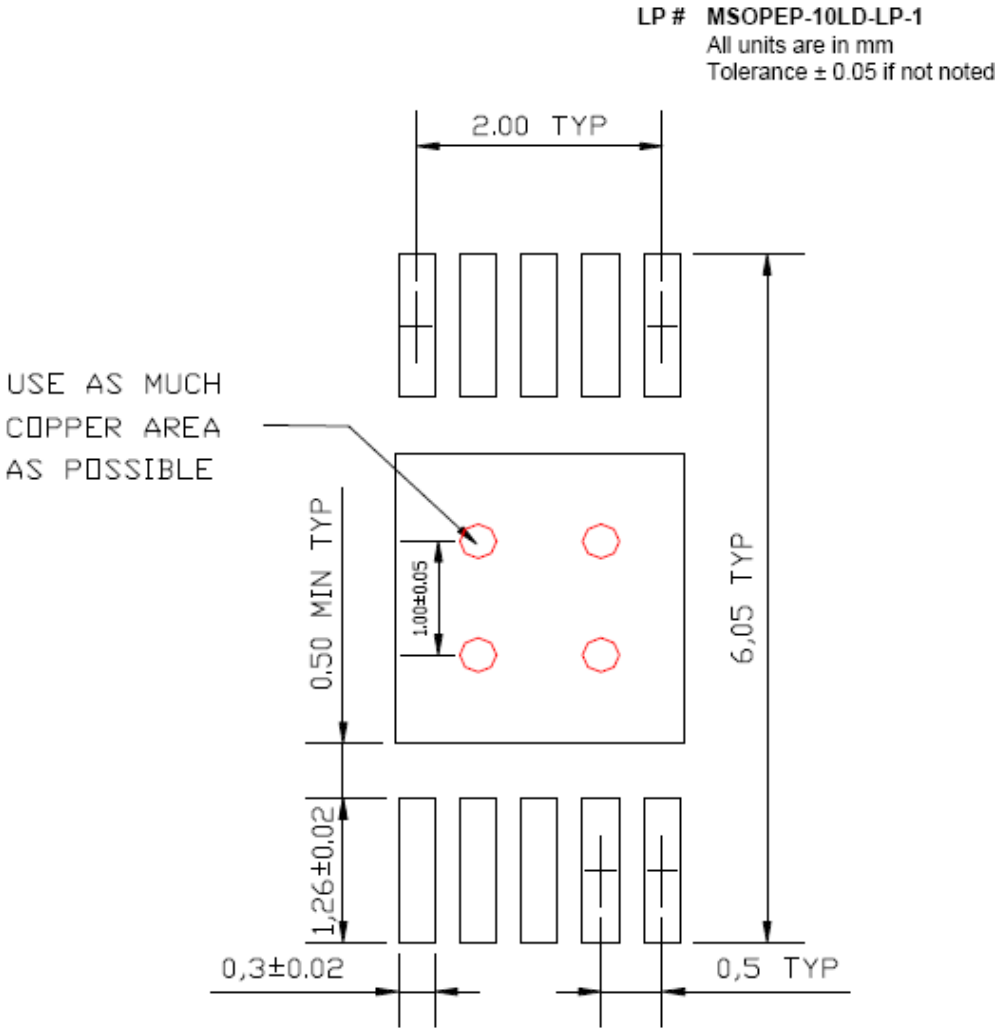
Figure 14. MIC2166 10A Evaluation Board Mid-Layer 2

Package Information



10-Pin ePad MSOP (MME)

Recommended Landing Pattern



Red circle indicates Thermal Via. Size should be .300-.350 mm in diameter, 1.00 mm pitch, and it should be connected to GND plane for maximum thermal performance.

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