# RD151TS3316ARP, RD151TS3326ARP

## Spread Spectrum Clock for EMI Solution

REJ03D0797-0100
Rev.1.00
May 11, 2006

### Description

RD151TS3316ARP and RD151TS3326ARP is a high-performance Spread Spectrum Clock generator. It is suitable for EMI solution of electric systems.

### Features

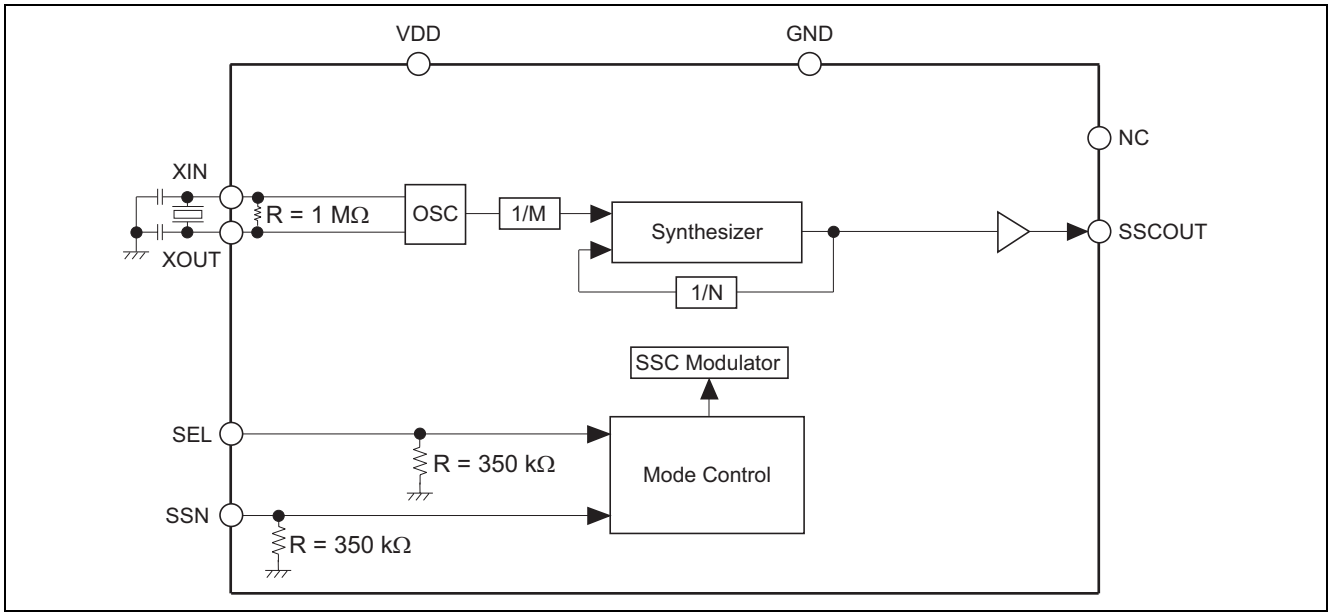
- Supports 40 MHz to 80 MHz operations. Multiple rate (XIN: SSCOUT) = 1: 1
  Input frequency 40 MHz to 80 MHz
- Spread spectrum modulation ; RD151TS3316ARP : ±1.5%, ±0.5% (Central spread modulation)
  RD151TS3326ARP : –3.0%, –1.0% (Down spread modulation)

### Key Specifications

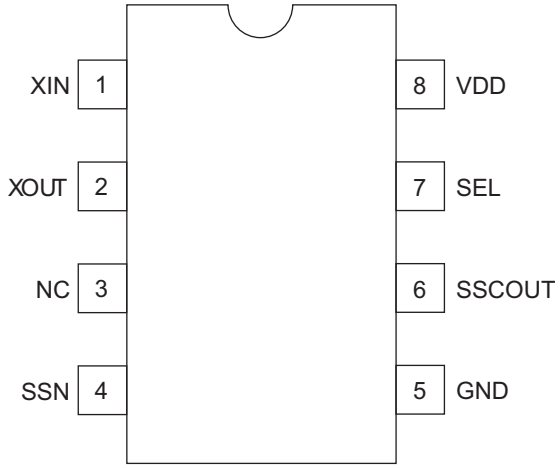
- Supply voltages: $V_{DD}$ = 3.3 V ±0.3 V
- Cycle to cycle jitter = ±100 ps typ.
- Clock output duty cycle = 50 ±5%
- Output slew rate = 0.7 V/ns typ.
- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---|---|---|---|---|
| RD151TS3316ARPH0<br>RD151TS3326ARPH0 | SOP-8 pin<br>(JEDEC) | PRSP0008DD-C<br>(FP-8DCV) | RP | H (2,500 pcs / Reel) |

### Block Diagram



## Pin Arrangement




(Top view)

## Pin Descriptions

| Pin name | No. | Type | Description |
|---|---|---|---|
| GND | 5 | Ground | GND pin |
| VDD | 8 | Power | Power supply pin. |
| NC | 3 | NC | Don't connect any VDD or GND. |
| SSCOUT | 6 | Output | Spread spectrum modulated clock output. |
| XIN | 1 | Input | Oscillator input. |
| XOUT | 2 | Output | Oscillator output. |
| SEL | 7 | Input | SSC% mode select pin. LVCMOS level input.<br>Pull-down by internal resistor (350 kΩ). |
| SSN | 4 | Input | SSC ON/OFF select pin. LVCMOS level input.<br>Pull–down by internal resistor (350 kΩ). |

## SSC Function Table

| STB | SEL | RD151TS3316ARP(Central spread) | RD151TS3326ARP(Down spread) |
|---|---|---|---|
| 0 | 0 | ±1.5%*[1] | –3.0%*[1] |
| 0 | 1 | ±0.5% | –1.0% |
| 1 | 0 | OFF | OFF |
| 1 | 1 | | |

Note: 1. ±1.5% (TS3316ARP) / -3.0%(TS3326ARP) SSC is selected for default by internal pull-down resistors.

## Clock Frequency Table

| PRODUCT | XIN(MHz) | SSCOUT(MHz) | Multiply rate (XIN: SSCOUT) |
|---|---|---|---|
| RD151TS3316ARP | 40 to 80 | 40 to 80 | 1:1 |
| RD151TS3326ARP | 40 to 80 | 40 to 80 | 1:1 |

## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | –0.5 to 4.6 | V | |
| Input voltage | $V_I$ | –0.5 to 4.6 | V | |
| Output voltage [*1] | $V_O$ | –0.5 to $V_{DD}$+0.5 | V | |
| Input clamp current | $I_{IK}$ | –50 | mA | $V_I < 0$ |
| Output clamp current | $I_{OK}$ | –50 | mA | $V_O < 0$ |
| Continuous output current | $I_O$ | ±50 | mA | $V_O$ = 0 to $V_{DD}$ |
| Maximum power dissipation | | 0.7 | W | Ta = 55°C (in still air) |
| Storage temperature | $T_{stg}$ | –65 to +150 | °C | |

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V | |
| DC input signal voltage | | –0.3 | — | $V_{DD}$+0.3 | V | |
| High level input voltage | $V_{IH}$ | 0.7×$V_{DD}$ | — | $V_{DD}$+0.3 | V | |
| Low level input voltage | $V_{IL}$ | –0.3 | — | 0.3×$V_{DD}$ | V | |
| Input clock duty cycle | | 45 | 50 | 55 | % | |
| Operating temperature | $T_a$ | –20 | — | 85 | °C | |

## DC Electrical Characteristics

Ta = –20 to 85 °C, $V_{DD}$ = 3.0 to 3.6 V

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input current | $I_I$ | — | — | ±20 | µA | $V_I$ = 0 V or 3.6 V, $V_{DD}$ = 3.6 V, XIN pin |
| | | — | — | ±100 | | $V_I$ = 0 V or 3.6 V, $V_{DD}$ = 3.6 V, SEL, SSN pins |
| Input capacitance | $C_I$ | — | 3 | — | pF | SEL, SSN pins |

## DC Electrical Characteristics / SSC Clock Output

Ta = –20 to 85 °C, $V_{DD}$ = 3.0 to 3.6 V

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output voltage | $V_{OH}$ | $V_{DD}$–0.2 | — | — | V | $I_{OH}$ = –1 mA |
| | $V_{OL}$ | — | — | 200 | mV | $I_{OL}$ = 1 mA |
| Output current | $I_{OH}$ | — | –19 | — | mA | $V_{OH}$ = 1.5 V, $V_{DD}$ = 3.3 V |
| | $I_{OL}$ | — | 19 | — | | $V_{OL}$ = 1.5 V, $V_{DD}$ = 3.3 V |
| Output impedance | | — | 40 | — | Ω | |

## AC Electrical Characteristics / SSC Clock Output

Ta = 25°C, $V_{DD}$ = 3.3 V, $C_L$ = 15 pF

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Operating current | $I_{DD}$ | — | 18 | 24 | mA | $V_{DD}$ = 3.3 V, $C_L$ = 15 pF, XIN = 40 MHz | |
| Cycle to cycle jitter *[1] | $t_{CCS}$ | — | \|100\| | — | ps | SEL = 0, $C_L$ = 0 pF<br>SSC= ±1.5%(TS3316ARP)<br>SSC= -3.0%(TS3326ARP) | Figure 1 |
| Slew rate | $t_{SL}$ | — | 0.7 | 4.0 | V/ns | $V_{DD}$ = 3.3 V, 0.2 × $V_{DD}$ to 0.8 × $V_{DD}$ | |
| Clock duty cycle | | 45 | 50 | 55 | % | | |
| Stabilization time *[2] | | — | — | 2 | ms | | |

Notes: Parameters are target of design. Not 100% tested in production.

1. Cycle to cycle jitter is included spread spectrum modulation.
2. Stabilization time is the time required for the integrated circuit to obtain phase lock of its input signal after power up.

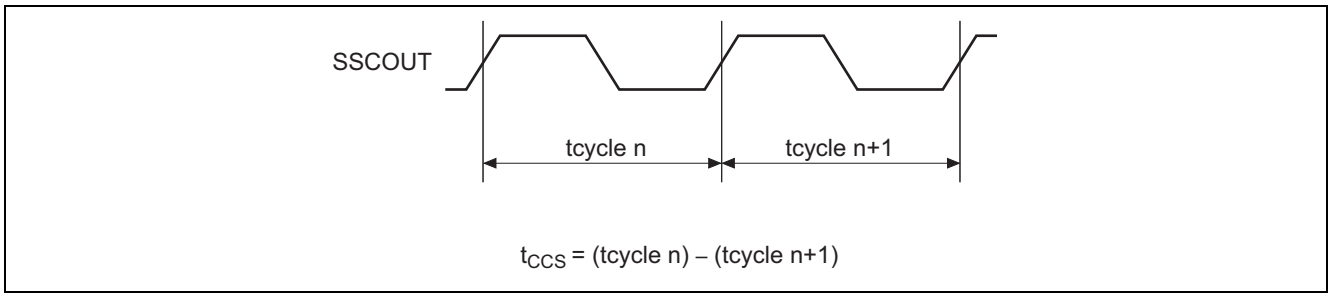



**Figure 1 Cycle to cycle jitter**

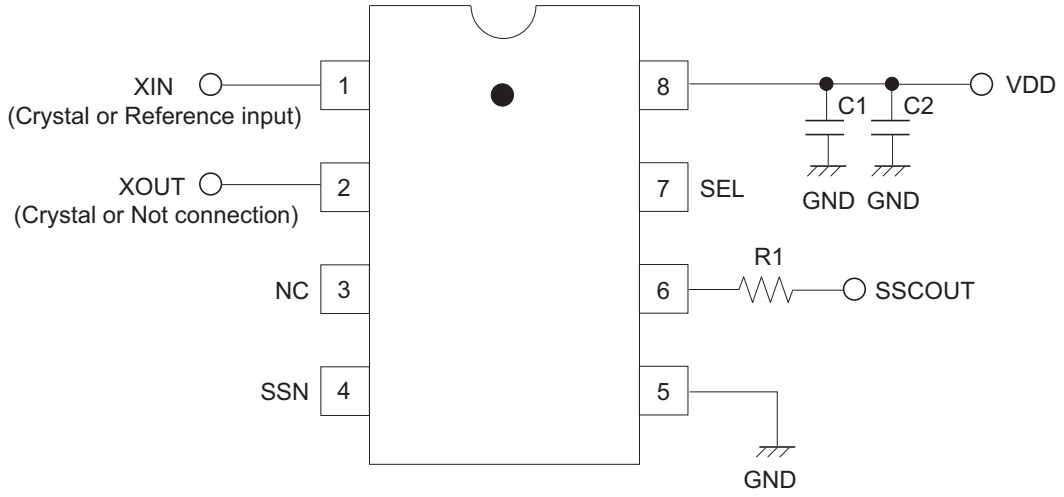
## Application Information

### 1. Recommended Circuit Configuration

The power supply circuit of the optimal performance on the application of a system should refer to Figure 2.

VDD decoupling is important to both reduce Jitter and EMI radiation.

The C1 decoupling capacitor should be placed as close to the VDD pin as possible, otherwise the increased trace inductance will negate its decoupling capability.




Notes: C1 = High frequency supply decoupling capacitor.
(0.1 µF recommended)
C2 = Low frequency supply decoupling capacitor.
(22 µF recommended)
R1 = Match value to line impedance.

**Figure 2 Recommended circuit configuration**

## 2. Example Board Layout Configuration

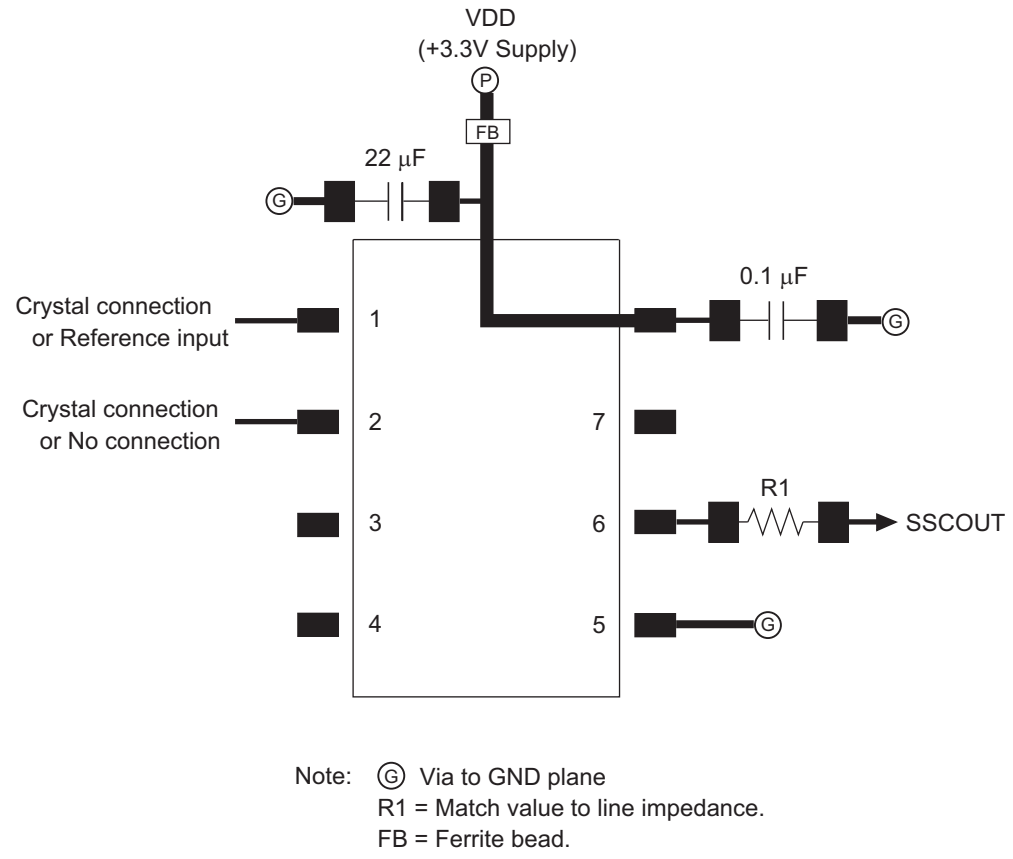



**Figure 3 Example Board Layout**

### 3. Example of TS33XX EMI Solution IC's Application

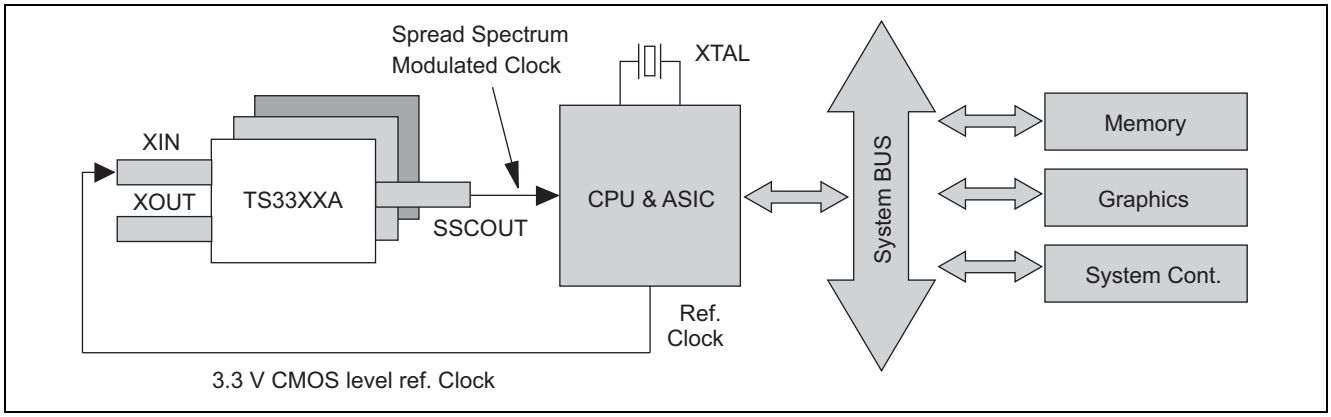



**Figure 4 Ref. Clock Input Example**

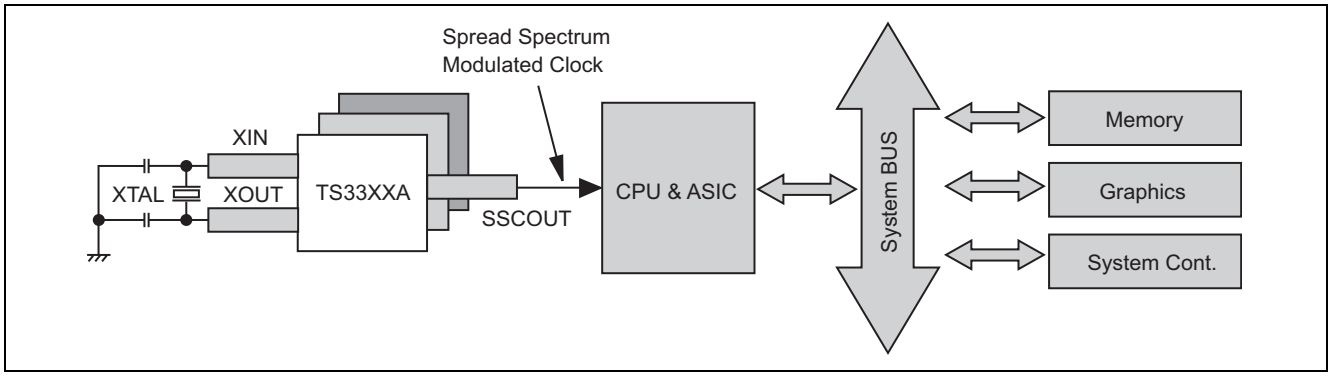
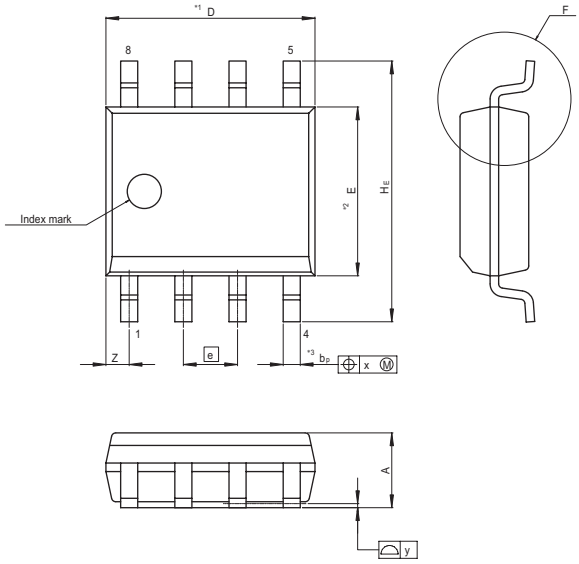



**Figure 5 XTAL Ref. Clock Input Example**

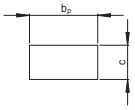
## Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP8-3.95x4.9-1.27 | PRSP0008DD-C | FP-8DCV | 0.085g |

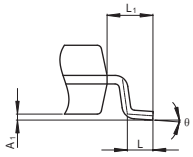









Terminal cross section
( Ni/Pd/Au plating )




Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 4.90 | 5.30 |
| E | — | 3.95 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.10 | 0.14 | 0.25 |
| A | — | — | 1.75 |
| $b_p$ | 0.34 | 0.40 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 5.80 | 6.10 | 6.20 |
| e | — | 1.27 | — |
| x | — | — | 0.25 |
| y | — | — | 0.10 |
| Z | — | — | 0.75 |
| L | 0.40 | 0.60 | 1.27 |
| $L_1$ | — | 1.08 | — |

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