TMUX611x 36-V, Low-Capacitance, Low-Leakage-Current, Precision, Quad SPST Switches

1 Features

- Low On-Capacitance: 4.2 pF
- Low Input Leakage: 1 pA
- Low Charge Injection: –0.6 pC
- Rail-to-Rail Operation
- Wide Supply Range: ±5 V to ±16.5 V (dual), 10 V to 16.5 V (single)
- Low On-Resistance: 125 Ω
- Fast Switch Turn-On Time: 66 ns
- Break-Before-Make Switching Action for TMUX6113
- EN Pin Connectable to V_{DD}
- Logic Levels: 2 V to V_{DD}
- Low Supply Current: 17 µA
- ESD Protection HBM: 2000 V
- Industry-Standard TSSOP and smaller WQFN Package

2 Applications

- Factory Automation and Industrial Process Controls
- Programmable Logic Controllers (PLC)
- Analog Input Modules
- ATE Test Equipment
- Digital Multimeters
- Battery Monitoring Systems

3 Description

The TMUX6111, TMUX6112, and TMUX6113 devices are modern complementary metal-oxide semiconductor (CMOS) devices that have four independently selectable single-pole/single-throw (SPST) switches. The devices work well with dual supplies (±5 V to ±16.5 V), a single supply (10 V to 16.5 V), or unsymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). All digital inputs have transistor-transistor logic (TTL) compatible thresholds, ensuring both TTL and CMOS logic compatibility.

The switches are turned on with Logic 0 on the digital control inputs in the TMUX6111. Logic 1 is required to turn on switches in the TMUX6112. The TMUX6113 has two switches with similar digital control logic to the TMUX6111 while the logic is inverted on the other two switches. The TMUX6113 has break-before-make (BBM) switching behavior, allowing the device to be used in multiplexer applications.

The TMUX611x devices are part of Texas Instruments Precision Switches and Multiplexers family. The devices have very low leakage current and charge injection, allowing them to be used in high-precision measurement applications. Low supply current of 17 µA enables the device usage in portable applications.

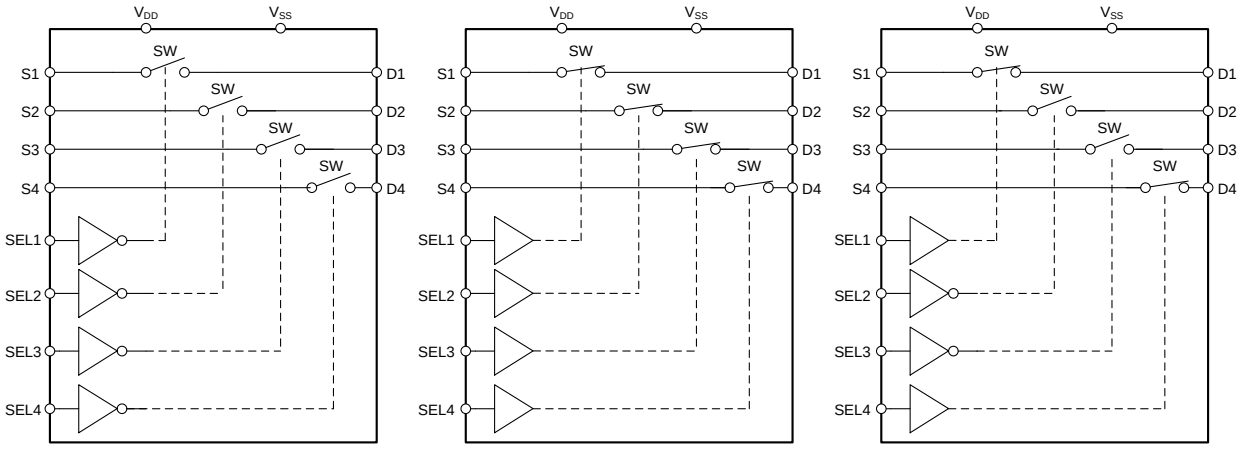
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX6111 TMUX6112 TMUX6113	TSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

Simplified Schematic



TMUX6111 TMUX6112 TMUX6113

Table of Contents

ADVANCE INFORMATION

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

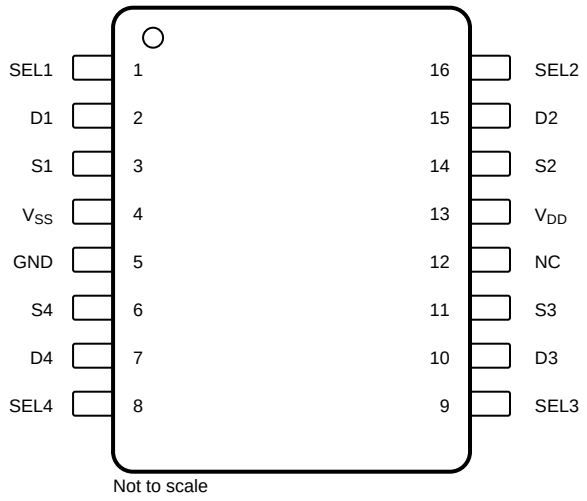
DATE	REVISION	NOTES
August 2018	*	Initial release.

5 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX6111	36-V, Low Capacitance, Low-Leakage-Current, Precision, Quad SPST Switches (Normally Closed)
TMUX6112	36-V, Low Capacitance, Low-Leakage-Current, Precision, Quad SPST Switches (Normally Open)
TMUX6113	36-V, Low Capacitance, Low-Leakage-Current, Precision, Quad SPST Switches (Dual Open + Dual Closed)

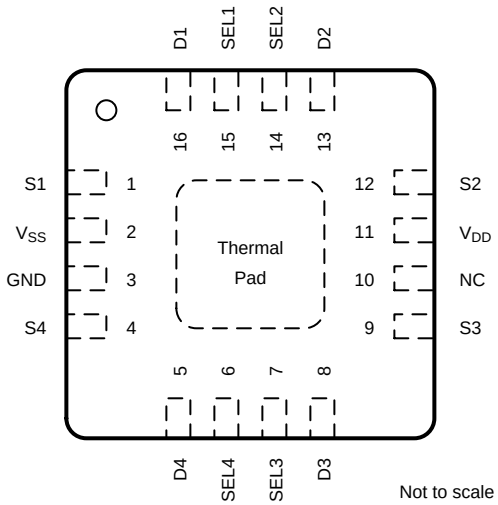
6 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Not to scale

RTE Package
16-Pin WQFN
Top View



Not to scale

Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	TSSOP	WQFN		
SEL1	1	15	I	Logic control input 1.
D1	2	16	I/O	Drain pin 1. Can be an input or output.
S1	3	1	I/O	Source pin 1. Can be an input or output.
V_{SS}	4	2	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
GND	5	3	P	Ground (0 V) reference
S4	6	4	I/O	Source pin 4. Can be an input or output.
D4	7	5	I/O	Drain pin 4. Can be an input or output.
SEL4	8	6	I	Logic control input 4.
SEL3	9	7	I	Logic control input 3.
D3	10	8	I/O	Drain pin 3. Can be an input or output.
S3	11	9	I/O	Source pin 3. Can be an input or output.
NC	12	10	–	No internal connection.
V_{DD}	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
S2	14	12	I/O	Source pin 2. Can be an input or output.
D2	15	13	I/O	Drain pin 2. Can be an input or output.
SEL2	16	14	I	Logic control input 2.
–	-	EP	–	Exposed Pad. The exposed pad is electrically connected to V_{SS} internally. Connect EP to V_{SS} to achieve rated thermal and ESD performance.

(1) I = input, O = output, I/O = input and output, P = power

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		36	V
V_{DD} to GND		–0.3	18	V
V_{SS} to GND		–18	0.3	V
V_{DIG}	Digital input pin (SEL1, SEL2, SEL3, SEL4) voltage	GND –0.3	V_{DD}+0.3	V
I_{DIG}	Digital input pin (SEL1, SEL2, SEL3, SEL4) current	–30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_IN}	Analog input pin (Sx) current	–30	30	mA
V_{ANA_OUT}	Analog output pin (D) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_OUT}	Analog output pin (D) current	–30	30	mA
T_A	Ambient temperature	–55	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC		TMUX6111/ TMUX6112/ TMUX6113		UNIT
		PW (TSSOP)	RTE (QFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.0	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.2	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.6	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	°C/W

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to V_{SS} (1)	Power supply voltage differential	10		33	V
V_{DD} to GND	Positive power supply voltage (singlle supply, V_{SS} = 0 V)	10		16.5	V
V_{DD} to GND	Positive power supply voltage (dual supply)	5		16.5	V
V_{SS} to GND	Negative power supply voltage (dual supply)	–5		–16.5	V
V_S (2)	Source pins voltage	V_{SS}		V_{DD}	V

(1) V_{DD} and V_{SS} can be any value as long as 10 V ≤ (V_{DD} – V_{SS}) ≤ 33 V.
(2) V_S is the voltage on all the S pins.

ADVANCE INFORMATION

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{DIG}	Digital input pin (SEL1, SEL2, SEL3, SEL4) voltage	0		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)	–25		25	V
T_A	Ambient temperature	–40		125	V

7.5 Electrical Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		T_A = –40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_S = 1 mA			120	135	Ω
		V_S = ±10 V, I_S = 1 mA			140	160	Ω
			T_A = –40°C to +85°C			210	Ω
			T_A = –40°C to +125°C			245	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_S = 1 mA			2.5	11	Ω
			T_A = –40°C to +85°C			12	Ω
			T_A = –40°C to +125°C			12	Ω
R_{ON_FLAT}	On-resistance flatness	V_S = –10 V, 0 V, +10 V, I_S = 1 mA			23	33	Ω
			T_A = –40°C to +85°C			37	Ω
			T_A = –40°C to +125°C			37	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.52		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V		–0.02	0.001	0.02	nA
			T_A = –40°C to +85°C	-0.13		0.05	nA
			T_A = –40°C to +125°C	–1		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.05	0.005	0.05	nA
			T_A = –40°C to +85°C	–0.14		0.1	nA
			T_A = –40°C to +125°C	–1		0.5	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.07	0.008	0.07	nA
			T_A = –40°C to +85°C	–0.27		0.15	nA
			T_A = –40°C to +125°C	–2		1	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(IN)}$	Pull-down resistance on SELx pins				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			17	21	µA
			T_A = –40°C to +85°C			21	µA
			T_A = –40°C to +125°C			22	µA
I_{SS}	V_{SS} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			8	10	µA
			T_A = –40°C to +85°C			10	µA
			T_A = –40°C to +125°C			11	µA

(1) When V_S is positive, V_D is negative, and vice versa.

ADVANCE INFORMATION

7.6 Switching Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		66	77	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			107	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			117	ns
t_{OFF}	Enable turn-off time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		56	68	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			77	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			81	ns
tBBM	Break-before-make time delay (TMUX6113 Only)	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	8	40		ns
Q_J	Charge injection	V_S = 0 V, R_S = 0 Ω , C_L = 1 nF		0.6		pC
		V_S = –15 V to 15 V, R_S = 0 Ω , C_L = 1 nF		1.3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, adjacent channel		–100		dB
		R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, non-adjacentchannel		–115		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–7.5		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{DD}, f= 1 MHz		–59		dB
		R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{SS}, f= 1 MHz		–59		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		800		MHz
THD	Total harmonic distortion + noise	R_L = 10k Ω , C_L = 5 pF, f= 20Hz to 20kHz		0.08		%
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.5		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 0 V, f = 1 MHz (PW package)		1.9	3.0	pF
		V_S = 0 V, f = 1 MHz (RTE package)		2.5	3.6	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 0 V, f = 1 MHz		2.4	3.1	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 0 V, f = 1 MHz		4.2	6.0	pF

7.7 Electrical Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range	T_A = –40°C to +125°C		V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_S = 1 mA			230	265	Ω
			T_A = –40°C to +85°C			355	Ω
			T_A = –40°C to +125°C			405	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 10 V, I_S = 1 mA			5	18	Ω
			T_A = –40°C to +85°C			18	Ω
			T_A = –40°C to +125°C			19	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.5		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.001	0.02	nA
			T_A = –40°C to +85°C	–0.1		0.05	nA
			T_A = –40°C to +125°C	-0.8		0.4	nA

(1) When V_S is positive, V_D is negative, and vice versa.

Electrical Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.03	0.005	0.03	nA
			T_A = –40°C to +85°C	–0.1		0.08	nA
			T_A = –40°C to +125°C	–0.8		0.4	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = floating, V_D = 1 V/ 10 V		–0.05	0.008	0.05	nA
			T_A = –40°C to +85°C	–0.2		0.15	nA
			T_A = –40°C to +125°C	–1.6		0.8	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(EN)}$	Pull-down resistance on SELx pins					6	MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			13	16	µA
			T_A = –40°C to +85°C			16	µA
			T_A = –40°C to +125°C			17	µA

7.8 Switching Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		72	84	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			117	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			128	ns
t_{OFF}	Enable turn-off time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		57	66	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			78	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			84	ns
t_{BBM}	Break-before-make time delay (TMUX6113 only)	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	17	47		ns
Q_J	Charge injection	V_S = 6 V, R_S = 0 Ω , C_L = 1 nF		–0.7		pC
		V_S = 0 V to 12 V, R_S = 0 Ω , C_L = 1 nF		–0.7		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–86		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, adjacent channel		–98		dB
		R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, non-adjacent channel		–117		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		-15		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V, f= 1 MHz		–59		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		750		MHz
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.6		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 6 V, f = 1 MHz (PW package)		2.2	3.1	pF
		V_S = 6 V, f = 1 MHz (RTE package)		2.9	4.0	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 6 V, f = 1 MHz		2.8	3.5	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 6 V, f = 1 MHz		4.6	6.3	pF

ADVANCE INFORMATION

8 Parameter Measurement Information

8.1 Truth Tables

Table 1, Table 2, Table 3and show the truth tables for the TMUX6111, TMUX6112, and TMUX6113, respectively.

Table 1. TMUX6111 Truth Table

SELx	STATE
0	All Switch ON
1	All Switch OFF

Table 2. TMUX6112 Truth Table

SELx	STATE
0	All Switch OFF
1	All Switch ON

Table 3. TUMUX6113 Truth Table

SELx	STATE
0	Switch 1, 4 OFF Switch 2, 3 ON
1	Switch 1, 4 ON Switch 2, 3 OFF

9 Detailed Description

9.1 Overview

The TMUX6111, TMUX6112, and TMUX6113 are 4-channel single-pole/ single-throw (SPDT) switches that supports dual supplies (±5 V to ±16.5 V) or single supply (10 V to 16.5 V) operation. Each channel of the switch is turned on or turned off based on the state of its corresponding SELx pin. The Functional Block Diagram section provides a top-level block diagram of the switches.

9.1.1 On-Resistance

The on-resistance of the TMUX611x is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 1. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in Equation 1:

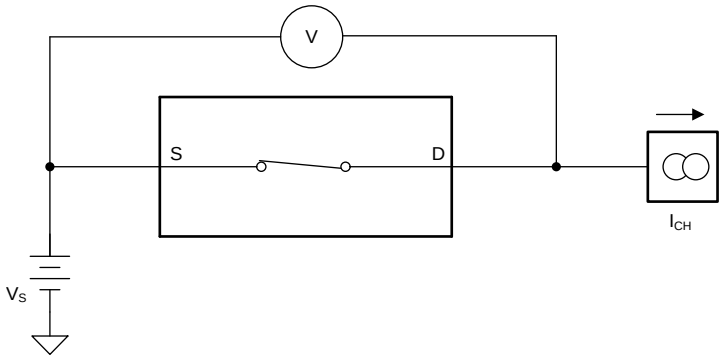


Figure 1. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

9.1.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 2

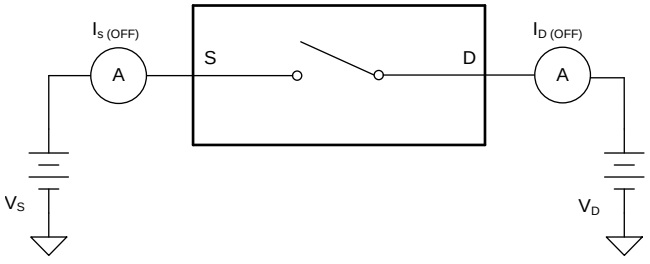


Figure 2. Off-Leakage Measurement Setup

ADVANCE INFORMATION

Overview (continued)

9.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. Figure 3 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

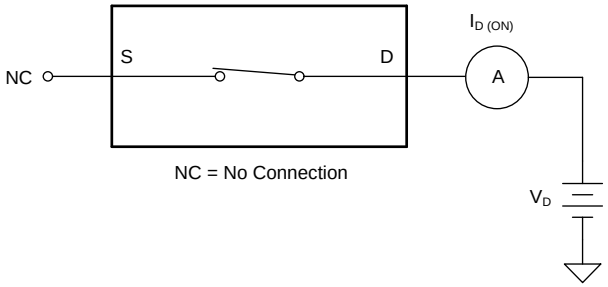


Figure 3. On-Leakage Measurement Setup

9.1.4 Break-Before-Make Delay

The break-before-make delay is a safety feature of the TMUX6113 switch. The TMUX6113's ON switches first break the connection before the OFF switches make connection. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 4 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

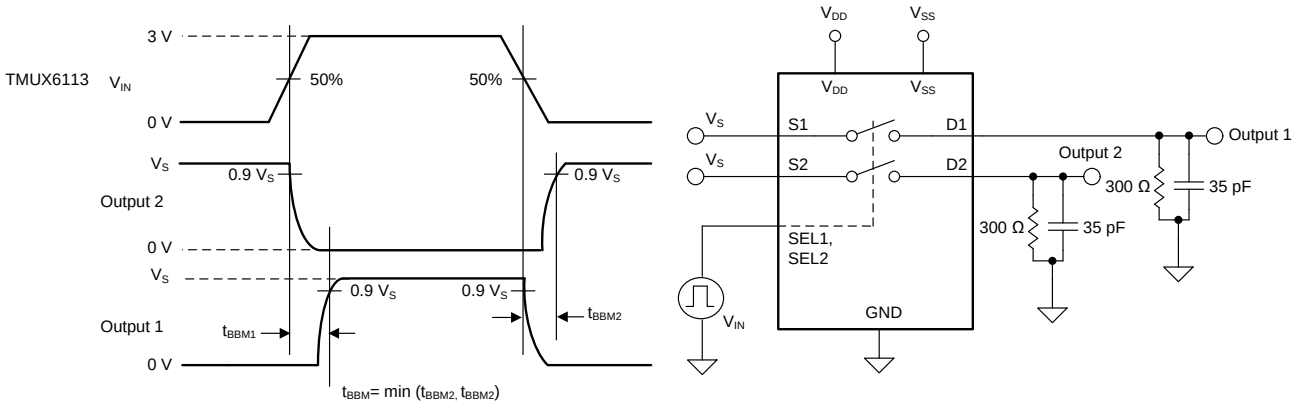


Figure 4. Break-Before-Make Delay Measurement Setup

9.1.5 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the TMUX611x to rise to a 90% final value after the SELx signal has risen (for NC switches) or fallen (for NO switches) to a 50% final value. Figure 5 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol t_{ON}.

Turn off time is defined as the time taken by the output of the TMUX611x to fall to a 10% initial value after the SELx signal has fallen (for NC switches) or risen (for NO switches) to a 50% initial value. Figure 5 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol t_{OFF}.

ADVANCE INFORMATION

Overview (continued)

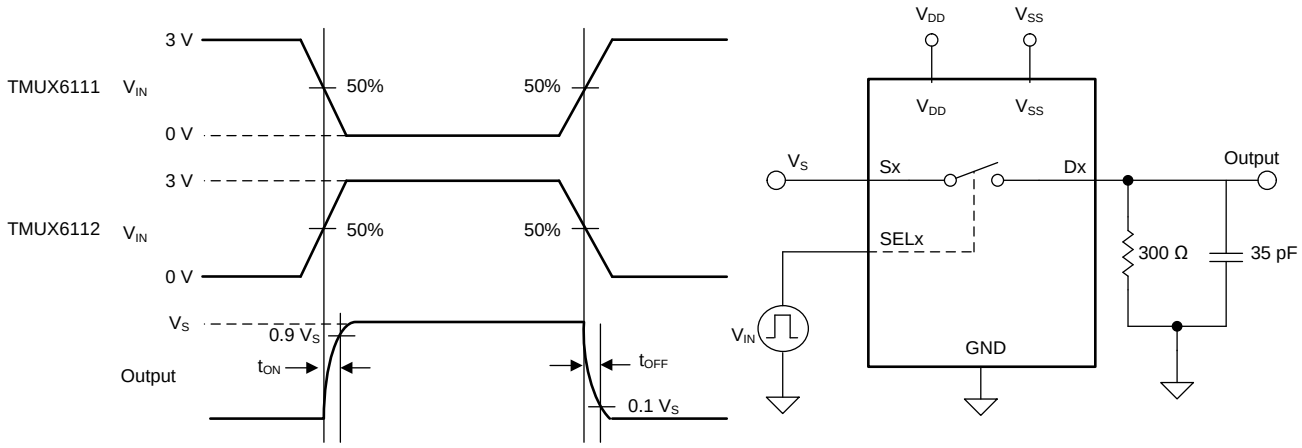


Figure 5. Turn-On and Turn-Off Time Measurement Setup

9.1.6 Charge Injection

The TMUX611x have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. Figure 6 shows the setup used to measure charge injection.

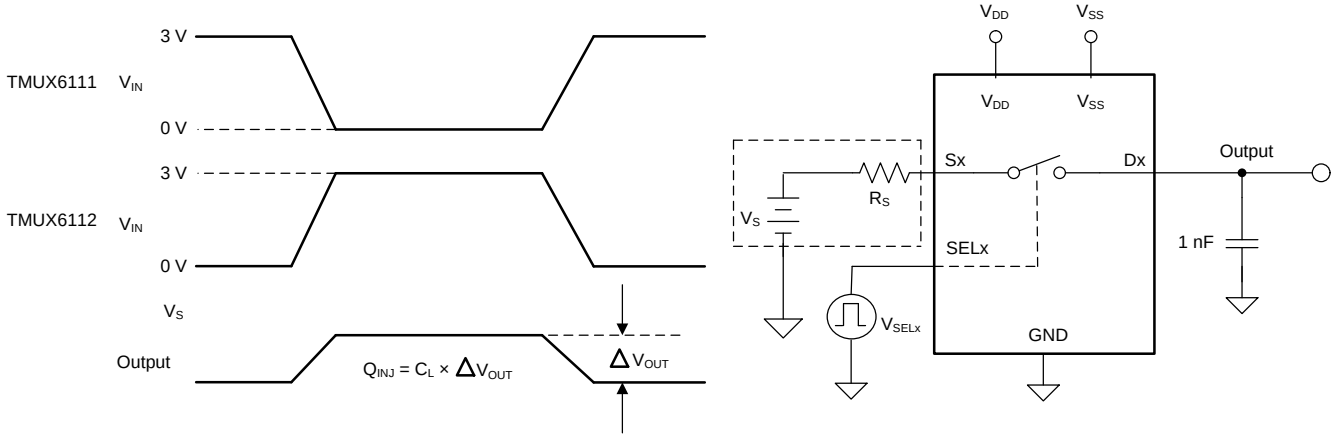


Figure 6. Charge-Injection Measurement Setup

9.1.7 Off Isolation

Off isolation is defined as the voltage at the drain pin (Dx) of the TMUX611x when a 1-V_{RMS} signal is applied to the source pin (Sx) of an OFF switch. Figure 7 shows the setup used to measure off isolation. Use Equation 2 to compute off isolation.

ADVANCE INFORMATION

Overview (continued)

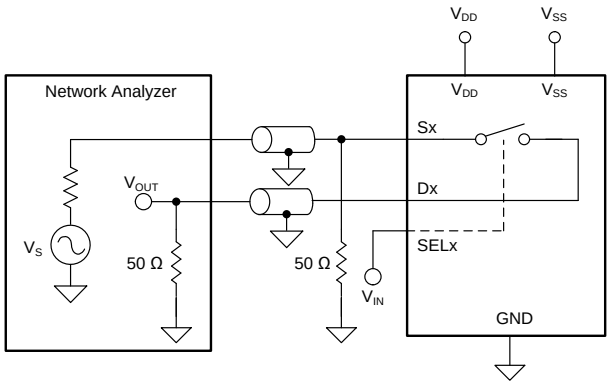


Figure 7. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

9.1.8 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx) of an off-channel, when a 1-V_{RMS} signal is applied at the source pin of an on-channel. Figure 8 shows the setup used to measure, and Equation 3 is the equation used to compute, channel-to-channel crosstalk.

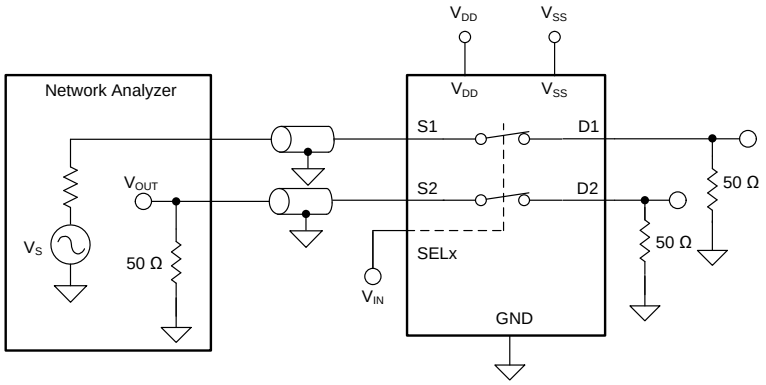


Figure 8. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

9.1.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the TMUX611x. Figure 9 shows the setup used to measure bandwidth of the switch. Use Equation 4 to compute the attenuation.

ADVANCE INFORMATION

Overview (continued)

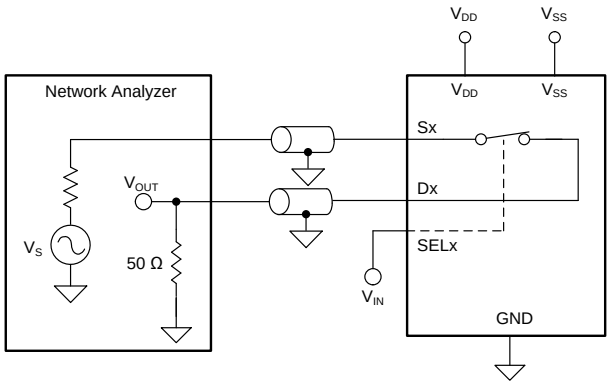


Figure 9. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \quad (4)$$

9.1.10 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX611x varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 10 shows the setup used to measure THD+N of the TMUX611x.

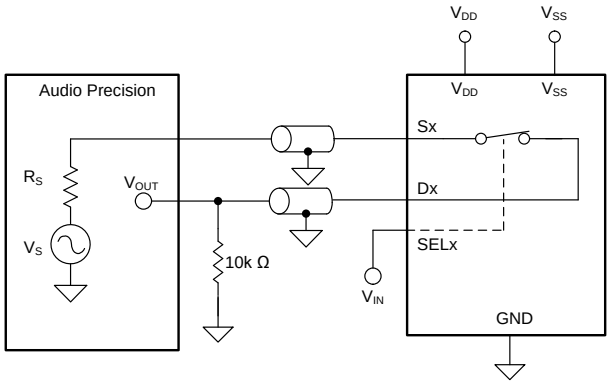
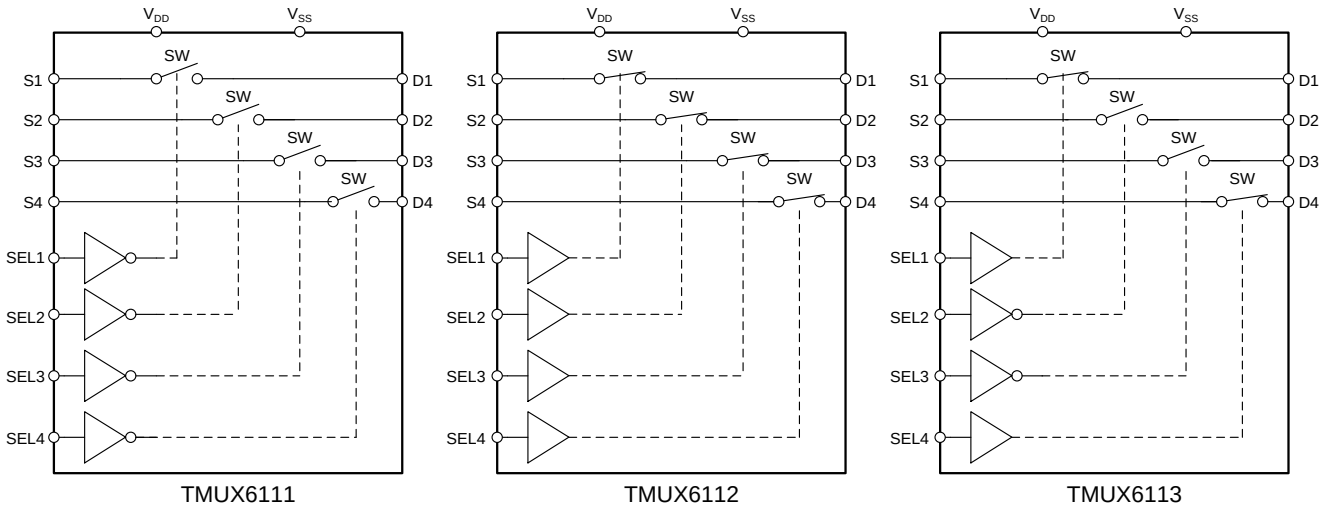


Figure 10. THD+N Measurement Setup

ADVANCE INFORMATION

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Ultra-low Leakage Current

The TMUX611x provide extremely low on- and off-leakage currents. The devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. Figure 11 shows typical leakage currents of the devices versus temperature.

Figure 11. Leakage Current vs Temperature

9.3.2 Ultra-low Charge Injection

The TMUX611x are implemented with simple transmission gate topology, as shown in Figure 12. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed. The devices utilize special charge-injection cancellation circuitry that reduces the source (Sx)-to-drain (Dx) charge injection to as low as –0.6 pC at V_S = 0 V, as shown in Figure 13.

ADVANCE INFORMATION

Feature Description (continued)

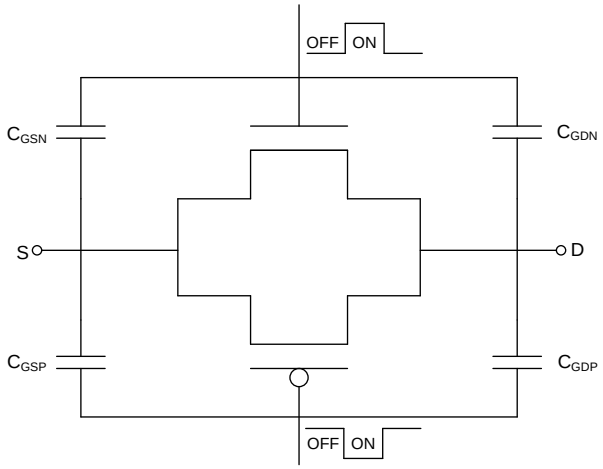


Figure 12. Transmission Gate Topology

Figure 13. Source-to-Drain Charge Injection vs Source or Drain Voltage

9.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX611x conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel of the switches has very similar characteristics in both directions. The input signal to the devices swings from V_{SS} to V_{DD} without any significant degradation in performance. The on-resistance of these devices varies with input signal.

9.4 Device Functional Modes

Each channel of the TMUX611x is turned on or turned off based on the state of its corresponding SELx pin. The SELx pins are weakly pulled-down through an internal 6M ohm resistor, allowing the switches to stay in a determined state when power is applies to the devices. The SELx pins can be connected to V_{DD}.

ADVANCE INFORMATION

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TMUX611x family offers outstanding input/output leakage currents and ultralow charge injection. These devices operate up to 33 (dual supply) or 16.5V (single supply), and offer true rail-to-rail input and output. The on-capacitance of the TMUX611x is very low. These features makes the TMUX611x a family of precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

10.2 Typical Application

One useful application to take advantage of TMUX611x family's precision performance is the sample and hold circuit. A sample and hold circuit can be useful for an analog to digital converter (ADC) to sample a varying input voltage with improved reliability and stability. It can also be used to store the output samples from a single digital-to-analog converter (DAC) in a multi-output application. A simple sample and hold circuit can be realized using an analog switch like one of the TMUX611x analog switches.

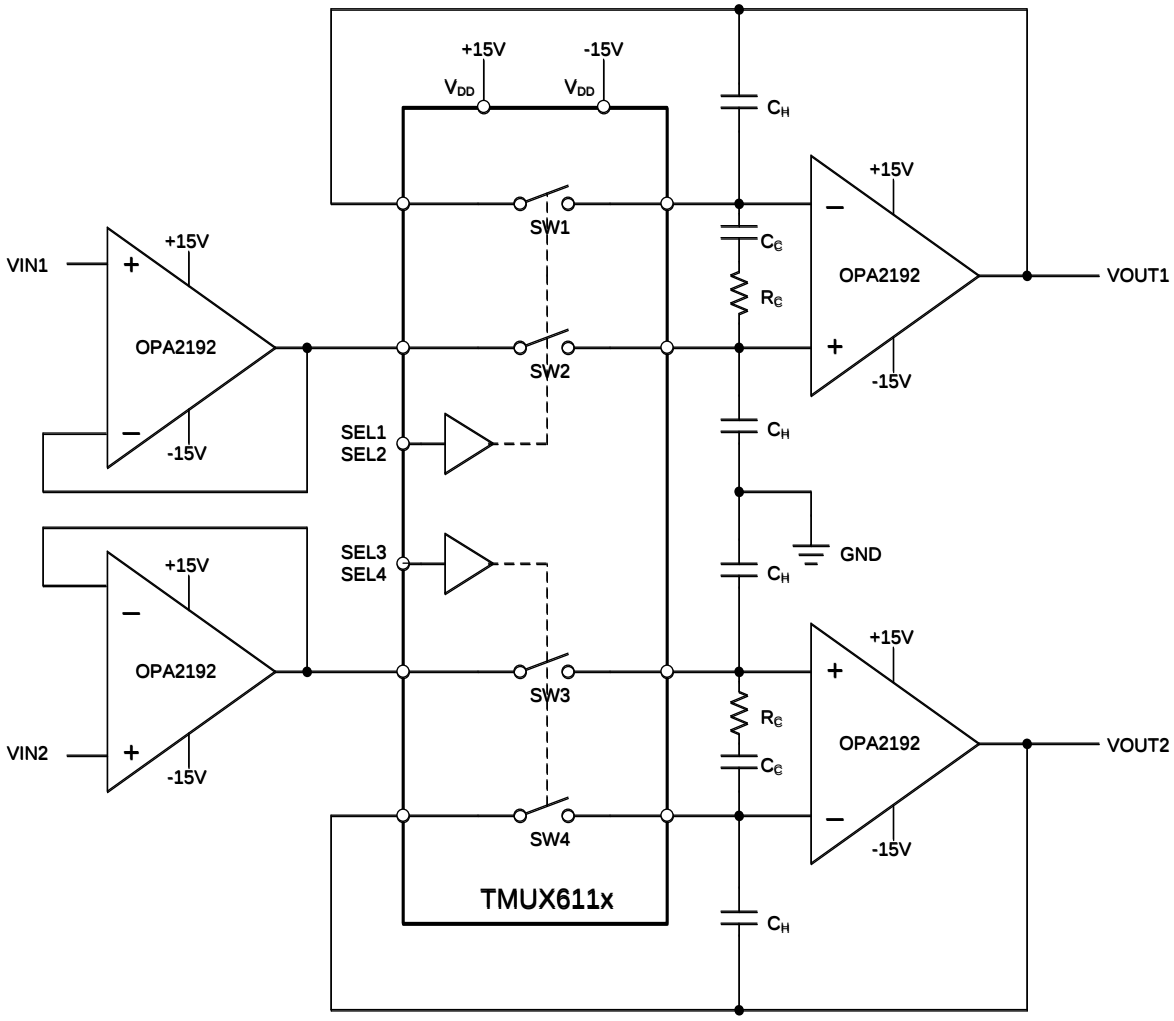


Figure 14. A 2-output Sample and Hold Circuit Realized Using the TMUX611x Analog Switch

ADVANCE INFORMATION

Typical Application (continued)

10.2.1 Design Requirements

The purpose of this precision design is to implement an optimized 2-output sample and hold circuit using a 4-channel SPST switch. The sample and hold circuit needs to be capable of supporting high voltage output swing up to ± 15V with minimized pedestal error and fast settling time. The overall system block diagram is illustrated in Figure 14.

10.2.2 Detailed Design Procedure

The TMUX611x switch is used in conjunction with the voltage holding capacitors (C_H) to implement the sample and hold circuit. The basic operation is:

1. When the switch (SW2 or SW3) is closed, it samples the input voltage and charges the holding capacitors (C_H) to the input voltages values.
2. When the switch (SW2 or SW3) is open, the holding capacitors (C_H) holds its previous value, maintaining stable voltage at the amplifier output (V_{OUT}).

Ideally, the switch delivers only the input signals to the holding capacitors. However, when the switch gets toggled, some amount of charge also gets transferred to the switch output in the form of charge injection, resulting slight sampling error. The TMUX611x switch family has excellent charge injection performance of only 0.6 pC, making it an ideal choice for this implementation to minimize sampling error.

Due to switch and capacitor leakage current, the voltage on the hold capacitors droops with time. The TMUX611x minimizes the droops due to its ultra-low leakage performance. At 25°C, the TMUX611x has extremely tiny leakage current at 1pA typical and 20pA max.

The TMUX611x device is also selected due to its high voltage capability. The device supports up to ± 16.5 V dual supply operation, making it an ideal solution in this high voltage sample and hold application.

A second switch SW1 (or SW4) is also included to operate in parallel with SW2 (or SW3) to reduce pedestal error during switch toggling. Because both switches are driven at the same potential, they act as common-mode signal to the op-amp, thereby minimizing the charge injection effects caused by the switch toggling action. Compensation network consisting of R_C and C_C is also added to further reduce the pedestal error, whiling reducing the hold-time glitch and improving the settling time of the circuit.

ADVANCE INFORMATION

11 Power Supply Recommendations

The TMUX611x operates across a wide supply range of ±5 V to ±16.5 V (10 V to 16.5 V in single-supply mode). They also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped. As a best practice, it is recommended to ramp V_{SS} first before V_{DD} in dual or asymmetrical supply applications.

The on-resistance of the devices varies with supply voltage, as illustrated in Figure 15

Figure 15. On-Resistance Variation With Supply and Input Voltage

12 Layout

12.1 Layout Guidelines

Figure 16 illustrates an example of a PCB layout with the TMUX6112PW. Some key considerations are:

- Decouple the V_{DD} and V_{SS} pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

12.2 Layout Example

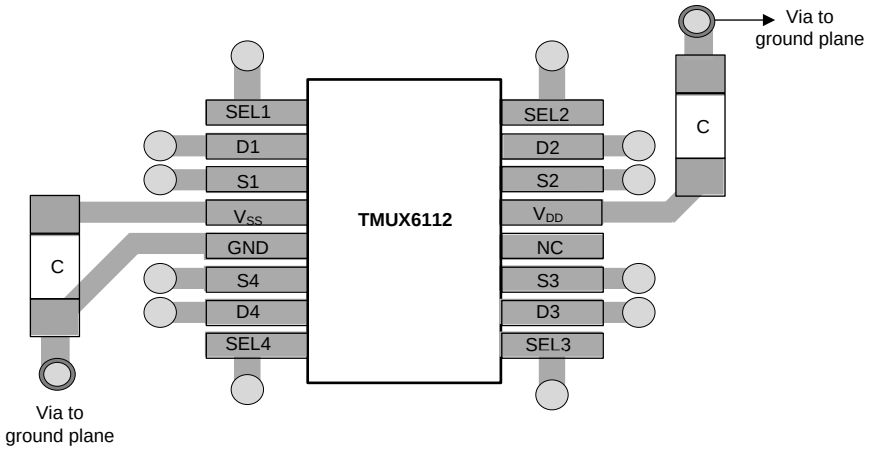


Figure 16. TMUX611x Layout Example

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

- *ADS8664 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges* (SBAS492)
- *OPA140 High-Precision, Low-Noise, Rail-to-Rail Output, 11-MHz JFET Op Amp* (SBOS498)
- *OPA192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-Trim™* (SBOS620)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TMUX6111	Click here	Click here	Click here	Click here	Click here
TMUX6112	Click here	Click here	Click here	Click here	Click here
TMUX6113	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX6112PWR	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125		Samples
TMUX6111PWR	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125		
TMUX6111RTER	PREVIEW	WQFN	RTE	16	3000	TBD	Call TI	Call TI	-40 to 125		
TMUX6112PWR	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125		
TMUX6112RTER	PREVIEW	WQFN	RTE	16	3000	TBD	Call TI	Call TI	-40 to 125		
TMUX6113PWR	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125		
TMUX6113RTER	PREVIEW	WQFN	RTE	16	3000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

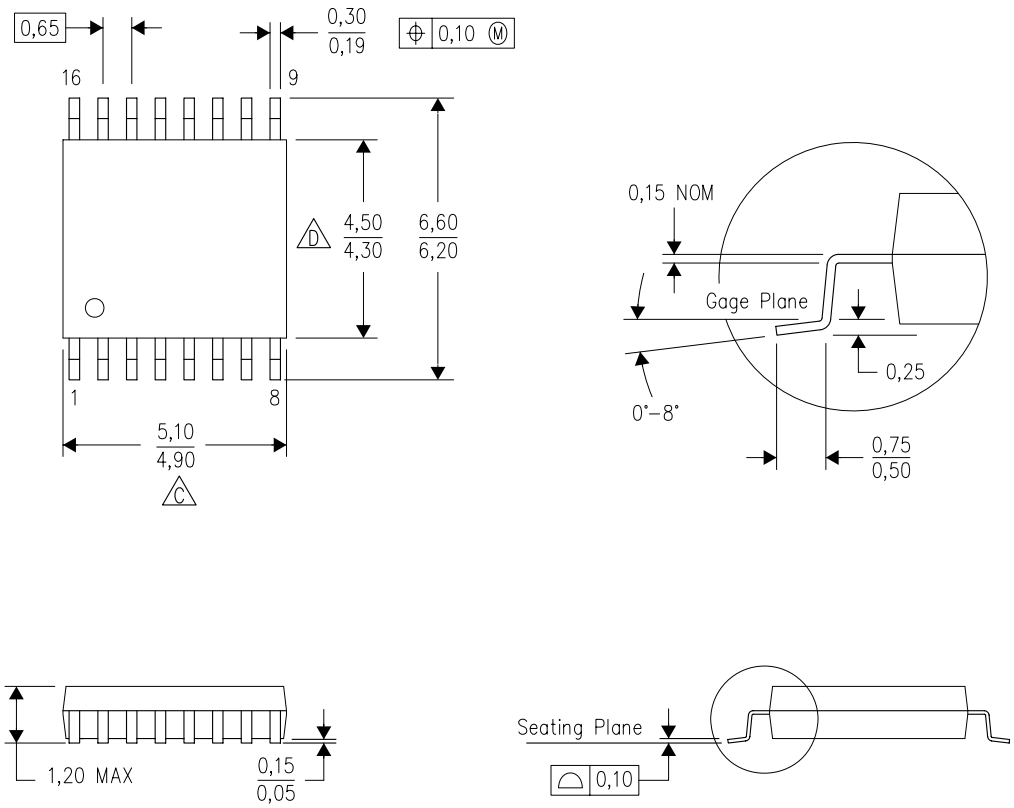
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

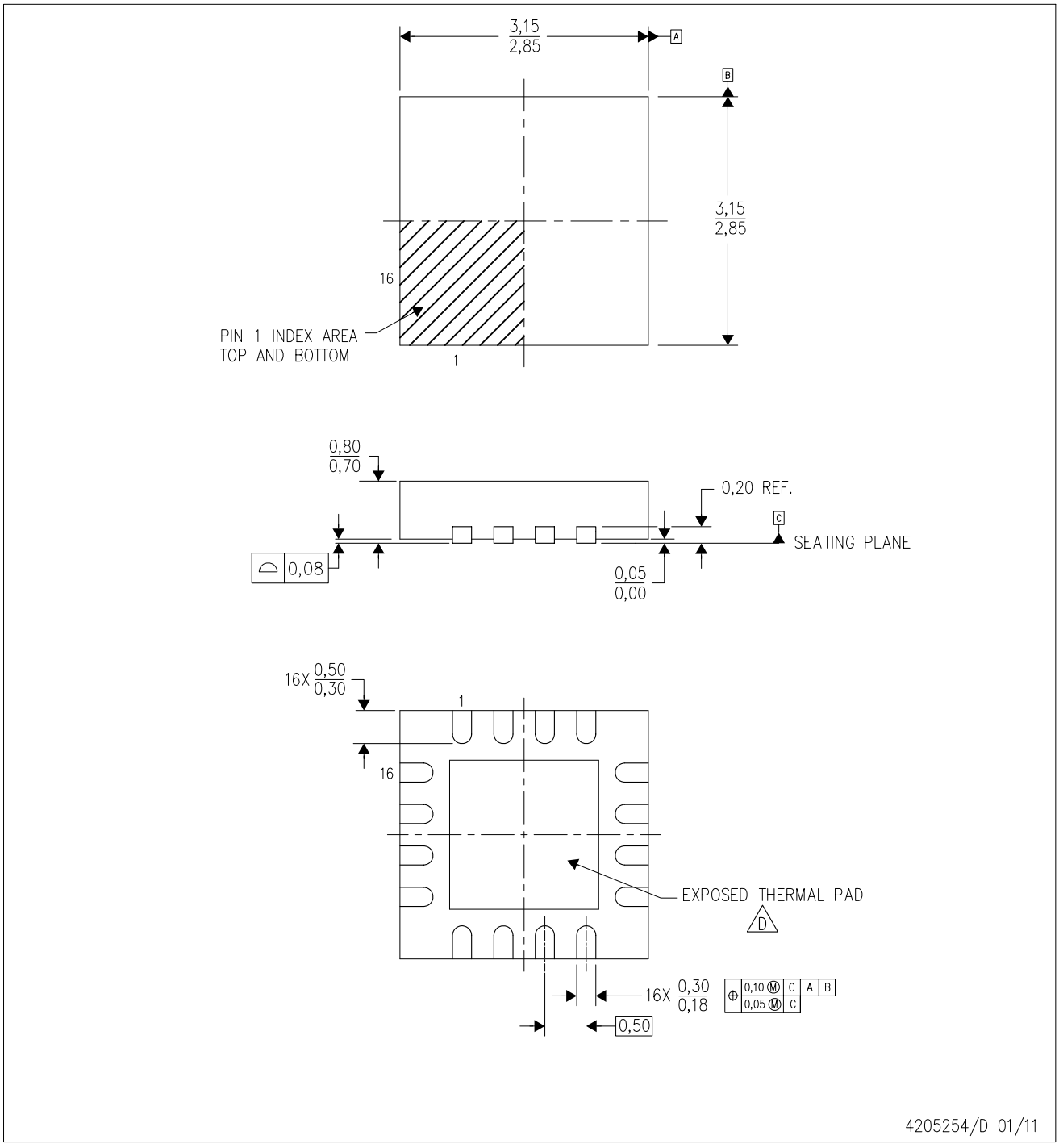
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265