LM6171 High Speed Low Power Low Distortion Voltage Feedback Amplifier

Check for Samples: LM6171

FEATURES

- **(Typical Unless Otherwise Noted)**
- **Easy-To-Use Voltage Feedback Topology**
- **Very High Slew Rate: 3600V/µs**
- **Wide Unity-Gain-Bandwidth Product: 100 MHz**
- **−3dB Frequency @ A_V = +2: 62 MHz**
- **Low Supply Current: 2.5 mA**
- **High CMRR: 110 dB**
- **High Open Loop Gain: 90 dB**
- **Specified for ±15V and ±5V Operation**

APPLICATIONS

- **Multimedia Broadcast Systems**
- **Line Drivers, Switchers**
- **Video Amplifiers**
- **NTSC, PAL® and SECAM Systems**
- **ADC/DAC Buffers**
- **HDTV Amplifiers**
- **Pulse Amplifiers and Peak Detectors**
- **Instrumentation Amplifier**
- **Active Filters**

DESCRIPTION

The LM6171 is a high speed unity-gain stable voltage feedback amplifier. It offers a high slew rate of 3600V/µs and a unity-gain bandwidth of 100 MHz while consuming only 2.5 mA of supply current. The LM6171 has very impressive AC and DC performance which is a great benefit for high speed signal processing and video applications.

The ±15V power supplies allow for large signal swings and give greater dynamic range and signal-to-noise ratio. The LM6171 has high output current drive, low SFDR and THD, ideal for ADC/DAC systems. The LM6171 is specified for ±5V operation for portable applications.

The LM6171 is built on TI's advanced VIP III (Vertically Integrated PNP) complementary bipolar process.

CONNECTION DIAGRAM

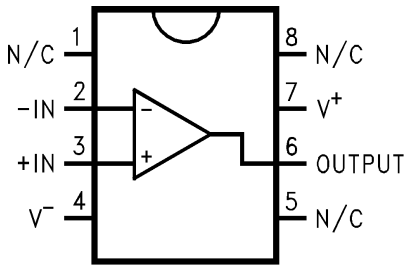

Figure 1. Top View
8-Pin SOIC/PDIP
See Package Number D (SOIC) or
See Package Number P (PDIP)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)		2.5 kV
Supply Voltage (V^+–V^-)		36V
Differential Input Voltage		±10V
Common-Mode Voltage Range		V^++0.3V to V^- −0.3V
Input Current		±10mA
Output Short Circuit to Ground(4)		Continuous
Storage Temperature Range		−65°C to +150°C
Maximum Junction Temperature(5)		150°C
Soldering Information	Infrared or Convection Reflow (20 sec.)	235°C
	Wave Soldering Lead Temp (10 sec.)	260°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(3) Human body model, 1.5 kΩ in series with 100 pF.
(4) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings(1)

Supply Voltage		$5.5V \le V_S \le 34V$
Operating Temperature Range	LM6171AI, LM6171BI	−40°C to +85°C
Thermal Resistance (θ_{JA})	P Package, 8-Pin PDIP	108°C/W
	D Package, 8-Pin SOIC	172°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

±15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	LM6171AI Limit (2)	LM6171BI Limit (2)	Units
V_{OS}	Input Offset Voltage		1.5	3 **5**	6 **8**	mV max
TC V_{OS}	Input Offset Voltage Average Drift		6			µV/°C
I_B	Input Bias Current		1	3 **4**	3 **4**	µA max
I_{OS}	Input Offset Current		0.03	2 **3**	2 **3**	µA max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	4.9			
R_O	Open Loop Output Resistance		14			Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	110	80 **75**	75 **70**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	95	85 **80**	80 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 60 dB	±13.5			V
A_V	Large Signal Voltage Gain (3)	R_L = 1 kΩ	90	80 **70**	80 **70**	dB min
		R_L = 100Ω	83	70 **60**	70 **60**	dB min
V_O	Output Swing	R_L = 1 kΩ	13.3	12.5 **12**	12.5 **12**	V min
			−13.3	−12.5 **−12**	−12.5 **−12**	V max
		R_L = 100Ω	11.6	9 **8.5**	9 **8.5**	V min
			−10.5	−9 **−8.5**	−9 **−8.5**	V max
	Continuous Output Current (Open Loop) (4)	Sourcing, R_L = 100Ω	116	90 **85**	90 **85**	mA min
		Sinking, R_L = 100Ω	105	90 **85**	90 **85**	mA max
	Continuous Output Current (in Linear Region)	Sourcing, R_L = 10Ω	100			mA
		Sinking, R_L = 10Ω	80			mA
I_{SC}	Output Short Circuit Current	Sourcing	135			mA
		Sinking	135			mA
I_S	Supply Current		2.5	4 **4.5**	4 **4.5**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = +5V, V_{OUT} = ±1V.
(4) The open loop output current is the output swing with the 100Ω load resistor divided by that resistor.

±15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	LM6171AI Limit (2)	LM6171BI Limit (2)	Units
SR	Slew Rate (3)	A_V = +2, V_{IN} = 13 V_{PP}	3600			V/µs
		A_V = +2, V_{IN} = 10 V_{PP}	3000			
GBW	Unity Gain-Bandwidth Product		100			MHz
	−3 dB Frequency	A_V = +1	160			MHz
		A_V = +2	62			MHz
φm	Phase Margin		40			deg
t_s	Settling Time (0.1%)	A_V = −1, V_{OUT} = ±5V R_L = 500Ω	48			ns
	Propagation Delay	V_{IN} = ±5V, R_L = 500Ω, A_V = −2	6			ns
A_D	Differential Gain (4)		0.03			%
$φ_D$	Differential Phase (4)		0.5			deg
e_n	Input-Referred Voltage Noise	f = 1 kHz	12			nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz	1			pA/√Hz

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Differential gain and phase are measured with A_V = +2, V_{IN} = 1 V_{PP} at 3.58 MHz and both input and output 75Ω terminated.

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	LM6171AI Limit (2)	LM6171BI Limit (2)	Units
V_{OS}	Input Offset Voltage		1.2	3 **5**	6 **8**	mV max
TC V_{OS}	Input Offset Voltage Average Drift		4			µV/°C
I_B	Input Bias Current		1	2.5 **3.5**	2.5 **3.5**	µA max
I_{OS}	Input Offset Current		0.03	1.5 **2.2**	1.5 **2.2**	µA max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	4.9			
R_O	Open Loop Output Resistance		14			Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V	105	80 **75**	75 **70**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	95	85 **80**	80 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 60 dB	±3.7			V
A_V	Large Signal Voltage Gain (3)	R_L = 1 kΩ	84	75 **65**	75 **65**	dB min
		R_L = 100Ω	80	70 **60**	70 **60**	dB min
V_O	Output Swing	R_L = 1 kΩ	3.5	3.2 **3**	3.2 **3**	V min
			−3.4	−3.2 **−3**	−3.2 **−3**	V max
		R_L = 100Ω	3.2	2.8 **2.5**	2.8 **2.5**	V min
			−3.0	−2.8 **−2.5**	−2.8 **−2.5**	V max
	Continuous Output Current (Open Loop) (4)	Sourcing, R_L = 100Ω	32	28 **25**	28 **25**	mA min
		Sinking, R_L = 100Ω	30	28 **25**	28 **25**	mA max
I_{SC}	Output Short Circuit Current	Sourcing	130			mA
		Sinking	100			mA
I_S	Supply Current		2.3	3 **3.5**	3 **3.5**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = +5V, V_{OUT} = ±1V.
(4) The open loop output current is the output swing with the 100Ω load resistor divided by that resistor.

±5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	LM6171AI Limit (2)	LM6171BI Limit (2)	Units
SR	Slew Rate (3)	A_V = +2, V_{IN} = 3.5 V_{PP}	750			V/µs
GBW	Unity Gain-Bandwidth Product		70			MHz
	−3 dB Frequency	A_V = +1	130			MHz
		A_V = +2	45			
φm	Phase Margin		57			deg
t_s	Settling Time (0.1%)	A_V = −1, V_{OUT} = +1V, R_L = 500Ω	60			ns
	Propagation Delay	V_{IN} = ±1V, R_L = 500Ω, A_V = −2	8			ns
A_D	Differential Gain (4)		0.04			%
$φ_D$	Differential Phase (4)		0.7			deg
e_n	Input-Referred Voltage Noise	f = 1 kHz	11			nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz	1			pA/√Hz

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Differential gain and phase are measured with A_V = +2, V_{IN} = 1 V_{PP} at 3.58 MHz and both input and output 75Ω terminated.

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C

Supply Current vs. Supply Voltage

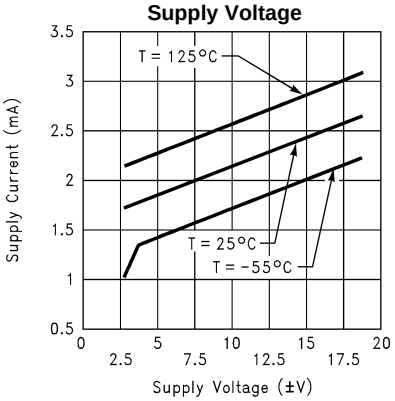


Figure 2.

Supply Current vs. Temperature

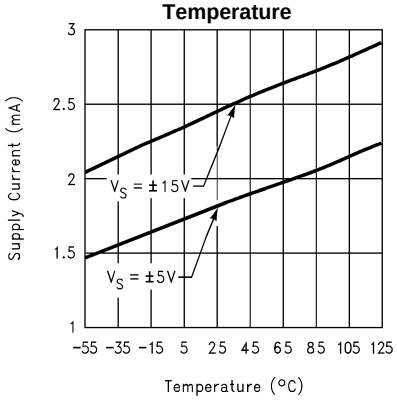


Figure 3.

Input Offset Voltage vs. Temperature

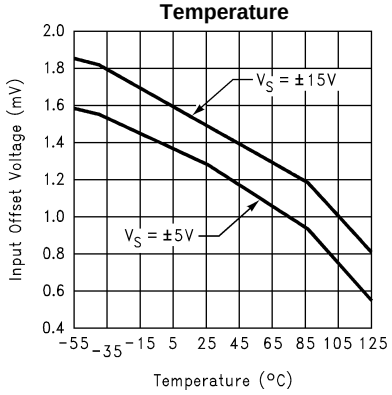


Figure 4.

Input Bias Current vs. Temperature

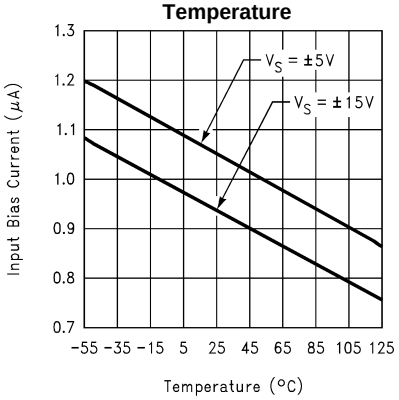


Figure 5.

Input Offset Voltage vs. Common Mode Voltage

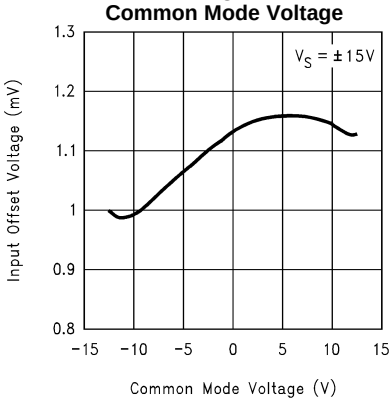


Figure 6.

Short Circuit Current vs. Temperature (Sourcing)

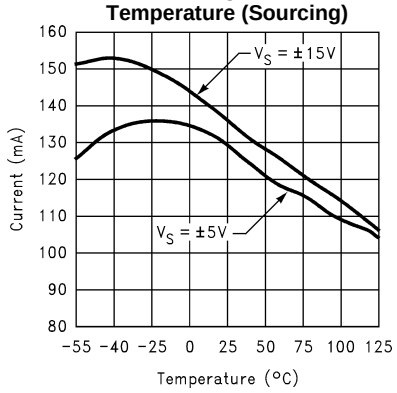


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

Short Circuit Current vs. Temperature (Sinking)

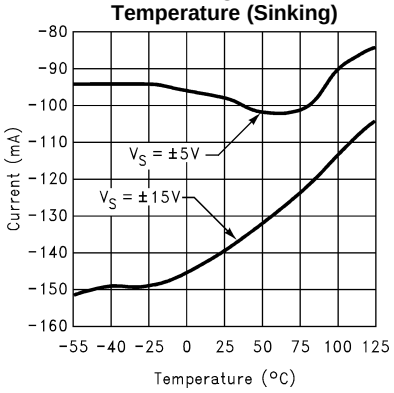


Figure 8.

Output Voltage vs. Output Current

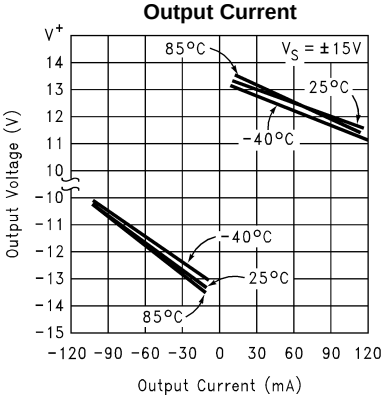


Figure 9.

Output Voltage vs. Output Current

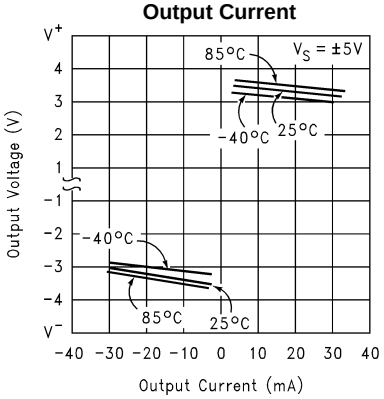


Figure 10.

CMRR vs. Frequency

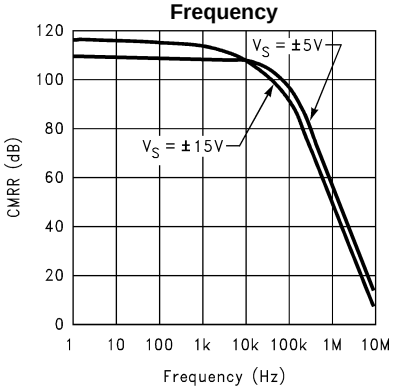


Figure 11.

PSRR vs. Frequency

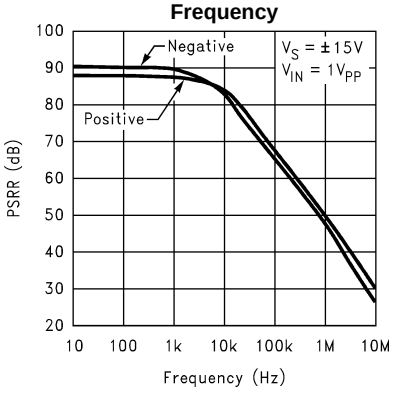


Figure 12.

PSRR vs. Frequency

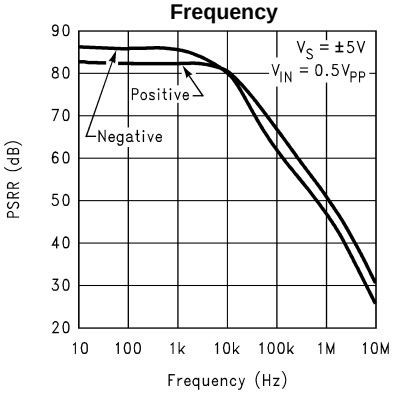


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

Open Loop Frequency Response

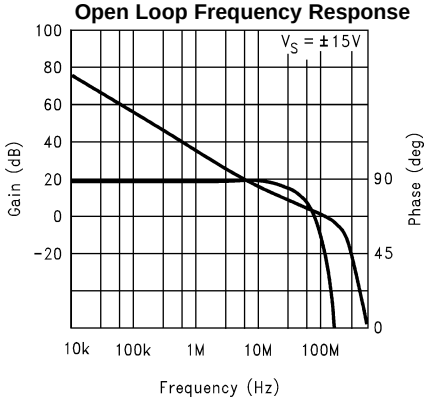


Figure 14.

Open Loop Frequency Response

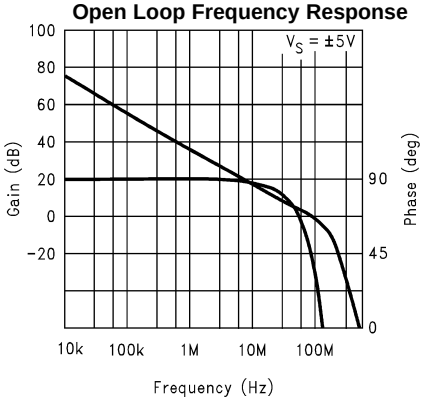


Figure 15.

Gain Bandwidth Product vs. Supply Voltage

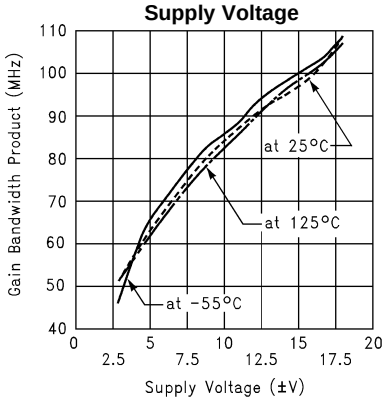


Figure 16.

Gain Bandwidth Product vs. Load Capacitance

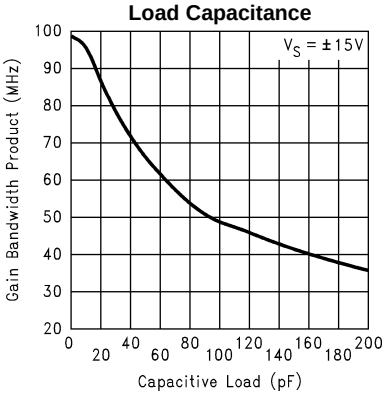


Figure 17.

Large Signal Voltage Gain vs. Load

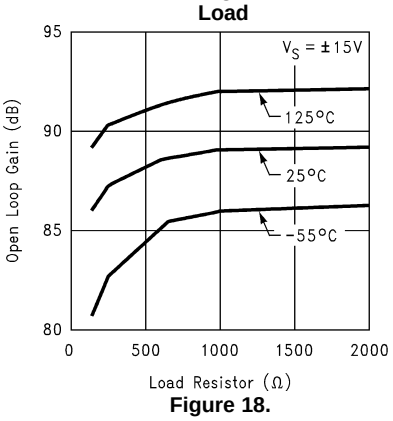


Figure 18.

Large Signal Voltage Gain vs. Load

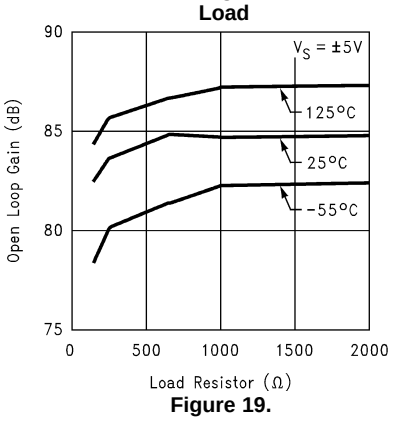


Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

Input Voltage Noise vs. Frequency

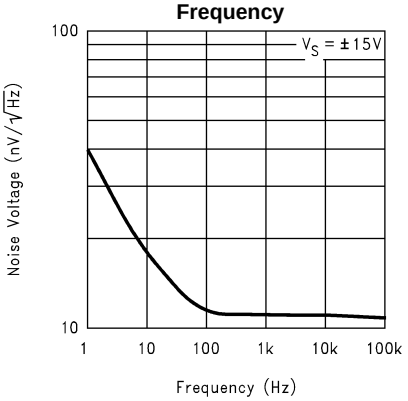


Figure 20.

Input Voltage Noise vs. Frequency

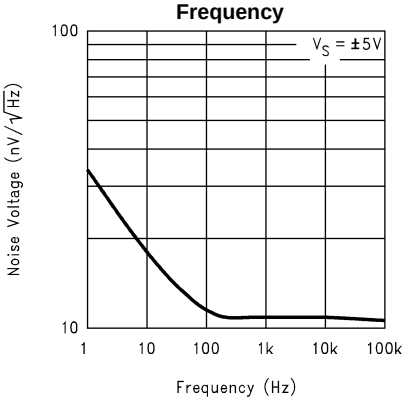


Figure 21.

Input Current Noise vs. Frequency

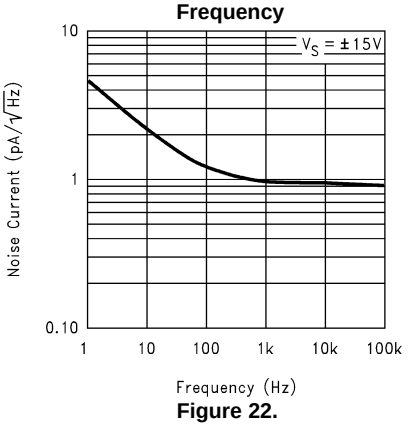


Figure 22.

Input Current Noise vs. Frequency

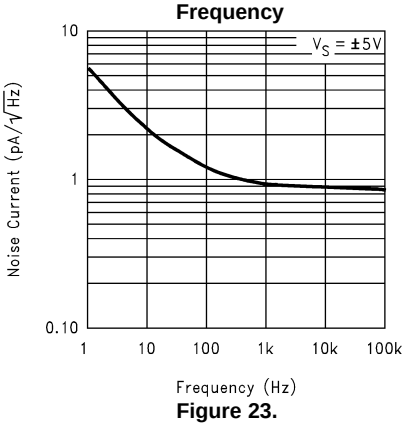


Figure 23.

Slew Rate vs. Supply Voltage

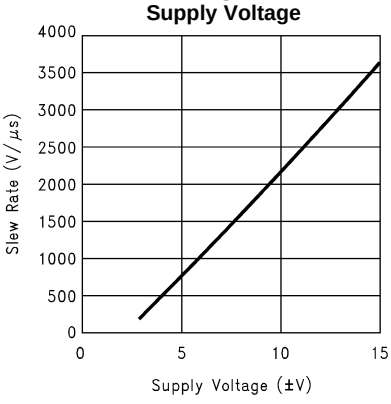


Figure 24.

Slew Rate vs. Input Voltage

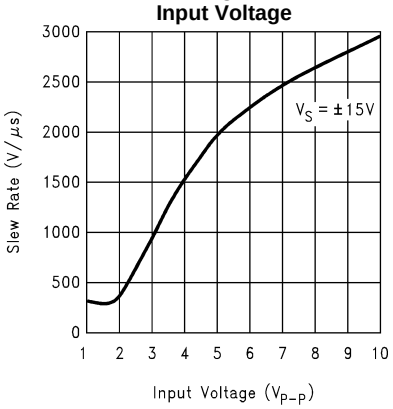


Figure 25.

Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

Slew Rate vs. Load Capacitance

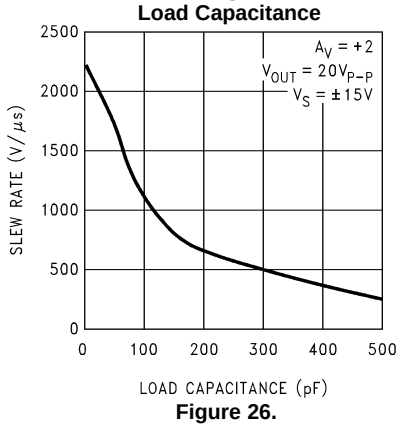


Figure 26.

Open Loop Output Impedance vs. Frequency

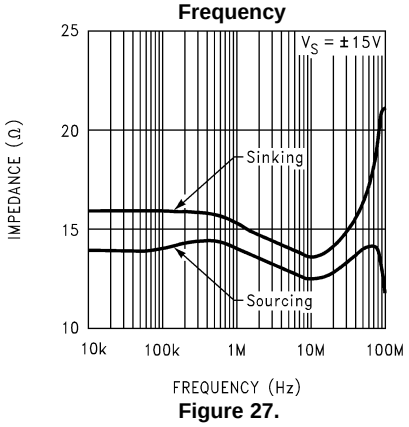


Figure 27.

Open Loop Output Impedance vs. Frequency

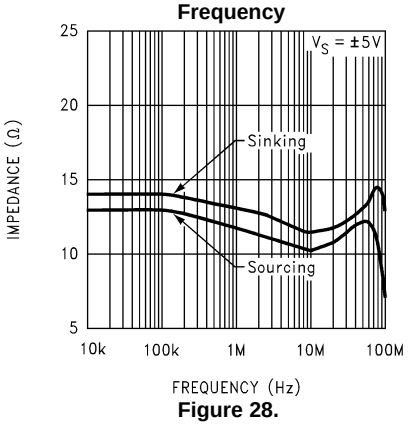


Figure 28.

Large Signal Pulse Response
A_V = −1, V_S = ±15V

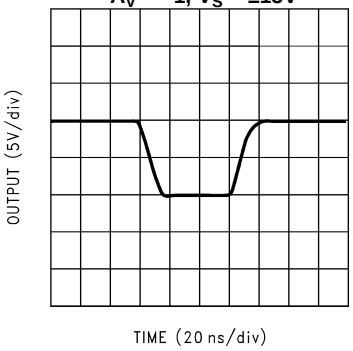


Figure 29.

Large Signal Pulse Response
A_V = −1, V_S = ±5V

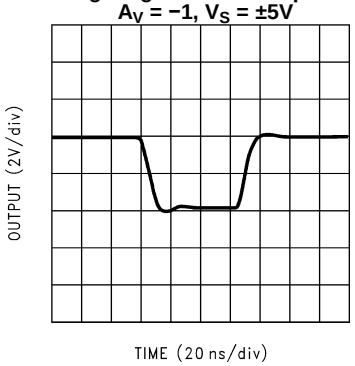


Figure 30.

Large Signal Pulse Response
A_V = +1, V_S = ±15V

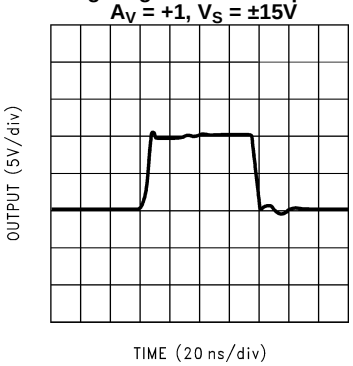


Figure 31.

Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

Large Signal Pulse Response
A_V = +1, V_S = ±5V

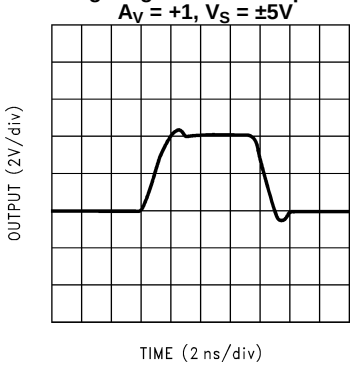


Figure 32.

Large Signal Pulse Response
A_V = +2, V_S = ±15V

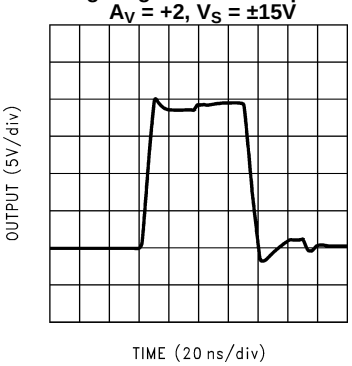


Figure 33.

Large Signal Pulse Response
A_V = +2, V_S = ±5V

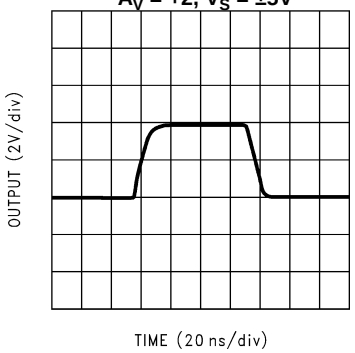


Figure 34.

Small Signal Pulse Response
A_V = −1, V_S = ±15V

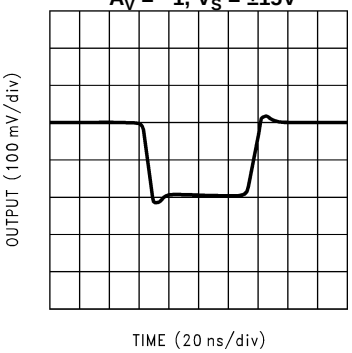


Figure 35.

Small Signal Pulse Response
A_V = −1, V_S = ±5V

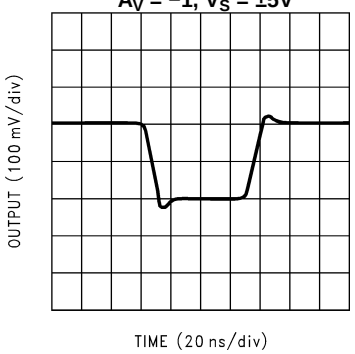


Figure 36.

Small Signal Pulse Response
A_V = +1, V_S = ±15V

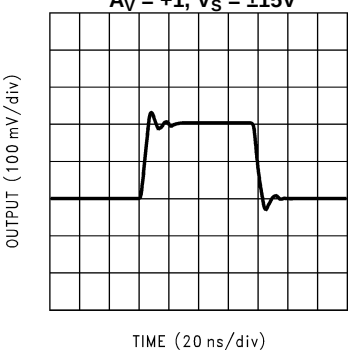


Figure 37.

Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

Small Signal Pulse Response
A_V = +1, V_S = ±5V

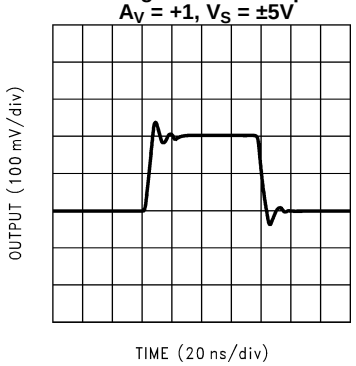


Figure 38.

Small Signal Pulse Response
A_V = +2, V_S = ±15V

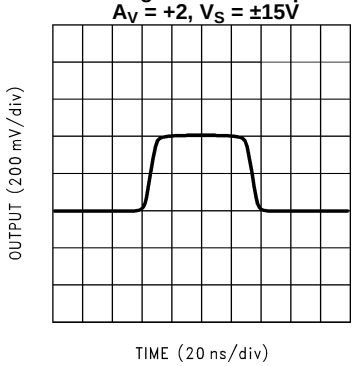


Figure 39.

Small Signal Pulse Response
A_V = +2, V_S = ±5V

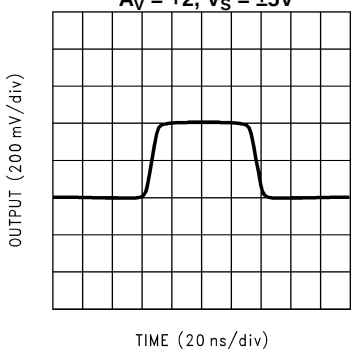


Figure 40.

Closed Loop Frequency Response vs. SupplyVoltage (A_V = +1)

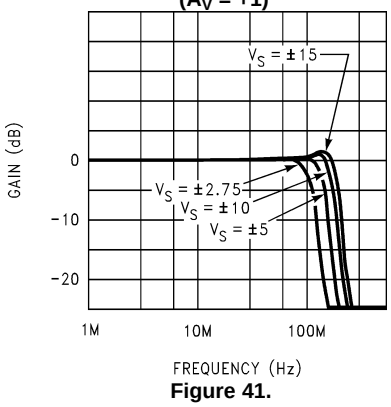


Figure 41.

Closed Loop Frequency Response vs. Supply Voltage (A_V = +2)

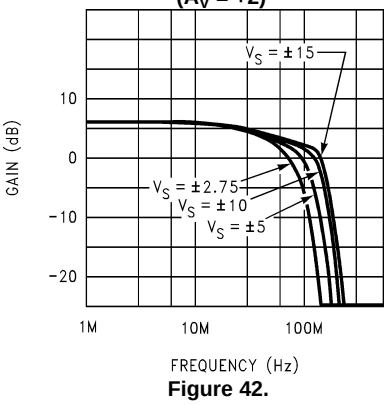


Figure 42.

Closed Loop Frequency Response vs. Capacitive Load (A_V = +1)

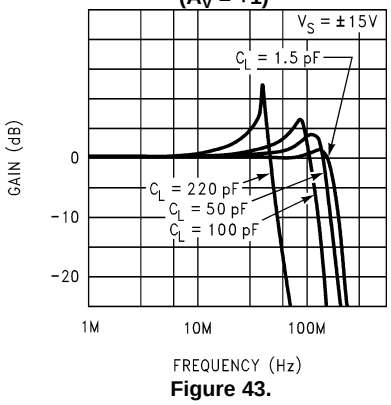


Figure 43.

Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

Closed Loop Frequency Response vs. Capacitive Load (A_V = +1)

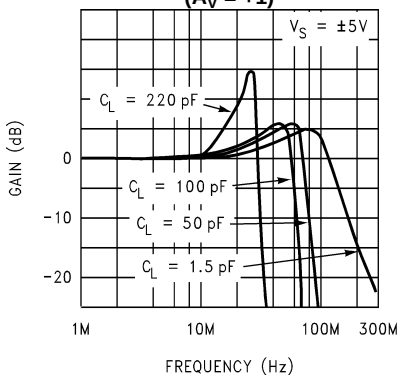


Figure 44.

Closed Loop Frequency Response vs. Capacitive Load (A_V = +2)

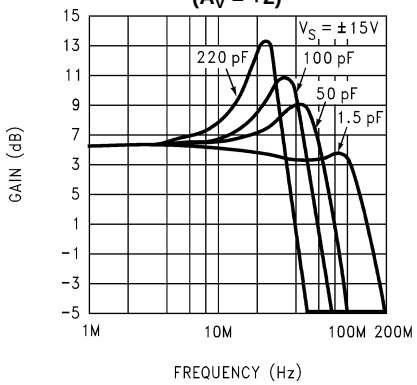


Figure 45.

Closed Loop Frequency Response vs. Capacitive Load (A_V = +2)

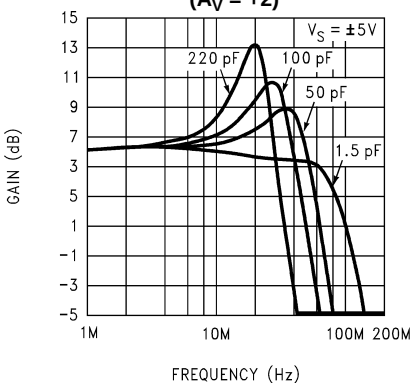


Figure 46.

Total Harmonic Distortion vs. Frequency

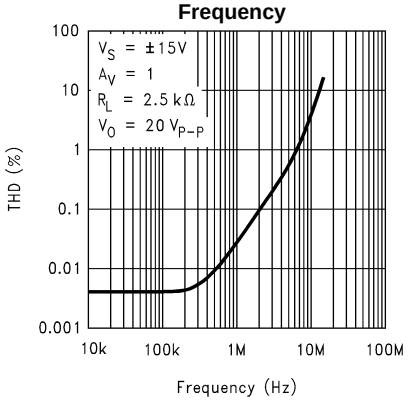


Figure 47.

Total Harmonic Distortion vs. Frequency

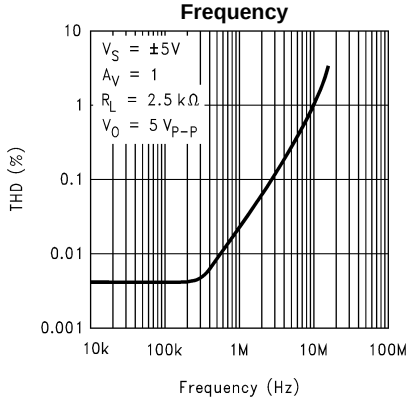


Figure 48.

Total Harmonic Distortion vs. Frequency

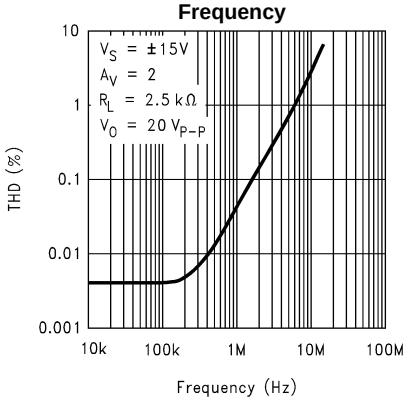


Figure 49.

Typical Performance Characteristics (continued)

Unless otherwise noted, T_A = 25°C

Total Harmonic Distortion vs. Frequency

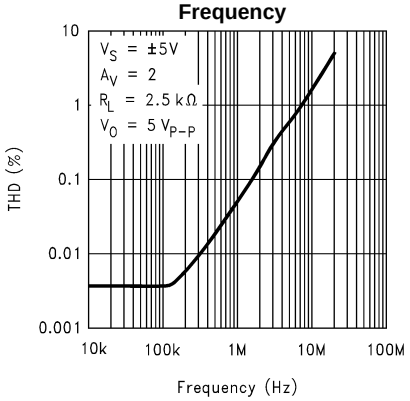


Figure 50.

Undistorted Output Swing vs. Frequency

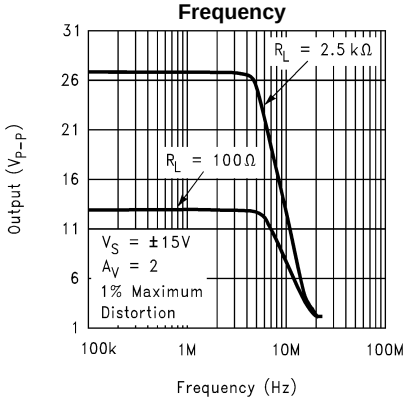


Figure 51.

Undistorted Output Swing vs. Frequency

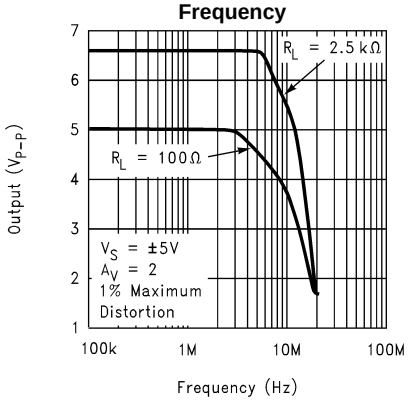


Figure 52.

Undistorted Output Swing vs. Frequency

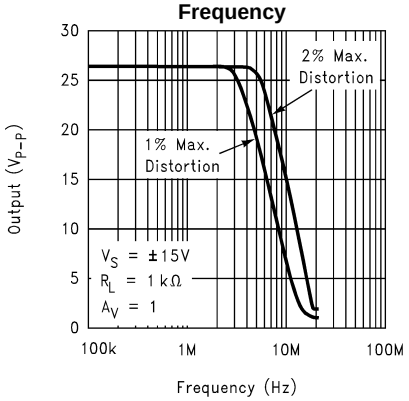


Figure 53.

Undistorted Output Swing vs. Frequency

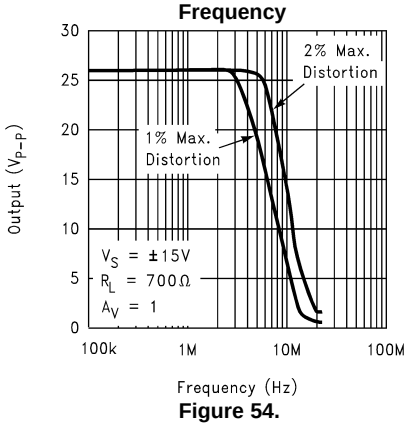


Figure 54.

Total Power Dissipation vs. Ambient Temperature

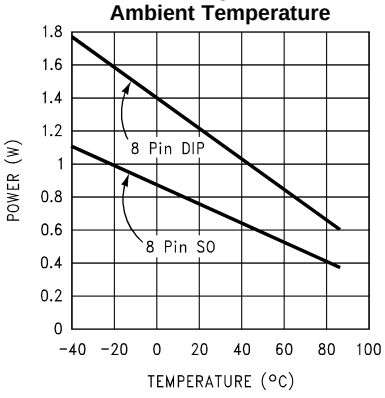


Figure 55.

LM6171 SIMPLIFIED SCHEMATIC

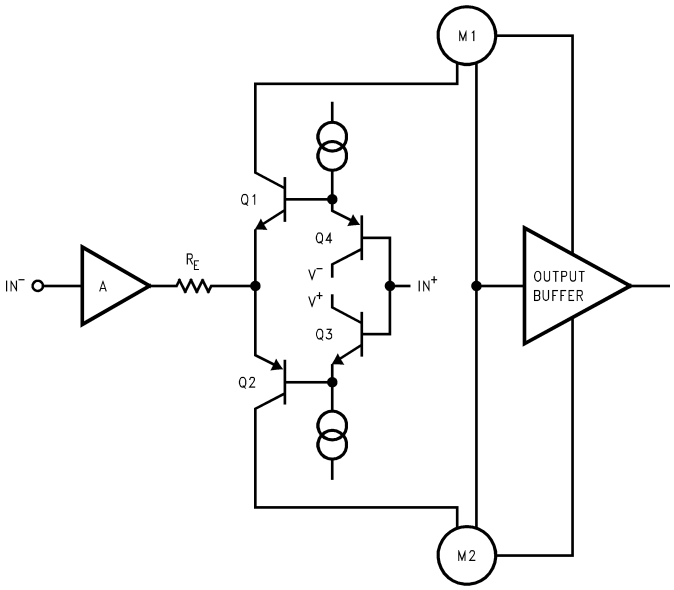


Figure 56.

APPLICATION INFORMATION

LM6171 PERFORMANCE DISCUSSION

The LM6171 is a high speed, unity-gain stable voltage feedback amplifier. It consumes only 2.5 mA supply current while providing a gain-bandwidth product of 100 MHz and a slew rate of 3600V/µs. It also has other great features such as low differential gain and phase and high output current. The LM6171 is a good choice in high speed circuits.

The LM6171 is a true voltage feedback amplifier. Unlike current feedback amplifiers (CFAs) with a low inverting input impedance and a high non-inverting input impedance, both inputs of voltage feedback amplifiers (VFAs) have high impedance nodes. The low impedance inverting input in CFAs will couple with feedback capacitor and cause oscillation. As a result, CFAs cannot be used in traditional op amp circuits such as photodiode amplifiers, I-to-V converters and integrators.

LM6171 CIRCUIT OPERATION

The class AB input stage in LM6171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In LM6171 Figure 56, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM6171 SLEW RATE CHARACTERISTIC

The slew rate of LM6171 is determined by the current available to charge and discharge an internal high impedance node capacitor. The current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor such as 1 kΩ to the input of LM6171, the bandwidth is reduced to help lower the overshoot.

LAYOUT CONSIDERATION

Printed Circuit Boards and High Speed Op Amps

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy and frustrating to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

Using Probes

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

Components Selection And Feedback Resistor

It is important in high speed applications to keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM6171, a feedback resistor of 510Ω gives optimal performance.

COMPENSATION FOR INPUT CAPACITANCE

The combination of an amplifier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F \quad (1)$$

can be used to cancel that pole. For LM6171, a feedback capacitor of 2 pF is recommended. Figure 57 illustrates the compensation circuit.

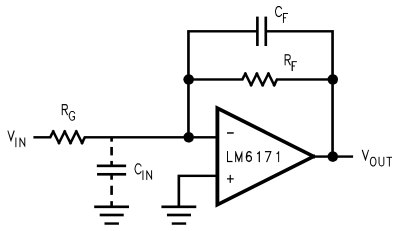


Figure 57. Compensating for Input Capacitance

POWER SUPPLY BYPASSING

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 µF ceramic capacitors directly to power supply pins and 2.2 µF tantalum capacitors close to the power supply pins.

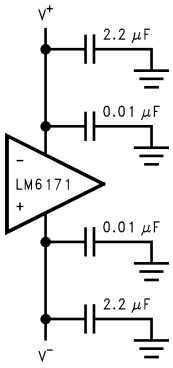


Figure 58. Power Supply Bypassing

TERMINATION

In high frequency applications, reflections occur if signals are not properly terminated. Figure 59 shows a properly terminated signal while Figure 60 shows an improperly terminated signal.

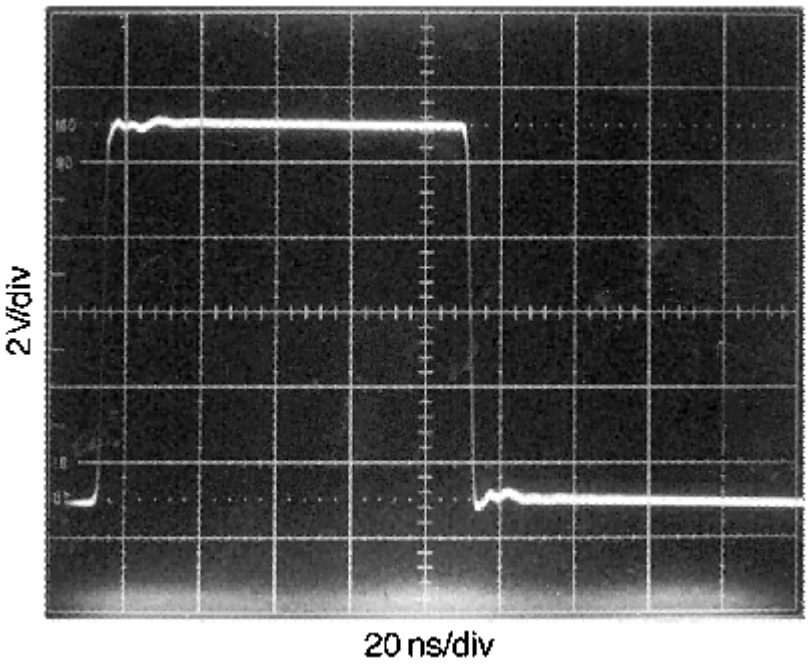


Figure 59. Properly Terminated Signal

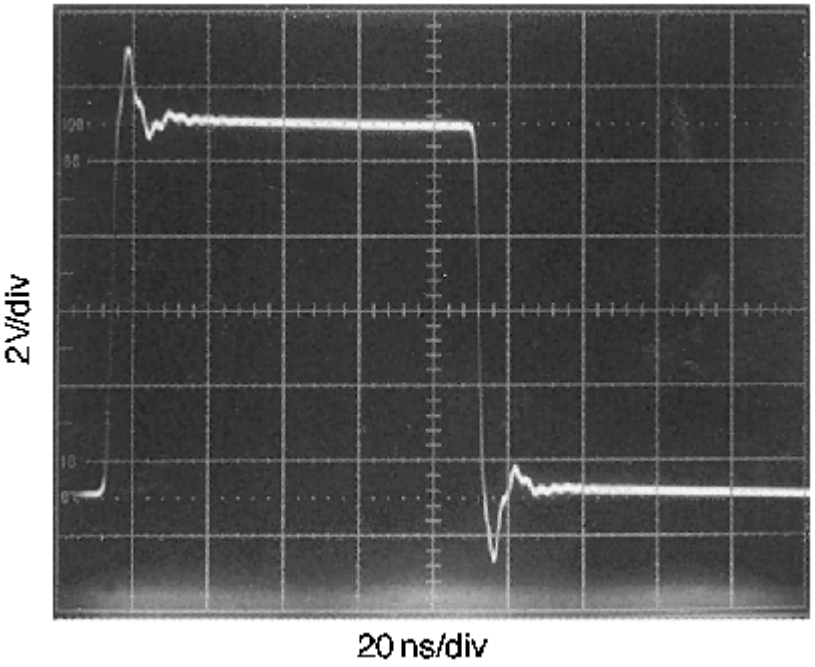


Figure 60. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

DRIVING CAPACITIVE LOADS

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown below in Figure 61. The combination of the isolation resistor and the load capacitor forms a pole to increase stablility by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM6171, a 50Ω isolation resistor is recommended for initial evaluation. Figure 62 shows the LM6171 driving a 200 pF load with the 50Ω isolation resistor.

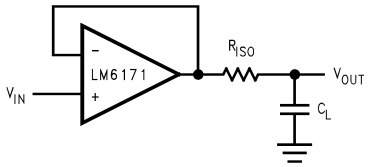


Figure 61. Isolation Resistor Used to Drive Capacitive Load

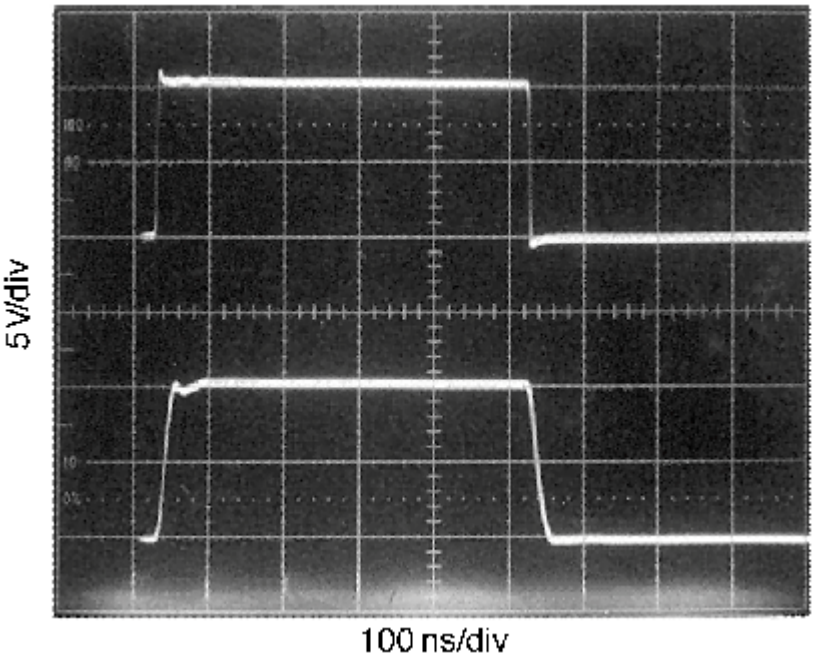


Figure 62. The LM6171 Driving a 200 pF Load with a 50Ω Isolation Resistor

POWER DISSIPATION

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A)/\theta_{JA}$$

where

- P_D is the power dissipation in a device
- $T_{J(max)}$ is the maximum junction temperature
- T_A is the ambient temperature
- θ_{JA} is the thermal resistance of a particular package (2)

For example, for the LM6171 in a SOIC-8 package, the maximum power dissipation at 25°C ambient temperature is 730 mW.

Thermal resistance, θ_{JA}, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin PDIP package has a lower thermal resistance (108°C/W) than that of 8-pin SOIC-8 (172°C/W). Therefore, for higher dissipation capability, use an 8-pin PDIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L \quad (3)$$

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

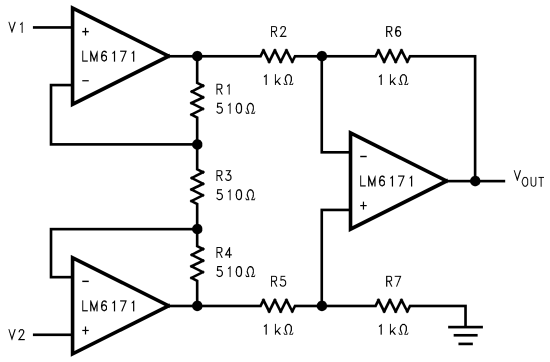
P_Q = supply current × total supply voltage with no load

P_L = output current × (voltage difference between supply voltage and output voltage of the same supply)

For example, the total power dissipated by the LM6171 with V_S = ±15V and output voltage of 10V into 1 kΩ load resistor (one end tied to ground) is

$$\begin{aligned} \mathbf{P_D} &= P_Q + P_L \\ &= (2.5\ \text{mA}) \times (30\text{V}) + (10\ \text{mA}) \times (15\text{V} - 10\text{V}) \\ &= 75\ \text{mW} + 50\ \text{mW} \\ &= 125\ \text{mW} \end{aligned}$$

APPLICATION CIRCUITS

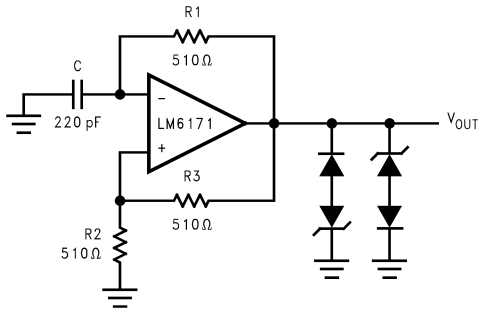


$V_{IN} = V2 - V1$

if R6 = R2, R7 = R5 and R1 = R4

$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2}\left(1 + 2\frac{R1}{R3}\right) = 3$$

Figure 63. Fast Instrumentation Amplifier



$$f = \frac{1}{2\left(R1C \ln\left(1 + 2\frac{R2}{R3}\right)\right)}$$

f = 4 MHz

Figure 64. Multivibrator

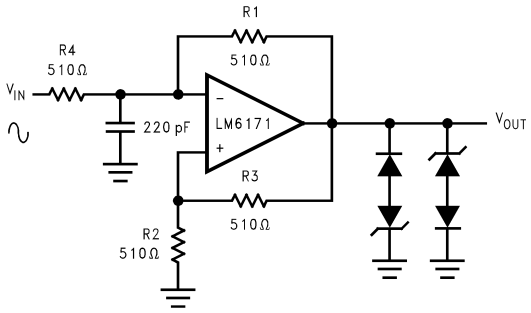


Figure 65. Pulse Width Modulator

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM6171AIM	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LM61 71AIM	
LM6171AIM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM61 71AIM	Samples
LM6171AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM61 71AIM	Samples
LM6171BIM	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LM61 71BIM	
LM6171BIM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM61 71BIM	Samples
LM6171BIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM61 71BIM	Samples
LM6171BIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6171 BIN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

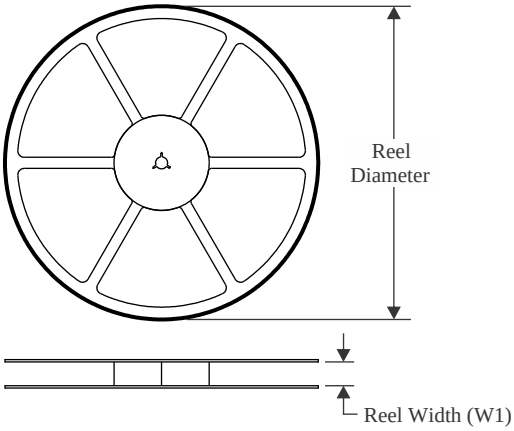
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

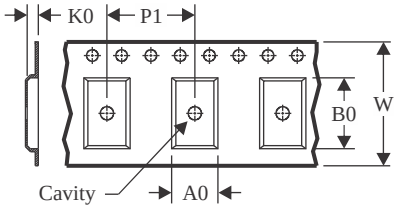
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

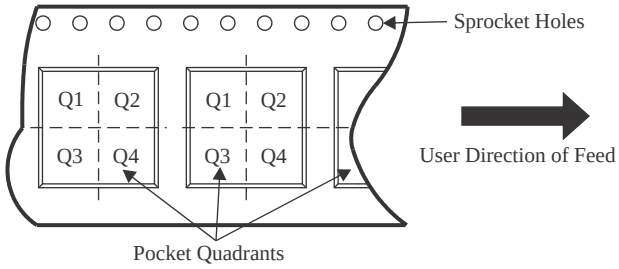


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

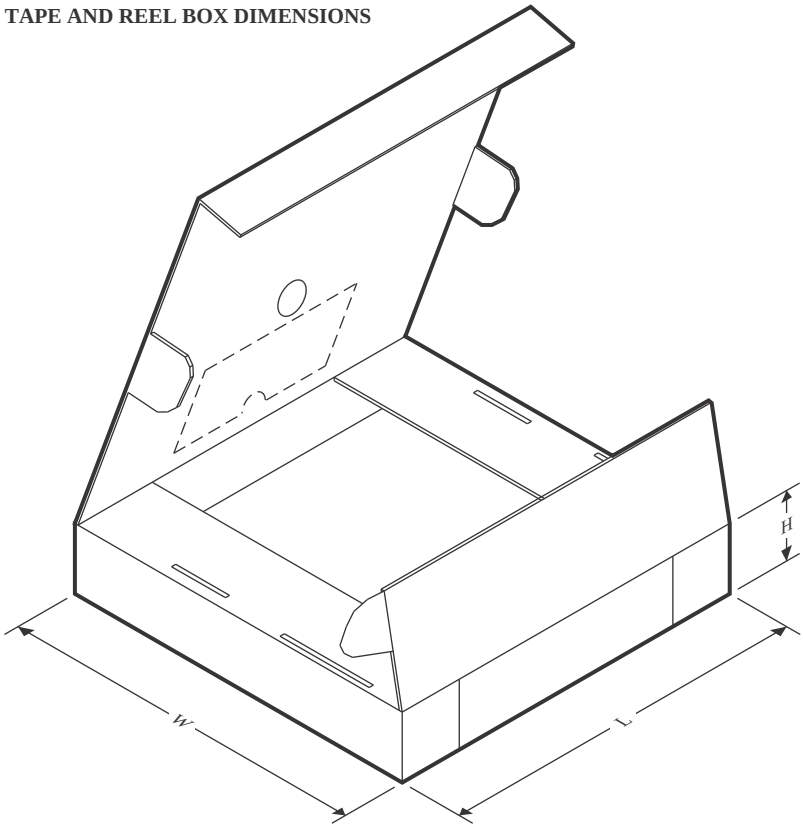
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6171AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6171BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

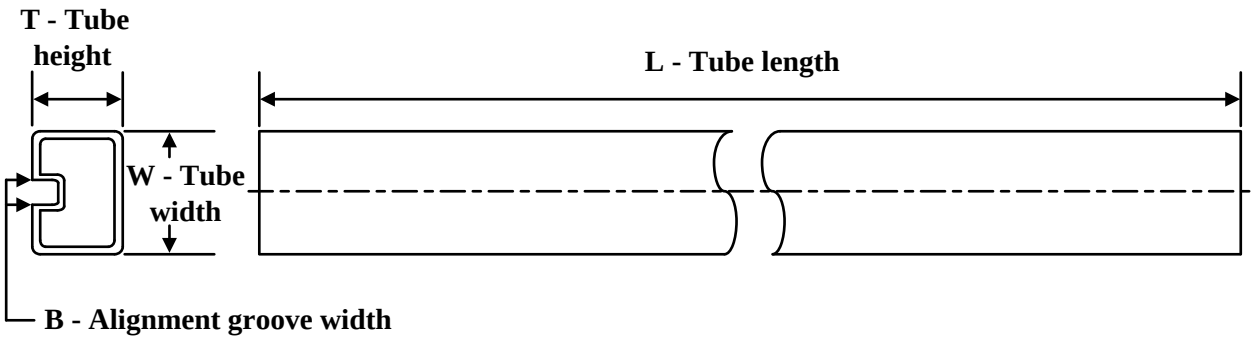
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

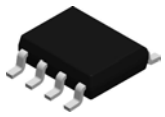
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6171AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6171BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM6171AIM	D	SOIC	8	95	495	8	4064	3.05
LM6171AIM	D	SOIC	8	95	495	8	4064	3.05
LM6171AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM6171BIM	D	SOIC	8	95	495	8	4064	3.05
LM6171BIM	D	SOIC	8	95	495	8	4064	3.05
LM6171BIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM6171BIN/NOPB	P	PDIP	8	40	502	14	11938	4.32

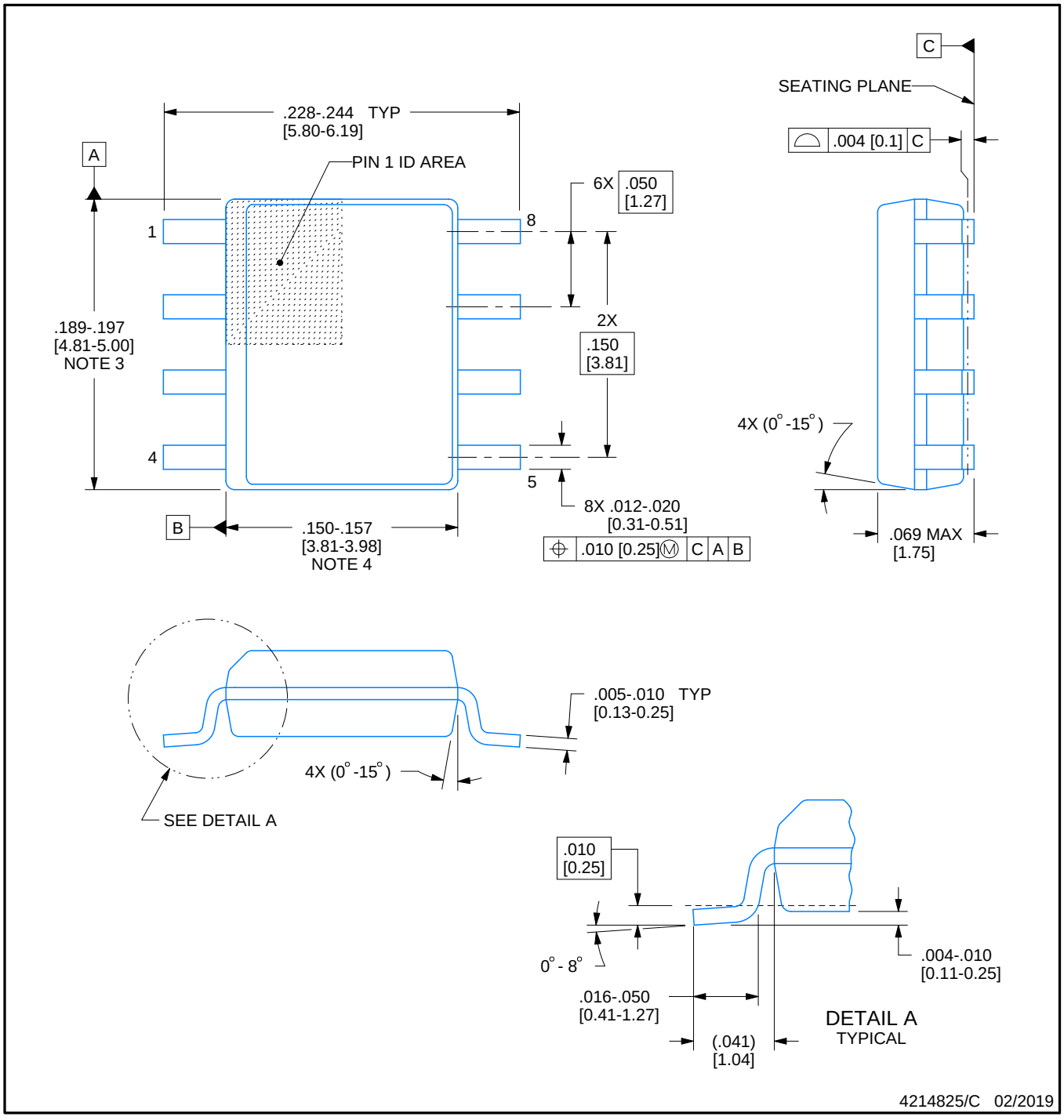


PACKAGE OUTLINE

D0008A

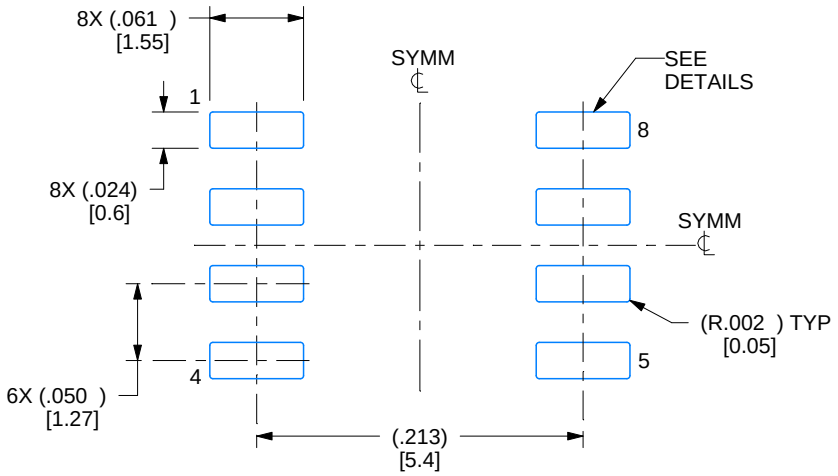
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

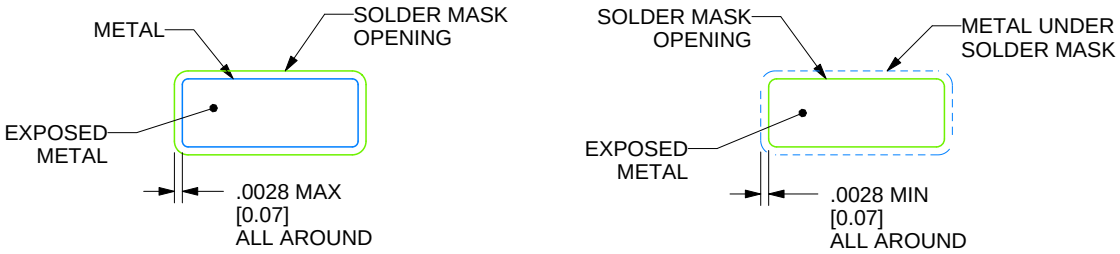


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

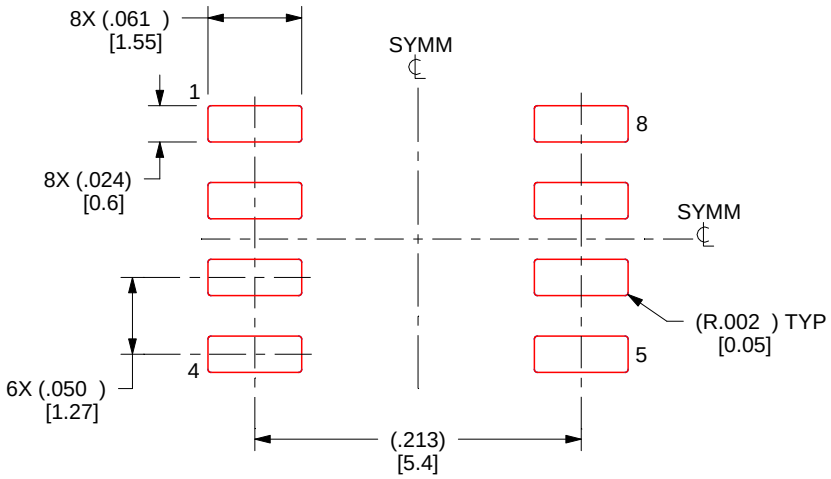
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



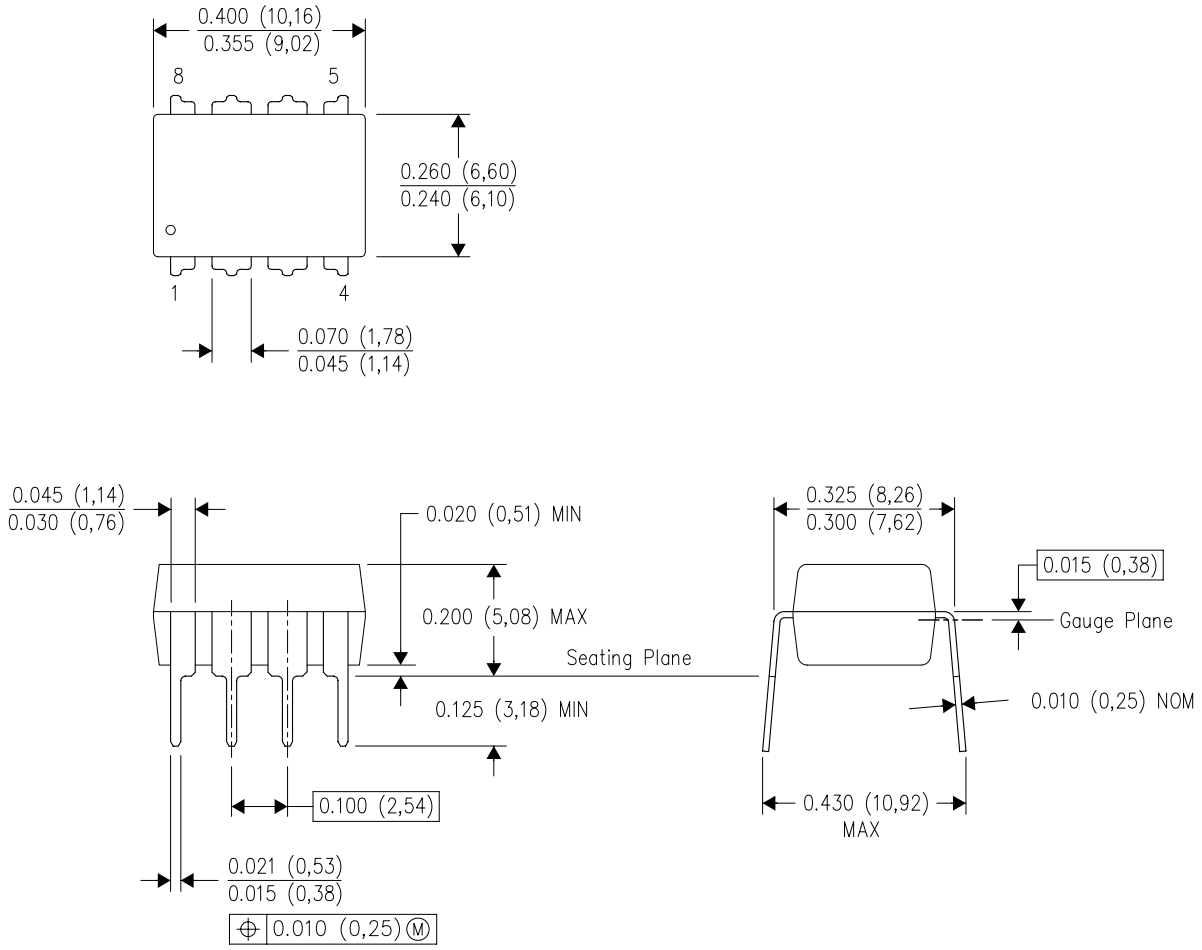
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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