TC5090AP

TC5090AP PENTAPHASIC INTEGRATION 8-BIT A/D CONVERTER

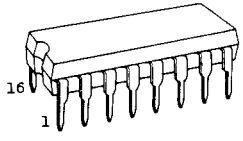
The TC5090AP is a pentaphase integration 8-bit A/D converter of high precision and low power consumption, which is mounted in a compact 16-pin standard package. The 8-bit output data can be taken out in the form of time-shared higher order 4 bits and lower order 4 bits on four 3-state data outputs.
This output system is designed specifically considering interface to 4-bit CPU.
The features of low power consumption and compact outline are applicable to battery-driven small-sized instruments.

FEATURES:

- High precision : ±1 LSB MAX.
- Low power consumption: 10mW(Typ.) @(V_{DD}=5V, f_{OSC}=1MHz)
- Single power supply : V_{DD}=5±1.5V
- High-speed conversion: 2mS(Max.) @f_{OSC}=1.5MHz
- Reference clock oscillation circuit contained (CR oscillation)
- 3-state output with output latch
- TTL/CMOS compatible digital Input/Output
- Offset automatic correction

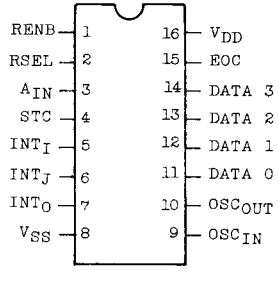
APPLICATIONS:

- Various control instruments (for temperature, humidity, pressure, etc.)
- Home electric appliances
- Electric wiring apparatuses
- Battery-driven instruments



DIP 16 (3D16A-P)

PIN ASSIGNMENT

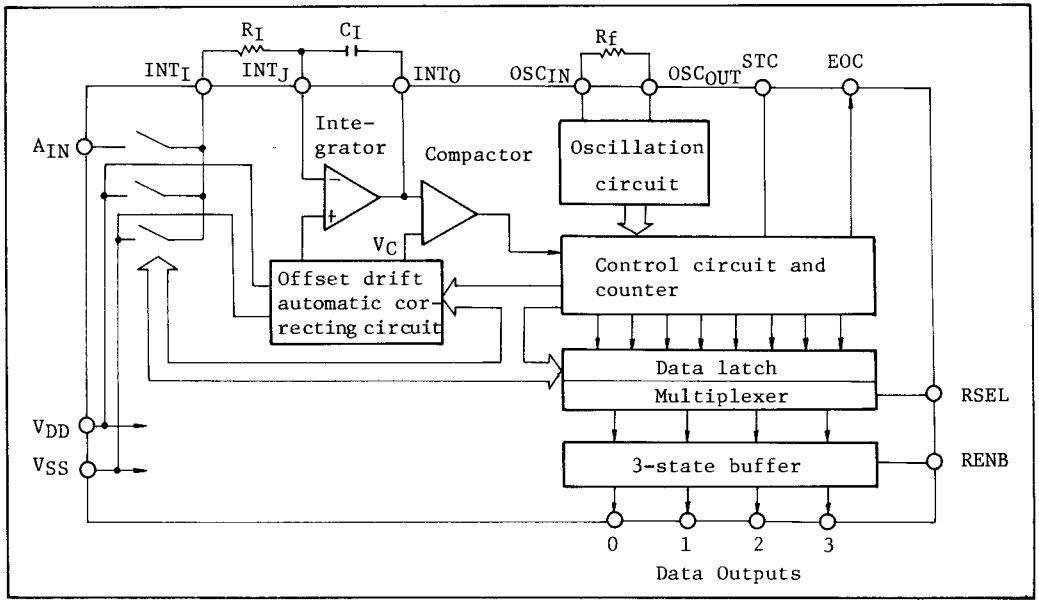


(TOP VIEW)

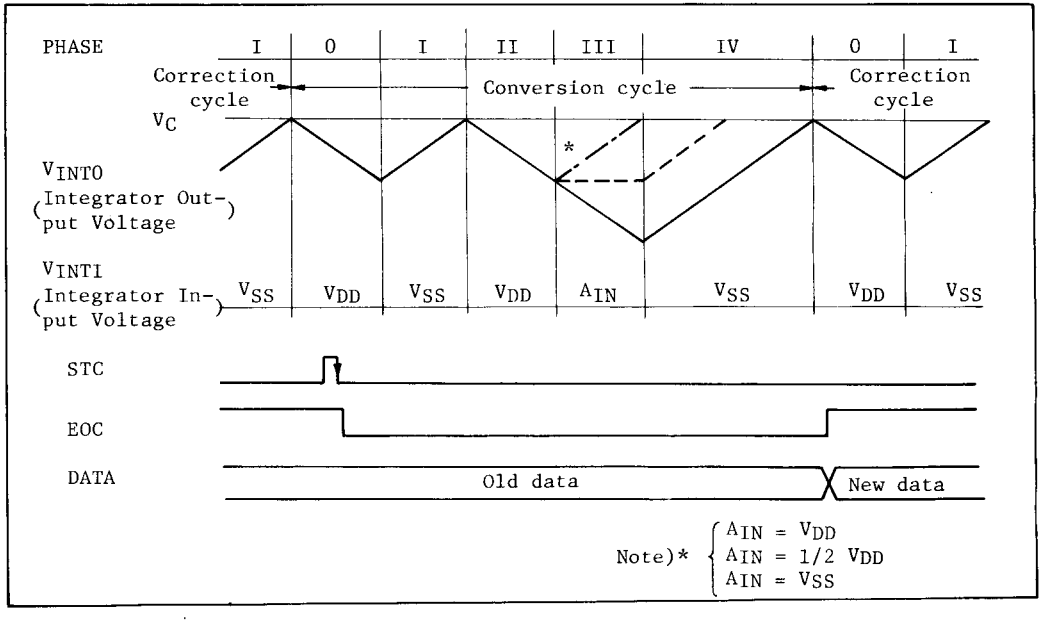
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+8	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C

BLOCK DIAGRAM



TIMING DIAGRAM



FUNCTION OF EACH PIN

PIN NO.	SYMBOL	NAME & FUNCTION
1	RENB	(Read Enable) Data read signal. "H": The data 0 ∿ 3 can be output. "L": The output above is at high impedance.
2	RSEL	(Read Select) Input to select the higher order 4 bits or the lower order 4 bits to 4-bit data output. "H": Output of the higher order 4 bits. "L": Output of the lower order 4 bits.
3	AIN	(Analog Input) Analog input terminals. Input voltage range is $V_{DD} \sim V_{SS}$.
4	STC	(Start Conversion) Conversion starting signal. Conversion starts at the falling edge.
5	INT I	(Integrator Input, Integrator Junction, Integrator Output) Integrator consists of external resistor R_I and external capacitor C_I.
6	INT J	
7	INT O	
8	V_{SS}	(Ground) Normally 0V
9	OSC IN	I/O for reference clock oscillation. Clock oscillation can be made by means of external registance. Clock can be supplied from outside through input of OSC IN.
10	OSC OUT	
11	DATA 0	(3-state Parallel Data Outputs) Conversion data output. The data 0 is LSB, and the data 3 is MSB.
12	DATA 1	
13	DATA 2	
14	DATA 3	
15	EOC	(End of Conversion) Conversion ending signal. EOC goes to "L" level at the fall of STC, and returns to "H" level at the end of conversion.
16	V_{DD}	(Power Supply) 5V±1.5V

FUNCTIONAL DESCRIPTION

(1) System Description (Pentaphasic Integration)

The operation of the TC5090AP is composed of the correction cycle and the conversion cycle as shown in the timing chart. While the power is switched on, the repetition of correction cycle and conversion cycle enables the TC5090AP at make A/D conversion under the optimum conditions at all times. The operation flowchart is shown in Fig. 1.

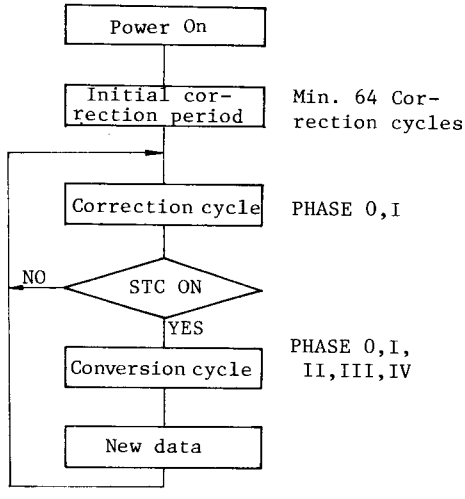


Fig. 1 Operation Flowchart

(a) Initial correction period

The internal state of this LSI is reasonably unsettled at the time when the power is switched on; therefore, the initial correction cycle is requires before stable converting operation becomes possible.

The correction cycle automatically corrects conversion error caused by offset voltage of the integrator or the like, and is composed of the period (PHASE 0) for which V_{DD} is integrated and the period (PHASE I) for which V_{SS} is integrated.

Since system correction is performed in steps at the end of this PHASE I, 64 correction cycles ($64 \times 1024 \cdot T_{OSC}$) are required as the initial correction period. (T_{OSC} denotes one clock cycle.)

(b) Conversion cycle

If the initial corection cycle period is completed, normal conversion becomes possible.
When STC input is given, (although the correction cycle in PHASE 0 or PHASE I is in operation at this time), the correction operation stops, and the conversion cycle starts.

In other words, even if STC input is given, this LSI performs the same operation as the correction cycle until PHASE I is completed; but it does not perform the correction at the time of completion of PHASE I, and shifts to PHASE II. Therefore, attention should be given to the fact that PHASE I prior to PHASE II does not act as correction cycle.
When STC input is given, the LSI integrates analog input in PHASE III through PHASE I and PHASE II, performing digital conversion in PHASE IV. When the LSI completes digital conversion in PHASE IV, the output is turned to the new data and the LSI returns to the correction cycle.

(c) Correction cycle

When the next STC input is given between completion of arbitrary conversion cycle (at the time of completion of PHASE IV) and completion of one correction cycle ($1024 \cdot T_{OSC}$), no correction is substantially made. Therefore, in case the STC input is consecutively given, another STC should be given after the lapse of one correction cycle at the earliest from completion of PHASE IV. When the STC input is given during conversion (while EOC is at "L" level), the STC cannot be accepted.

(d) Constant of integration

The R_I and C_I composing the integrator should be selected to satisfy the following equation.

$$R_I C_I = (0.9 \sim 2.5) \cdot \frac{10^3}{f_{OSC}} \quad [S]$$

Attention should be paid to the fact that, when the external R oscillation is used, f_{OSC} has ±30% variations in regard to the typ. value in Fig. 5 due to variations in sample and temperature characteristic.

In other words, if the typ. value in Fig. 5 is denoted by $f_{R \cdot TYP}$, the R_I and C_I should be selected according to the following equation.

$$R_I C_I = (1.2 \sim 1.75) \cdot \frac{10^3}{f_{R \cdot TYP}} \quad [S]$$

(2) Output Data Mode

TRUTH TABLE

RENB	ANALOG INPUT	DIGITAL OUTPUTS							
		RSEL = "L"				RSEL = "H"			
		DATA 0	DATA 1	DATA 2	DATA 3	DATA 0	DATA 1	DATA 2	DATA 3
L	Don't care	High Impedance							
H	$< \frac{1}{2}$ LSB	L	L	L	L	L	L	L	L
H	$-\frac{1}{2}$ LSB $\sim \frac{1}{2}$ LSB	L	L	L	L	L	L	L	L
H	$\frac{1}{2}$ LSB $\sim \frac{3}{2}$ LSB	H	L	L	L	L	L	L	L
H	.....	Straight Binary							
H	"FS"$-\frac{5}{2}$ LSB $\sim$ "FS"$-\frac{3}{2}$ LSB	L	H	H	H	H	H	H	H
H	"FS"$-\frac{3}{2}$ LSB $\sim$ "FS"$-\frac{1}{2}$ LSB	H	H	H	H	H	H	H	H
H	"FS"$-\frac{1}{2}$ LSB <	H	H	H	H	H	H	H	H

Note : V_{SS} = 0V 1 LSB = $V_{DD}/256$

"FS" ..... Full Scale (V_{DD})

8-bit digital data is output on four data lines after having been divided into the higher order 4 bits and the lower order 4 bits. Either the higher order bits or the lower order bits can be selected by RSEL.

(3) System Clock Oscillation Circuit

For oscillating reference clock the oscillation circuit is composed of external resistors as shown in Fig. 2.

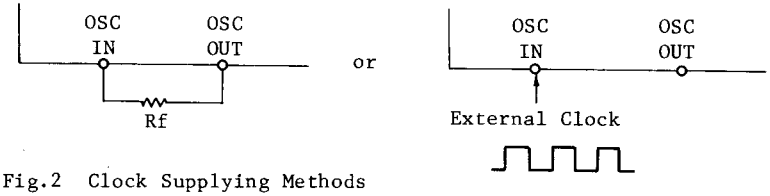


Fig.2 Clock Supplying Methods

(4) Timings for STC-EOC and EOC-DATA

o Time (t_{SE}) from the fall of STC to the fall of EOC.

$$t_{SE}=\frac{1}{2}T_{OSC} \sim \frac{3}{2}T_{OSC}$$

o Time (t_{DE}) from the out of DATA output to the rise of EOC

$$t_{DE} = \frac{1}{2}T_{OSC}$$

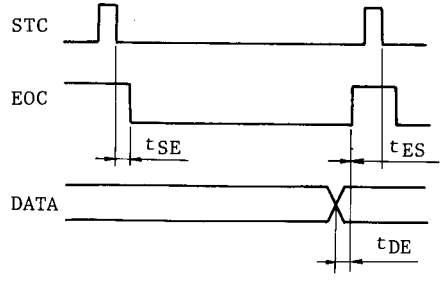


Fig.3 Timing chart of STC/EOC

o Min. time (t_{ES}) from the rise of EOC to the accpetance of another STC.

$$t_{ES} = \frac{1}{2}T_{OSC} \sim \frac{3}{2}T_{OSC}$$

(5) Timings for STC Input and RSEL/RENB Input

STC signal is taken in synchronously with the internal clock; therefore, if T_{OSC} denotes one clock cycle of OSC terminal, the pulse width of more than $(2 \cdot T_{OSC})$ is required.

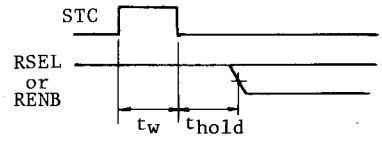


Fig.4 Timing chart of Control Input

Either RSEL input or RENB input is required to be set to "H" level at the falling time of STC by reason of internal structure.

Further, the hold time of $(T_{OSC} + 50ns)$ or more after the falling time of STC at least for "H" level time of RSEL or REMB is required.

NOTE : $t_w > 2 \cdot T_{OSC}$, $t_{hold} > T_{OSC} + 50ns$

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3.5	5	6.5	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Integral Resistor	R_I		0.4	-	2	MΩ
Integral Capacitor	C_I		Note			
Oscillatory Resistance	R_f	V_{DD} = 5V	10	-	-	kΩ

Note: Refer to Fuction Description (1) for determing the values of R_I and C_I, respectively.

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

ITEM	SYM-BOL	TEST CONDITIONS	V_{DD} [V]	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Input High Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
Output Low Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.0V * $V_{IN}=V_{SS},V_{DD}$	5	-1.2	-	-1.0	-2.0	-	-0.7	-	mA
Output Low Current	I_{OL}	V_{OL}=0.4V * $V_{IN}=V_{SS},V_{DD}$	5	2.4	-	2.0	4.0	-	1.6	-	
Input High Voltage	V_{IH}	*	5	2.4	-	2.4	-	-	2.4	-	V
Input Low Voltage	V_{IL}	*	5	-	0.8	-	-	0.8	-	0.8	
Output Disable Current	I_{DH} I_{DL}	V_{OH}=6.5V * V_{OL}=0V	6.5	-	±0.5	-	$\pm 10^{-4}$	±0.5	-	±5	μA
Input Current	I_{IH} I_{IL}	V_{IH}=6.5V * V_{IL}=0V	6.5	-	±0.3	-	$\pm 10^{-5}$	±0.3	-	±1	
Analog Switch Off-Leak Current	I_{OFF}	I_{IH}=6.5V V_{IL}=0V	6.5	-	±0.3	-	$\pm 10^{-5}$	±0.3	-	±1	
Operating Con-sumption Current	I_{DD} (opr)	f_{OSC} = 1 MHz	5	-	-	-	2.0	3	-	-	mA

* Applicable to digital input/output. Not applicable to analog input/output and OSC_{IN}/OSC_{OUT}.

SWITCHING CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C, C_L = 50 pF)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{TLH}		-	50	100	ns
Output Fall Time	t_{THL}		-	40	100	
(Low-High) Propagation Delay Time	t_{pLH}	RSEL("L"→"H")-DATA OUT	-	180	400	
(High-Low) Propagation Delay Time	t_{pHL}		-	150	400	
(Low-High) Propagation Delay Time	t_{pLH}	RSEL("H"→"L")-DATA OUT	-	380	700	
(High-Low) Propagation Delay Time	t_{pHL}		-	300	700	
Output Enable Time	t_{ZL} t_{ZH}	RENB-DATA OUT	-	80	250	
Output Disable Time	t_{LZ} t_{HZ}		-	280	500	
Max. Clock Frequency	$f_{MAX\phi}$	OSC Input	1.5	3.0	-	MHz
Min. Clock Frequency	$f_{MIN\phi}$	OSC Input	-	-	100	kHz
Input Capacity	C_{IN}	Digital Inputs	-	4	-	pF
Analog Input Capacity	C_{IN}		-	7	-	pF
3-State Output Capacity	C_{OUT}		-	8	-	pF

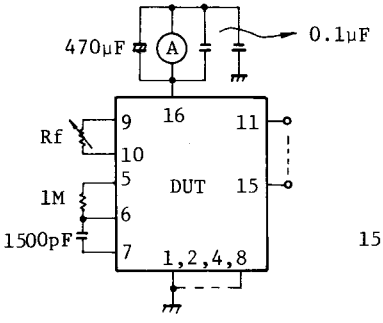
SYSTEM CHARACTERISTICS (Ta = -40 ∿ 85°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Zero Point Error	E_{ZP}	V_{DD}=5V, V_{SS}=0V	-	$\pm\frac{1}{4}$	$\pm\frac{1}{2}$	LSB
Full Scale Error	E_{FS}		-	$\pm\frac{1}{4}$	±1	
Nonlinearity			-	$\pm\frac{1}{4}$	±1	
STC Min. Pulse Width	t_w	*	-	-	$\frac{2}{f_{OSC}}$	s
Conversion Time	$t_{conv.}$	A_{IN} = 0 ∿ FS *	$\frac{10^3}{f_{OSC}}$	-	$\frac{3.1\times10^3}{f_{OSC}}$	s

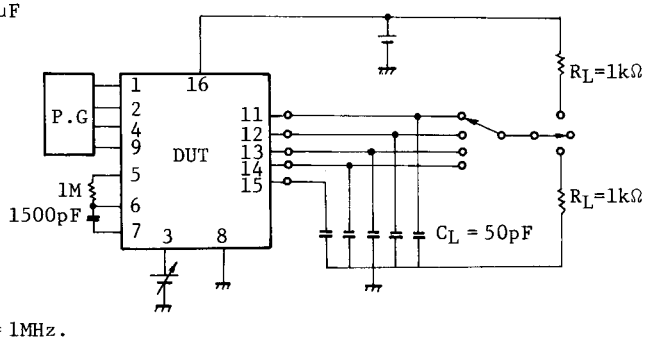
* f_{OSC} : OSC terminal clock frequency [Hz], FS : Full Scale voltage, V_{DD} level

TEST CIRCUIT

$I_{DD(opr.)}$ Test Circuit



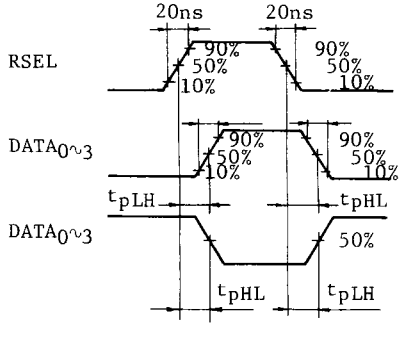
Switching Time Test Circuit



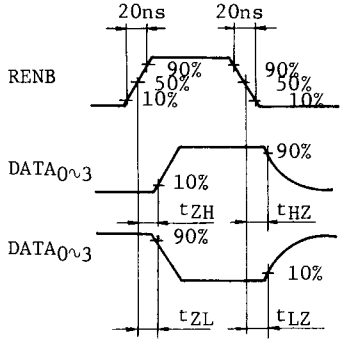
Rf is adjusted as f_{OSC} = 1MHz.

SWITCHING CHARACTERISTICS TEST WAVEFORMS

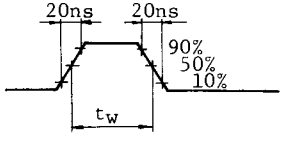
1. t_{pLH}, t_{pHL} (RSEL-DATA)



2. t_{ZL}, t_{ZH}, t_{LZ}, t_{ZL}



3. t_w (STC)



STANDARD CHARACTERISTICS CHARTS

Fig. 1 V_{DD} - $I_{DD(opr)}$

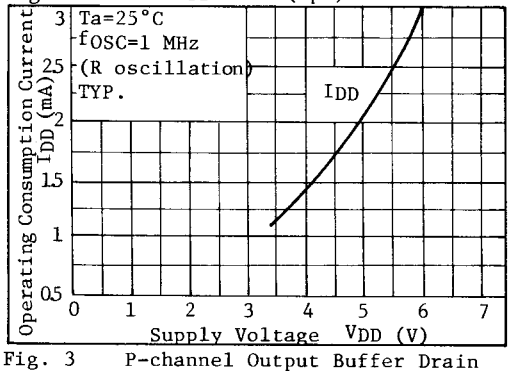


Fig. 2 $I_{DD(opr)}$ - f_{OSC}

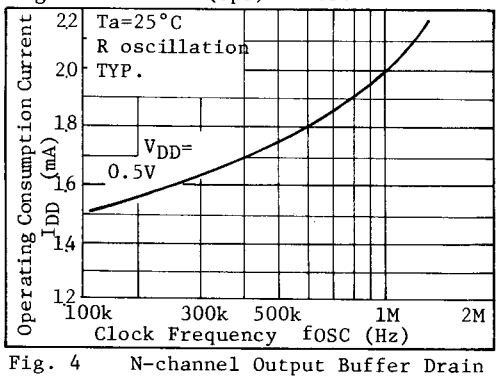


Fig. 3 P-channel Output Buffer Drain Current Characteristics

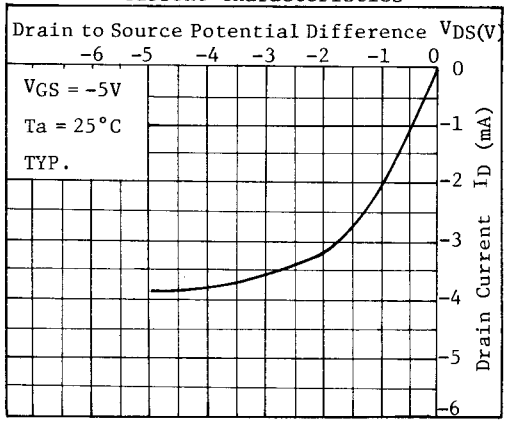


Fig. 4 N-channel Output Buffer Drain Current Characteristics

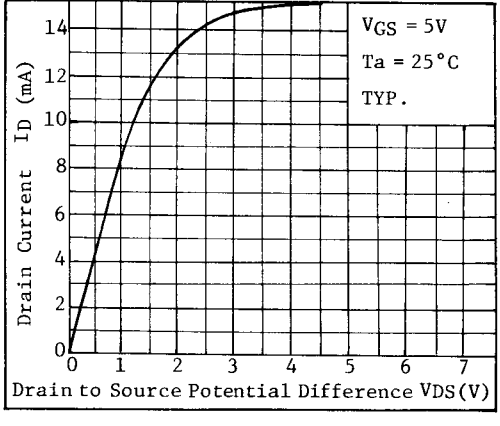


Fig.5 R_f - f_{OSC}

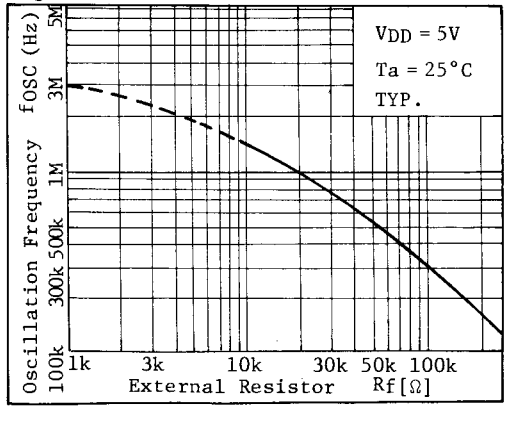


Fig. 6 f_{OSC} - V_{DD}

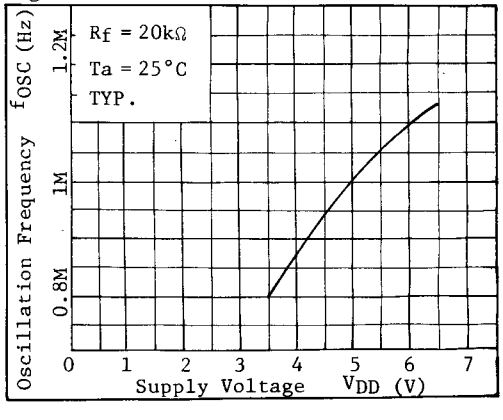


Fig. 7 t_{pd} - V_{DD} (PENB-DATA)

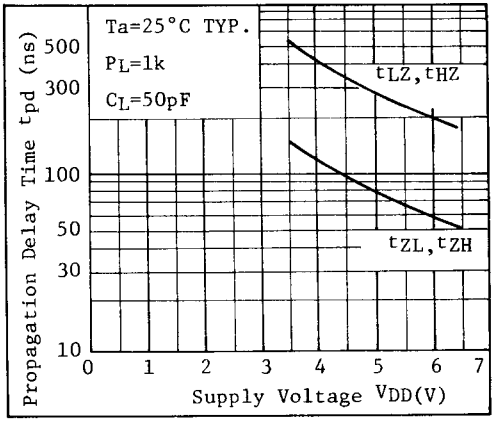


Fig. 8 t_{pd} - V_{DD} (RSEL (L→H)-DATA)

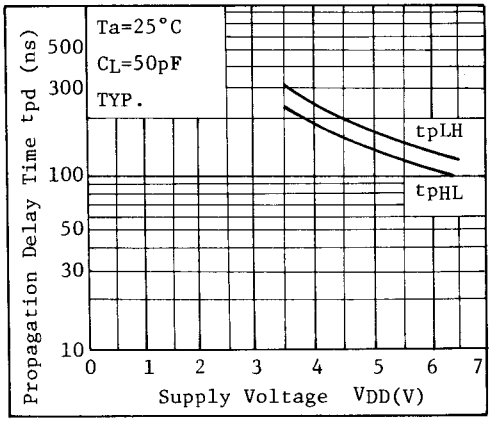


Fig. 9 t_{pd} - V_{DD}(RSEL(H→L)-DATA)

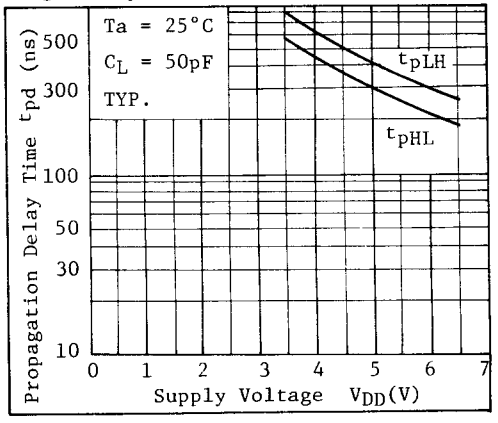
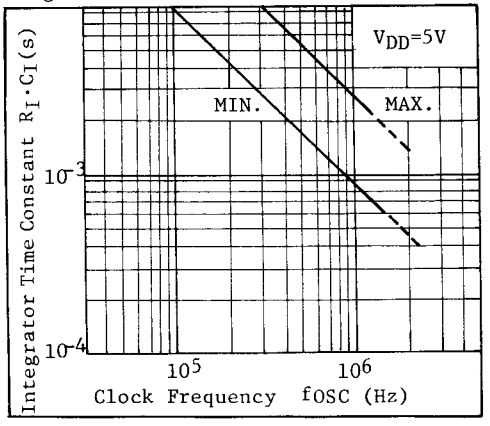


Fig.10 $R_I.C_I$ - fOSC



(Note) The characteristics at Fig. 10 have been prepared for reference at the time of determination of an integrator time constant, according to the equation of

$$(R_I \cdot C_I = (0.9 \sim 2.5) \frac{10^3}{f_{osc}} [\text{Sec}])$$

for determing $R_I \cdot C_I$.

In case of the determination of R_I and C_I, the product, or the value, of R_I and C_I is required to be within the range of MIN. to MAX. as shown in Fig. 10 after due consideration of dispersion.