ML4902

High Current Synchronous Buck Controller

GENERAL DESCRIPTION

The ML4902 high current synchronous buck controller provides high efficiency DC/DC conversion to generate V_{CCP} for processors such as the Pentium® Pro and Pentium II from Intel®.

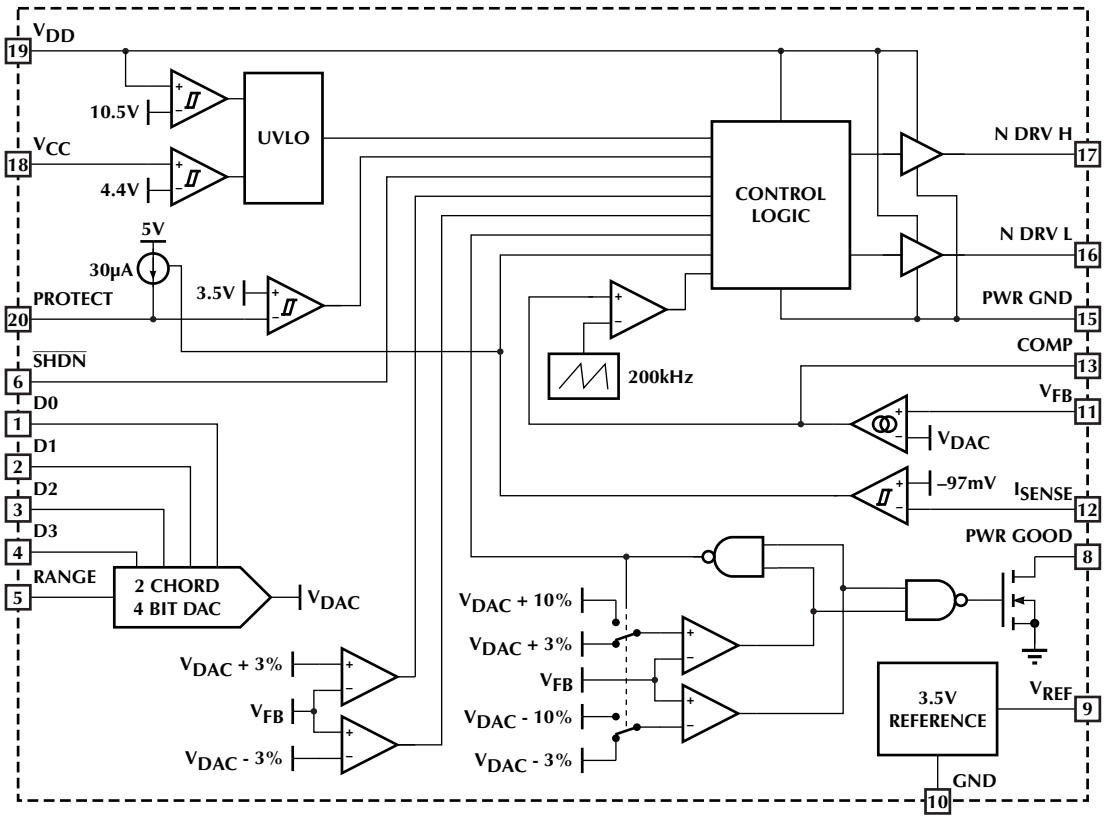
The ML4902 controller, when combined with 2 N-channel MOSFETs, generates output voltages between 1.8V and 3.5V from a 5V supply. The output voltage is selected via an internal 2 chord 4-bit DAC. In the upper range, the output can be set between 2.1V and 3.5V in 100mV steps. In the lower range, the output can be set between 1.8V and 2.05V in 50mV steps. Output currents in excess of 20A can be attained at efficiencies greater than 90%.

The ML4902 can be enabled/disabled via the $\overline{SHDN}$ pin. While disabled, the output of the regulator is completely isolated from the circuit's input supply. The ML4902 employs fixed-frequency PWM control combined with a sophisticated control loop enhancement circuit to provide excellent load transient response.

FEATURES

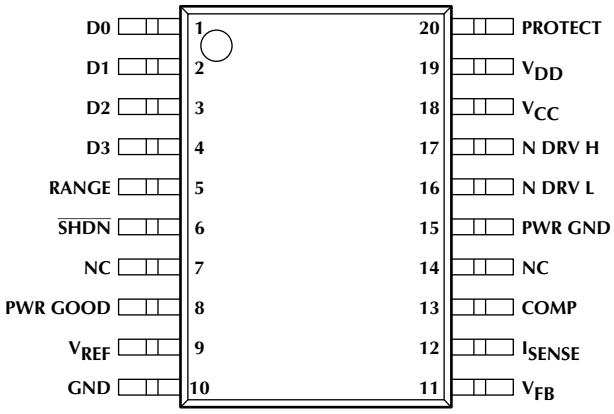
- Designed to meet Pentium Pro and Pentium II VRM power supply requirements
- DC regulation to ±1% maximum
- Proprietary circuitry provides transient response of ±5% maximum over a 0A to 20A load range
- Programmable output voltage (1.8V to 3.5V) is set by an onboard 2 chord 4-bit DAC
- Synchronous N-channel buck topology for maximum power conversion efficiency
- Fixed frequency operation for easier system integration
- Integrated anti-shootthrough logic, short circuit protection, shutdown, and UV lockout

BLOCK DIAGRAM



PIN CONFIGURATION

ML4902
20-Pin TSSOP (T20)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	D0	LSB input to the DAC which sets the output voltage
2	D1	Input to the DAC which sets the output voltage
3	D2	Input to the DAC which sets the output voltage
4	D3	MSB input to the DAC which sets the output voltage
5	RANGE	Range selection bit for the 2 chord 4-bit DAC. Logic 1 sets the range at 2.1V to 3.5V with an LSB of 100mV. Logic 0 sets the range at 1.8V to 2.05V with an LSB of 50mV
6	$\overline{SHDN}$	Grounding this pin shuts down the regulator
8	PWR GOOD	This open drain output goes low whenever $\overline{SHDN}$ goes low or when the output is not within $\pm$10% of its nominal value
9	V_{REF}	Bypass connection for the internal 3.5V reference
10	GND	Analog signal ground
11	V_{FB}	Output voltage feedback pin
12	I_{SENSE}	Current sense input
13	COMP	Connection for the compensation and optional soft-start delay network
15	PWR GND	Power ground
16	N DRV L	Synchronous rectifier driver output
17	N DRV H	Buck switch driver output
18	V_{CC}	Connection point for monitoring the 5V supply to determine the proper condition of PWR GOOD
19	V_{DD}	12V power supply input
20	PROTECT	Connection for the integrating current limit network

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{DD} 13.5V
V_{CC} 7V
Peak Driver Output Current ..... ±2A
V_{FB} Voltage ..... GND - 0.3V to 5.5V
I_{SENSE} Voltage ..... GND - 0.5V to 5.5V
All Other Inputs ..... GND - 0.3V to V_{DD} + 0.3V
$\overline{SHDN}$ Input Current 100µA

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C
Thermal Resistance (θ_{JA}) ..... 100°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
V_{DD} Range ..... 11.4V to 12.6V
V_{CC} Range ..... 4.75V to 5.25V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD} = 12V, V_{CC} = $\overline{SHDN}$ = 5V, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
V_{REF}	Output Voltage		3.51	3.535	3.56	V
	Line Regulation	11V < V_{DD} < 13V		0.5		mV/V
UV LOCKOUT						
	V_{DD} Start-up Threshold		10.2	10.5	10.8	V
	V_{DD} Hysteresis		300	450	600	mV
	V_{CC} Start-up Threshold		4.25	4.4	4.5	V
	V_{CC} Hysteresis		300	400	500	mV
SHUTDOWN						
	Input Low Voltage				0.8	V
	Input High Voltage		2.0			V
	Delay to Output			50		ns
POWER GOOD COMPARATOR						
	Output Voltage in Regulation	5kΩ pull-up to 5V	4.8			V
	Output Voltage out of Regulation	V_{FB} < 90% V_{DAC} or >110% V_{DAC}			0.4	V
	Output Voltage in Shutdown	$\overline{SHDN}$ = 0V, 5kΩ pull-up to 5V			0.4	V
BUCK REGULATOR						
	Oscillator Frequency		160	200	230	kHz
	Duty Cycle Ratio	RANGE = 1, V_{FB} = 0V, DAC (D3-D0) Code = 0100	85		98	%
		RANGE = 1, V_{FB} > 3.193V, DAC (D3-D0) Code = 0100			0	%
	DAC (RANGE, D3-D0) Input Low Voltage				0.8	V
	DAC (RANGE, D3-D0) Input High Voltage		2.0			V

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BUCK REGULATOR (Continued)						
	V_{FB} Threshold Voltage (Note 2)	RANGE = 0, (D3-D0) Code = 0000	2.050	2.071	2.092	V
		RANGE = 0, (D3-D0) Code = 0001	2.000	2.020	2.04	V
		RANGE = 0, (D3-D0) Code = 0010	1.950	1.970	1.989	V
		RANGE = 0, (D3-D0) Code = 0011	1.900	1.919	1.938	V
		RANGE = 0, (D3-D0) Code = 0100	1.850	1.869	1.887	V
		RANGE = 0, (D3-D0) Code = 0101	1.800	1.818	1.836	V
		RANGE = 1, (D3-D0) Code = 0000	3.500	3.535	3.570	V
		RANGE = 1, (D3-D0) Code = 0001	3.400	3.434	3.468	V
		RANGE = 1, (D3-D0) Code = 0010	3.300	3.333	3.366	V
		RANGE = 1, (D3-D0) Code = 0011	3.200	3.232	3.264	V
		RANGE = 1, (D3-D0) Code = 0100	3.100	3.131	3.162	V
		RANGE = 1, (D3-D0) Code = 0101	3.000	3.030	3.060	V
		RANGE = 1, (D3-D0) Code = 0110	2.900	2.929	2.958	V
		RANGE = 1, (D3-D0) Code = 0111	2.800	2.828	2.856	V
		RANGE = 1, (D3-D0) Code = 1000	2.700	2.727	2.754	V
		RANGE = 1, (D3-D0) Code = 1001	2.600	2.626	2.652	V
		RANGE = 1, (D3-D0) Code = 1010	2.500	2.525	2.550	V
		RANGE = 1, (D3-D0) Code = 1011	2.400	2.424	2.448	V
		RANGE = 1, (D3-D0) Code = 1100	2.300	2.323	2.346	V
		RANGE = 1, (D3-D0) Code = 1101	2.200	2.222	2.244	V
		RANGE = 1, (D3-D0) Code = 1110	2.100	2.121	2.142	V
	I_{SENSE} Threshold Voltage		-87	-97	-107	mV
	I_{SENSE} Hysteresis			10		mV
	PROTECT Threshold Voltage		3.2	3.5	3.8	V
	PROTECT Hysteresis		1.8	2	2.2	V
	PROTECT Charging Current	$V(I_{SENSE})$ = -100mV		30		µA
	PROTECT Leakage Current			±100		nA
	Transition Time, N DRV H and N DRV L	C_L = 5000pF, 10-90%		40		ns
SUPPLY						
I_{DD}	V_{DD} Current	$\overline{SHDN}$ = 0V DAC (D3-D0) Code = 0000		650	900	µA
		$\overline{SHDN}$ = 5V, V_{FB} = 5V		1	2	mA
		$\overline{SHDN}$ = 5V, V_{FB} = 0V, C_L = 5000pF		20		mA
I_{CC}	V_{CC} Current			1	10	µA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: Codes 00110 to 01111, and 11111 are not valid; applying these codes to the DAC will shut off N DRV H and N DRV L.

FUNCTIONAL DESCRIPTION

The ML4902 PWM controller permits the construction of a simple yet sophisticated power supply for Intel's Pentium Pro and Pentium II microprocessor families. The ML4902 and its associated circuitry can be built either as a Voltage Regulator Module (VRM) or as a dedicated supply on the motherboard. The ML4902 controls two N-channel MOSFETs in a synchronous buck regulator topology to convert a 5V input to the voltage required by the microprocessor. The output voltage can be set between 1.8V and 3.5V, as selected by an onboard DAC. Other features which facilitate the design of DC-DC converters for any type of processor include a trimmed 1% reference, special transient-response optimization in the feedback paths, a shutdown input, input and output power good monitors, and overcurrent protection.

OUTPUT VOLTAGE SELECTION

The inputs of the internal 2-chord 4-bit DAC come from open collector signals provided by the processor. These signals specify what supply voltage the microprocessor requires. The output voltage of the buck converter is compared directly with the DAC voltage to maintain regulation. D3 is the MSB input and D0 is the LSB input of the DAC, while RANGE selects the output voltage range and the LSB voltage increment of the DAC. The output of the DAC is between 2.121V to 3.535V in 100mV steps when RANGE = 1, and between 1.818V to 2.071V in 50mV steps when RANGE = 0. The output voltage set by the DAC is 1% above the processor's nominal operating voltage to counteract the effects of connector and PC trace resistance, and of the instantaneous output voltage droop which occurs when a transient load is applied. For codes 00110 to 01111 and code 11111, the N DRV H and N DRV L outputs are disabled.

VOLTAGE FEEDBACK LOOP

The ML4902 contains two control loops to improve the load transient response. The output voltage is directly monitored via the V_{FB} pin and compared to the desired output voltage set by the internal DAC. When the output voltage is within $\pm$3% of the DAC voltage, the proportional control loop (closed by the voltage error amplifier) keeps the output voltage at the correct value. If the output falls below the DAC voltage by more than 3%, one side of the transient loop is activated, forcing the output of the ML4902 to maximum duty cycle until the output comes back within the $\pm$3% limit. If the output voltage rises above the DAC voltage by more than 3%, the other side of the transient loop is activated, and the upper MOSFET drive is disabled until the output comes back within the $\pm$3% limit. If the output voltage rises above the DAC voltage by more than 10%, both N DRV H and N DRV L will be disabled to turn the converter off. During start-up, the transient loop is disabled until the output voltage is within -3% of the DAC voltage.

POWER GOOD (PWR GOOD)

An open drain signal is provided by the ML4902 which tells the microprocessor when the entire power system is functioning within the expected limits. PWR GOOD will be false (low) if either the 5V or 12V supply is not in regulation, when the $\overline{SHDN}$ pin is pulled low, or when the output is not within $\pm$10% of the nominal output voltage selected by the internal DAC.

When PWR GOOD is false, the PWR GOOD voltage window is held to $\pm$3%; when PWR GOOD is true (high), the window is expanded to $\pm$10%. Using different windows for coming into and going out of regulation makes sure that PWR GOOD does not oscillate during the start-up of the microprocessor.

INTERNAL REFERENCE

The ML4902 contains a 3.535V, temperature compensated, precision band-gap reference. The V_{REF} pin is connected to the output of this reference, and should be bypassed with a 100nF to 220nF ceramic capacitor for proper operation.

OVERCURRENT PROTECTION

Overcurrent sensing for the ML4902 application circuit is typically accomplished by monitoring the voltage drop across the synchronous rectifier MOSFETs (Q3||Q4) during their conduction period. Alternately, current can be sensed using a low-value, low-inductance sense resistor connected between the most negative end of the current recirculating element and ground. In either case, the resulting IR drop is presented to the ML4902's internal overcurrent comparator via the part's I_{SENSE} pin. The overcurrent comparator has approximately 250ns of leading-edge blanking. This blanking interval allows the ML4902 to ignore spurious circuit voltages such as inductive transients and the synchronous rectifier's drain-body diode voltage during the anti-shootthrough interval. Following this blanking interval, the comparator will turn on if the voltage on the I_{SENSE} pin is more negative than –97mV.

Each time the overcurrent comparator turns on, the PROTECT pin of the ML4902 sources a small current (30µA) into an external RC network. If this current source is activated over a number of cycles, the voltage on the PROTECT pin will charge above 3.5V, signaling a sustained overcurrent or short circuit at the load. This will cause the N DRV H output to turn off. N DRV H will remain off until the capacitor attached to the PROTECT pin has discharged down to 1.5V, at which time the converter is re-enabled. If the fault causing the overcurrent condition has not been cleared, the overcurrent protection cycle will repeat, and the ML4902 circuit will operate in a "hiccup" mode to protect itself, the input supply, and the output.

FUNCTIONAL DESCRIPTION (Continued)

UNDERVOLTAGE LOCKOUT

The ML4902 has hysteretic undervoltage lockout protection circuits for both the 12V (V_{DD}) and 5V (V_{CC}) supplies. During an input undervoltage condition, the internal reference and voltage monitor circuits remain in operation, but N DRV H and N DRV L are disabled and the PWR GOOD output will be false (low).

COMPENSATION

The COMP pin is connected to the output of the transconductance amplifier which forms the gain block for the proportional control loop of the ML4902. An RC network from this pin to GND is used to compensate the amplifier.

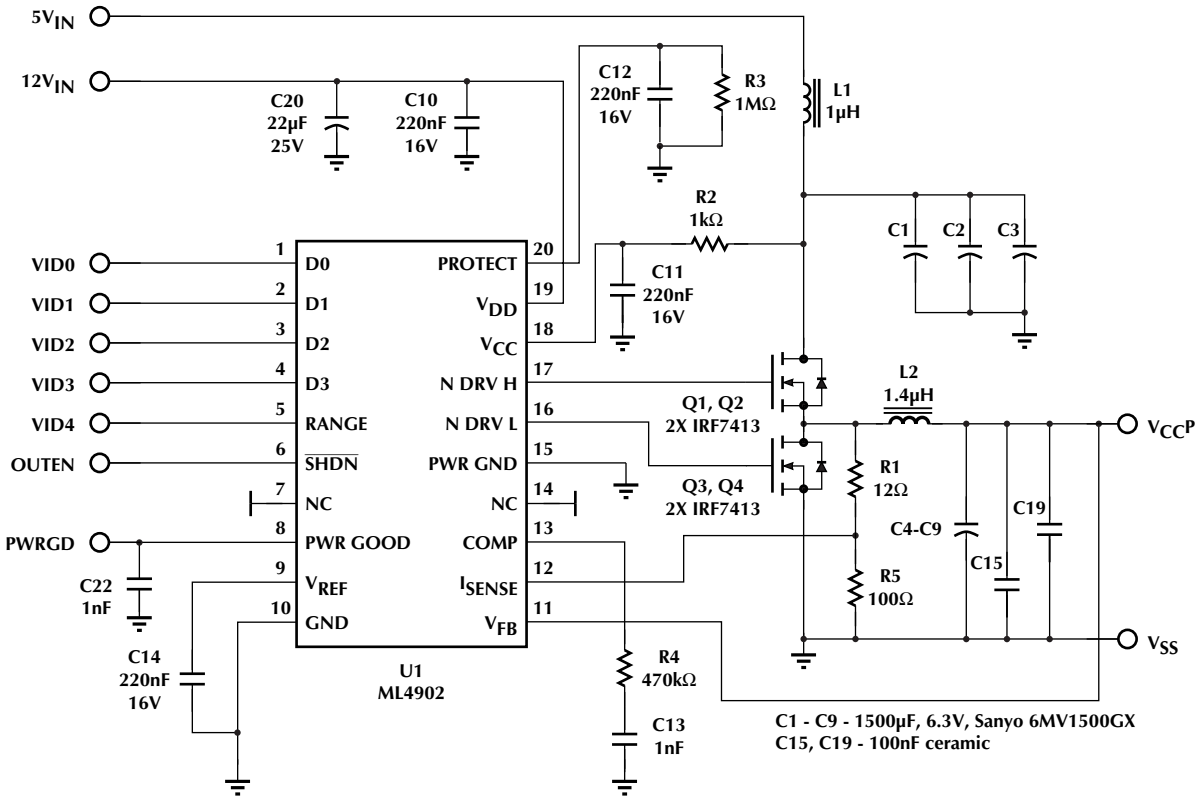


Figure 1. Typical VRM Circuit

DESIGN CONSIDERATIONS

This section is a quick-check guide for getting ML4902 circuits up and running, with a special emphasis on Pentium Pro and Pentium II applications. Unless otherwise noted, all component designators refer to the circuit shown in Figure 1.

COMPENSATION

The R and C values connected to the COMP pin for loop compensation are 330kΩ and 33pF, respectively. These values yield stable operation and rapid transient response for a most values of L2 and C_{OUT} (1µH to 5µH, 3600µF to 10,000µF), and will generally not need to be altered. If changes do need to be made, note that the drive capability of the transconductance error amplifier is typically 20µA, its Z_{OUT} is 5MΩ, and its unity-gain crossover frequency is approximately 10 MHz.

INPUT AND OUTPUT CAPACITORS

The input and output capacitors used in conjunction with the ML4902, especially in Pentium Pro and Pentium II applications, must be able to meet several criteria:

1. The input capacitors must be able to handle a relatively high ripple current

2. The output capacitors must have a low Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL)

3. The output capacitors must be able to hold up the output during the time that the current through the buck inductor is slewing to meet a transient load step.

The circuit's input bypass capacitance should be able to handle a ripple current equal to 0.5 x I_{LOAD}. If the converter sees load peaks only occasionally, and for less than 30 seconds at a time during those intervals, then the aluminum electrolytic or OS-CON® input capacitors need only be sized to accommodate the average output load. Note that tantalum input capacitors have much less thermal mass than aluminum electrolytics, so this relaxation of ripple current requirements may not apply to them.

During a 30A/µs load transient, it is not practical for a buck converter to slew the its current fast enough to regulate the instantaneous output voltage required by this application. During the first few microseconds following such a "load step," the output capacitance of the converter must act as a passive energy source. In delivering its energy to the load, the output capacitance must not introduce any considerable impedance, or its purpose will be defeated. A total voltage aberration during load transients of ±5% is allowed for the Pentium Pro and Pentium II. The voltage transient due to ESL and ESR is:

$$\Delta V = \left[(ESR \times \Delta V_{OUT}) + \left(ESL \times \frac{di}{dt} \right) \right] \quad (1)$$

For example, assume that the output voltage of the ML4902 is set to 2.8V. To allow no more than 3% of ΔV_{OUT} to be contributed by the ESR (84mV) of the output capacitance, and 2% by its ESL (56mV), the output ESR should not exceed:

$$ESR(MAX) = \frac{84mV}{14A} = 6m\Omega \quad (2)$$

Similarly, the output ESL should be less than or equal to:

$$ESL(MAX) = \frac{1\mu s}{30A} \times 56mV = 1.8nH \quad (3)$$

Achieving these low values of ESL and ESR is not trivial; doing so typically requires using multiple high-quality capacitors in parallel, often with dedicated power and ground planes to minimize interconnection impedance.

The output capacitance should have a value of > 2200µF to hold the output voltage relatively constant (< 50mV of sag) until the current in the buck inductor can catch up with the change in output current. To meet the ESR and ESL requirements, the actual output capacitance will usually be significantly greater than this theoretical minimum. These capacitors can be of all one type, or a combination of aluminum electrolytic, OS-CON®, and tantalum devices.

Figures 2(a) and 2(b) show oscilloscope photographs of the transient response of the circuit shown in Figure 1.

OVERCURRENT PROTECTION

Overcurrent protection for the ML4902 application circuit can be accomplished either by using a low value sense resistor placed between the current recirculating rectifier and ground, or by directly monitoring the voltage drop across a synchronous rectifier MOSFET (Q3||Q4) during its conduction period. Using a current sense resistor has the advantages of accuracy over the entire operating temperature range, and of allowing the use of a Schottky diode in place of a synchronous rectifier if the efficiency loss is acceptable. The disadvantages to using a sense resistor are higher cost and increased power dissipation. Sensing across the synchronous rectifier has the advantages of lower cost and of enhanced protection against overtemperature conditions (the current limit point is linearly reduced as the MOSFET temperature rises).

If a current sensing resistor is employed (see Figure 3), the resistor monitors the inductor current during the buck converter's off period. This is the interval during which current will recirculate through the synchronous rectifier, or the Schottky diode if no synchronous rectifier is used. Given a –87mV minimum trip point for the overcurrent comparator, the value required for the sense resistor can be found by:

$$R_{SENSE} = \frac{|-87mV|}{(1.05 \times I_{OUT(MAX)})} \quad (4)$$

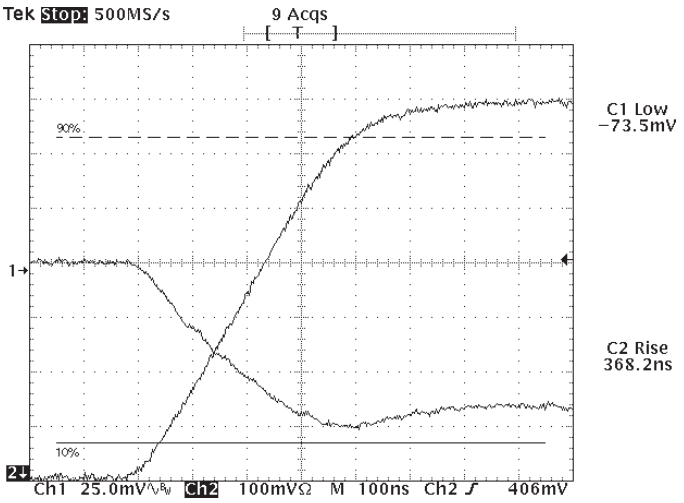


Figure 2a. Output Transient Response of Figure 1 Circuit, I_{OUT} from 0A to 14A (Channel 1 = V_{OUT}, Channel 2 = I_{OUT}).

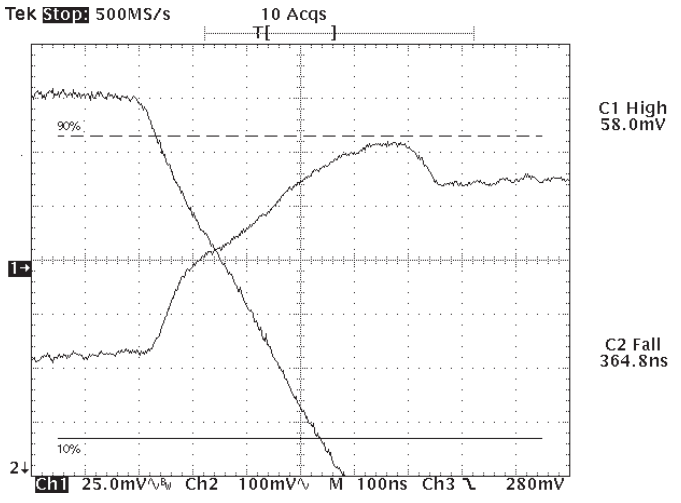


Figure 2b. Output Transient Response of Figure 1 Circuit, I_{OUT} from 14A to 0A (Channel 1 = V_{OUT}, Channel 2 = I_{OUT}).

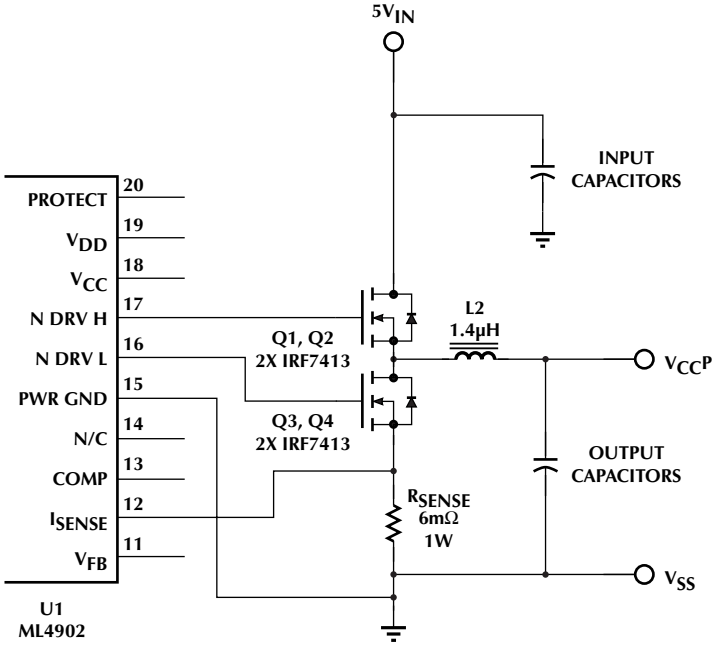


Figure 3. Connecting a Sense Resistor to the ML4902

DESIGN CONSIDERATIONS (Continued)

The power handling requirement for R_{SENSE} is given by:

$$P_D = I_{OUT(MAX)}^2 \times \left[\sqrt{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \times R_{SENSE} \right] \quad (5)$$

For example, for a 14A output, R_{SENSE} should be:

$$R_{SENSE} = \frac{|-87mV|}{1.05 \times 14A} = 5.92m\Omega \cong 6m\Omega$$

The maximum dissipation in R_{SENSE} for a 5.0V input occurs at 1.80V out, where P_{DISS} is ≅ 0.94W.

R_{SENSE} must be a low inductance part, such as Dale/ Vishay's type WSL-2512 series (WSL–2512–.006±1%). Using a PCB trace as a current sense element is not recommended due to the high temperature coefficient of copper, and due to etching and plating tolerances which can occur from board to board.

If a current sense resistor is not employed for overcurrent protection, the voltage drop across (Q3||Q4)'s channel during its conducting interval (the synchronous rectification interval) is used to monitor the inductor current. Ignoring the AC component of the current in the buck inductor, the voltage across (Q3||Q4) will be:

$$V_{SENSE} = I_{(Q3\|Q4)} \times R_{DS(ON)(Q3\|Q4)} \quad (6)$$

$R_{DS(ON)}$ is typically specified at a MOSFET junction temperature (T_j) of 25ºC, but its value at other junction temperatures can either be found graphically in the MOSFET data sheet, or can be estimated by:

$$R_{DS(ON)(T2)} = R_{DS(ON)(25ºC)} \times [1.007 \times (T2 - 25º C)] \quad (7)$$

With a nominal threshold of -97mV for the I_{SENSE} comparator, the current limit threshold is then:

$$I_{LIMIT} = \frac{|-97mV|}{R_{DS(ON)(T2)}} \quad (8)$$

For Pentium Pro and Pentium II applications, the continuous current may be as high as 14A, so the current limit threshold should be set for a minimum value of 16A at the (Q3||Q4)'s highest anticipated T_j. If necessary, the voltage across the channel of (Q3||Q4) may be divided using two moderately-valued resistors (use R5 = 100Ω) and presented after that division to the ML4902.

The R and C values connected to the PROTECT pin for setting the current limit delay and the off-time of the hiccup mode are 1MΩ and 220nF, respectively. These values will protect the external power components and the power source from overheating during an overcurrent condition. If it is necessary to change the ratio of on and off times during overcurrent conditions, this can be done by selecting a different value for C12. Larger values of C12 will increase the delay between retry attempts (the length of the "hiccup"), and smaller values will reduce the delay.

HIGHER CURRENT LEVELS

Next generation processor chips will require currents of up to 20A. Additionally, it is often desirable in larger systems to distribute all power from one 5V buss, regulating it down to other voltages as needed at the points of use. These applications are readily met by the ML4902. For instance, the circuit shown in Figure 1 will deliver an output current of 20A with only three changes:

- As I_{OUT} increases, the ripple current through the input capacitor bank will also increase. Add at least one 1500µF, 6.3V input capacitor in parallel with the three shown (C1 - C3).

- Synchronous rectifier transistors Q3 and Q4 will see a significantly greater RMS drain current at 20A output than at 14A. Therefore, the use of lower $R_{DS(ON)}$ parts such as Siliconix' Si4420DY is required.

- The value of R1 may require adjustment, depending upon factors such as the specific MOSFET type chosen for Q3 and Q4, and the required operating ambient temperature.

In dealing with circuits handling greater than 50W, it is always important to pay attention to thermal issues. When the circuit of Figure 1 is modified for >20A applicatons, a key consideration is that it be provided with adequate heatsinking. Ideally, the system should provide 100 linear feet per minute (LFM) of airflow as specified in Intel's standards relating to VRMs. Micro Linear does not recommend using the sense resistor method of overcurrent protection at high output current levels, as this does not provide the inherent thermal foldback of $I_{OUT(MAX)}$ which is obtained by directly sensing the $V_{DS(ON)}$ of the rectifier MOSFETs.

DESIGN CONSIDERATIONS (Continued)

LAYOUT ISSUES

The two pins of the ML4902 which actually sense the current limit voltage are I_{SENSE} and GND. To facilitate the required low-level sensing of the voltage between these pins, there is no connection inside the ML4902 between GND and PWR GND. Because of this, there must be an external connection between the ML4902 GND and PWR GND pins. PWR GND must have a low impedance connection to the ground plane used on the board, as high instantaneous currents will flow in PWR GND when N DRV L and N DRV H switch the capacitive loads of the output MOSFET gates. At the same time, GND must not see the resulting switching spikes.

If a current sensing resistor is used, the voltage across the resistor must be Kelvin-sensed. This ensures that the ML4902 monitors only the voltage across the resistor, and ignores the voltage drops and inductive transients in the PCB traces which carry current into and out of this resistor. The two pins of the ML4902 which must be Kelvin-connected to the sense resistor are I_{SENSE} and GND. PWR GND should then return to the to the grounded end of R_{SENSE} as well, using a high current Kelvin connection. This causes any noise across the resistor to appear primarily as a common-mode signal on I_{SENSE}, GND, and PWR GND. Figure 4 shows a recommended implementation of these PCB layout requirements.

When directly monitoring the voltage across the channel of the synchronous rectifier, the voltage across that MOSFET should be sensed as closely as possible to its drain. If a resistor divider is used to reduce the voltage at the I_{SENSE} pin for a given current through (Q3||Q4)'s channel resistance, then the lower end of the divider should be returned to the immediate vicinity of its source. This ensures that the ML4902 monitors only the voltage across the synchronous rectifier, and not the voltage drops or inductive transients in the PCB traces which carry current into and out of it. If a PC board with a dedicated ground plane is used (recommended), the best return points for GND and PWR GND are directly into the ground plane. If the board does not have a dedicated ground plane, GND must be returned to a point near the IC which is relatively free from switching transients. Such a point may need to be empirically determined but will usually be near the ground connection of the output capacitor bank.

MISCELLANEOUS POINTS

I_{SENSE} is the input to a medium-speed, high-sensitivity comparator (roughly comparable to an LM339-type comparator in terms of speed of response). Because of the leading-edge blanking on this comparator, it has a substantial ability to reject switching noise. Still, proper circuit function requires that the comparator not see significant noise at the time during which the synchronous rectifier MOSFET is on.

The compensation components R4 and C13 are high-impedance nodes connected to the output of the voltage loop error amplifier. These components should be kept in close proximity to the ML4902. C13 should be returned to GND, not to PWR GND or the ground plane of the PC board.

Keep the V_{REF} bypass capacitor C8 close to the ML4902. Ensure that its ground connection is to GND, not to PWR GND.

The 12V V_{DD} input is the supply from which the internal circuitry of the ML4902 operates. V_{DD} also provides the gate drive for N DRV H and N DRV L. The V_{DD} bypass capacitors C10 and C20 should be returned to PWR GND or to the PC board ground plane. They should not be returned to GND due to high transient currents which could interfere with the current sensing function.

V_{CC} is the input to the 5V undervoltage lockout comparator circuitry. The 5V UVLO function makes the start-up of the ML4902 independent of power sequencing. It also provides additonal overcurrent protection in case V_{CC} should go below acceptable levels (current drawn from the bulk 5V supply will rise as the actual voltage of that supply decreases). To reject switching noise on the 5V input, an RC filter should be used between the 5V source and V_{CC}. Typical values for this filter are R2 = 1kΩ, and C11 = 220nf.

Optional capacitor C22 may be needed in some layouts to filter out "glitches" which could occur on the PWR GOOD signal. In conjunction with the resistive pullup for the PWR GOOD line, its value should yield an RC product of approximately 5µs.

In order to reduce circuit size, complexity, and cost, an all N-channel power MOSFET output stage is employed. The gate drive voltage for both the sourcing and the rectifying MOSFETs is derived from the 12V input bus. This delivers at least 10V of V_{GS} enhancement to the rectifier MOSFET(s). The power sourcing MOSFET(s), however, have a worst-case V_{GS} enhancement of about 6V, and must therefore be logic-level parts.

If a given design uses power MOSFETs in an 8 pin SOIC package style, keep in mind that the thermal dissipation capability of these parts is largely dictated by the copper area available to their drains. A good layout will maximize this area.

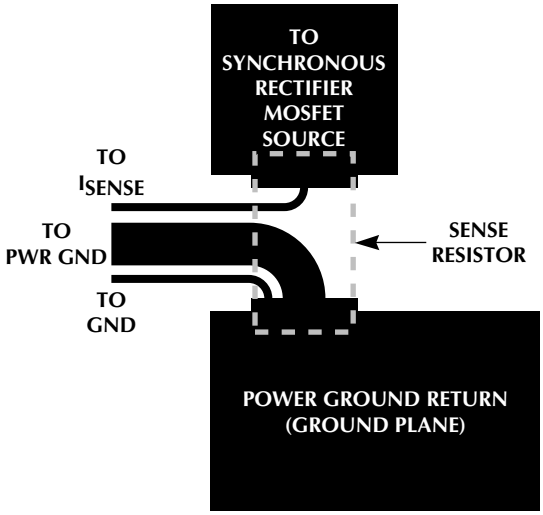
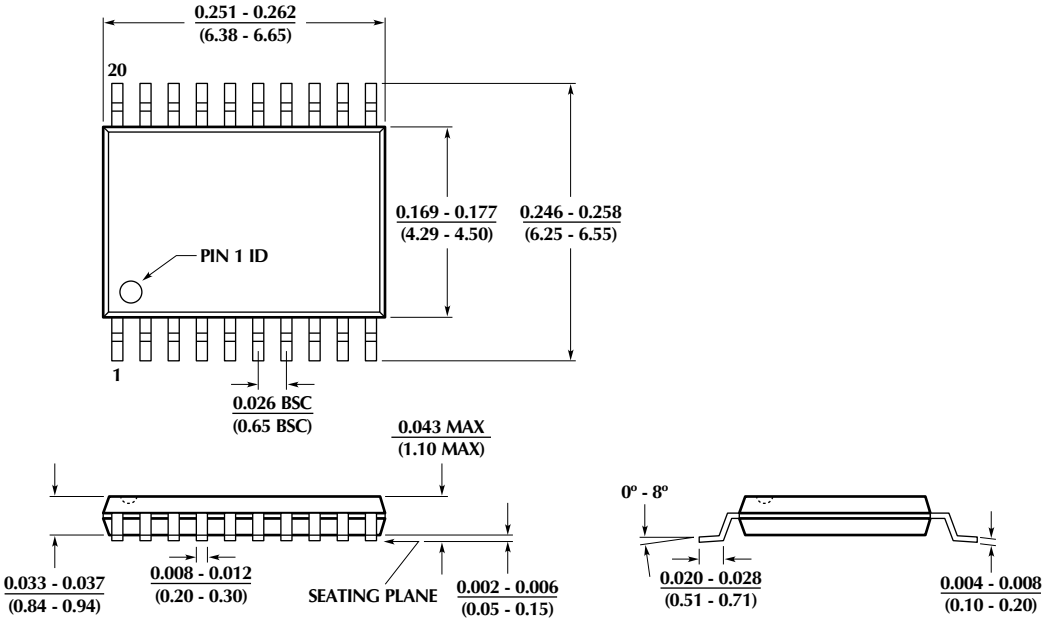


Figure 4. Kelvin Sense Connections

PHYSICAL DIMENSIONS inches (millimeters)

Package: T20
20-Pin TSSOP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4902CT	0°C to 70°C	20 Pin TSSOP (T20)

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,754,012; 5,757,174. Japan: 2,598,946; 2,619,299; 2,704,176. Other patents are pending.

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