F75223

BIOS Guard

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F75223 Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	2011/8	-	Preliminary Version
V0.11P	2011/8	26	Update Application Circuit
V0.12P	2011/8	--	Typo correction
V0.13P	2011/09	--	Update Package Information / Register Descirption.
V0.14P	2011/10	--	Update Package Information / Register Descirption.
V0.15P	2011/11	--	Update Register Description
V0.16P	2012/01	--	Add New Function Description

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1. General Description

The F75223 is a BIOS Guard which can copy the BIOS code from one SPI flash to another. The F75223 provides an interface to connect 2 SPI flashes and supports manual/auto mode option. Mode option can be decided by hardware strapping (by PWROK pin) or register setting.

Two SPI flashes can be assumed to flash A and flash B. For manual mode, the F75223 controls flash A or B to read or program by the SPI host which means only one flash could be accessed by the SPI host.

For auto mode, the F75223 sequentially controls flash A and B to read or program by the SPI host. F75223 provides a watch dog timer and PWROK detect function. When system power on, the WDT function will count down to zero and the PWROK status would be detected in the meantime. Timeout or the PWROK failure will trigger the reset signal to the system and sequentially change to backup flash for booting. Also, the F75223 would alternate the flash when PWROK failure occurs.

The F75223 is programmed by SMBUS interface, and only support Byte Read/Write protocol. The chip is powered by VSB and packaged in 20 QFN Green Spec.

2. Feature List

- **General Functions**
  - Bi-directional BIOS recovery
  - Manual copy by button (low pulse, de-bounce 4 seconds)
  - Strap status when PWROK rising and load to state machine immediately
  - 4 modes of LED status blinking (A, B, burn in from B to A or A to B)
  - WDT timer (1sec ~ 16sec, default 10sec)
  - PWROK counter
  - Power-Down mode
  - Programmable SPI command, register include

    Chip Erase command (0xC7)

    Read command (0x03)

    Program command (0x02)

    Write enable command (0x06)

    Write disable command (0x04)

    Read status command (0x05)

    Enable Write Status command (0x50)

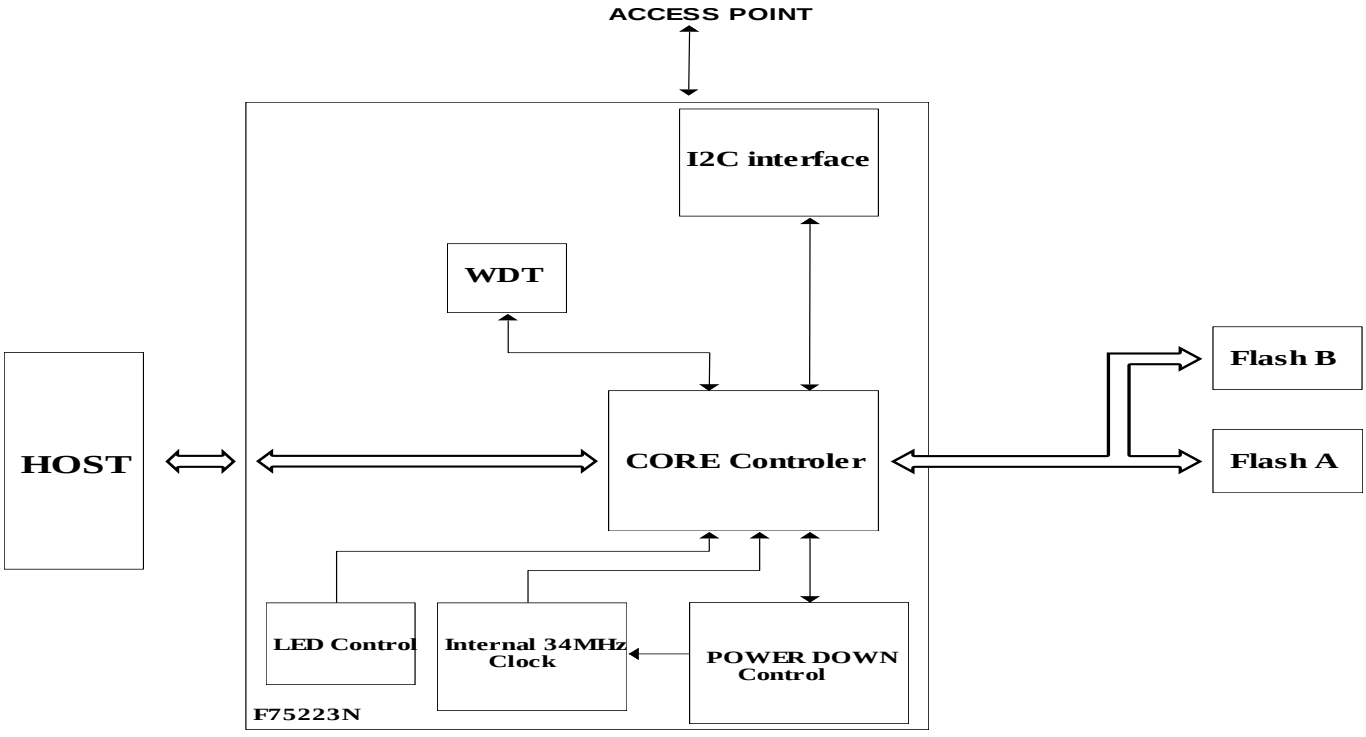
    Write Status command (0x01)

    Long Wait time register
- **Package**
  - 20-pin QFN Green Package

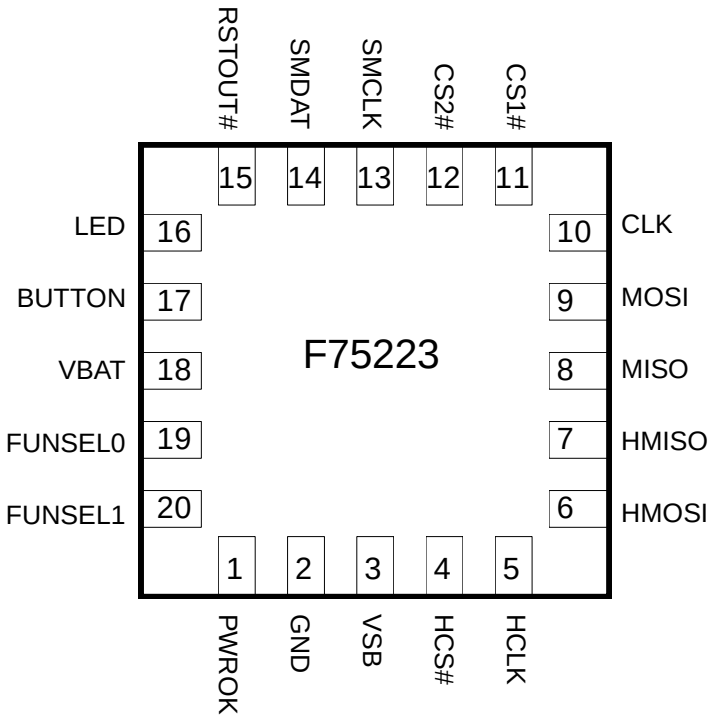
3. Key Specification

- Supply Voltage 3.0V to 3.6V
- Maximum Operation Supply Current (VSB) 5mA Max.
- Idle Current (VSB) 3.5mA Max.
- Power Down Mode Current (VSB) 10uA Max
- VBAT Current (Operation / Idel / Power Down) <1uA

4. Block Diagram



5. Pin Configuration



6. Pin Description

I	Input, 5V tolerance
$IN_{st,5v}$	TTL level input pin and schmitt trigger, 5V tolerance.
O	Output, 5V tolerance
O_{16}	Output pin with 16 mA sink capability.
$OD_{12,5v}$	Open drain, 12mA sink capability, 5V tolerance
$I/OD_{12st,5v}$	TTL level bi-directional pin and schmitt trigger,Open-drain output with 12 mA source-sink capability, 5V tolerance.
P	Power pin

Power Pin

Pin No.	Pin Name	Type	Description
2	GND	P	Ground.
3	VSB	P	3V power.
18	VBAT	P	3V power

SMBUS Interface

Pin No.	Pin Name	Type	PWR	Description
13	SMCLK	$I/OD_{12st,5v}$	VSB	SMBUS clock.
14	SMDAT	$I/OD_{12st,5v}$	VSB	SMBUS data.

Host SPI Interface

Pin No.	Pin Name	Type	PWR	Description
4	HCS#	I	VSB	SPI chip select from Master.
5	HCLK	I	VSB	Master SPI clock.
6	HMOSI	I	VSB	Master data out and slave data input.
7	HMISO	O	VSB	Master data in and slave data out.

Slave SPI Interface

Pin No.	Pin Name	Type	PWR	Description
8	MISO	I	VSB	Master data input and slave data output.(Bypass Mode)
		$IN_{st,5v}$		Master data input and slave data output.(Refresh Mode)
9	MOSI	O	VSB	Master data output and slave data input.(Bypass Mode)
		O_{16}		Master data output and slave data input with 16 mA sink capability.(Refresh Mode)
10	CLK	O	VSB	Slave SPI clock.(Bypass Mode)
		O_{16}		Slave SPI clock with 16 mA sink capability.(Refresh Mode)
11	CS1#	O	VSB	SPI chip select 1.(Bypass Mode)
		O_{16}		SPI chip select 1 with 16 mA sink capability. (Refresh Mode)
12	CS2#	O	VSB	SPI chip select 2.(Bypass Mode)
		O_{16}		SPI chip select 2 with 16 mA sink capability. (Refresh Mode)

System Signal Interface

Pin No.	Pin Name	Type	PWR	Description
1	PWROK	$IN_{st,5v}$	VSB	Power OK signal input from SIO.
15	RSTOUT#	$OD_{12,5v}$	VSB	Reset output.

Flash Strap and Status

Pin No.	Pin Name	Type	PWR	Description
16	LED	$OD_{12,5v}$	VSB	LED output signal, indicate current block.
17	BUTTON	$IN_{st,5v}$	VSB	Input signal for manual back up flash, de-bounce 4s. Strap SMBUS address when VSB power on.
20,19	FUNSEL[1:0]	$IN_{st,5v}$	VSB	FUNSEL0: Strap flash block when PWROK rising.(1: A Flash / 0: B Flash) FUNSEL1: Strap auto or manual when PWROK rising.(1: Auto mode / 0: Manual mode)

7. Function Description

7.1 Strapping Function

The F75223 provides 3 pins of hardware power on strapping to select functions. There is a form to describe how to set the functions you want. These pin will strap signal when VSB power on or PWROK rising.

Table 7.1.1. Power on strapping configuration

Pin NO.	Symbol	Value	Description	Trapping by
17	BUTTON	-	Pull high 100K to select SMBUS address 0X58	VSB
		-	Pull high 1K to select SMBUS address 0x96	VSB
19	FUNSEL0	1	Pull high 1K to select A block	PWROK
		0	Pull down 1K to select B block	PWROK
20	FUNSEL1	1	Pull high 1K to select auto mode	PWROK
		0	Pull down 1K to select manual mode	PWROK

7.2 SPI

The F75223 could work in two modes, bypass mode and auto refresh SPI flash mode. The default function is bypass mode. In the situation that the main block flash (block A) crashed, the F75223 will assert a RSTOUT# signal to the system and switch to the block B flash. When BIOS detects the system is using secondary (block B) flash. The BIOS can refresh the flash from block B to block A , by sending a command to F75223 . When refreshing. The status of

BIOS recovery burn-in can be tracked from F75223's register. After refreshing, then the BIOS can assert a full reset command from IO base 0xCF9.

Figure 7.2.1 describe what is SPI signal source for SPI flash.

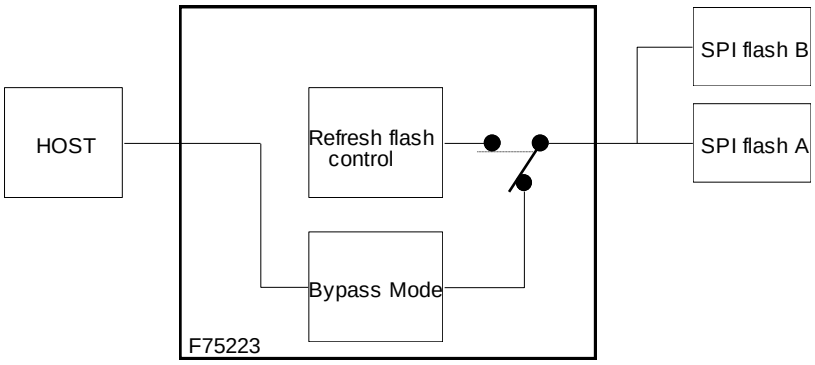


Figure 7.2.1 SPI signal path diagram

7.3 System Signal

7.3.1 RSTOUT#

When WDT timeout occurs, the F75223 will send a RSTOUT# signal to the system. The RSTOUT# can be set to assert the reset signal once or twice. The RSTOUT# issued low pulse least 200 ms. The high time space between first pulse and second pulse is 1 second. Figure 7.5.1 show as RSTOUT's status after WDT timeout occurs.

7.3.2 PWROK

After the F75223 receive the PWROK signal from SIO. A counter inside the F75223 counts the rising edges of PWROK. The F75223 will switch the flash from one to another, if the counter exceeds the limit threshold that set by the user. When the WDT_EN at index 0x02 was disable by host, the PWROK_VALUE at index 0x0a would be clear to zero. PWROK is also be used to control power-on strapping, The FUNSEL pins will strap signals when PWROK rising. Figure 7.3.2.1 show as PWROK counter exceeds the high limit illustrator.

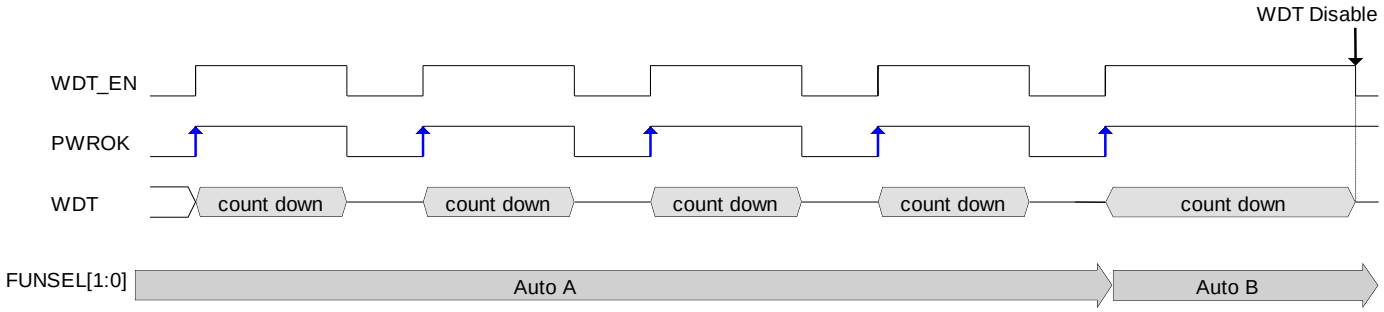


Figure 7.3.2.1 PWROK counter exceeds the high limit illustrator(when the PWROK_CNT at index 0x0ah has be set to 4)

7.4 Flash strap and status

7.4.1 LED

There are four types of LED status which can indicate which flash block is beening used or the F75223 is refreshing BIOS.

.

Table 7.4.1.1 LED Status Table

LED status	Description
Tri-state	Block A is in use
Sink low	Blcok B is in use
10 Hz pulse	Refreshing from B to A
1 Hz pulse	Refreshing from A to B

7.4.2 Function Select Pin

FUNSEL is the strap pin which controls the beheavers of F75223 when a BIOS error occurs.

Table 7.4.1.1 Function Select Status Table

FUNSEL[1:0]	Description
11	Auto Mode, using Block A flash as primary BIOS storage device. When an error occurs, it will automaticaly switch the flash from Block A to Block B.
10	Auto Mode, using Block B flash as primary BIOS storage device. When an error occurs, it will automaticaly switch the flash from Block B to Block A.
01	Manual select Block A flash. It won't switch to block B under any circumstance.
00	Manual select Block B flash. It won't switch to block A under any circumstance.

Auto mode: the F75223 will issue RSTOUT# to system and switch to the alternate flash device.

Manual mode: In manual mode. The system will only use the selected flash block to boot-up and the BIOS error protection mechanism are been disabled.

7.4.3 BUTTON

F75223 provides a button pin let user can refresh the flash from B to A or from A to B. The button de-bounce time is 4 seconds. When the button is pressed low for more than 4 seconds, the F75223 will set a start bit and auto refresh the flash block.

There are 2 correspond features of F75223 BIOS refersh function. The button event can sink the RSTOUT# signal low till the burn-in process been finished. Also, the F75223 can assert RSTOUT# to the system when the burn-in Flash finish. Figure 7.4.3.1 and Figure 7.4.3.2 show how the RSTOUT# actual behaves when the burn-in SPI flash starts.

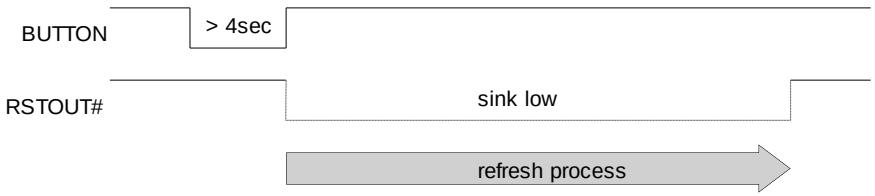


Figure 7.4.3.1 BUTTON illustrator with RSTOUT# sink low

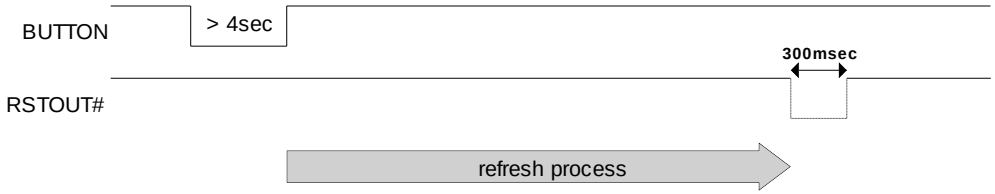


Figure 7.4.3.2 BUTTON illustrator with RSTOUT# low pulse

7.5 WDT

WDT, the watch dog timer counting is range from 1~16 seconds (default 10sec). It can be reset by PWROK low level signal and re-start counting again after PWROK rising.

In auto mode, and PWROK happened, the WDT will default enable. In manual mode, the WDT will default disable. The F75223 will issue RSTOUT# to system if the WDT timeout. Figure 7.5.1 and Figure 7.5.2 show as RSTOUT's status after WDT happened timeout.

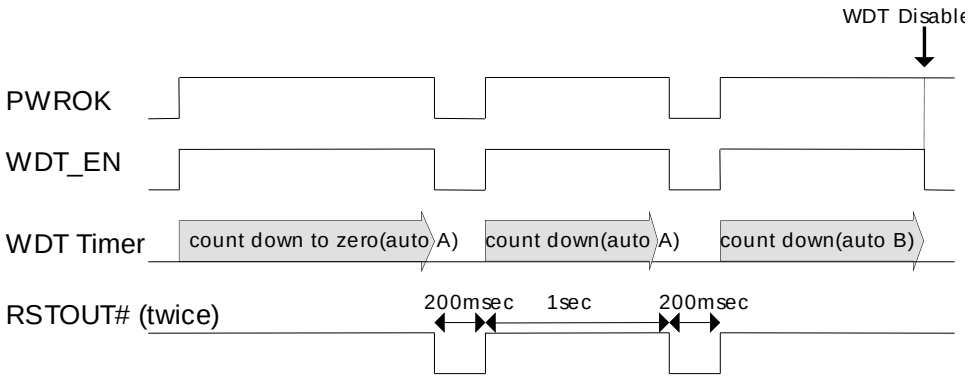


Figure 7.5.1 WDT timeout illustrator with two low pulse of RSTOUT

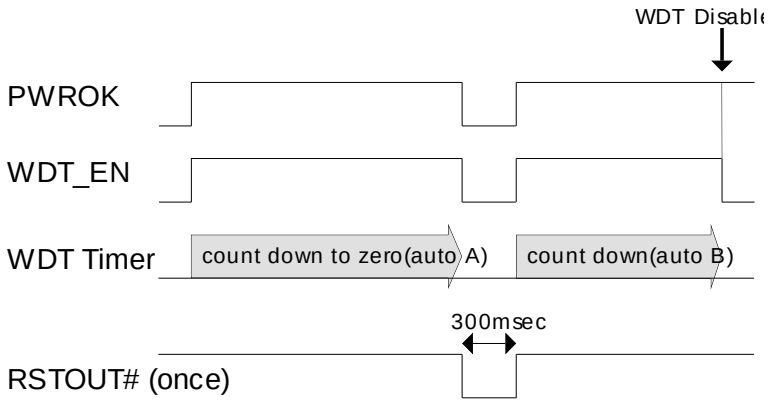


Figure 7.5.2 WDT timeout illustrator with single low pulse of RSTOUT (Default)

7.6 Auto Refreshing

The auto-refreshing would include erase function, read function and program function. The F75223 would support a complete auto-refreshing. Users only set the start bit for auto-refreshing (bit 7 at index 03h) or the button has been press low for more than 4 seconds after the flash size, SPI frequency, the destination of program would be set. The Figure 7.6.1 shows as Auto-refresh process flow.

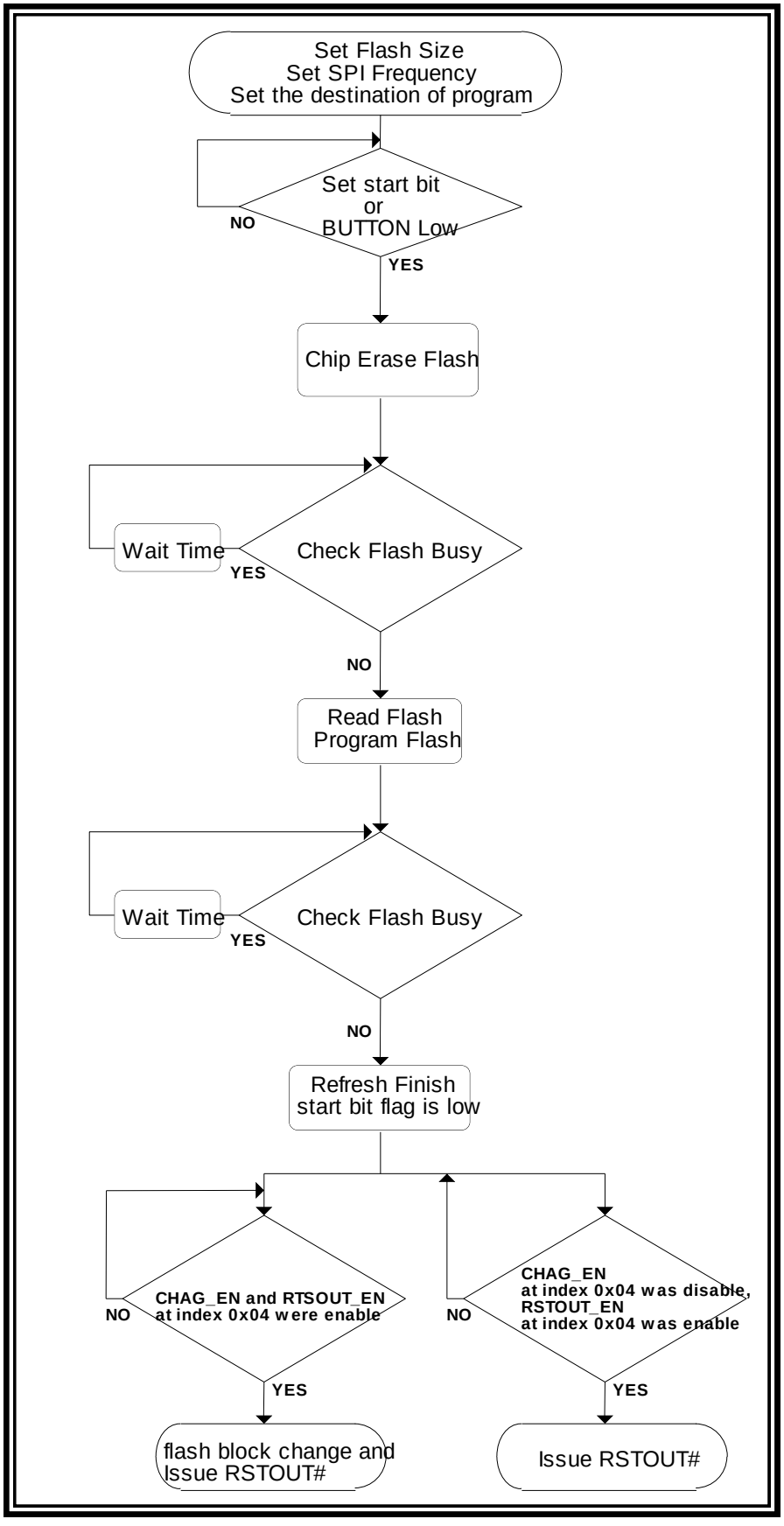


Figure 7.6.1 describe RSTOUT's status and flash block status after WDT happened timeout.

7.7 Auto Power Down mode

F75223 provides an auto power saving feature (**default disable**). User may enable this function, then the F75223 will go into power down mode automatically. If none of the six wakeup events (refresh enable, WDT enable, SMBUS busy, rstout low pulse, button pin low and pwrok rising edge) be asserted, the power down control module will count down to zero for power down internal clock(default 2 sec.). The F75223 will return to work, if one of those six wakeup events has been triggered, and stops the power down control module. The register at index 0x0bh controls the timing of count down. The Figure 7.7.1 describes how the system power down.

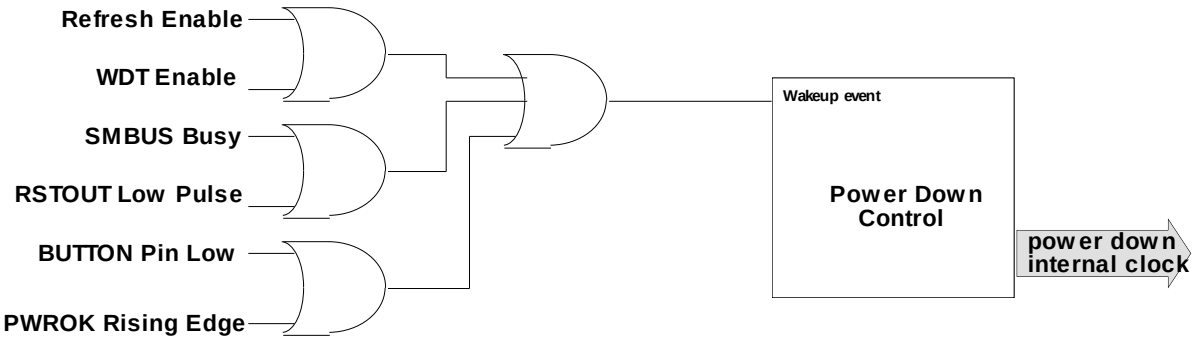


Figure 7.7.1 Power Down Control illustrator

8. Register Description

8.1 Flash Control

8.1.1 Flash Status Register – Index 00h

Bit	Name	R/W	Default	Description
7	AM_ST	R	-	The bit always shows the strap status of selected mode configuration. (AUTO or MANUAL mode, FUNSEL0 pin).
6	BK_ST	R	-	The bit always shows the strap status of selected primary block. (A block flash or B block flash, FUNSEL1 pin).
5	GET_AM	R	0h	This bit shows the SMBus modified mode configuration. This bit shows the corresponding setting status of AM_SEL bit at Index01h.
4	GET_BK	R	0h	This bit shows the SMBus modified block configuration. This bit shows the corresponding setting status of BK_SEL bit at Index01h.
3	WDT_TOFAG	R	0h	The flag would be set to 1, when the WDT count down to zero. Write 1 to clear this bit.
2	PWROK_TOFAG	R	0h	The flag would be set to 1, when the counter exceeds the high limit. Write 1 to clear this bit.
1	ACS_FAG	R	0h	When HOST accessed register at index 01h by SMBUS interface, the flag would be set to 1. Write 1 to clear this bit.
0	Reserve	-	-	Reserve

8.1.2 Flash Control Register – Index 01h

Bit	Name	R/W	Default	Description
7-2	Reserve	-	-	Reserve
1	AM_SEL	R/W	-	F75223 control flash status by AM_SEL (auto or manual mode). 1: Auto mode 0: Manual mode
0	BK_SEL	R/W	-	F75223 control flash block by BK_SEL (A block flash or B block flash). 1: A block flash 0: B block flash

If ACS_FAG flag at index 00h has be set to 1 and reboot of system, the AM_SEL register at index 01h will ignore the strap setting (FUNSEL0 pins). ACS_FAG flag at index 00h must be cleard to 0 and reboot of system, the AM_SEL register at index 01h will then follow the strap setting (FUNSEL0 pin).

In the conditional that one of flags (WDT_TO, PWROK_TO, ACS_FAG at index 00h) has be set to 1, the BK_SEL register at index 01h will ignore the strap setting (FUNSEL1 pin). All the flags (WDT_TO, PWROK_TO, ACS_FAG at index 00h) must be cleard to 0 and reboot of system, the BK_SEL register at index 01h will then follow the strap setting (FUNSEL1 pins).

8.2 WDT Control

8.2.1 WDT Control Register – Index 02h

Bit	Name	R/W	Default	Description
7	WDT_EN	R/W	0h	When PWROK rising happened, the bit would be set to 1.
6	RSTOUT_SEL	R/W	0h	0: RSTOUT# would issue one low pulse. 1: RSTOUT# would issue two low pulse.
5-4	Reserve	-	-	Reserve
3-0	WDT_SEC	R/W	9h	The WDT would count down to zero with WDT_SEC timing. 0000: 1sec 0001: 2sec 0010: 3sec 0011: 4sec … 1001: 10sec(Default) … 1110: 15sec 1111: 16sec

8.3 Auto Refresh Control

8.3.1 Auto Refresh Control1 Register – Index 03h

Bit	Name	R/W	Default	Description
7	REFH_EN	R/W	0h	When users set the bit to 1 or BUTTON pin has been pressed low for more than 4 seconds, the auto-refresh function would auto refresh the crashed flash. If the bit was set to 1, F75223 would refresh SPI flash.
6-4	SIZE_SEL	R/W	1h	Users would select the SPI flash's size by the register. 000: 1Mbyte 001: 2Mbyte (Default) 010: 4Mbyte 011: 8Mbyte 100: 16Mbyte Others: Reserve
3	DN_PRAM	R/W	0h	Users would set the destination of program by the register. 0: B block flash copy to A block flash. 1: A block flash copy to B block flash.
2-0	FREQ_SEL	R/W	3h	Users would select SPI frequency in auto-refresh mode by the register. 000: 34MHz (Duty cycle is not 50%) 001: 17MHz (Duty cycle is 50%) 010: 8MHz (Duty cycle is 50%) 011: 4MHz (Duty cycle is 50%, default) 100: 1MHz (Duty cycle is 50%) Others: Reserve

8.3.2 Auto Refresh Control2 Register – Index 04h

Bit	Name	R/W	Default	Description
7-6	Reserve	-	0h	Reserve

5	CHAG_EN	R/W	0h	When the bit and RTSOUT_EN must be set to 1 and auto-refresh has finish, the flash block would change to another flash block. Also, the RSTOUT# would issue the low pulse to system.
4	RTSOUT_EN	R/W	0h	When the bit has be set to 1 and auto-refresh has finish, the RSTOUT# would issue the low pulse to system.
3	CR_PWROK	R/W	1h	If the bit was set to 1 and PWROK has be 1, the bypass mode would be enable by F75223. Also, the bit was set to 0, the bypass mode wouldn't care PWROK signal.
2	SST_EN	R/W	0h	Set this bit to 1, if the flash been recovered is a SST Flash.
1	SINKL_EN	R/W	0h	When the bit was set to 1 and auto-refresh was processing, RSTOUT# would sink low until auto-refresh finish.
0	FLASH_BUSY	R	0h	When the bit was set to 1, F75223 would erasing or programing flash now.

8.3.3 Wait Time High Byte Register – Index 05h

Bit	Name	R/W	Default	Description
7-0	WAIT_TIMEH	R/W	10h	When flash has be busy, the auto-refresh state match would wait.

8.3.4 Wait Time Low Byte Register – Index 06h

Bit	Name	R/W	Default	Description
7-0	WAIT_TIMEL	R/W	9ch	When flash has be busy, the auto-refresh state match would wait. 0x109c indicate state match would wait 4253 refreshed clock cycles.

8.3.5 Refresh Status High Byte Register – Index 07h

Bit	Name	R/W	Default	Description
7-0	PERC_H	R/W	00h	Percentage of auto-refresh precess status.(high byte register)

8.3.6 Refresh Status Medium Byte Register – Index 08h

Bit	Name	R/W	Default	Description
7-0	PERC_M	R/W	00h	Percentage of auto-refresh precess status.(medium byte register)

8.3.7 Refresh Status Low Byte Register – Index 09h

Bit	Name	R/W	Default	Description
7-0	PERC_L	R/W	00h	Percentage of auto-refresh precess status.(low byte register)

The percentage of auto-refresh process status show as index 0x07h, 0x08h and 0x09h. Table 7.3.1 describles how the of refresh progress be shown in regesters.

Table 7.3.1 Percentage of auto-refresh precess status

Flash size	PERC({PERC_H,PERC_M, PERC_L)	percentage	PERC(SST Flash)	percentage
1M	0F,FF,00h	100%	0F,FF,FFh	100%
	00,00,00h	0%	00,00,00h	0%
2M	1F,FF,00h	100%	1F,FF,FFh	100%

	00,00,00h	0%	00,00,00h	0%
4M	3F,FF,00h	100%	3F,FF,FFh	100%
	00,00,00h	0%	00,00,00h	0%
8M	7F,FF,00h	100%	7F,FF,FFh	100%
	00,00,00h	0%	00,00,00h	0%
16M	FF,FF,00h	100%	FF,FF,FFh	100%
	00,00,00h	0%	00,00,00h	0%

8.4 PWROK Timeout Control

8.4.1 PWROK Timeout Control Register – Index 0ah

Bit	Name	R/W	Default	Description
7-5	PWROK_VALUE	R	0h	This The register show as happened pwrok times when system would not process into OS yet. When the WDT_EN at index 0x02 was disable by host, the PWROK_VALUE would be clear to zero.
6-3	Reserve		-	Reserve
2-0	PWROK_CNT	R/W	4h	When the register was set to 4 and PWROK counter exceed 4 times(5th), the F75223 would change another flash.

8.4.2 Power Down Control Register – Index 0bh

Bit	Name	R/W	Default	Description
7	PD_EN	R/W	0h	When the bit was set to 1, system would begin to count down to zero.
6-0	PD_SEC	R/W	32h	If wakeup event didn't happen, system would count PD_SEC timing. 0000000B: **Reserve** … 0110000B: **Reserve** 0110001B: **Reserve** 0110010B: ~2.04sec (Default) 0110011B: ~2.08sec 0110100B: ~2.12sec … 1111110B: ~5.08sec 1111111B: ~5.12sec

8.5 Instruction Control

8.5.1 Write Enable Instruction Register – Index 10h

Bit	Name	R/W	Default	Description
7-0	WREN	R/W	06h	Write Enable instruction.

8.5.2 Chip Erase Instruction Register – Index 11h

Bit	Name	R/W	Default	Description

7-0	CE	R/W	C7h	Chip Erase instruction.

8.5.3 Read Status Instruction Register – Index 12h

Bit	Name	R/W	Default	Description
7-0	READ_STUS	R/W	05h	Read status register instruction.

8.5.4 Read Instruction Register – Index 13h

Bit	Name	R/W	Default	Description
7-0	READ	R/W	03h	Read instruction.

8.5.5 Write Disable Instruction Register – Index 14h

Bit	Name	R/W	Default	Description
7-0	WRDIS	R/W	04h	Write Disable instruction.

8.5.6 Program Instruction Register – Index 15h

Bit	Name	R/W	Default	Description
7-0	PRGM	R/W	02h	Program instruction.

8.5.7 Enable Write Status Register Instruction Register – Index 16h

Bit	Name	R/W	Default	Description
7-0	ENWRSTUS	R/W	50h	Enable Write Status Register instruction.

8.5.8 Write Status Register Instruction Register – Index 17h

Bit	Name	R/W	Default	Description
7-0	WRSTUS	R/W	01h	Write Status Register instruction.

8.5.9 Reserve Register – Index 18h

Bit	Name	R/W	Default	Description
7-0	Reserve	-	00h	Reserve

8.5.9 Reserve Register – Index 19h

Bit	Name	R/W	Default	Description
7-0	Reserve	-	00h	Reserve

8.5.9 Reserve Register – Index 1ah

Bit	Name	R/W	Default	Description
7-0	Reserve	-	01h	Reserve

8.6 Chip Number

8.6.1 Chip ID1 Register – Index 5ah

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	11h	CHIP ID1

8.6.2 Chip ID2 Register – Index 5bh

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	07h	CHIP ID2

8.6.4 Vender ID1 Register – Index 5dh

Bit	Name	R/W	Default	Description
7-0	VENDER_ID1	R	19h	VENDER ID1

8.6.4 Vender ID2 Register – Index 5eh

Bit	Name	R/W	Default	Description
7-0	VENDER_ID2	R	34h	VENDER ID2

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VCC+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

9.2 DC Characteristics

(Ta = 0° C to 70° C, VCC = 3.3V ± 10% , VSS = 0V)

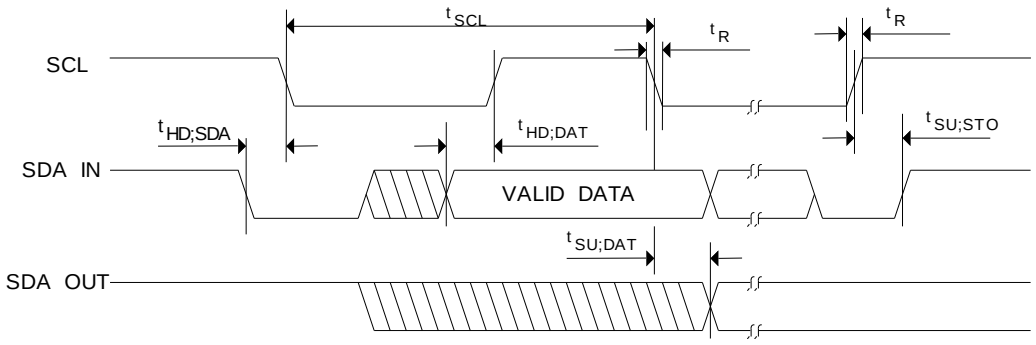
PARAMETER	RATING	
Operating Voltage	3.0 to 3.6	VCC
Operating Voltage	2.4 to 3.6	VBAT

PARAMETER	SYM.	MIN	TYP	MAX.	UNIT	CONDITIONS
I/OD$_{12st5v}$ - Open-drain output pin with 12mA source-sink capability(3.3V) and schmitt trigger, 5V tolerance						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		12		mA	0.4V
Input High Leakage	ILIH	-1		1	μA	
Input Low Leakage	ILIL	-1		1	μA	
OD$_{12st5v}$ - Open-drain output pin with 12mA source-sink capability, 5V tolerance						
Output Low Current	IOL		12		mA	0.4V
I/O$_{12st5v}$ - TTL level bi-directional pin with 4 mA source-sink capability(3.3V) and schmitt trigger, 5V tolerance						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		12		mA	0.4V
Output High Current	IOH		12		mA	2.4V
Input High Leakage	ILIH	-1		1	μA	
Input Low Leakage	ILIL	-1		1	μA	
O$_{16}$ - Open-drain output pin with 16mA source-sink capability, 5V tolerance						

Output Low Current	IOL		16		mA	0.4V
I – TTL level input pin and schmitt trigger, 5V tolerance						
Input Low Threshold Voltage				0.8	V	
Input Hign Threshold Voltage	2.0				V	
Hysteresis		0.5			V	
Input High Leakage				+1	µA	
Input Low Leakage	-1				µA	

9.3 AC Characteristics

9.3.1 SMBus Interface

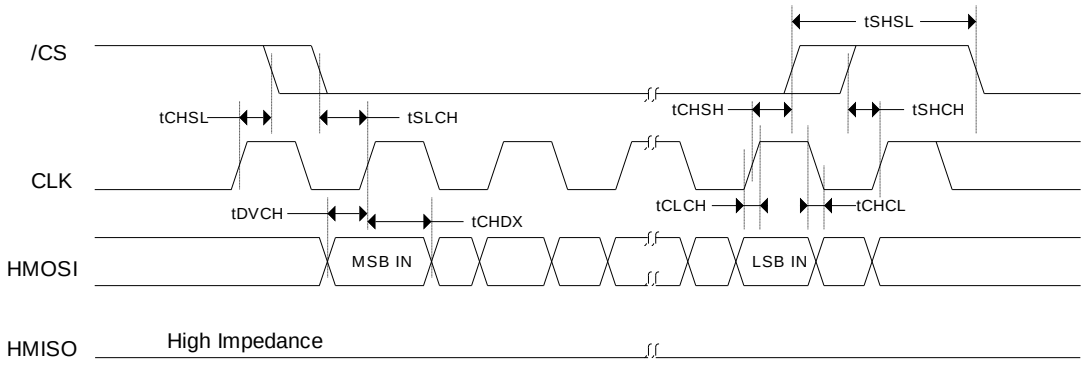


Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

9.3.2 SPI Interface



SPI Timing Diagram

SPI Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
/CS not active hold time relative to CLK	t_{CHSL}	5		nS
Data in setup time	t_{DVCH}	2		nS
/CS active setup time relative to CLK	t_{SLCH}	5		nS
Data in hold time	t_{CHDX}	5		nS
Clock rise time peak to peak	t_{CLCH}	0.1		V/nS
/CS active hold time relative to CLK	t_{CHSH}	10		nS
/CS deselect time	t_{SHSL}	100		nS
/CS not active setup time relative to CLK	t_{SHCH}	0		nS
Clock fall time peak to peak	t_{CHCL}	0.1		V/nS

9.3.3 Internal Clock

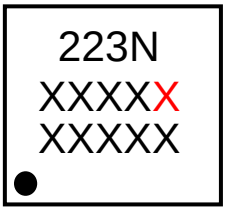
DESCRIPTION	TYP.		UNIT
Internal Clock	36	±20%	MHz

10.Ordering Information

Part Number	Package Type	Production Flow
F75223N	20-QFN Green Package	Commercial, 0°C to +70°C

11.Top Marking Specification

The version identification is shown as the bold red three characters. Please refer to below table for detail:



● : Pin 1 Identifier

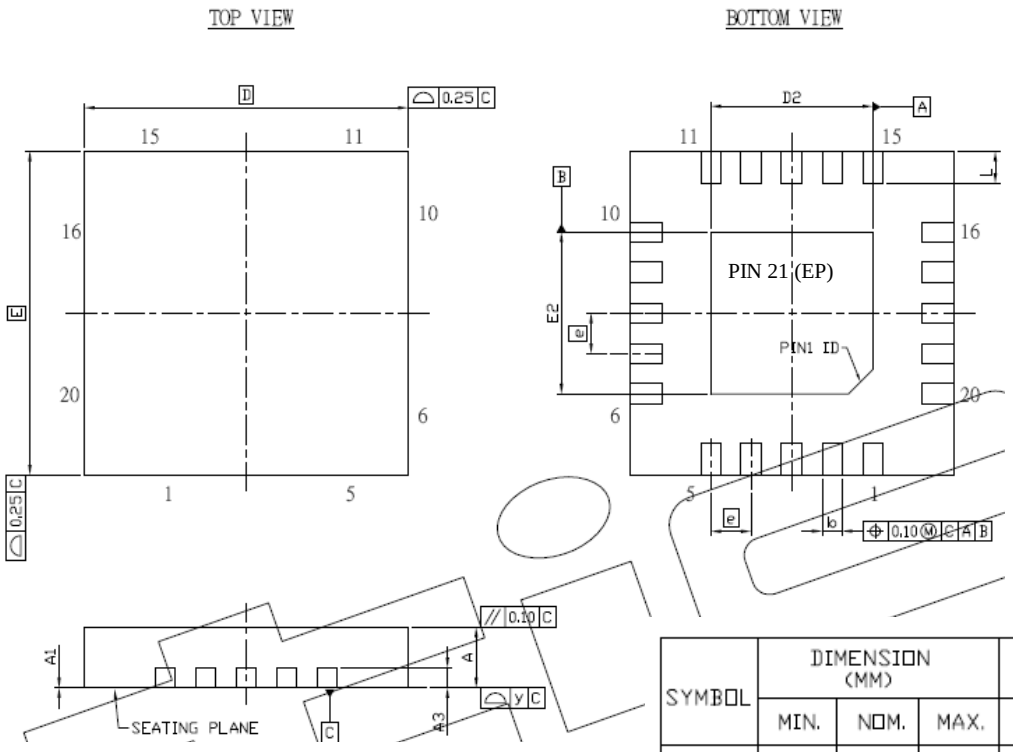
1st Line: Device Name → 223N, where N means the package code

2nd Line: Week Code (xx) + Fintek Internal Code (xx) + **IC Version (x)** where A means version A, B means version B, …

3rd Line: Wafer Fab Code (XXX…XX)

12.Package Dimensions

20 QFN



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.56	29.53	31.50
A1	0	0.02	0.05	0	0.79	1.97
A3		0.203 REF			8 REF	
b	0.18	0.25	0.30	7.09	9.84	11.81
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	1.90	2.00	2.10	74.8	78.7	82.7
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	1.90	2.00	2.10	74.8	78.7	82.7
e		0.50 BSC			19.69 BSC	
L	0.30	0.40	0.50	11.81	15.74	19.69
y		0.08			3.15	

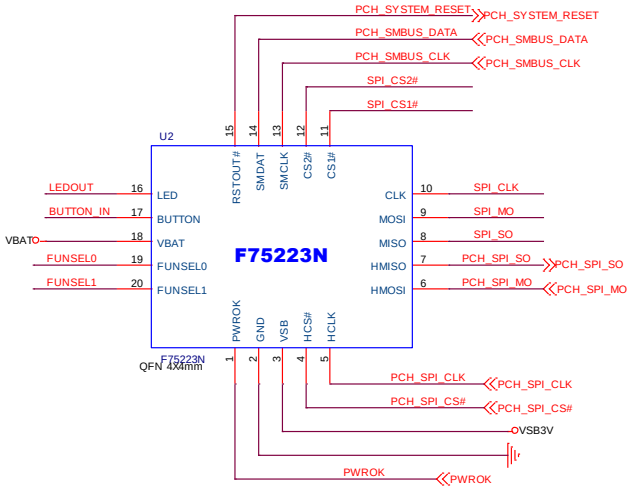
Feature Integration Technology Inc.

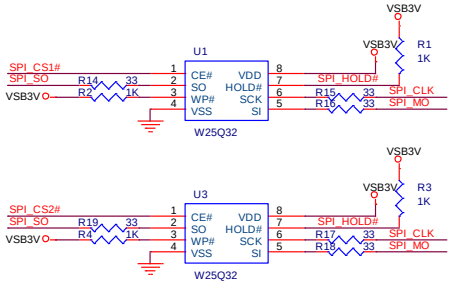
Headquarters
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Chupei City, Hsinchu, Taiwan 302, R.O.C.
TEL : 886-3-5600168
FAX : 886-3-5600166
www: http://www.fintek.com.tw

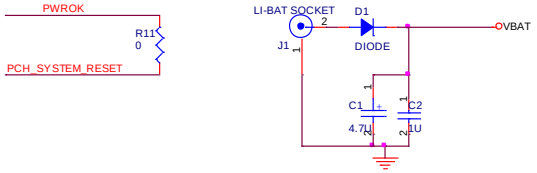
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TEL : 866-2-8227-8027
FAX : 866-2-8227-8037

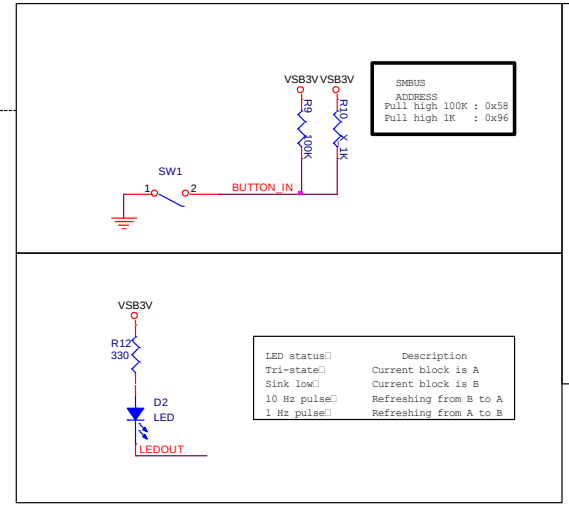
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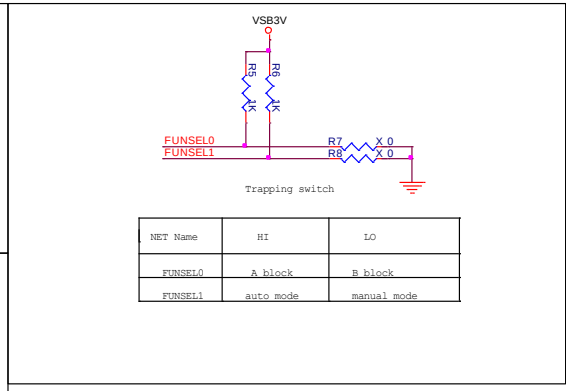
13. Application Circuit











Title	Feature Intergration Technology Inc	
Size B	Document Number F75223N Module Board	Rev 0.1
Date: Tuesday, October 18, 2011	Sheet 1 of 1	