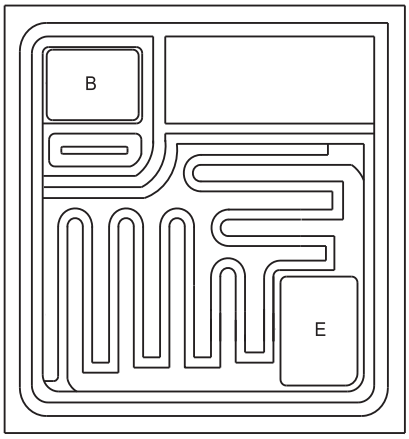
PROCESS CP707
Small Signal Transistor
PNP - Darlington Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	27 x 27 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	5.3 x 3.8 MILS
Emitter Bonding Pad Area	5.3 x 6.5 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



R1

BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER

15,165

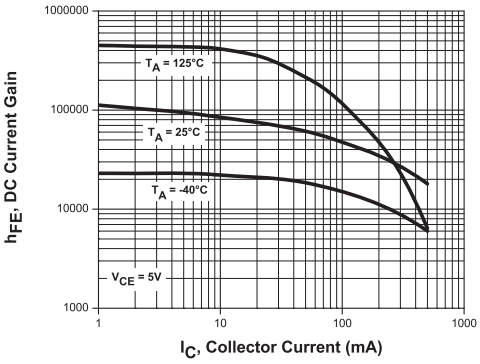
PRINCIPAL DEVICE TYPES

CMPTA63
CMPTA64
CXTA64
CZTA64
MPSA63
MPSA64

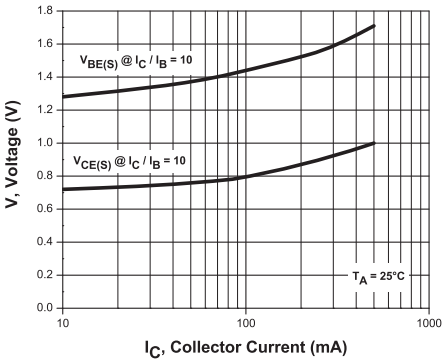
PROCESS CP707

Typical Electrical Characteristics

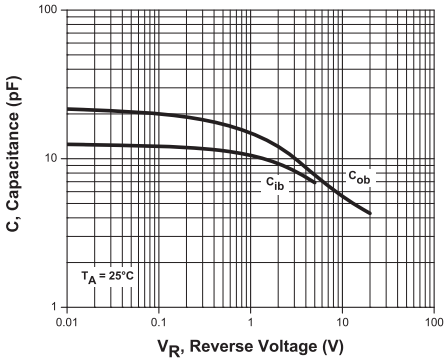
DC Current Gain



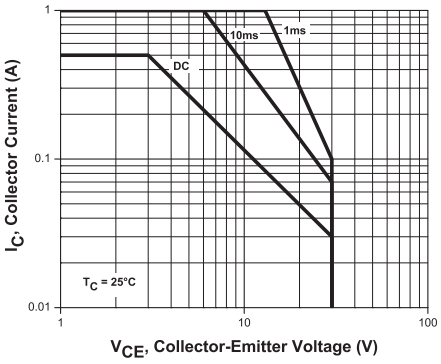
"ON" Voltage



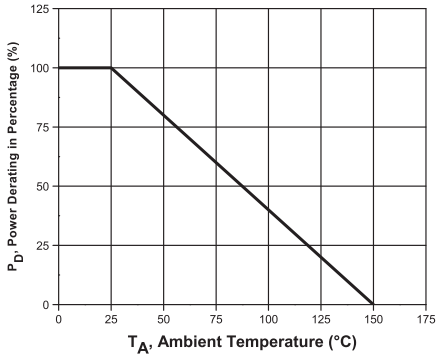
Capacitance



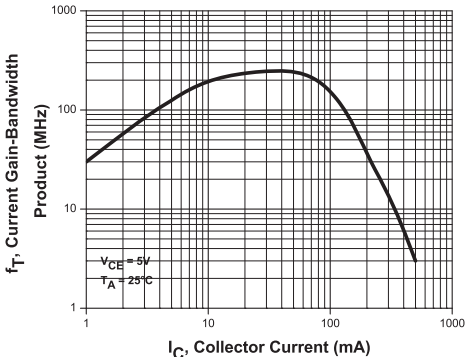
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



R6 (22-March 2010)