



# Bipolar TTL Logic – 7406

High Voltage Hex Inverter Buffer / Driver Logic IC in bare die form

Rev 1.0  
29/07/20

## Description

The 7406 comprises x6 inverter buffer/drivers with high voltage open-collector outputs. The device finds use as high-level circuit interface or for driving high-current loads and is also characterised to drive TTL inputs as inverted buffer. The device has a 30V minimum breakdown voltage and 40mA maximum sink current.

## Features:

- High Sink-Current Capability: 40mA
- High Voltage Open-Collector Driver
- Minimum breakdown voltage: 30V
- Input Clamp Diodes minimize transmission-line effects
- TTL compatible inputs
- Direct drop-in replacement for obsolete components in long term programs.

## Ordering Information

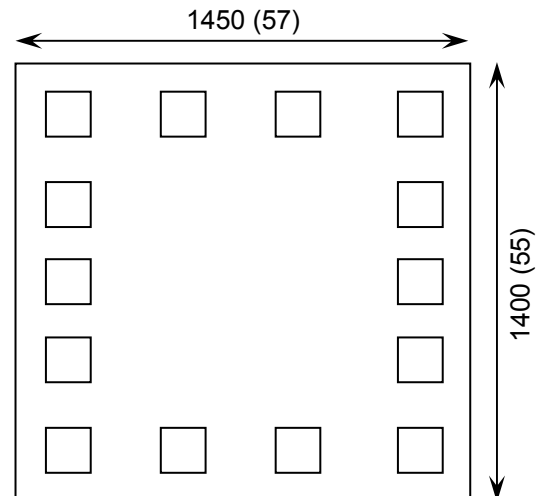
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[5406](#)

## Die Dimensions in $\mu\text{m}$ (mils)



## Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness  $\leftrightarrow$  350 $\mu\text{m}$ (14 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

Die Size (Unsawn)	1450 x 1400 57 x 55	$\mu\text{m}$ mils
Minimum Bond Pad Size	140 x 140 5.5 x 5.5	$\mu\text{m}$ mils
Die Thickness	350 ( $\pm$ 20) 13.78 ( $\pm$ 0.79)	$\mu\text{m}$ mils
Top Metal Composition	Al 1%Si 1.1 $\mu\text{m}$	
Back Metal Composition	N/A – Bare Si	

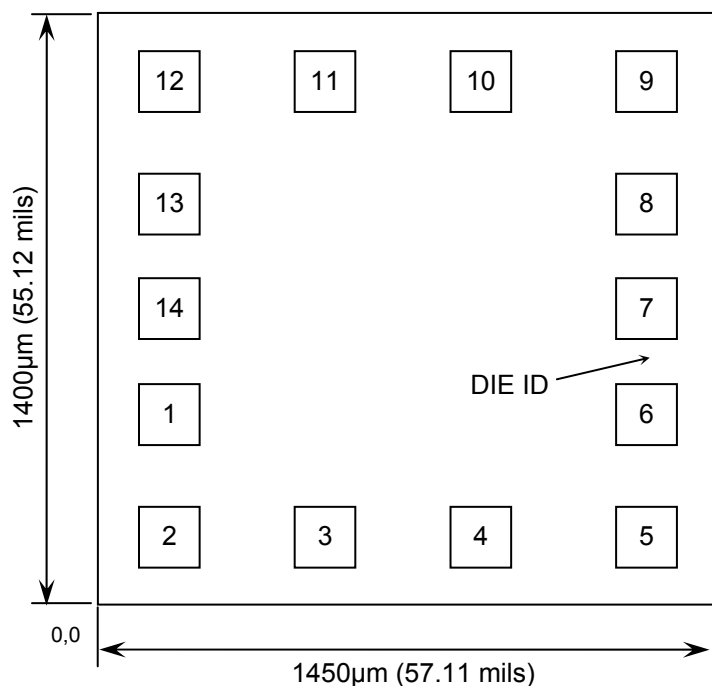




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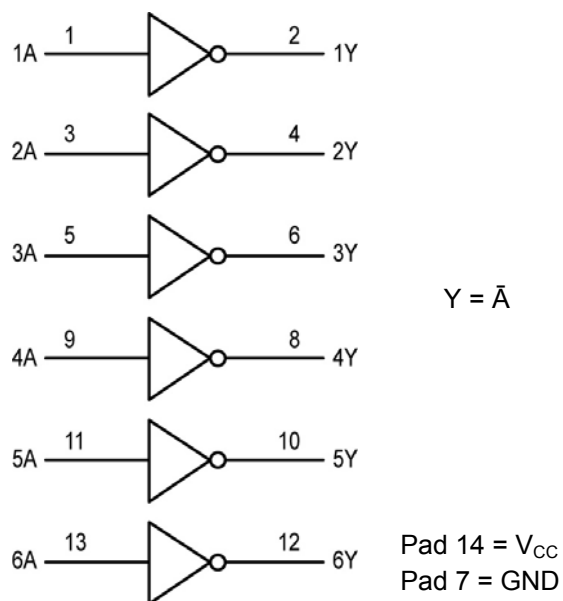
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.090	0.380
2	1Y	0.090	0.090
3	2A	0.460	0.090
4	2Y	0.830	0.090
5	3A	1.220	0.090
6	3Y	1.220	0.380
7	GND	1.220	0.630
8	4Y	1.220	0.880
9	4A	1.220	1.170
10	5Y	0.830	1.170
11	5A	0.460	1.170
12	6Y	0.090	1.170
13	6A	0.090	0.880
14	V <sub>CC</sub>	0.090	0.630

CONNECT CHIP BACK TO GND OR FLOAT

## Logic Diagram



## Truth Table

INPUTS	OUTPUT
A	Y
L	Z
H	L

H = High level (steady state)  
L = Low level (steady state)  
Z = High Impedance





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## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	$V_{CC}$	7.0	V
DC Input Voltage	$V_{IN}$	5.5	V
DC Output Voltage	$V_{OUT}$	30	
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

## Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{CC}$	4.75	5.25	V
High-Level Input Voltage	$V_{IH}$	2	-	V
Low-Level Input Voltage	$V_{IL}$	-	0.8	V
High-Level Output Voltage	$V_{OH}$	-	30	V
Low-Level Output Current	$I_{OL}$	-	40	mA
Operating Temperature Range	$T_J$	-40	+85	°C

## DC Electrical Characteristics<sup>2</sup> $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input Clamp Voltage	$V_{IK}$	$V_{CC} = 4.25\text{V}$ , $I_{IN} = -12\text{mA}$	-	-	-1.5	V
High-Level Output Current	$I_{OH}$	$V_{CC} = 4.25\text{V}$ , $V_{IL} = 0.8\text{V}$ , $V_{OH} = 30\text{V}$	-	-	0.25	mA
Low-Level Output Voltage	$V_{OL}$	$V_{CC} = 4.25\text{V}$ , $V_{IH} = 2\text{V}$ , $I_{OL} = 16\text{mA}$	-	-	0.4	V
		$V_{CC} = 4.25\text{V}$ , $V_{IH} = 2\text{V}$ , $I_{OL} = 40\text{mA}$	-	-	0.7	
Input Current	$I_{IN}$	$V_{CC} = 5.25\text{V}$ , $V_{IN} = 5.25\text{V}$	-	-	1	mA
High-Level Input Current	$I_{IH}$	$V_{CC} = 5.25\text{V}$ , $V_{IH} = 2.4\text{V}$	-	-	0.04	mA
Low-Level Input Current	$I_{IL}$	$V_{CC} = 5.25\text{V}$ , $V_{IL} = 0.4\text{V}$	-	-	-1.6	mA
Supply Current	$I_{CC}$	$V_{CC} = 5.25$ ,Output High	-	-	48	mA
		$V_{CC} = 5.25$ ,Output Low	-	-	51	





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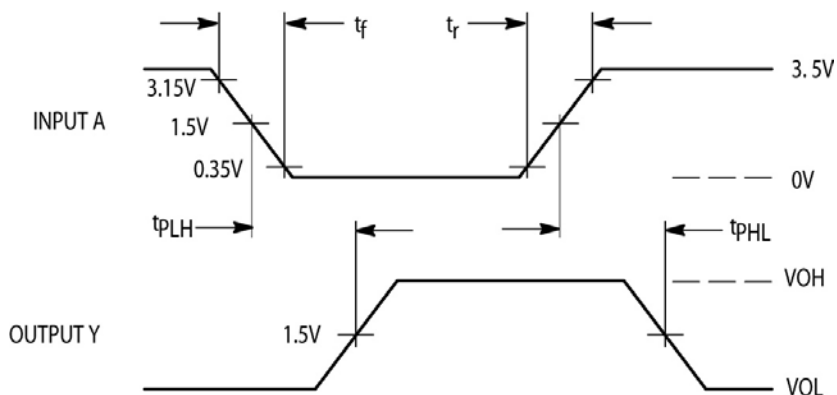
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## AC Electrical Characteristics<sup>2</sup>

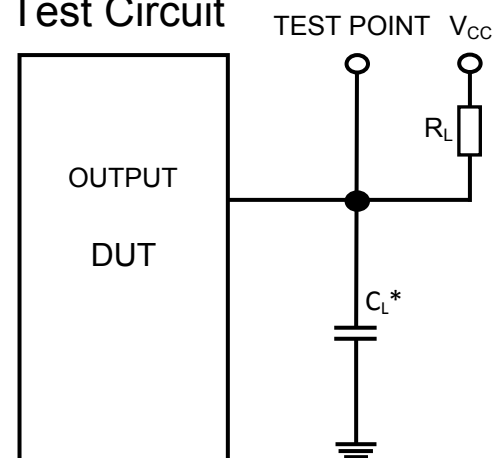
PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Turn-Off Delay, Input to Output	$t_{PLH}$	$T_A = 25^\circ\text{C}$ , $V_{CC} = 5\text{V}$ , $R_L = 110\Omega$ , $C_L = 15\text{pF}$ , Input $t_r = t_f = 10\text{ns}$	-	-	18	ns
Turn-On Delay, Input to Output	$t_{PHL}$		-	-	28	

2. Not production tested in die form, characterized by chip design

## Switching Waveform



## Test Circuit



\* Includes all probe and jig capacitance

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