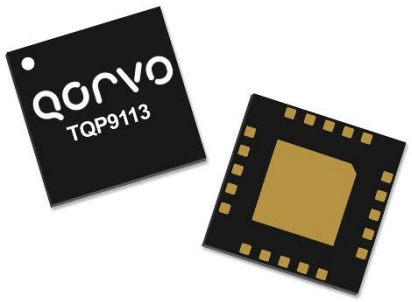
TQP9113

1 Watt Linear Amplifier

Applications

- Wireless Infrastructure
- FDD / TDD Base Stations
- Repeaters, Boosters, DAS
- High Power Amplifiers

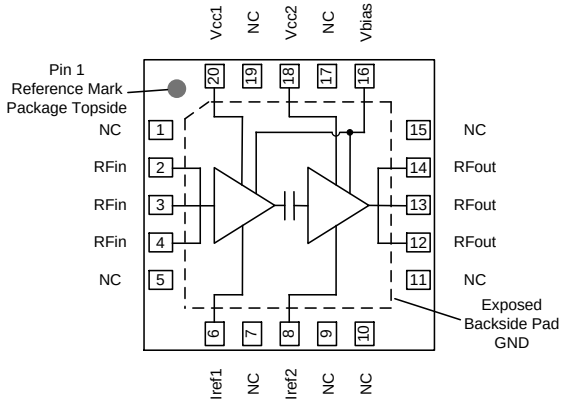


20-Pin 4 x 4 mm Leadless QFN Package

Product Features

- 1800 – 2700 MHz Frequency Range
- 27.6 dB Gain
- +41 dBm Output IP3
- +30.6 dBm P1dB
- +5 V supply, 215 mA Current
- Internal Input and Interstage Matching
- Bias Adjustable
- Power down functionality for TDD systems

Functional Block Diagram



Top View

General Description

The TQP9113 is a 1 W, linear, two-stage driver amplifier in a low-cost surface-mount package. The amplifier is able to achieve high performance with +41 dBm OIP3 and +30.6 dBm P1dB while only consuming 215 mA current. The input is internally matched and the amplifier only requires only a few external components for operation. The integrated interstage match minimizes performance variation that would otherwise be attributed to external matching component value and placement tolerances.

The TQP9113 is bias adjustable allowing the amplifier's power consumption to be reduced for occasions when linear performance is not required. The amplifier can also switched on and off for TDD applications. The output match is tunable externally to allow the amplifier to be optimized for high power or high linearity applications.

The TQP9113 is available in a RoHS-compliant 20-pin 4 x 4 mm surface mount package.

Pin Configuration

Pin No.	Label
1, 5, 7, 9, 10, 11, 15, 17, 19	NC
2, 3, 4	RF in
6	I_{REF1}
8	I_{REF2}
12, 13, 14	RF out
16	V_{BIAS}
18	V_{CC2}
20	V_{CC1}
Backside Pad	GND

Ordering Information

Part No.	Description
TQP9113	1800 – 2700 MHz Linear Amplifier
TQP9113-PCB2140	1800 – 2200 MHz Evaluation Board
TQP9113-PCB2600	2300 – 2700 MHz Evaluation Board
Standard T/R size = 2,500 pieces on a 13" reel	

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Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to 150 °C
Supply Voltage (V_{CC})	+6 V
RF Input Power, CW, 50 Ω, T=25 °C	+15 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC} = +5.0 V, Temp = +25 °C, in a matched 2140 MHz reference circuit.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1800		2700	MHz
Test Frequency			2140		MHz
Gain			27.6		dB
Input Return Loss			14		dB
Output Return Loss			14		dB
Noise Figure			4.7		dB
Output P1dB			+30.6		dBm
Output IP3	Pout = +16 dBm / tone, Δf = 1 MHz		+41		dBm
WCDMA Channel Power(1)	−50 dBc ACLR		+18.4		dBm
Current, I_{CC}			212		mA
Current, I_{REF1}			1.2		mA
Current, I_{REF2}			2.2		mA
Total Current			215		mA
Thermal Resistance, θ_{jc}	Junction to case		41.7		°C/W

Notes:
1. ACLR test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

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S-Parameters

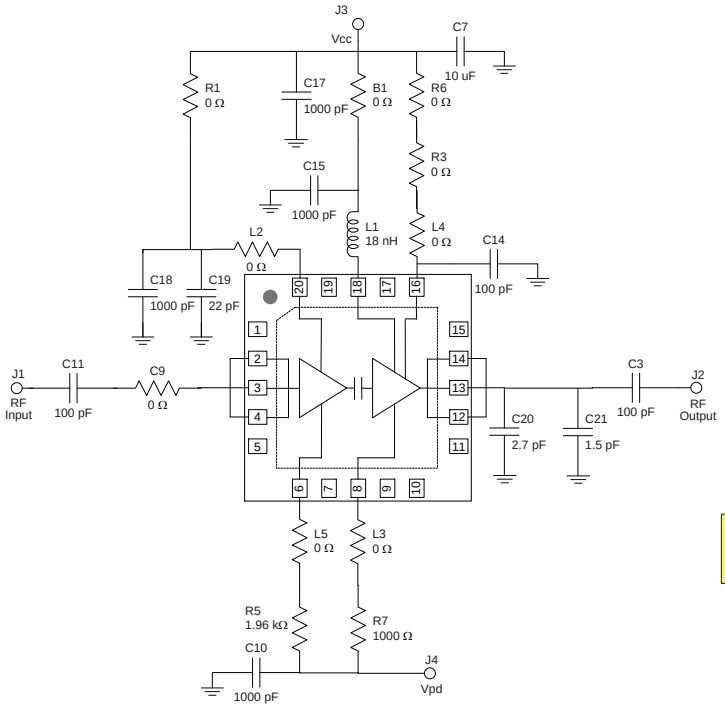
Test Conditions: V_{CC} = V_{PD} = +5 V, I_{CQ} = 215 mA, Temp. = +25 °C, unmatched 50 Ω system, calibrated to device leads

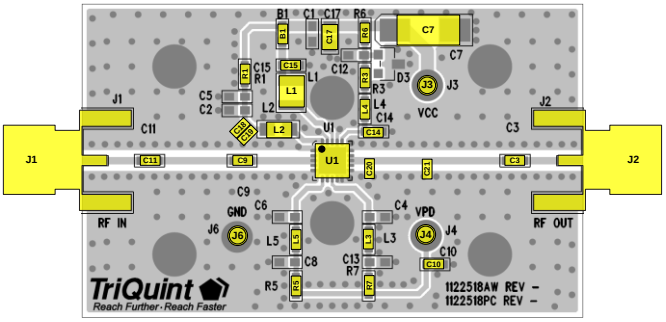
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.1	-0.7	175	-59.9	-133	-64.4	-170	-2.6	-173
0.2	-0.7	171	-34.4	-150	-68.6	78	-2.1	-177
0.3	-0.8	166	-24.8	-147	-57.9	122	-1.9	-180
0.4	-0.8	160	-17.9	-151	-73.6	-80	-2.0	179
0.5	-1.0	156	-12.1	-159	-56.4	-49	-2.2	178
0.6	-1.0	149	-7.1	-164	-63.4	-43	-2.3	177
0.7	-1.1	143	-2.3	-173	-52.0	167	-2.5	175
0.8	-1.2	135	2.1	177	-50.7	62	-2.7	175
0.9	-1.3	126	6.3	165	-52.4	54	-3.2	173
1	-1.6	117	10.4	149	-61.0	53	-3.7	172
1.1	-2.0	104	14.3	127	-63.1	160	-4.3	172
1.2	-2.8	94	15.8	99	-60.3	97	-4.7	171
1.3	-3.2	79	18.6	95	-60.8	-144	-5.7	171
1.4	-4.9	60	22.4	69	-65.7	108	-6.3	178
1.5	-7.9	49	24.4	39	-55.5	137	-6.2	-177
1.6	-10.7	50	25.3	10	-50.3	124	-5.8	-175
1.7	-11.6	55	25.6	-15	-48.6	94	-5.3	-175
1.8	-11.7	50	25.8	-37	-51.8	86	-5.1	-175
1.9	-11.7	39	25.9	-57	-48.6	59	-5.2	-174
2	-12.1	22	26.0	-77	-48.6	54	-4.9	-174
2.1	-12.6	0	26.0	-97	-50.7	64	-4.8	-173
2.2	-13.1	-27	25.9	-118	-52.6	29	-4.5	-171
2.3	-13.0	-54	25.6	-138	-51.6	29	-3.8	-170
2.4	-12.4	-79	25.1	-158	-51.3	-12	-3.3	-170
2.5	-11.7	-95	24.3	-178	-56.0	-31	-2.7	-171
2.6	-11.2	-106	23.3	163	-60.6	7	-2.2	-171
2.7	-10.5	-113	22.1	144	-58.0	-113	-1.7	-174
2.8	-9.9	-115	20.7	126	-63.8	89	-1.5	-175
2.9	-9.1	-116	19.0	110	-53.0	138	-1.3	-176
3	-8.2	-117	17.2	94	-55.3	112	-1.3	-177
3.2	-6.8	-120	12.8	65	-50.9	88	-1.1	-178
3.4	-5.9	-116	3.6	54	-58.9	-133	-1.0	-179
3.6	-3.5	-117	7.8	82	-57.0	178	-1.6	179
3.8	-3.2	-123	6.7	51	-46.7	134	-2.3	-177
4	-3.3	-125	4.4	32	-49.3	154	-2.7	-176

Notes:
1. Pins 6, 8, 16, 18, 20 are loaded as shown in the PCB2140 design.

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1.8 – 2.2 GHz Evaluation Board (TQP9113−PCB2140)





Notes:

2. See Evaluation Board PCB Information section for PCB material and stack-up
3. Components (C11 and C3) are blocking capacitors and their locations are not critical to the matching network.
4. All components are of 0603 size unless otherwise specified.
5. Critical component placement locations:
   Distance from U1 Package (right edge) to C20 (left edge): 25 mils
   Distance from U1 Package (right edge) to C21 (left edge): 310 mils

Bill of Material TQP9113-PCB2140

Ref Des	Value	Description	Manuf.	Part Number
U1		TQP9113	TriQuint	TQP9113
C10, C15, C18	1000 pF	CAP, 0603, 5%, 50V, NPO	various	
C3, C11, C14	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C19	22 pF	CAP, 0603, 5PCT, 50V, NPO/COG	various	
C20	2.7 pF	CAP, 0603, +/-0.1PF, 50V, NPO/COG	various	
C21	1.5 pF	CAP, 0603, 5PCT, 50V, NPO/COG	various	
C7	10 uF	CAP, 6032, 20%, 50V, Tantalum	various	
R5	1.96 kΩ	RES, 0603, 1PCT, 1/16W	various	
R7	1000 Ω	RES, 0603, 1PCT, 1/16W	various	
B1, R1, R3, R6, L3, L4, L5, C9	0 Ω	RES, 0603, 1/16W, Chip	various	
L2	0 Ω	RES, 0805, 1/10W, Chip	various	
L1	18 nH	IND, 1008, 5%, Ceramic	various	
C17	1000pF	CAP, 0805, 5PCT, 50V, NPO	various	

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Typical Performance TQP9113– PCB2140

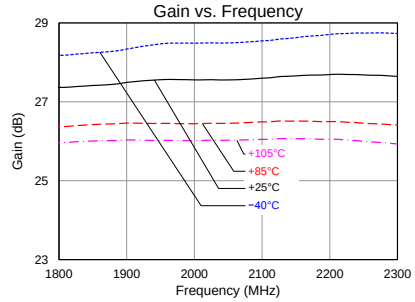
Test conditions unless otherwise noted: V_{CC} = +5 V, Vpd = +5 V, I_{CQ} = 215 mA (typ.), Temp. = +25 °C

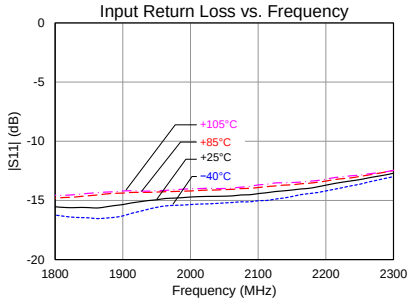
Parameter	Conditions	Typical Value			Units
Frequency		1840	1960	2140	MHz
Gain		27.4	27.6	27.6	dB
Input Return Loss		16	15	14	dB
Output Return Loss		12	13	14	dB
Output P1dB		+30.5	+30.6	+30.6	dBm
OIP3	Pout= +16 dBm/tone, Δf=1 MHz	+37	+39	+41	dBm
Noise Figure		5.2	4.9	4.7	dB
WCDMA Channel Power(1)	−50 dBc ACLR	+17.9	+19.3	+18.4	dBm

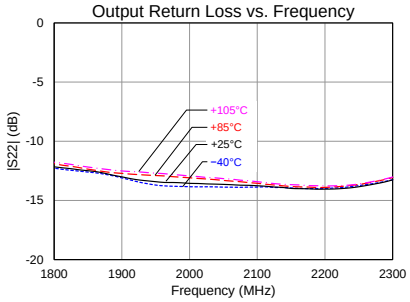
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

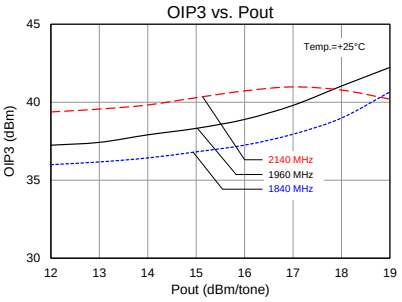
Typical Performance TQP9113-PCB2140

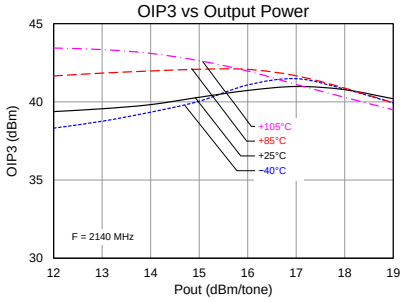
Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ} = 215 mA (typ.), Temp. = +25 °C

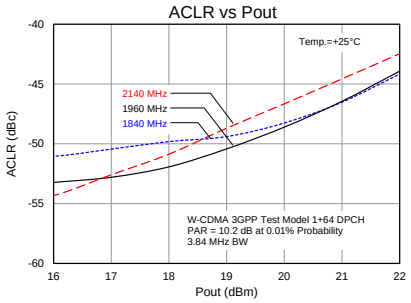


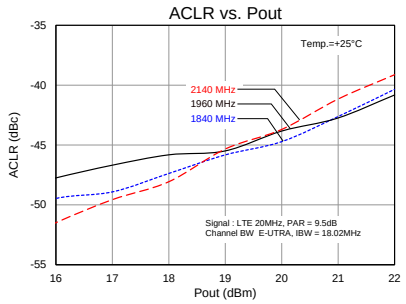


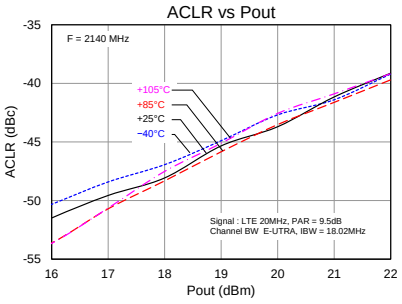






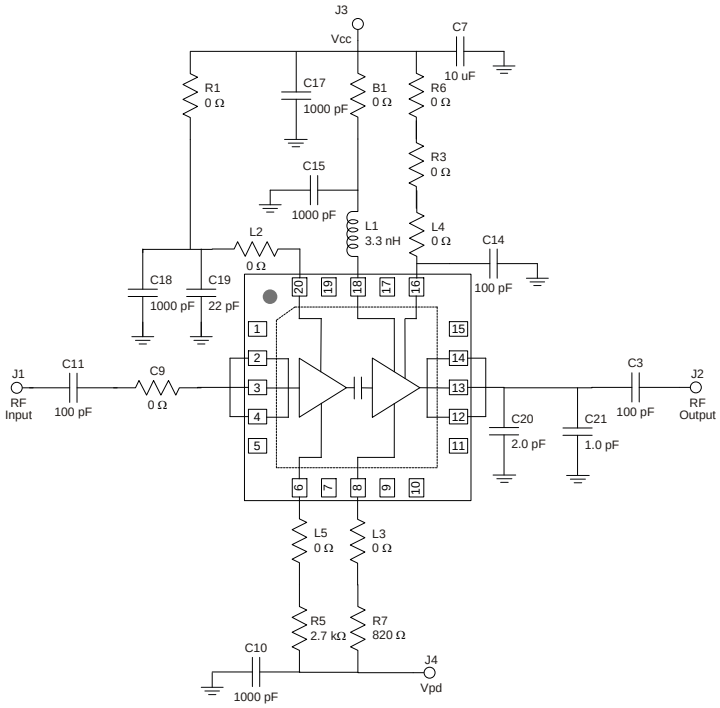


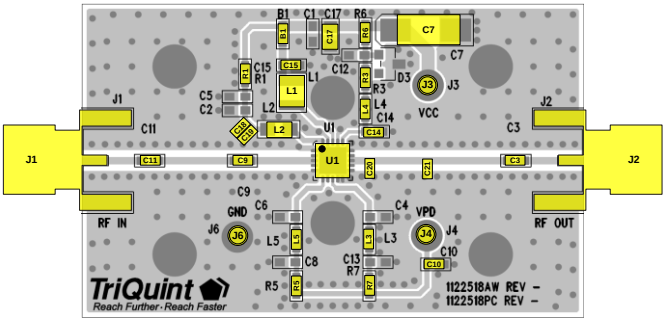




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2.3 – 2.7 GHz Evaluation Board (TQP9113–PCB2600)





Notes:

1. See Evaluation Board PCB Information section for PCB material and stack-up
2. Components (C11 and C3) are blocking capacitors and their locations are not critical to the matching network.
3. All components are of 0603 size unless otherwise specified.
4. Critical component placement locations:
   Distance from U1 Package (right edge) to C20 (left edge): 25 mils
   Distance from U1 Package (right edge) to C21 (left edge): 285 mils

Bill of Material TQP9113-PCB2600

Ref Des	Value	Description	Manuf.	Part Number
U1		TQP9113	TriQuint	TQP9113
C10, C15, C18	1000 pF	CAP, 0603, 5%, 50V, NPO	various	
C3, C11, C14	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C19	22 pF	CAP, 0603, 5PCT, 50V, NPO/COG	various	
C20	2.0 pF	CAP, 0603, +/-0.1PF, 50V, NPO/COG	various	
C21	1.0 pF	CAP, 0603, 5PCT, 50V, NPO/COG	various	
C7	10 uF	CAP, 6032, 20%, 50V, Tantalum	various	
R5	2.7 kΩ	RES, 0603, 1PCT, 1/16W	various	
R7	820 Ω	RES, 0603, 1PCT, 1/16W	various	
B1, R1, R3, R6, L3, L4, L5, C9	0 Ω	RES, 0603, 1/16W, Chip	various	
L2	0 Ω	RES, 0805, 1/10W, Chip	various	
L1	3.3 nH	IND, 1008, 5%, Ceramic	various	
C17	1000pF	CAP, 0805, 5PCT, 50V, NPO	various	

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Typical Performance TQP9113– PCB2600

Test conditions unless otherwise noted: V_{CC} = +5 V, Vpd = +5 V, I_{CQ} = 250 mA (typ.), Temp. = +25 °C

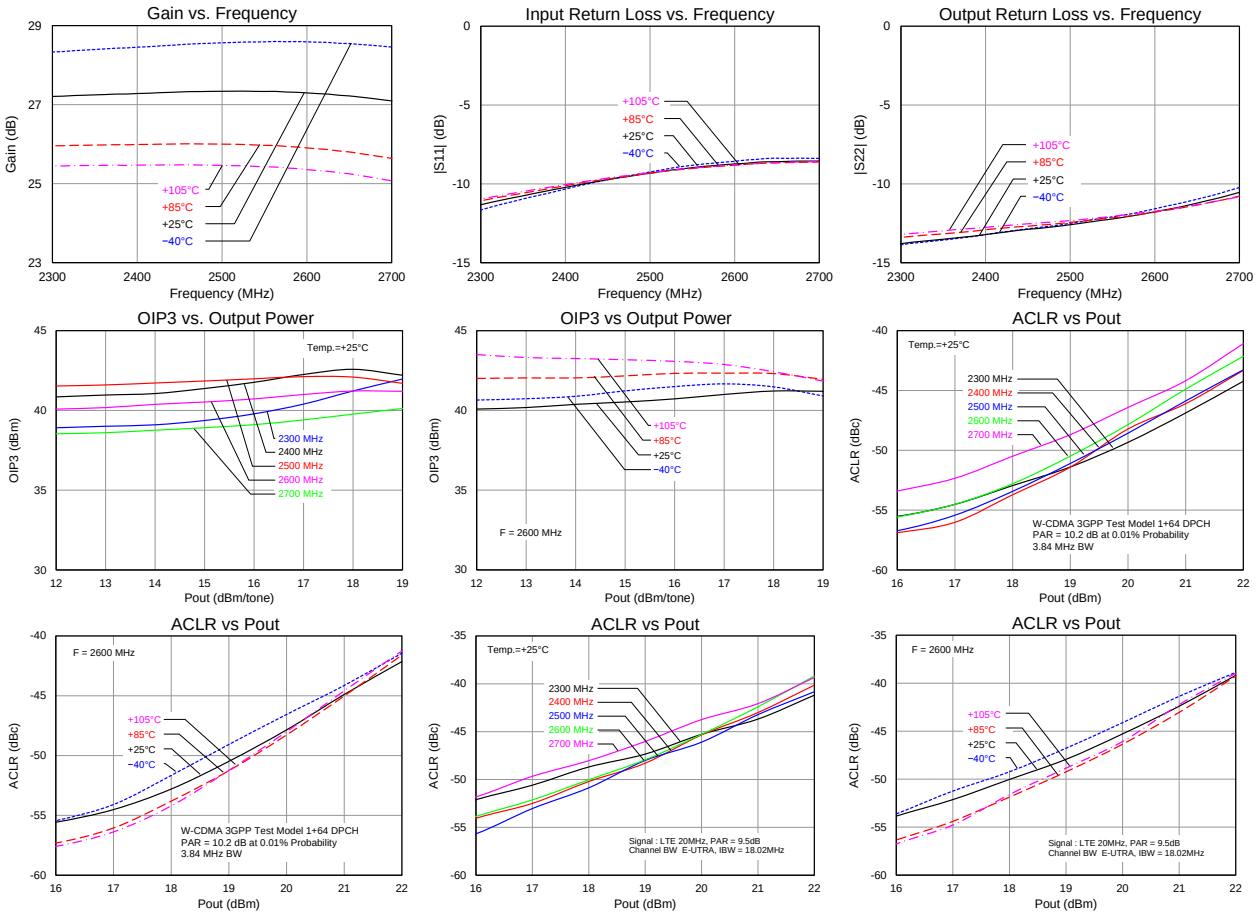
Parameter	Conditions	Typical Value			Units
Frequency		2300	2500	2700	MHz
Gain		27.2	27.3	27.1	dB
Input Return Loss		11	9.3	8.6	dB
Output Return Loss		14	12	11	dB
Output P1dB		+30.8	+30.3	+29.8	dBm
OIP3	Pout= +16 dBm/tone, Δf=1 MHz	+39.8	+42.0	+39.1	dBm
Noise Figure		4.7	4.9	5.0	
WCDMA Channel Power(1)	−50 dBc ACLR	+19.7	+19.4	+18.3	dBm

Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

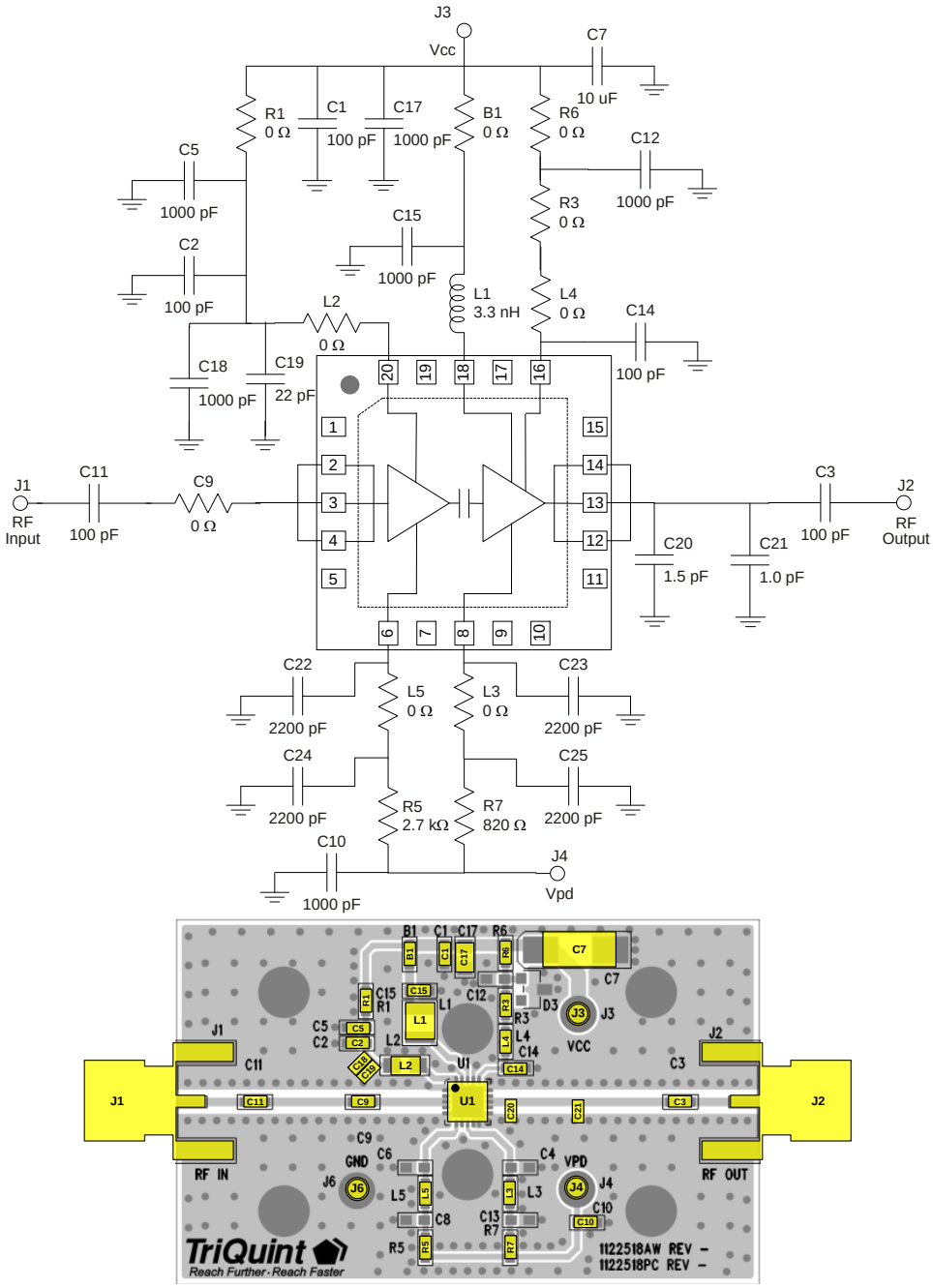
Typical Performance TQP9113-PCB2600

Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ} = 250 mA (typ.), Temp. = +25 °C



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Application Circuit for Improved Intermodulation Balance



Notes:

1. See Evaluation Board PCB Information section for PCB material and stack-up
2. Components (C11 and C3) are blocking capacitors and their locations are not critical to the matching network.
3. All components are of 0603 size unless otherwise specified.
4. Critical component placement locations:
   Distance from U1 Package (right edge) to C20 (left edge): 25 mils
   Distance from U1 Package (right edge) to C21 (left edge): 285 mils

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Typical Performance TQP9113 Improved IM Balance

Test conditions unless otherwise noted: V_{CC} = +5 V, Vpd = +5 V, I_{CQ} = 250 mA (typ.), Temp. = +25 °C

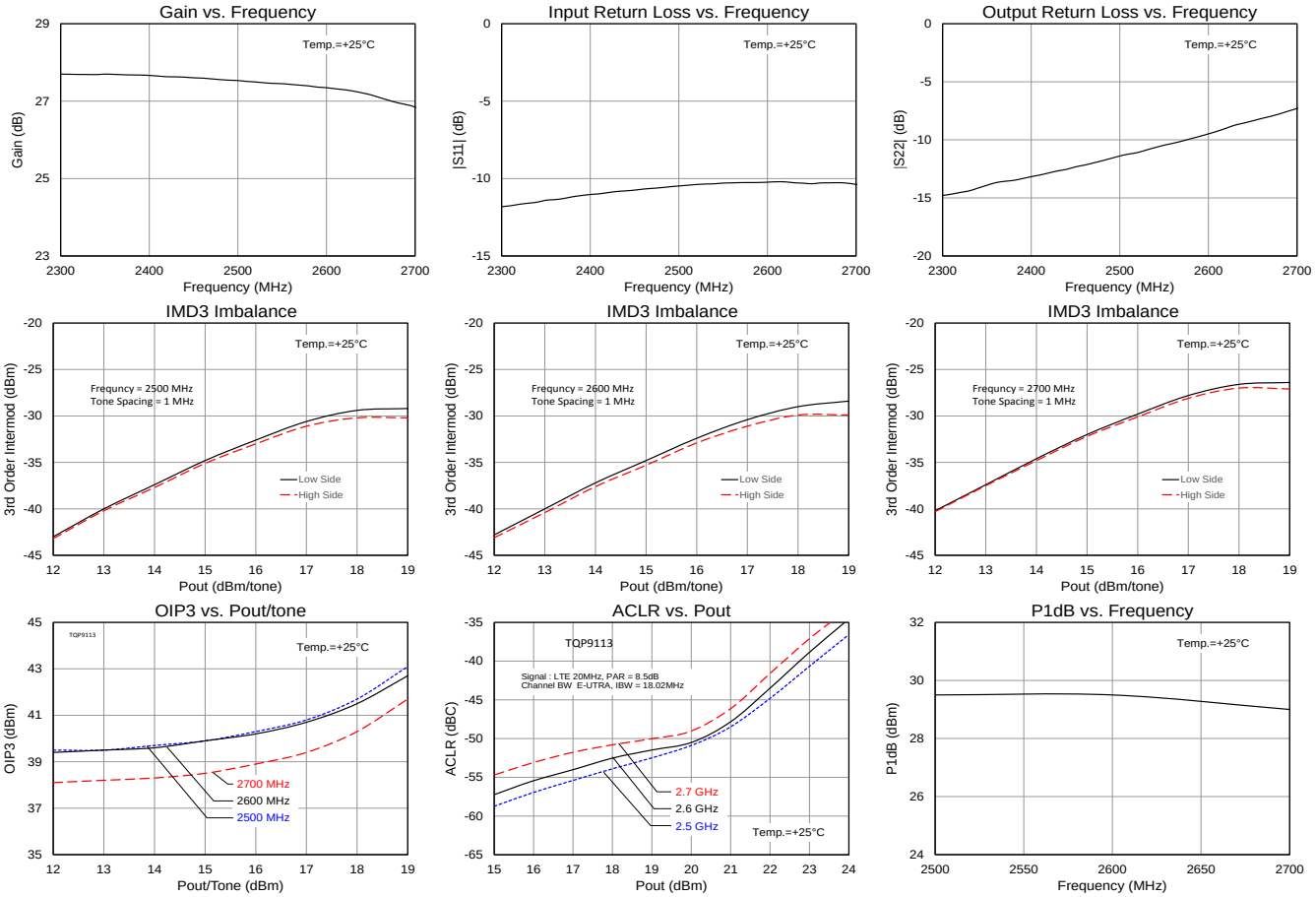
Parameter	Conditions	Typical Value			Units
Frequency		2500	2600	2700	MHz
Gain		27.7	27.4	26.9	dB
Input Return Loss		11	11	10	dB
Output Return Loss		15	12	7	dB
Output P1dB		+29.5	+29.5	+29.0	dBm
OIP3	Pout= +19 dBm/tone, Δf=1 MHz	+43.0	+42.7	+41.7	dBm
Noise Figure		4.7	4.8	4.8	dB
WCDMA Channel Power(1)	−50 dBc ACLR	+20.5	+20.4	+19.0	dBm

Notes:

1. ACLR Test set-up: 20 MHz LTE, 1-CH, +20 MHz offset, PAR = 8.5 dB at 0.01% Probability

Typical Performance TQP9113 Improved IM Balance

Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ} = 250 mA (typ.), Temp. = +25 °C



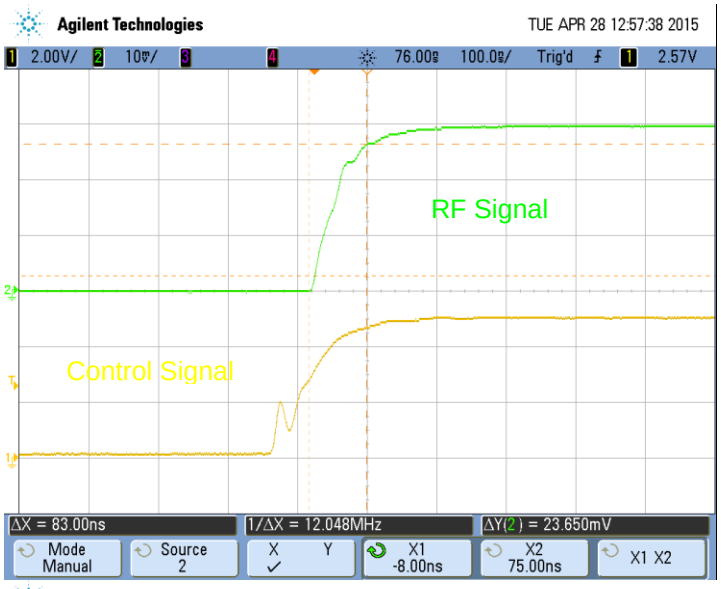
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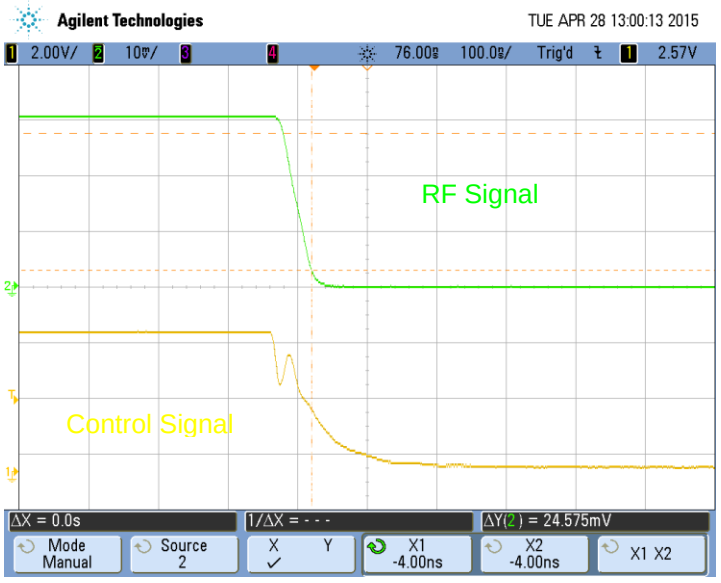
Switching Speed

Switching Speed Measurement based on TQS Application Board

Using Shutdown Circuit: V_{PD}=3V, V_{DD}=5V

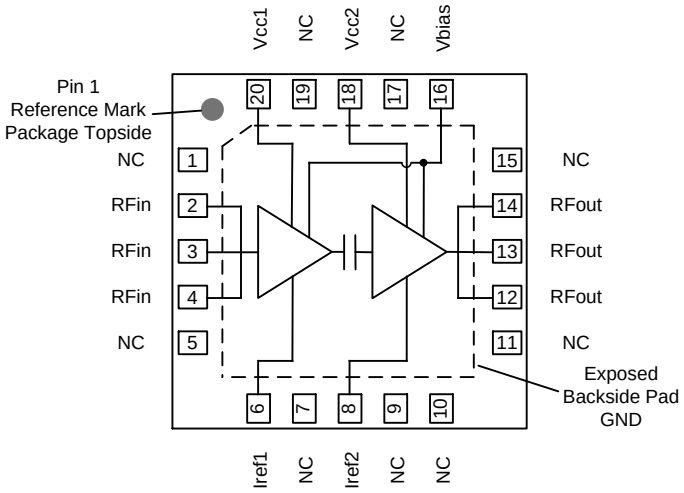
Parameter	+25C
Turn-off Transition (50% CNTR – 10% RF)	140 ns
Turn-on Transition (50% CNTR – 90% RF)	50 ns





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Pin Configuration and Description

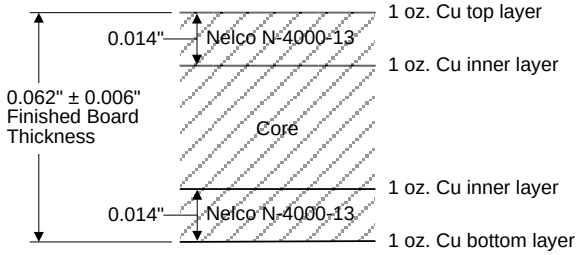


Top View

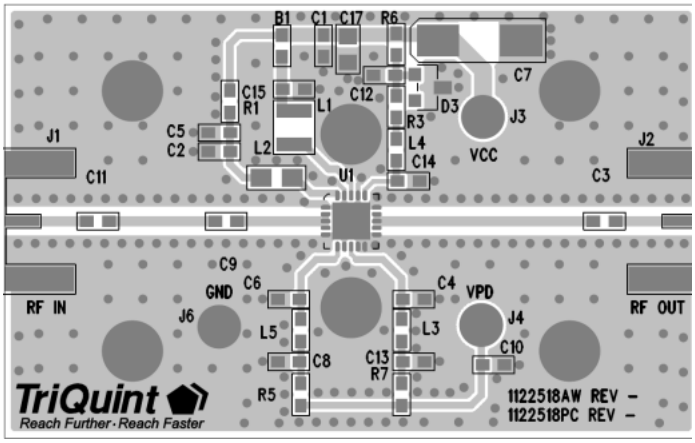
Pin No.	Label	Description
1, 5, 7, 9, 10, 11, 15, 17, 19	NC	No internal connection. Provide grounded land pads for PCB mounting integrity.
2, 3, 4	RF in	RF input pins. Requires only DC blocking cap for operation.
6	I_{REF1}	Sets the bias current for Amp1. Also can be used to power down Amp 1.
8	I_{REF2}	Sets the bias current for Amp2. Also can be used to power down Amp 2.
12, 13, 14	RF out	RF output pins. Require DC blocking and RF match for optimal performance.
16	V_{BIAS}	Bias circuit supply voltage.
18	V_{CC2}	2nd Stage DC voltage supply connection.
20	V_{CC1}	1st Stage DC voltage supply connection.
Backside Pad	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

TriQuint PCB 1100415 Material and Stack-up



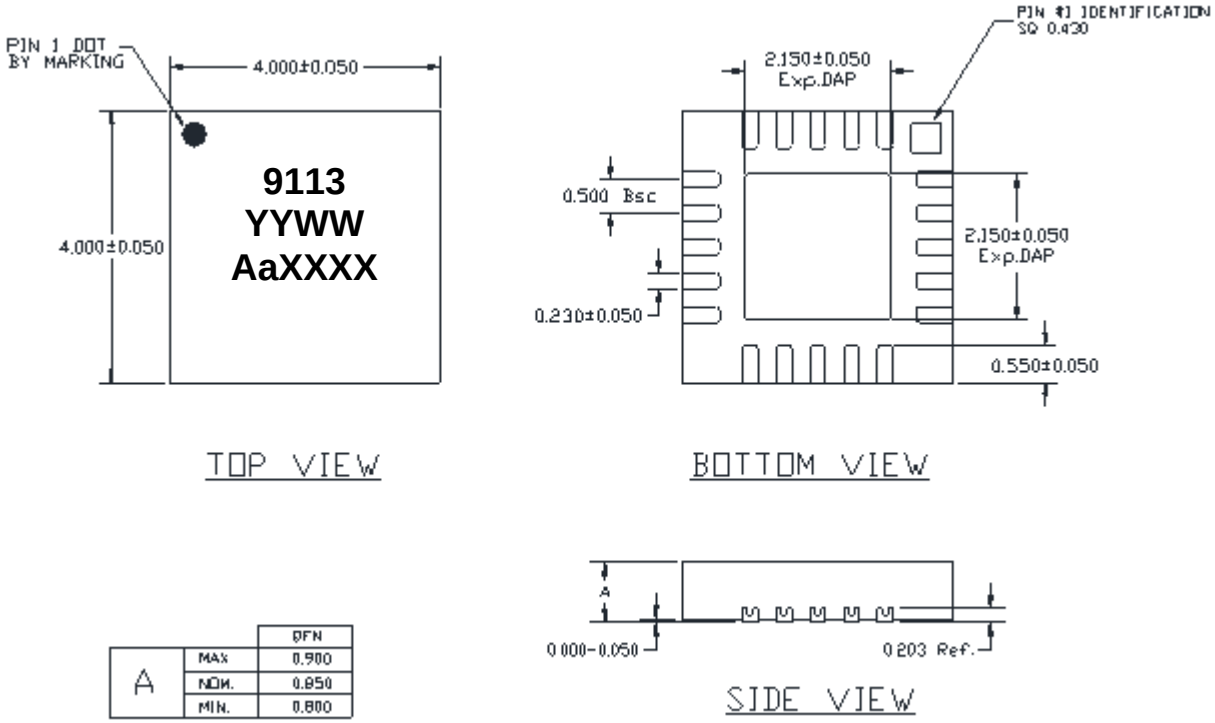
50 ohm line dimensions: width = .028”
spacing = .028”.



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Package Marking and Dimensions

Marking: Part number – 9113
Date - YYWW
Country Code - CCCC
Lot code – AaXXXX



		QFN
A	MAX	0.900
	NOM.	0.850
	MIN.	0.800

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

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Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Class: Class 1C
Volt. Range: ≥ 1000 V to < 2000 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Class: Class C3
Volt. Range: > 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.triquint.com **Tel: 1-844-890-8163**
Email: customer.support@qorvo.com

For information about the merger of RFMD and TriQuint as Qorvo:

Web: www.qorvo.com

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