WM8816

Stereo Digital Volume Control

DESCRIPTION

The WM8816 is a highly linear stereo volume control for audio systems. The design is based on resistor chains with external op-amps, which provides flexibility for the supply voltage, signal swing, noise floor and cost optimisation. The gain of each channel can be independently programmed from -111.5dB to +15.5dB through a digital serial control interface.

Audible clicks on gain changes are eliminated by changing gains only when a zero crossing has been detected in the signal. The device also features peak level detection, which can be used for Automatic Gain Control. The WM8816 operates from a single +5V supply and accepts signal input levels up to ±18V.

The WM8816 is available in a 16-pin SOIC package. It is guaranteed over a temperature range of -20° to +60°C.

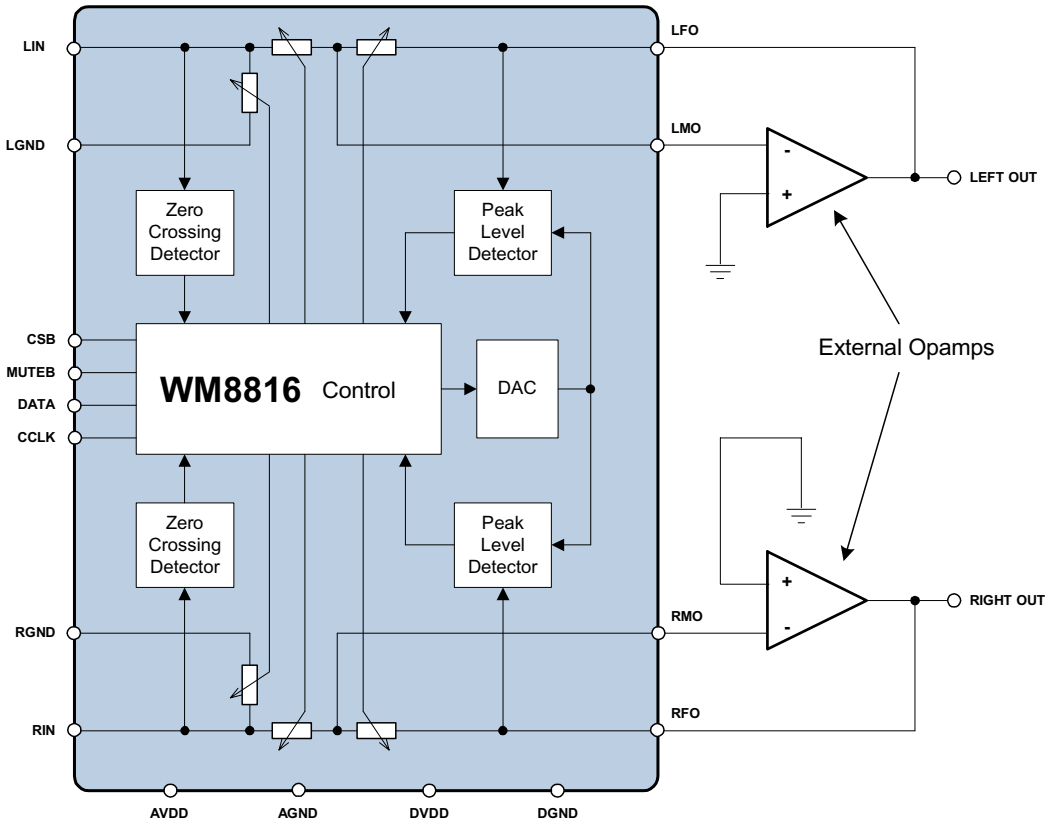
FEATURES

- Gain range from -111.5dB to +15.5dB
- 0.5dB Gain step size
- Total Harmonic Distortion 0.001% (100dB) typical
- Crosstalk -110dB typical
- Input signals up to ±18V
- Zero Detection for Gain Changes
- Hardware and Software Mute
- Power On/Off Transient Suppression

APPLICATIONS

- Audio Amplifiers
- Consumer Audio / Entertainment Systems
- Mixing Desks
- Audio Recording Equipment

BLOCK DIAGRAM



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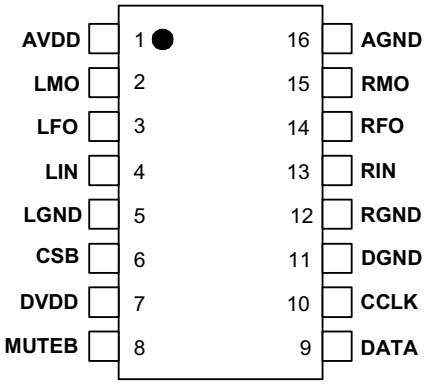
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
XWM8816EDW/V	-20 to +60°C	16-pin SOIC (plastic) Wide	MSL3	240°C
XWM8816GEDW/V	-20 to +60°C	16-pin SOIC Wide (Lead Free)	MSL3	260°C

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AVDD	Supply	Supply Voltage for Analogue Circuitry
2	LMO	Analogue Output	External Op-amp Inverting Input (Left Channel)
3	LFO	Analogue Input	External Op-amp Feedback Signal (Left Channel)
4	LIN	Analogue Input	Input Signal (Left Channel)
5	LGND	Analogue Input	Input Signal Ground (Left Channel)
6	CSB	Digital Input	Chip Select (active low)
7	DVDD	Supply	Supply Voltage for Digital Circuitry
8	MUTEB	Digital Input	Mute (active low)
9	DATA	Digital In / Out	Serial Interface Data Input / Output (tri-state)
10	CCLK	Digital Input	Serial Interface Clock
11	DGND	Supply	Digital Ground
12	RGND	Analogue Input	Input Signal Ground (Right Channel)
13	RIN	Analogue Input	Input Signal (Right Channel)
14	RFO	Analogue Input	External Op-amp Feedback Signal (Right Channel)
15	RMO	Analogue Output	External Op-amp Inverting Input (Right Channel)
16	AGND	Supply	Analogue Ground

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore susceptible to damage from excessive static voltages. To optimise the distortion and noise performance of pins 3, 4, 13 and 14, the on-chip ESD protection circuitry has been restricted, and consequently only achieves 300V when characterised to the Human Body Model. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Input signal voltage	-20V	+20V
Positive supply voltage (AVDD to AGND, DVDD to DGND)	-0.5V	6V
Input voltage (all other pins)	-0.5V	AVDD + 0.5V
Operating temperature	-40°C	85°C
Storage temperature	-55°C	125°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input signal voltage			-18		+18	V
Positive supply voltage	AVDD, DVDD		4.5	5	5.5	V
Negative supply voltage	AGND, DGND			0		V
Input signal grounds	LGND, RGND			0		V
Operating temperature			-20	60	60	°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS

AVDD=5.0V, AGND = 0V, T_A = 25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs / Outputs						
Input resistance	R_{IN}	For any gain	7	10		kΩ
Input capacitance	C_{IN}	For any gain		2		pF
Input offset voltage (note 1)	V_{offset}	Op-amp gain = -15.5		0.8		mV
		Op-amp gain = 1		3		mV
		Op-amp gain = 15.5		12		mV
Supply current	I_{DD}	From AVDD / AGND		2.5	5	mA
Power supply rejection ratio (Note 2)	PSRR	From AVDD		80		dB
Gain Control						
Gain range	G		-111.5		+15.5	dB
Gain step size	D			0.5		dB
Gain error (Note 2)	DE	Lowest gains guaranteed by design, not tested in production.			0.5	dB
Gain match error (Note 2)	ME	Between channels			0.2	dB
Mute attenuation	MATT		113			dB
Audio Performance						
Noise (Note 2) V_{IN} = 0V, V_{OUT} with OP275, A-weighted	N	Gain = 0dB			13	μVrms
		Gain = -60dB		4		
		Gain = mute		2.5		
Total Harmonic Distortion plus Noise	THD+N	V_{IN}= 1Vrms, gain=0dB, V_{OUT} with OP275, DC to 20 kHz		0.001 (100)		% (dB)
Dynamic Range (Note 2)	DNR		120	130		dB
Crosstalk (Note 2)	CR	Between channels, gain=0dB, f_{IN}=1kHz	-100	-110		dB
Digital Inputs / Outputs						
Input low voltage	V_{IL}	All digital inputs			0.3 DVDD	V
Input high voltage	V_{IH}	All digital inputs	0.7 DVDD			V
Output low voltage	V_{OL}	I_{Load} = 2mA			0.4	V
Output high voltage	V_{OH}	I_{Load} = 2mA	DVDD -0.4			V
Control Interface Timing						
Clock Frequency	f_{CCLK}				1	MHz
Period of CCLK high	t_{WHC}	V_{IH} to V_{IH}	500			ns
Period of CCLK low	t_{WLC}	V_{IL} to V_{IL}	500			ns
Rise time of CCLK	t_{RC}	V_{IL} to V_{IH}			100	ns
Fall time of CCLK	t_{FC}	V_{IH} to V_{IL}			100	ns
Hold time, CCLK high to CSB low	t_{HCSH}		20			ns
Setup time, CSB low to CCLK high	t_{SSLCH}		100			ns
Setup time, valid DATA to CCLK high	t_{SDCH}		100			ns
Hold time, CCLK high to invalid DATA	t_{HCHD}		100			ns
Setup time, CCLK low to valid DATA	t_{DCLD}	Load = 100pF			200	ns
Hold time, CSB high or 16th CCLK low to invalid DATA	t_{DSZ}	Load = 3.3kΩ	20		200	ns

TEST CONDITIONS

AVDD=5.0V, AGND = 0V, T_A = 25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hold time, 16th CCLK high to CSB high	t_{HLCHS}		200			ns
Setup time, CSB high to CCLK high	t_{SSHCH}		200			ns

Note:

1. External MC33078 op-amp. Will vary depending on op-amp input bias current and input offset voltage.
2. Guaranteed by design.

CONTROL INTERFACE TIMING DIAGRAM

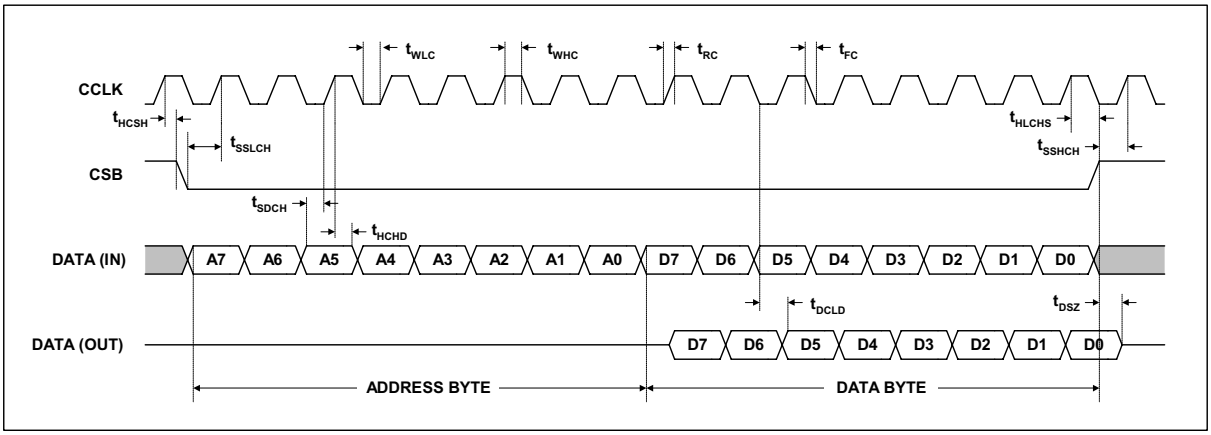


Figure 1 Control Interface Timing Diagram

DEVICE DESCRIPTION

The WM8816 is a stereo digital volume control designed for audio systems. The levels of the left and right analogue channels can be programmed independently through the serial interface. The resistor values in the internal resistor chains are decoded to 0.5 dB resolution with multiplexers, giving a gain range of -111.5 to +15.5 dB. The code for -112 dB activates mute for maximum attenuation.

The WM8816 has two constant impedance signal inputs. The left channel input is between LIN and LGND, and the right channel between RIN and RGND. The output pins LFO, LMO (left) and RFO, RMO (right) are designed to interface directly to two external op-amps, which produce the volume controlled output signals. This provides flexibility for the supply voltage and signal swing; while the WM8816 runs at 5V, the output signal swing depends solely on the op-amp supply.

INTERFACES

Control information is written into or read back from the internal register via the serial control port. This port consists of a bi-directional data pin (DATA), an active low chip select pin (CSB) and the control clock (CCLK). Control data is shifted into the serial input register on the rising edges of CCLK pulses, while CSB is low. All control instructions require two bytes of data. The first byte contains a 4-bit register address and a read/write bit, and the second byte is the control word. CSB must return to high at the end of each word. When reading from the control registers, data is shifted out on the falling edges of CCLK.

When CSB is high, the DATA pin is in a high impedance state. In a multi-channel system, the same DATA and CCLK lines can thus be connected to several WM8816 volume controllers, and each device can be independently addressed by pulling its CSB pin low.

OPERATING MODES

When power is first applied, a power-on reset initialises the control registers and mutes the WM8816. To activate the device, the MUTEB pin must be high and a non-zero value must be written to the gain register. After that the device can be muted again either by pulling the MUTEB pin low or by writing zero (00hex) to the gain register.

CHANGING THE GAIN OF THE CHANNEL

The WM8816 has two gain registers for the left and right channels respectively. There is also an alias register address to update both gain registers simultaneously. When a new gain value is written into a gain register the WM8816 will wait until the next falling edge zero crossing in the input signal before changing the gain. This ensures that no audible click is produced at the output. If there are no zero crossings in the signal after 23ms internal delay generators change the gain regardless, right channel followed by the left channel. If both gain registers are changed simultaneously, the gain is changed first on the right and then the left channel.

Note: The block diagrams in this datasheet only show a representation of the feedback resistor paths and should be thought of as the exact internal device structure. As the internal structure is different, it is not possible to correlate the measured impedance between input and output, and the actual gain attenuation.

PEAK LEVEL DETECTION

The WM8816 has an on-chip 8-bit digital-to-analogue converter (DAC) used for monitoring the peak level of the output signal. The DAC input value is programmed via the serial interface. The reference value V_{REF} is calculated from $V_{REF} = k/256 \times 18V$, where k is the DAC input code. When a positive peak signal level exceeds this value, the peak detector sets Bit 1 (for the left channel) or Bit 0 (right channel) of the status register. These bits remain set until the status register is read.

REGISTER MAP

REGISTER	ADDRESS BYTE BITS								DATA BYTE	
	7	6	5	4	3	2	1	0	MSB…LSB	Function
Peak Detector Status R4	X	1	0	1	1	R/W	X	X	Output code 00000000 00000001 00000010 00000011	 No overload Right overload Left overload Both overload
Peak Detector Reference R3	X	1	1	0	0	R/W	X	X	Input code 11111111 11111110 11111101 : 00000010 00000001 00000000	DAC output 255/256 × 18V 254/256 × 18V 253/256 × 18V : 2/256 × 18V 1/256 × 18V AGND
Left Channel Gain R2	X	1	1	0	1	R/W	X	X	Input code 11111111 11111110 11111101 : 11100000 00000010 00000001 00000000	Gain dB +15.5 +15.0 +14.5 : 0.0 -111.0 -111.5 mute
Right Channel Gain R1	X	1	1	1	0	R/W	X	X	Input code 11111111 11111110 11111101 : 11100000 00000010 00000001 00000000	Gain dB +15.5 +15.0 +14.5 : 0.0 -111.0 -111.5 mute
Both Channel Gains R5	X	1	0	0	1	W	X	X	Write to both gain registers	

Table 1 Register Map Description

Notes:

1. Address bit 2 is the read / write bit (1 for read, 0 for write).
2. X represents 'do not care' entries. Set to 1 for minimum power consumption.
3. All registers are set to their default value (all zeros) during power-on reset, except R3 which is set to 255.

PERFORMANCE GRAPHS

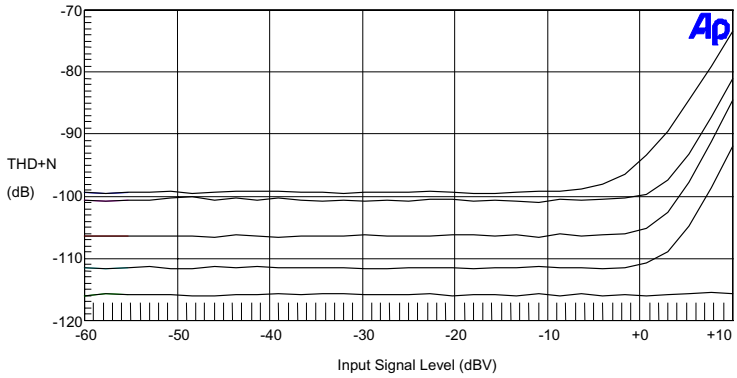


Figure 2 THD + Noise versus input level at gains of +6dB, 0dB, -6dB, -12dB and mute

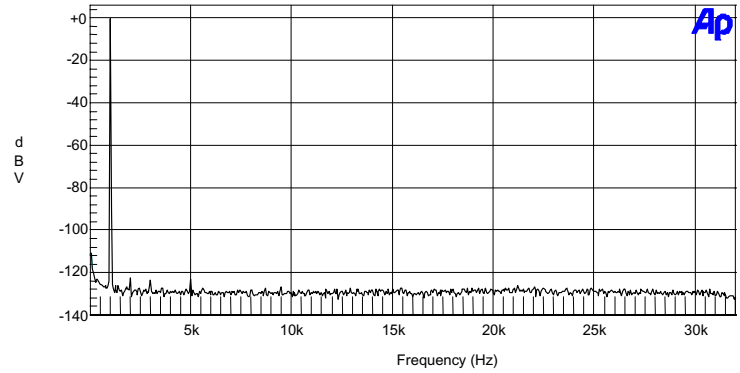


Figure 3 FFT of output signal with 1kHz, 1Vrms sine wave input

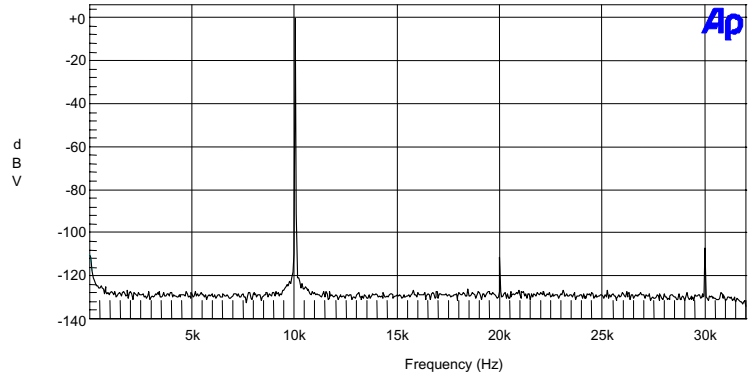
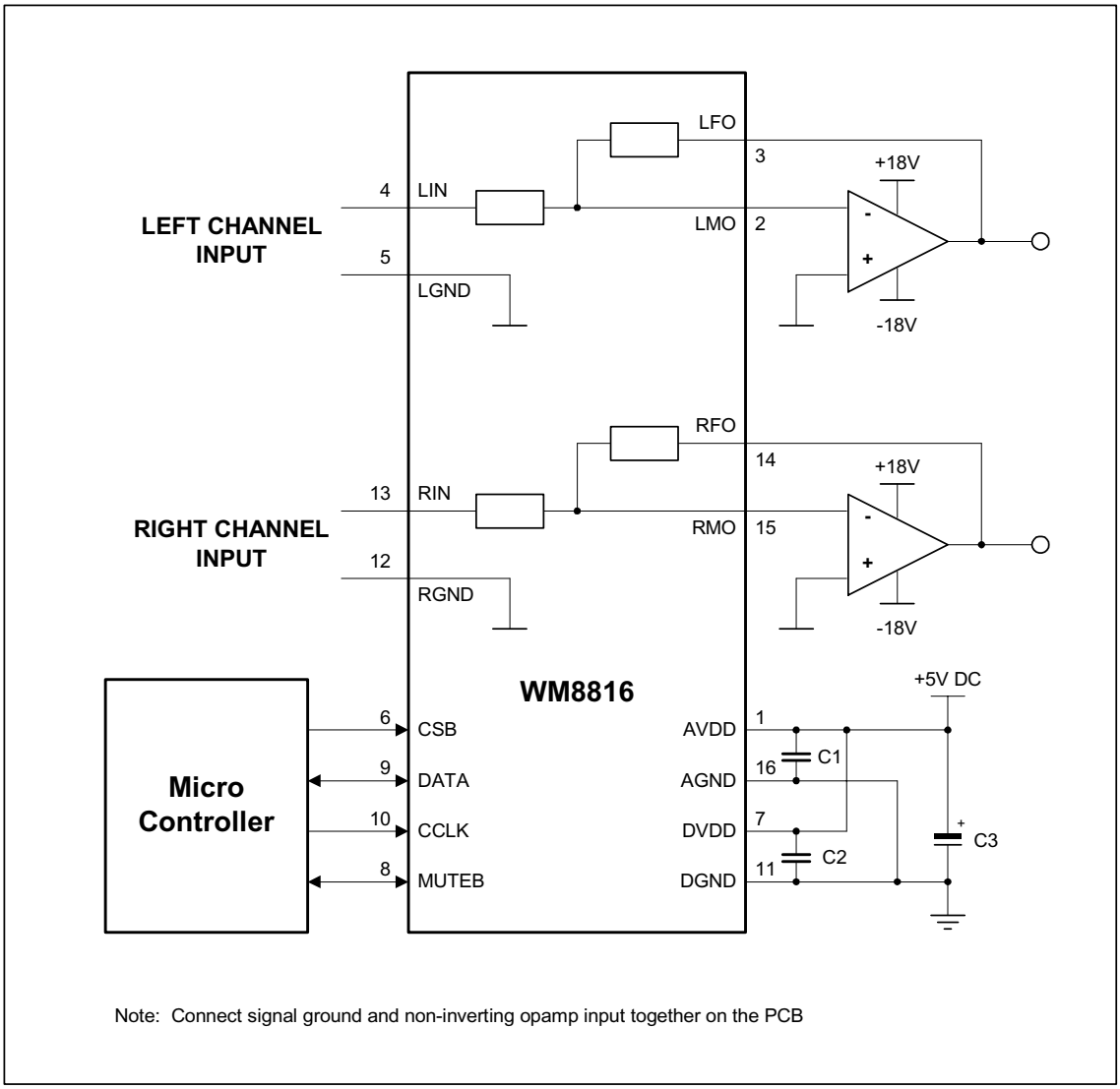


Figure 4 FFT of output signal with 10kHz, 1Vrms sine wave input

RECOMMENDED EXTERNAL COMPONENTS



Note: Connect signal ground and non-inverting opamp input together on the PCB

Figure 5 Typical Application.

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	220nF	Analogue Supply Decoupling
C2	220nF	Digital Supply Decoupling
C3	10µF	General Supply Decoupling

Table 2 Recommended External Components Values

APPLICATION RECOMMENDATIONS

1. For best audio performance, all digital activities should be minimised during analogue signal processing. Special attention should be paid to power and ground decoupling. Decoupling capacitors should be located as close to the WM8816 as possible. A clean analogue power supply should always be used.

2. Damage can be caused to the internal delay generators if AVDD and DVDD supply voltages differ to any degree. The AVDD and DVDD pins must therefore be tied together in all designs.

3. During operation of the hardware MUTEB function between setting mute and then un-mute, the device may either not un-mute or the gain setting after un-mute will be incorrect. It is advised to re-write the gain settings immediately following hardware un-mute to guarantee faultless operation.

4. Voltage greater than 500mV on the digital pins while the device is powered down may prevent successful POR of the device when power is re-applied. It is preferable that all digital pins are pulled low during power up or alternatively ensure that there are no residual voltages held on the digital pins during power down.

5. The WM8816 output offset voltage can vary dependent upon the op-amp used usually with the largest level of offset voltage occurring at +15.5dB gain. Output offset voltage has linear relationship on input bias current and offset voltage amplitudes. Using differing op-amp types causes a large variation in offset voltage. Below is a list of recommended op-amps which are found to give the least offset issues when used with the WM8816. Channel matching is also important factor and not necessarily only the absolute offset value.

DEVICE	MANUFACTURER	OFFSET IN MV
OP275	Analog Devices	8.55
MC33078/9	On-Semi/ST	28.4
AD8610	Analog Devices	1.49
LT1793	Linear	18.5
OP1177	Analog Devices	0.505
OP277	BurrBrown	0.228

Table 3 Recommended Op-amps

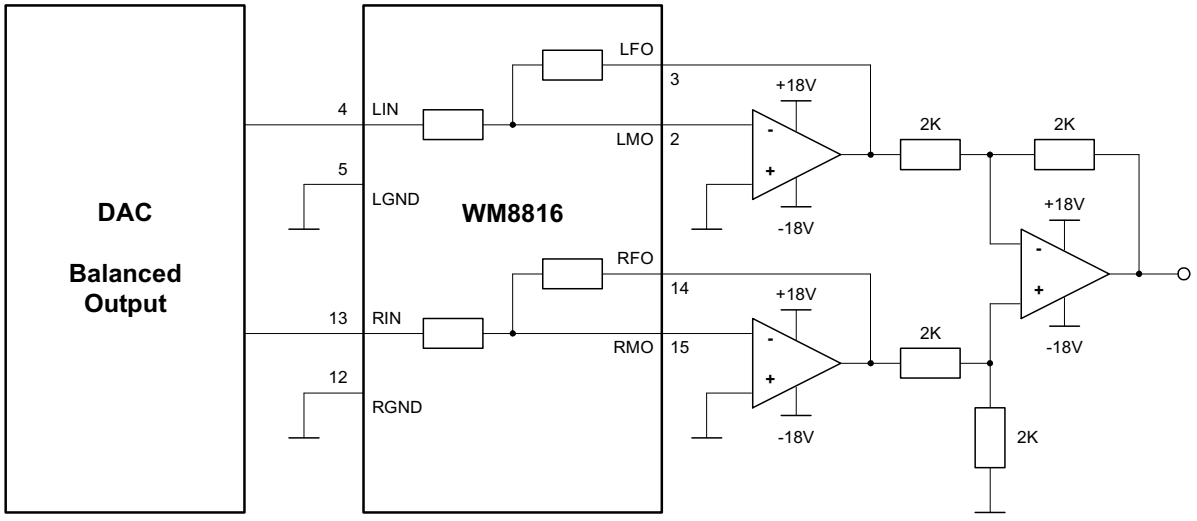
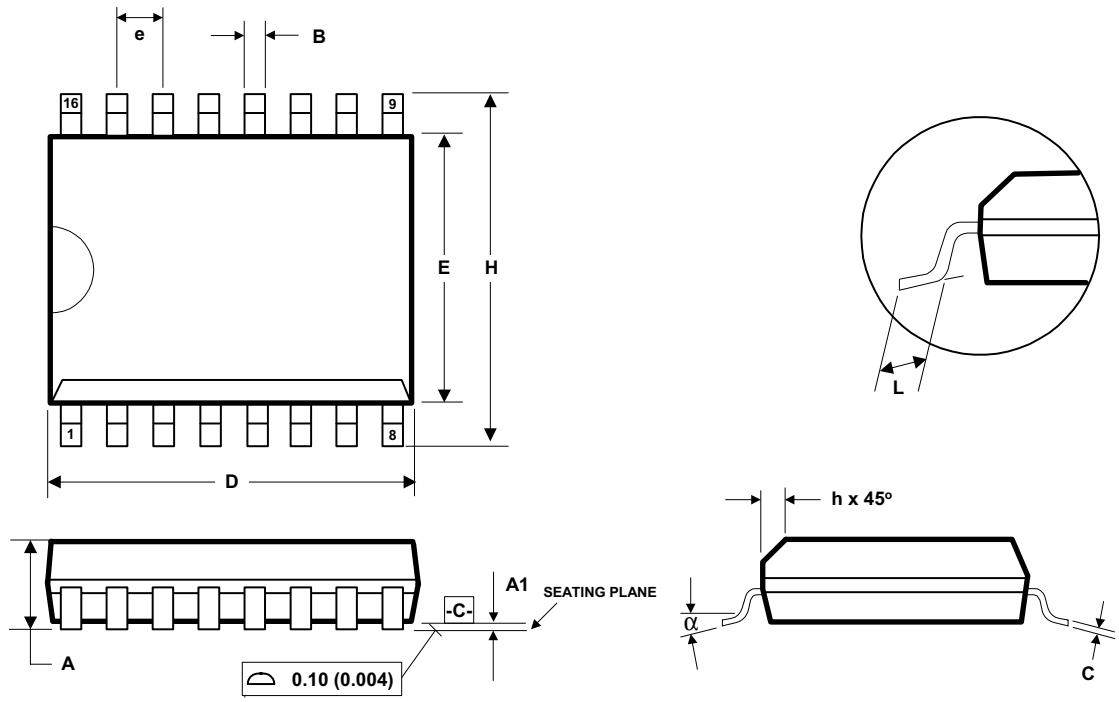


Figure 6 Configuration for Double Balanced Output (One Channel)

PACKAGE DIMENSIONS

DW: 16 PIN SOICW 7.5mm (0.3") Wide Body, 1.27mm Lead Pitch **DM019.A**



Symbols	Dimensions (mm)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.0926	0.1043
A_1	0.10	0.30	0.0040	0.0118
B	0.33	0.51	0.0130	0.0200
C	0.23	0.32	0.0091	0.0125
D	10.10	10.50	0.3465	0.3622
e	1.27 BSC		0.0500 BSC	
E	7.40	7.60	0.2914	0.2992
h	0.25	0.75	0.0100	0.0290
H	10.00	10.65	0.3940	0.4190
L	0.40	1.27	0.0160	0.0500
α	0^o	8^o	0^o	8^o
REF:	JEDEC.95, MS-013			

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D. MEETS JEDEC.95 MS-013, VARIATION = AA. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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