

January 1997

CD74FCT863A

BiCMOS FCT Interface Logic, 9-Bit Bus Transceiver, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay: 6.0ns at $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50pF$
- CD74FCT863A
 - Noninverting
- SCR Latchup Resistant BiCMOS Process and

**NOT RECOMMENDED
FOR NEW DESIGNS**
Use CMOS Technology

Circuit Design

- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at $V_{CC} = 5V$
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

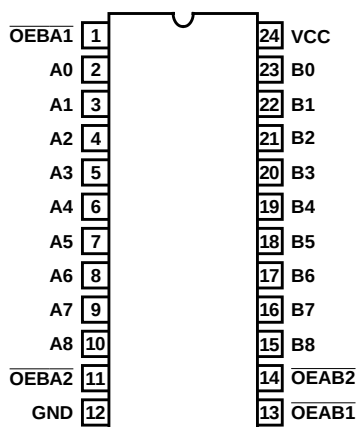
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT863AM	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

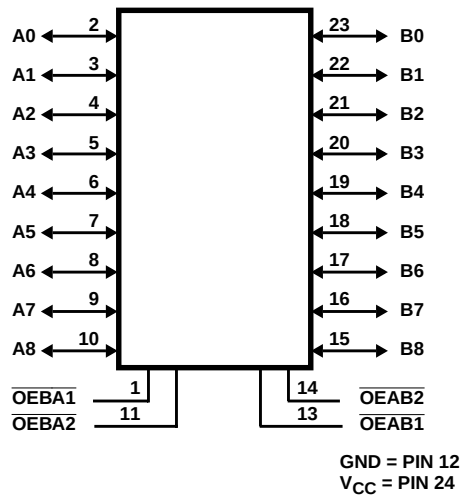
Pinout

CD74FCT863A
(SOIC)
TOP VIEW



CD74FCT863A

Functional Diagram



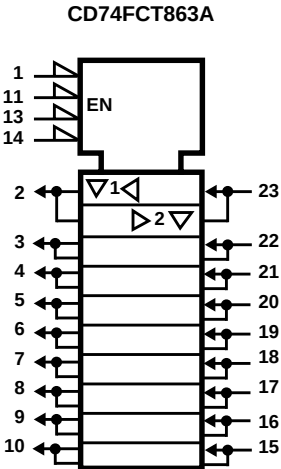
TRUTH TABLE (Note 1)

INPUTS				OUTPUTS		FUNCTION
OEBA	OEAB	B	A	B	A	
L	H	L	N/A	N/A	L	B Data to A Bus
L	H	H	N/A	N/A	H	B Data to A Bus
H	L	N/A	L	L	N/A	A Data to B Bus
H	L	N/A	H	H	N/A	A Data to B Bus
H	H	X	X	Z	Z	High Z
L	L	-	-	-	-	A Data to B Bus, B Data to A Bus

NOTE:

1. H= HIGH Voltage Level
L = LOW Voltage Level
N/A = Not Applicable
X = Immaterial
Z = HIGH Impedance

IEC Logic Symbol



CD74FCT863A

Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) -0.5V to 6V
DC Diode Current, I_{IK} (For $V_I < -0.5V$) -20mA
DC Output Diode Current, I_{OK} (for $V_O < -0.5V$) -50mA
DC Output Sink Current per Output Pin, I_O 70mA
DC Output Source Current per Output Pin, I_O -30mA
DC V_{CC} Current (I_{CC}) 234mA
DC Ground Current (I_{GND}) 455mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} ($^{\circ}C/W$)
SOIC Package 75
Maximum Junction Temperature 150 $^{\circ}C$
Maximum Storage Temperature Range -65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s) 300 $^{\circ}C$
(Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A 0 $^{\circ}C$ to 70 $^{\circ}C$
Supply Voltage Range, V_{CC} 4.75V to 5.25V
DC Input Voltage, V_I 0 to V_{CC}
DC Output Voltage, V_O 0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, dt/dv 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0 $^{\circ}C$ to 70 $^{\circ}C$, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A)				UNITS
					25°C		0°C TO 70°C		
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V _{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V _{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I _{IH}	V _{CC}		Max	-	0.1	-	1	μA
Low Level Input Current	I _{IL}	GND		Max	-	-0.1	-	-1	μA
Three-State Leakage Current	I _{OZH}	V _{CC}		Max	-	0.5	-	10	μA
	I _{OZL}	GND		Max	-	-0.5	-	-10	μA
Input Clamp Voltage	V _{IK}	V _{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I _{OS}	V _O = 0 V _{CC} or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	Max	-	8	-	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI _{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

- Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- Inputs that are not measured are at V_{CC} or GND.
- FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max. at 70 $^{\circ}C$.

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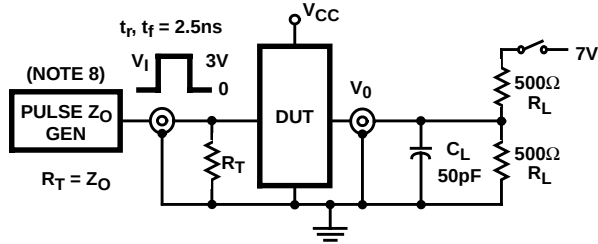
Switching Specifications Over Operating Range FCT Series $t_r, t_f = 2.5\text{ns}$, $C_L = 50\text{pF}$, R_L (Figure 1)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Propagation Delays						
Data to Outputs	t_{PLH}, t_{PHL}	5 (Note 6)	6	1.5	8	ns
Output Enable to Output	t_{PZL}, t_{PZH}	5	9	1.5	12	ns
Output Disable to Output	t_{PLZ}, t_{PHZ}	5	7.5	1.5	10	ns
Power Dissipation Capacitance	C_{PD} (Note 7)	-	-	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	15	pF

NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
7. C_{PD} , measured per flip-flop, is used to determine the dynamic power consumption.
 P_D (per package) = $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
 V_{CC} = supply voltage
 ΔI_{CC} = flow through current x unit load
 C_L = output load capacitance
 D = duty cycle of input high
 f_O = output frequency
 f_I = input frequency

Test Circuits and Waveforms



NOTE:

8. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_r, t_f \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

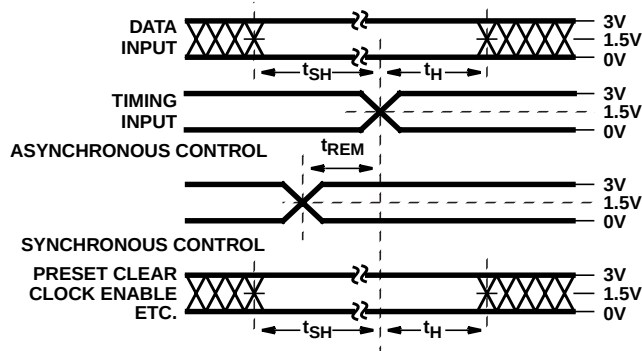


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

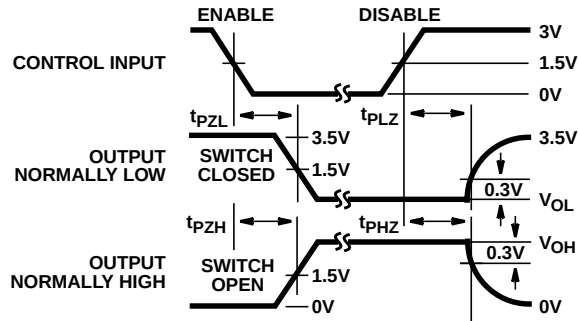


FIGURE 4. ENABLE AND DISABLE TIMING

SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL} , Open Drain	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

$V_{IN} = 0\text{V}$ to 3V .

Input: $t_r = t_f = 2.5\text{ns}$ (10% to 90%), unless otherwise specified

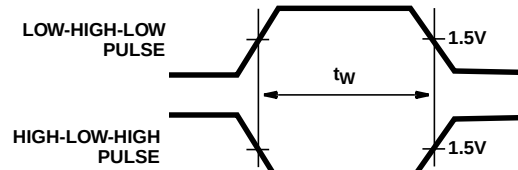


FIGURE 3. PULSE WIDTH

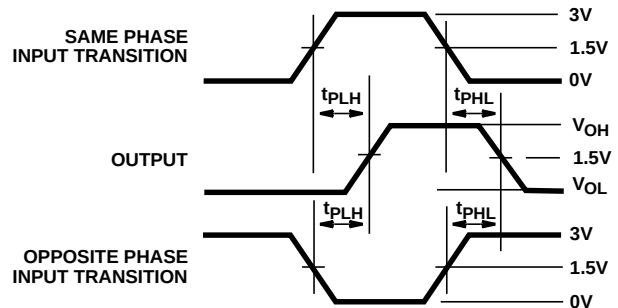
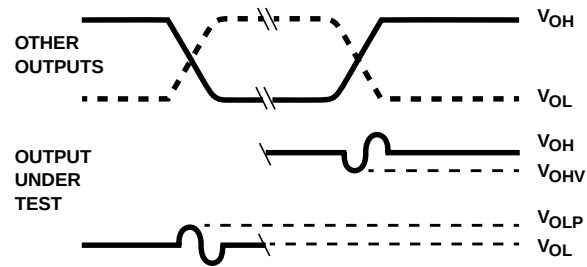


FIGURE 5. PROPAGATION DELAY

Test Circuits and Waveforms (Continued)



NOTES:

9. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH} .
10. Input pulses have the following characteristics:
 $P_{RR} \leq 1\text{MHz}$, $t_r = 2.5\text{ns}$, $t_f = 2.5\text{ns}$, skew 1ns .
11. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with $0.1\mu\text{F}$ capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74FCT863AM	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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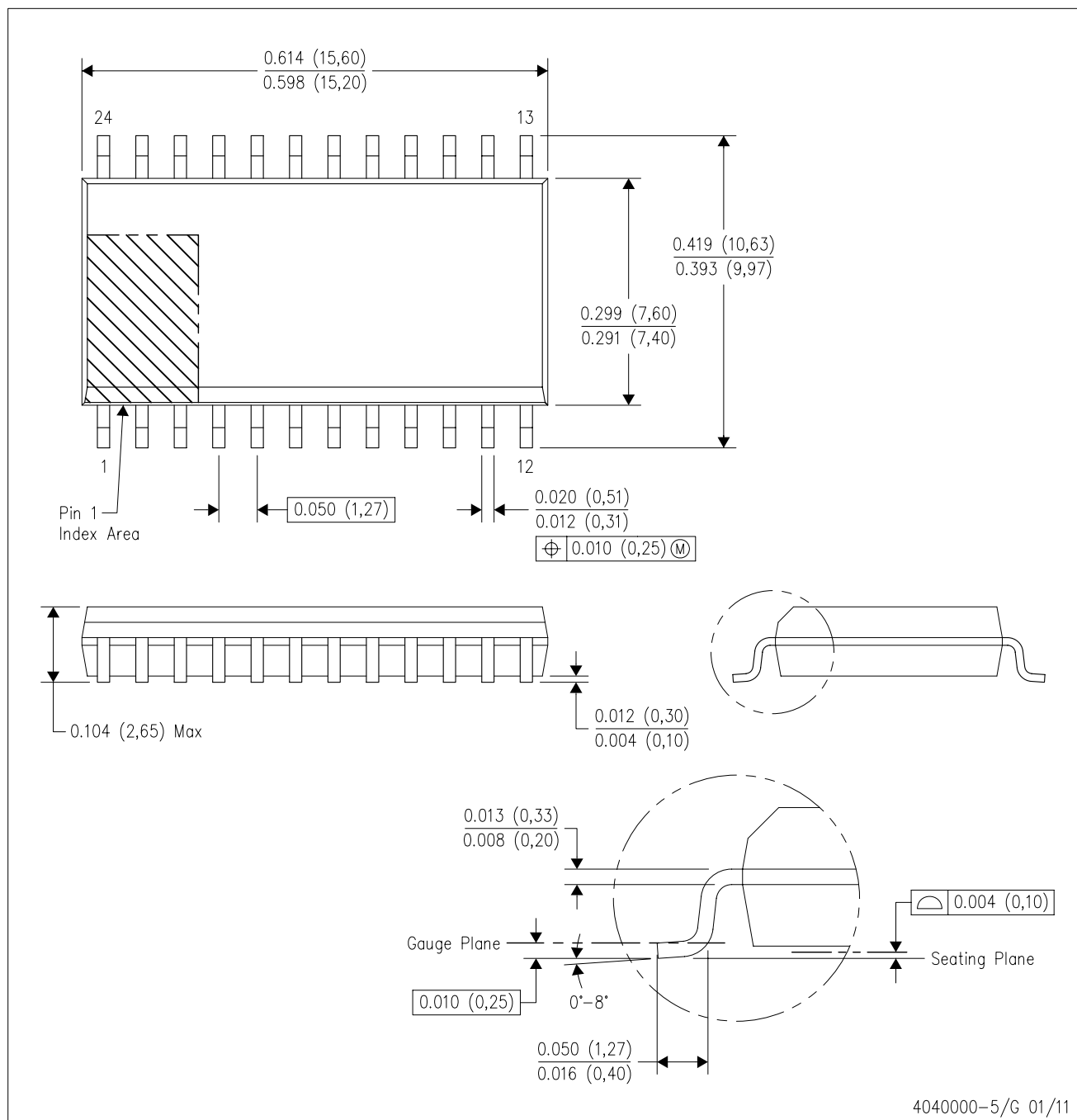
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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