Holtek 32-bit Microcontroller with ARM® Cortex™-M3 Core

HT32F1251/51B/52/53 Series Datasheet

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Table of Contents

1 General Description 6

2 Features 7

Core 7
On-chip Memory 7
Flash Memory Controller 8
Reset Control Unit 8
Clock Control Unit 8
Power Management 9
Analog to Digital Converter 9
Analog Operational Amplifier/Comparator 9
I/O Ports 10
PWM Generation and Capture Timers 10
Watchdog Timer 11
Real Time Clock 11
Inter-integrated Circuit (I^2C) 12
Serial Peripheral Interface (SPI) 12
Universal Synchronous Asynchronous Receiver Transmitter (USART) 13
Debug Support 13
Package and Operation Temperature 13

3 Overview 14

Device Information 14
Block Diagram 15
Memory Map 16
Clock Structure 17
Pin Assignment 18

4 Electrical Characteristics 22

Absolute Maximum Ratings 22
DC Characteristics 22
On-Chip LDO Voltage Regulator Characteristics 22
Power Consumption 23
Reset and Supply Monitor Characteristics 23
External Clock Characteristics 24
Internal Clock Characteristics 25
PLL Characteristics 26
Memory Characteristics 26

I/O Port Characteristics 26
ADC Characteristics 28
Operation Amplifier/Comparator Characteristics 29
GPTM Characteristics 29
I²C Characteristics 30
SPI Characteristics 31

5 Package Information 33
48-pin LQFP (7mmx7mm) Outline Dimensions 33

List of Tables

Table 1. HT32F125x Series Features and Peripheral List 14
Table 2. HT32F125x Pin Descriptions 20
Table 3. Absolute Maximum Ratings 22
Table 4. DC Operating Conditions 22
Table 5. LDO Characteristics 22
Table 6. Power Consumption Characteristics 23
Table 7. LVD/BOD Characteristics 23
Table 8. High Speed External Clock (HSE) Characteristics 24
Table 9. Low Speed External Clock (LSE) Characteristics 24
Table 10. High Speed Internal Clock (HSI) Characteristics 25
Table 11. Low Speed Internal Clock (LSI) Characteristics 25
Table 12. PLL Characteristics 26
Table 13. Flash Memory Characteristics 26
Table 14. I/O Port Characteristics 26
Table 15. ADC Characteristics 28
Table 16. OPA/CMP Characteristics 29
Table 17. GPTM Characteristics 29
Table 18. I^2C Characteristics 30
Table 19. SPI Characteristics 31

List of Figures

Figure 1. HT32F125x Block Diagram 15
Figure 2. HT32F125x Memory Map 16
Figure 3. HT32F125x Clock Structure Diagram 17
Figure 4. HT32F1251B 48LQFP Pin Assignment 18
Figure 5. HT32F1251/52/53 48LQFP Pin Assignment 19
Figure 6. I^2C Timing Diagram 30
Figure 7. SPI Timing Diagram – SPI Master Mode 31
Figure 8. SPI Timing Diagram – SPI Slave Mode and CPHA=1 32

1 General Description

The Holtek HT32F125x series of devices are high performance, low power consumption 32-bit microcontrollers based on the ARM® Cortex™-M3 processor core. The Cortex™-M3 is a next-generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The HT32F125x device operates at a frequency of up to 72 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 32 KB of embedded Flash memory for code/data storage and up to 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I²C, USART, SPI, SW-DP (Serial Wire Debug Port), etc., are also implemented in this device series. Several power saving modes provide the flexibility for maximum optimisation between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the HT32F125x device suitable for a wide range of applications, especially in areas such as white goods and application control, power monitor and alarm systems, consumer and handheld equipment, data logging applications and so on.

2 Features

Core

- 32-bit ARM® Cortex™-M3 processor core
- Up to 72 MHz operation frequency
- 1.25 DMIPS/MHz (Dhrystone 2.1)
- Single-cycle multiplication and hardware division
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex™-M3 processor is a general-purpose 32-bit processor core especially suitable for products requiring high performance and low power consumption microcontrollers. It offers many new features such as a Thumb-2 instruction set, hardware divider, low latency interrupt respond time, atomic bit-banding access and multiple buses for simultaneous accesses. The Cortex™-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex™-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, System bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocell (ETM)
- Trace Port Interface Unit (TPIU)

On-chip Memory

- 9 to 32 KB on-chip Flash memory for instruction/data and option storage
- 2 to 8 KB on-chip SRAM
- Supports several boot modes

The ARM® Cortex™-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. The instruction code and data are both located in the same memory address space but in different address ranges. The maximum address range of the Cortex™-M3 is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex™-M3 processor to reduce the software complexity of repeated implementation of different device vendors. However, some regions are used by the ARM® Cortex™-M3 system peripherals. Refer to the ARM® Cortex™-M3 Technical Reference Manual for more information. The Figure 2. HT32F125x Memory Map shows the memory map of the HT32F125x series of devices, including Code, SRAM, peripheral, and other pre-defined regions.

Flash Memory Controller

- Flash accelerator for maximum efficiency
- 32-bit word programming (ISP and IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit

- Supply supervisor:
  - Power On Reset (POR)
  - Brown Out Detector (BOD)
  - Programmable Low Voltage Detector (LVD)

The Reset Control Unit (RSTCU) has three kinds of reset, the power on reset, system reset and APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8MHz RC oscillator trimmed to 1% accuracy at 3.3V operating voltage and 25°C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers and clock gating circuitry. The clocks of the AHB, APB and Cortex™-M3 are derived from the system clock (CK_SYS) which can come from the HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source. The maximum operating frequency of the system core clock (CK_AHB) can be up to 72 MHz. (**NOTE:** LSE is not supported by HT32F1251B).

Power Management

- Single 3.3 V power supply: 2.7 V to 3.6 V
- Integrated 1.8 V LDO regulator for core and peripheral power supply
- V_{BAT} battery power supply for RTC and backup registers
- Three power domains: 3.3V, 1.8V and Backup
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

The Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption. (**NOTE:** HT32F1251B does not support V_{BAT} battery power supply).

Analog to Digital Converter

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate - 1 μs at 56 MHz, 1.17 μs at 72 MHz
- 8 external analog input channels
- Supply voltage range: 2.7 V ~ 3.6 V
- Conversion range: V_{SSA} ~ V_{DDA}

A 12-bit multi-channel ADC is integrated in the device. There are a total of 10 multiplexed channels, which include 8 external channels on which the external analog signals can be supplied, and 2 internal channels. If the input voltage is required to remain within a specific threshold window, the Analog Watchdog function will monitor and detect the signal. An interrupt will then be generated to inform that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

Analog Operational Amplifier/Comparator

- 2 Operational Amplifiers or 2 Comparator functions which are software configurable
- Supply voltage range: 2.7 V ~ 3.6 V

Two Operational Amplifiers/Comparators (OPA/CMP) are implemented within the devices. They can be configured either as Operational Amplifiers or as Analog Comparators. When configured as comparators, they are capable of asserting interrupts to the NVIC.

I/O Ports

- Up to 32 GPIOs
- Port A and Port B are mapped as 16 external interrupts (EXTI)
- Almost all I/O pins are 5 V-tolerant except for pins shared with analog inputs

There are up to 32 General Purpose I/O pins, (GPIO), named PA0 ~ PA15 and PB0 ~ PB15 for the device to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications.

The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the AF input or output pins.

The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI).

PWM Generation and Capture Timers

- Two 16-bit General-Purpose Timers (GPTM)
- Up to 4CHs PWM compare output or input capture for each GPTM
- External trigger input

The General-Purpose Timers, known as GPTM0 and GPTM1, consist of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output. The GPTM supports an Encoder Interface using a decoder with two inputs.

Watchdog Timer

- 12-bit down counter with 3-bit prescaler
- Interrupt or reset event for the system
- Programmable watchdog timer window function
- Write protection function

The Watchdog Timer is a hardware timing circuitry that can be used to detect system failures due to software malfunctions. It includes a 12-bit down-counting counter, a prescaler, a WDT counter value register, a WDT delta value register, interrupt related circuits, WDT operation control circuitry and the WDT protection mechanism. The Watchdog Timer can be operated in an interrupt mode or a reset mode. The Watchdog Timer will generate an interrupt or a reset when the counter counts down and reaches a zero value. If the software does not reload the counter value before the Watchdog Timer underflow occurs, an interrupt or a reset will be generated when the counter underflows. In addition, an interrupt or reset is also generated if the software reloads the counter when the counter value is greater than or equal to the WDT delta value. That means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. The register write protection function can be enabled to prevent it from changing the configuration of the Watchdog Timer unexpectedly.

Real Time Clock

- 32-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, circuitry includes the APB interface, a 32-bit up-counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the V_{DD18} domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{DD18} domain is powered off, i.e., when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume from the Power-Down mode.

Inter-integrated Circuit (I^2C)

- Support both master and slave mode with a frequency of up to 400 kHz
- Provide arbitration function
- Supports 7-bit and 10-bit addressing mode and general call addressing

The I^2C Module is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides two data transfer rates: (1) 100 kHz in the Standard mode or (2) 400 kHz in the Fast mode. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected to the whole I^2C bus is a bi-directional data line between the master and slave devices used for the transmission and reception of data. The I^2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface (SPI)

- SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, among which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master which controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried in a similar way but with a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter (USART)

- Operating frequency: up to 4.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- Full Modem function
- FIFO Depth: 16 x 9 bits for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is also commonly used for RS232 standard communication. The USART peripheral function supports five-types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt, Time Out Interrupt and MODEM Status Interrupt. The USART module includes a 16-byte transmitter FIFO, (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO).

Software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

The USART includes a programmable baud rate generator which is capable of dividing the CK_AHB to produce a clock for the USART transmitter and receiver.

Debug Support

- Serial Wire Debug Port - SW-DP
- 6 instruction comparators and 2 literal comparators for hardware breakpoint or code / literal patch
- 4 comparators for hardware watchpoint
- 1-bit asynchronous trace - TRACESWO

Package and Operation Temperature

- 48-pin LQFP package
- Operation temperature range: -40°C to +85°C

3 Overview

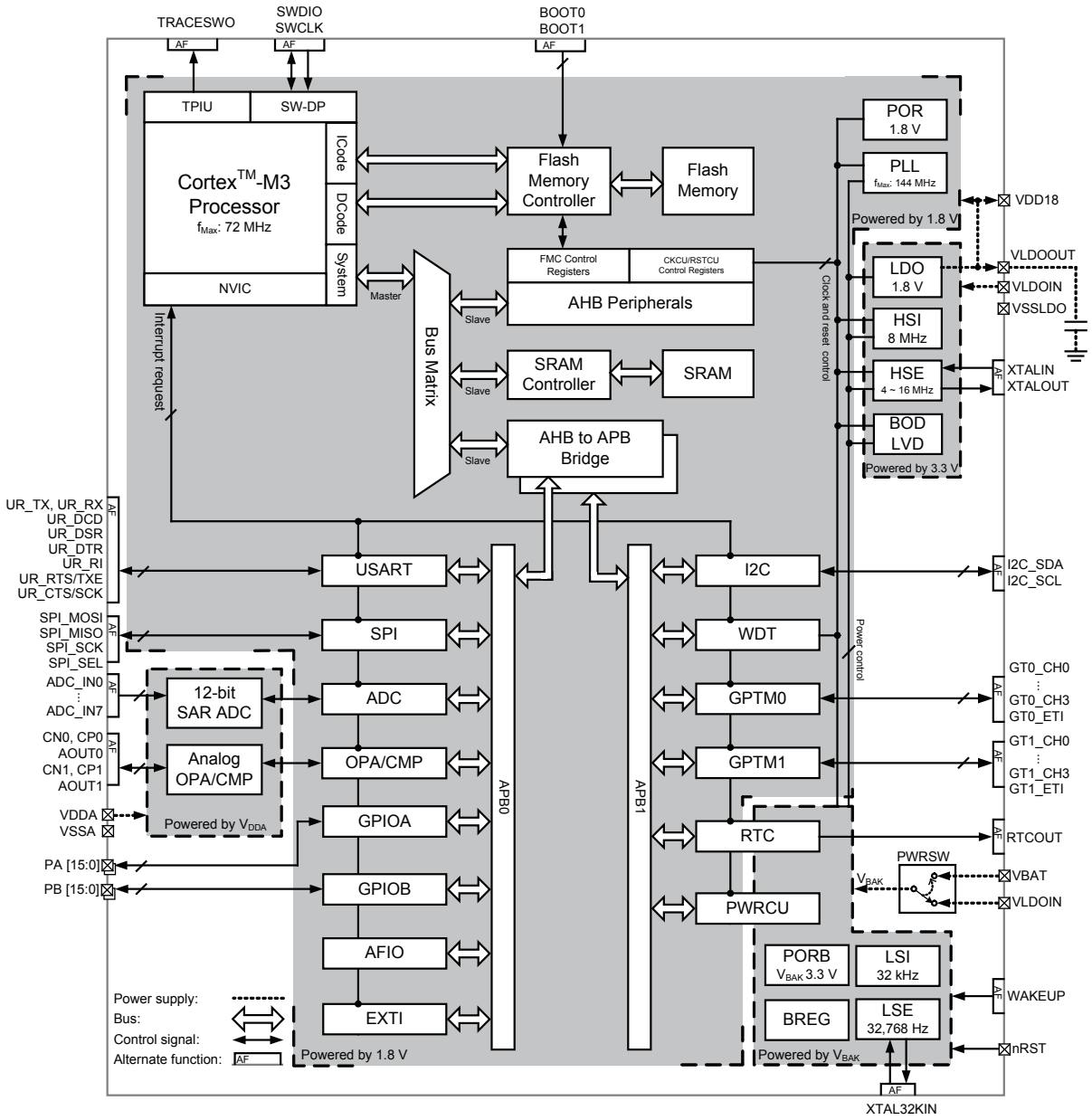
Device Information

Most features are common to all devices while the main features distinguishing them are Flash memory and SRAM memory capacities.

Table 1. HT32F125x Series Features and Peripheral List

Peripherals		HT32F1253	HT32F1252	HT32F1251	HT32F1251B
Main Flash (KB)		31	16	8	8
Option Bytes Flash (KB)		1	1	1	1
SRAM (KB)		8	4	2	2
Timers	GPTM	2			
	RTC	1			
	WDT	1			
Communication	USART	1			
	SPI	1			
	I²C	1			
GPIO		32			30
EXTI		16			
12-bit ADC Number of channels		1 8 Channels			
OPA/Comparator		2			
CPU frequency		Up to 72 MHz			
Operating voltage		2.7 V ~ 3.6 V			
Operating temperature		-40 °C ~ +85 °C			
Package		LQFP48			

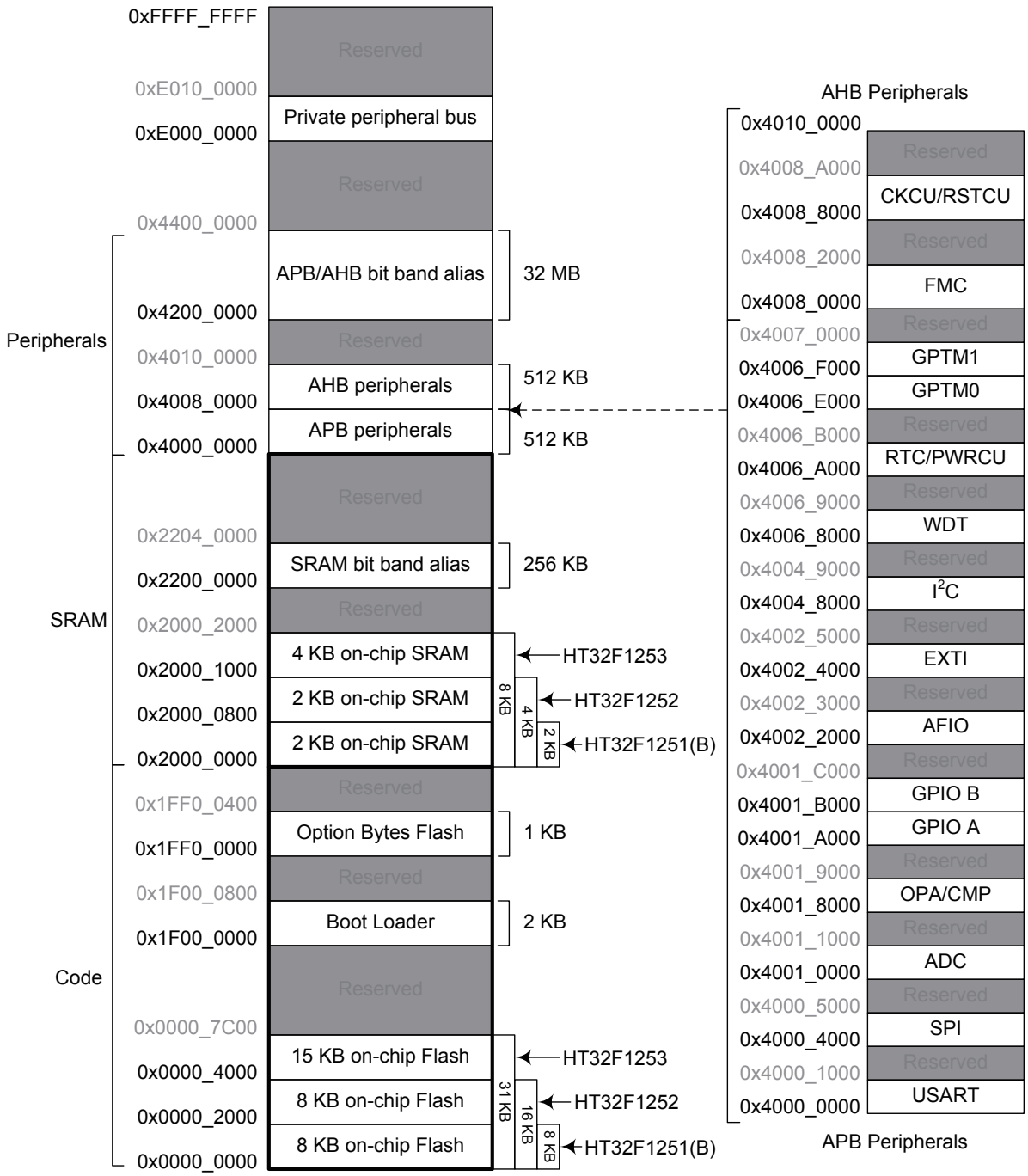
Block Diagram



NOTE: HT32F1251B does not include the VBAT, XTAL32KIN and XTAL32KOUT pins.

Figure 1. HT32F125x Block Diagram

Memory Map

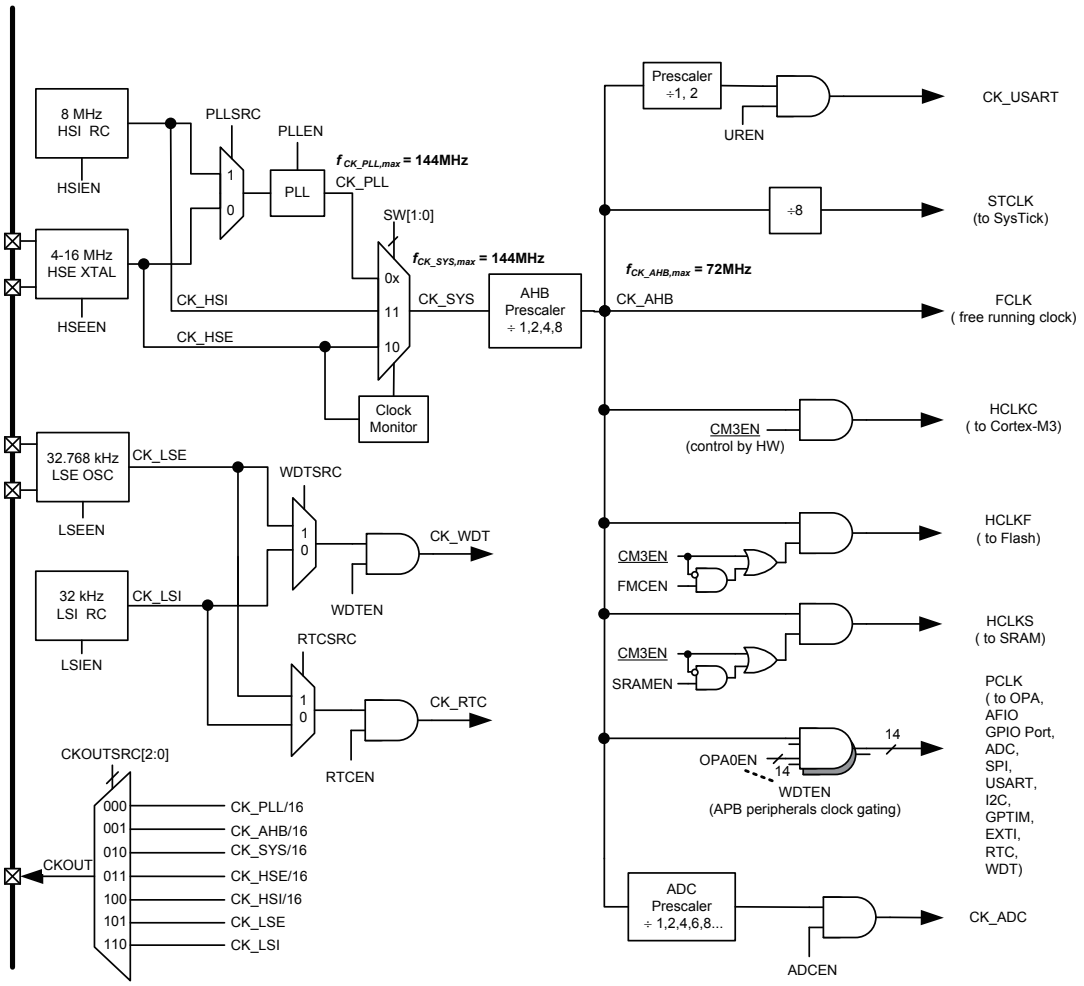


NOTES: 1. For HT32F1251(B), the Flash memory space at 0x0000_2000 to 0x0000_7BFF and the SRAM memory space at 0x2000_0800 to 0x2000_1FFF are reserved.

2. For HT32F1252, the Flash memory space at 0x0000_4000 to 0x0000_7BFF and the SRAM memory space at 0x2000_1000 to 0x2000_1FFF are reserved.

Figure 2. HT32F125x Memory Map

Clock Structure



Legend: HSE = High Speed External clock
HSI = High Speed Internal clock
LSE = Low Speed External clock
LSI = Low Speed Internal clock

NOTE: 1. Control bits LSIEN & LSEEN are located at RTC Control Register (RTCCR).
2. HT32F1251B does not include the VBAT, XTAL32KIN and XTAL32KOUT pins.

Figure 3. HT32F125x Clock Structure Diagram

Pin Assignment

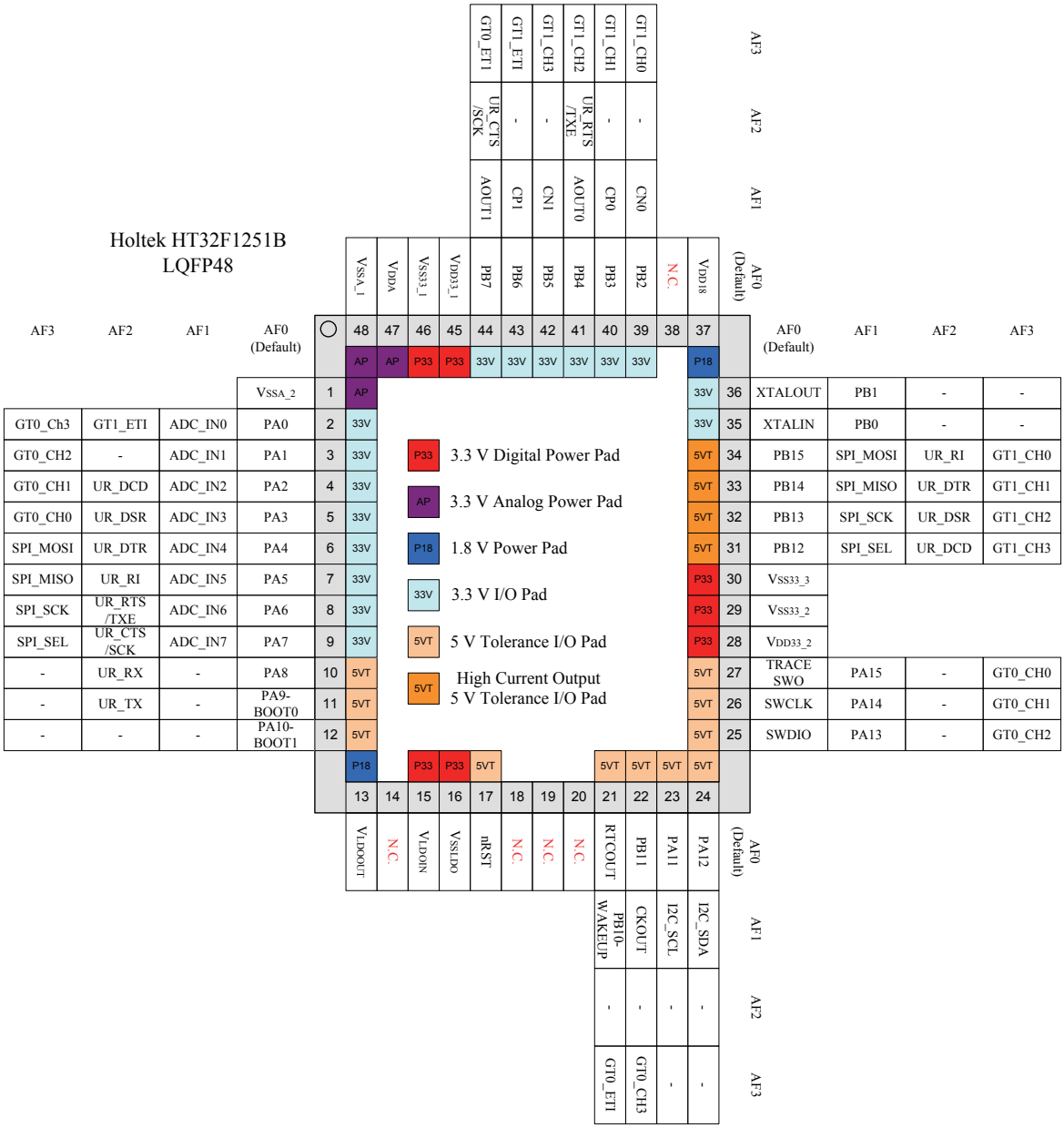


Figure 4. HT32F1251B 48LQFP Pin Assignment

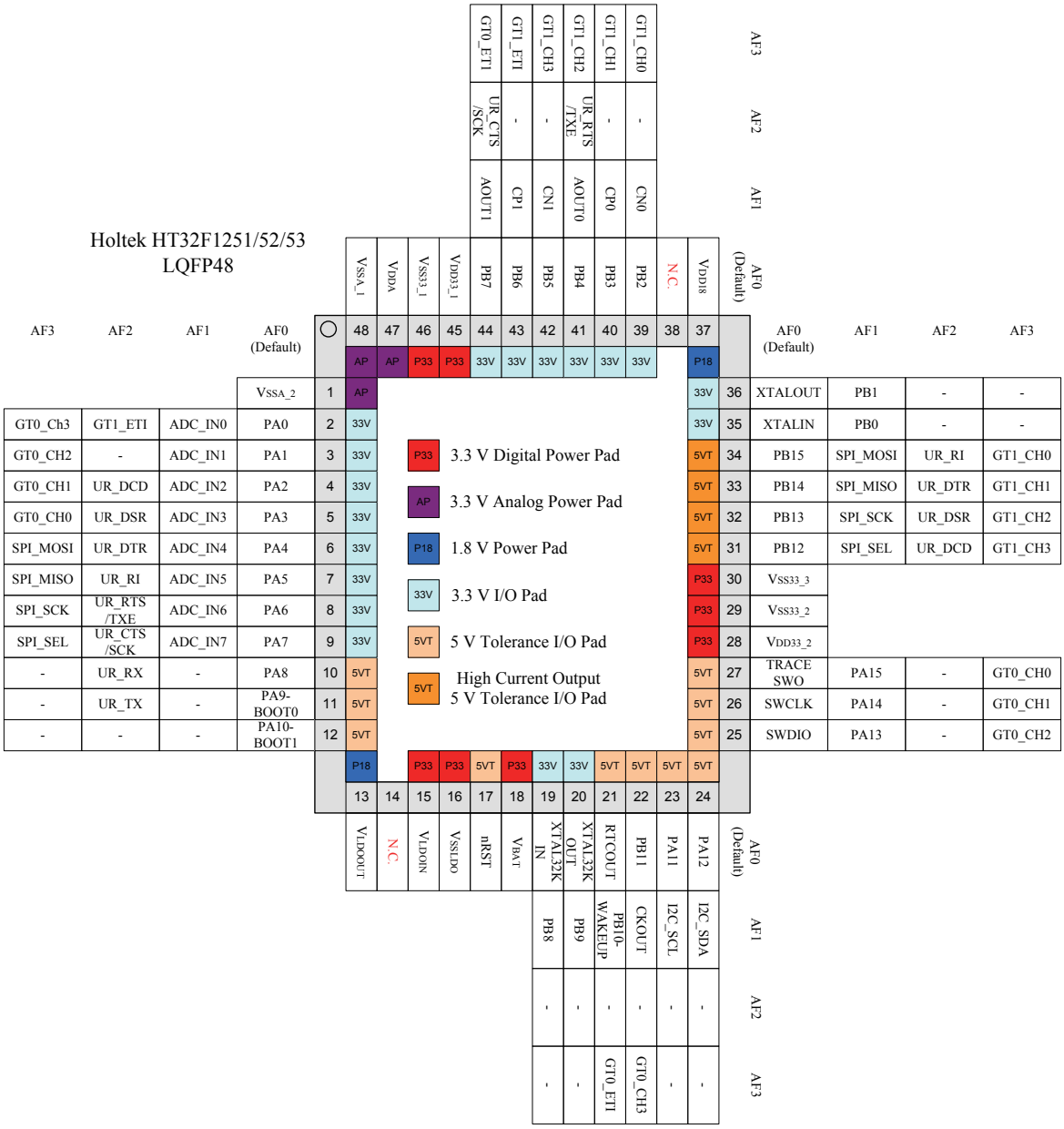


Figure 5. HT32F1251/52/53 48LQFP Pin Assignment

Table 2. HT32F125x Pin Descriptions

Pin Name	Pins	Type (Note1)	IO Level (Note2)	Description			
	48 LQFP			Default function (AF0)	AF1	AF2	AF3
V_{SSA_2}	1	P		Ground reference for ADC and OPA/Comparator			
PA0	2	I/O		GPIO PA0	ADC_IN0	GT1_ETI	GT0_CH3
PA1	3	I/O		GPIO PA1	ADC_IN1		GT0_CH2
PA2	4	I/O		GPIO PA2	ADC_IN2	UR_DCD	GT0_CH1
PA3	5	I/O		GPIO PA3	ADC_IN3	UR_DSR	GT0_CH0
PA4	6	I/O		GPIO PA4	ADC_IN4	UR_DTR	SPI_MOSI
PA5	7	I/O		GPIO PA5	ADC_IN5	UR_RI	SPI_MISO
PA6	8	I/O		GPIO PA6	ADC_IN6	UR_RTS/TXE	SPI_SCK
PA7	9	I/O		GPIO PA7	ADC_IN7	UR_CTS/SCK	SPI_SEL
PA8	10	I/O	5V-T	GPIO PA8		UR_RX	
PA9	11	I/O	5V-T	GPIO PA9-BOOT0		UR_TX	
PA10	12	I/O	5V-T	GPIO PA10-BOOT1			
V_{LDOOUT}	13	P		LDO 1.8 V output. Please put a 10μF capacitor to GND in those pins as close as possible.			
N.C	14						
V_{LDOIN}	15	P		LDO 3.3 V power source, also connected to the power switch of the backup domain.			
V_{SSLDO}	16	P		LDO ground reference			
nRST	17	I (Backup domain)	5V-T	External reset pin and external wakeup pin in Power-Down mode			
V_{BAT}(note3)	18	P		VDD 3.3 V for backup domain			
PB8(note3)	19	I/O (Backup domain)		XTAL32KIN	PB8		
PB9(note3)	20	I/O (Backup domain)		XTAL32KOUT	PB9		
PB10	21	I/O (Backup domain)	5V-T	RTCOUT	PB10-WAKEUP		GT0_ETI
PB11	22	I/O	5V-T	GPIO PB11	CKOUT		GT0_CH3
PA11	23	I/O	5V-T	GPIO PA11	I2C_SCL		
PA12	24	I/O	5V-T	GPIO PA12	I2C_SDA		
PA13	25	I/O	5V-T	SWDIO	PA13		GT0_CH2
PA14	26	I/O	5V-T	SWCLK	PA14		GT0_CH1
PA15	27	I/O	5V-T	TRACESWO	PA15		GT0_CH0
V_{DD33_2}	28	P		3.3 V voltage for digital I/O			
V_{SS33_2}	29	P		Ground reference for digital I/O			
V_{SS33_3}	30	P		Ground reference for digital core			
PB12	31	I/O	5V-T	GPIO PB12	SPI_SEL	UR_DCD	GT1_CH3

Pin Name	Pins	Type (Note1)	IO Level (Note2)	Description			
	48 LQFP			Default function (AF0)	AF1	AF2	AF3
PB13	32	I/O	5V-T	GPIO PB13	SPI_SCK	UR_DSR	GT1_CH2
PB14	33	I/O	5V-T	GPIO PB14	SPI_MISO	UR_DTR	GT1_CH1
PB15	34	I/O	5V-T	GPIO PB15	SPI_MOSI	UR_RI	GT1_CH0
PB0	35	I/O		XTALIN	PB0		
PB1	36	I/O		XTALOUT	PB1		
V_{DD18}	37	P		1.8 V voltage for core			
N.C	38						
PB2	39	I/O		GPIO PB2	CN0		GT1_CH0
PB3	40	I/O		GPIO PB3	CP0		GT1_CH1
PB4	41	I/O		GPIO PB4	AOUT0	UR_RTS/TXE	GT1_CH2
PB5	42	I/O		GPIO PB5	CN1		GT1_CH3
PB6	43	I/O		GPIO PB6	CP1		GT1_ETI
PB7	44	I/O		GPIO PB7	AOUT1	UR_CTS/SCK	GT0_ETI
V_{DD33_1}	45	P		3.3 V voltage for digital I/O			
V_{SS33_1}	46	P		Ground reference for digital I/O			
V_{DDA}	47	P		3.3 V analog voltage for ADC and OPA/Comparator			
V_{SSA_1}	48	P		Ground reference for ADC and OPA/Comparator			

NOTES: 1. I = input, O = output, P = power supply.

2. 5V-T = 5 V tolerant.

3. HT32F1251B does not include the VBAT, XTAL32KIN and XTAL32KOUT pins.

4. The GPIOs are in AF0 state after VDD18 power on reset (POR) except the RTCOUT pin of Backup Domain I/O. The RTCOUT pin is reset by the Backup Domain power-on-reset (PORB) or Backup Domain software reset (BAK_RST bit in BAK_CR register).

5. The backup domain of I/O pins has driving current capability limitation (< 1mA @ V_{BAT} = 3.3 V).

4 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD33}	External main supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5 V-tolerant I/O	V_{SS} - 0.3	V_{SS} + 5.5	V
	Input voltage on other I/O	V_{SS} - 0.3	V_{DD33} + 0.3	V
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C
P_D	Total power dissipation	—	500	mW
V_{ESD}	Electrostatic discharge voltage (human body mode)	-4000	+4000	V

DC Characteristics

Table 4. DC Operating Conditions

TA = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	Operating voltage of I/O	—	2.7	3.3	3.6	V
V_{DDA}	Analog operating voltage	—	2.7	3.3	3.6	V
V_{BAT}	Operating voltage of Battery supply	—	2.7	3.3	3.6	V
V_{DD18}	Operating voltage of core power	—	1.62	1.8	1.98	V

On-Chip LDO Voltage Regulator Characteristics

Table 5. LDO Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LDOOUT}	Internal regulator output voltage	V_{LDOIN} = 3.3 V Regulator input	1.71	1.8	1.89	V
I_{DD18}	Output current	V_{LDOIN} = 2.4 V Regulator input	—	—	200	mA
C_{LDO}	External filter capacitor value for internal core power supply	The capacitor value is dependent on the core power current consumption	2.2	—	10	μF

Power Consumption

Table 6. Power Consumption Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD33} = V_{BAT} = 3.3 V, HSE = 8MHz, PLL = 144 MHz, f_{HCLK} = 72 MHz, f_{PCLK} = 72 MHz, All peripherals enabled	—	47	—	mA
		V_{DD33} = V_{BAT} = 3.3 V, HSE = 8MHz, PLL = 144 MHz, f_{HCLK} = 72 MHz, f_{PCLK} = 72 MHz, All peripherals disabled	—	28	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{BAT} = 3.3 V, HSE = 8MHz, PLL = 144 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 72 MHz, All peripherals enabled	—	30	—	mA
		V_{DD33} = V_{BAT} = 3.3 V, HSE = 8MHz, PLL = 144 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 72 MHz, All peripherals disabled	—	7	—	mA
	Supply current (Deep-Sleep1 mode)	V_{DD33} = V_{BAT} = 3.3 V, All clock off (HSE/PLL/f_{HCLK}), LDO in low power mode, LSI on, RTC on	—	66	—	µA
	Supply current (Deep-Sleep2 mode)	V_{DD33} = V_{BAT} = 3.3 V, All clock off (HSE/PLL/f_{HCLK}), LDO off (DMOS on), LSI on, RTC on	—	11	—	µA
	Supply current (Power-Down mode)	V_{DD33} = V_{BAT} = 3.3 V, LDO off, LSE on, LSI off, RTC on	—	4.2	—	µA
		V_{DD33} = V_{BAT} = 3.3 V, LDO off, LSE on, LSI off, RTC off	—	4.1	—	µA
		V_{DD33} = V_{BAT} = 3.3 V, LDO off, LSE off, LSI on, RTC on	—	4.3	—	µA
		V_{DD33} = V_{BAT} = 3.3 V, LDO off, LSE off, LSI on, RTC off	—	4.2	—	µA
I_{BAT}	Battery supply current (Power-Down mode)	V_{DD33} not present, V_{BAT} = 3.3 V, LDO off, LSE off, LSI on, RTC on	—	4	—	µA
		V_{DD33} not present, V_{BAT} = 3.3 V, LDO off, LSE off, LSI on, RTC off	—	3.9	—	µA

NOTES: 1. HSE is the high speed external oscillator while HSI is the 8MHz high speed internal oscillator.

2. LSE is the low speed external oscillator while LSI is the 32 KHz low speed internal oscillator.

3. RTC means real time clock.

4. Code = while (1) { NOP x n } executed in Flash (n > 200).

Reset and Supply Monitor Characteristics

Table 7. LVD/BOD Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOD}	Voltage of Brown Out Detector	—	—	2.5	—	V
V_{LVD}	Voltage of Low Voltage Detector	LVDS (Note1) = '00'	—	2.7	—	V
		LVDS (Note1) = '01'	—	2.8	—	V
		LVDS (Note1) = '10'	—	2.9	—	V
		LVDS (Note1) = '11'	—	3.0	—	V
V_{POR}	Voltage of Power On Reset	—	—	1.36	—	V

NOTE: LVDS field is in PWRCU LVDCSR register

External Clock Characteristics

Table 8. High Speed External Clock (HSE) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High Speed External oscillator frequency (HSE)	V_{DD33} = 3.3 V	4	—	16	MHz
C_{HSE}	Recommended load capacitance on XTALIN and XTALOUT		—	TBD	—	pF
R_{FHSE}	Recommended external feedback resistor between XTALIN and XTALOUT		—	1.0	—	MΩ
D_{HSE}	HSE Oscillator Duty cycle		40	—	60	%
I_{DDHSE}	HSE Oscillator Operating Current	V_{DD33} = 3.3 V, T_A = 25°C	—	0.96	—	mA
I_{STBHSE}	HSE Oscillator Standby current	V_{DD33} = 3.3 V, T_A = 25°C	—	—	0.1	μA
t_{SUHSE}	HSE Oscillator Startup time	V_{DD33} = 3.3 V, T_A = 25°C	—	—	4	ms

Table 9. Low Speed External Clock (LSE) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low Speed External oscillator frequency (LSE)	V_{DD33} = V_{BAT} = 3.3 V	—	32.768	—	kHz
C_{LSE}	Recommended load capacitance on XTAL32IN and XTAL32OUT	—	—	TBD	—	pF
R_{FLSE}	Recommended external feedback resistor between XTAL32IN and XTAL32OUT	—	—	10	—	MΩ
D_{LSE}	LSE Oscillator Duty cycle	—	40	—	60	%
I_{DDLSE}	LSE Oscillator Operating Current	V_{DD33} = V_{BAT} = 3.3 V, LSESM = 0 (Normal startup mode)	—	1.7	—	μA
I_{STBLSE}	LSE Oscillator Standby current	V_{DD33} = V_{BAT} = 3.3 V, LSESM = 1 (Fast startup mode)	—	3	8	μA
t_{SULSE}	LSE Oscillator Startup time	V_{DD33} = V_{BAT} = 3.3 V, LSESM = 1 (Fast startup mode)	—	200	—	ms

Internal Clock Characteristics

Table 10. High Speed Internal Clock (HSI) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	High Speed Internal Oscillator Frequency (HSI)	V_{DD33} = 3.3 V, T_A = -40°C ~ +85°C	TBD	8	TBD	MHz
ACC_{HSI}	HSI Oscillator Frequency accuracy	Factory-trimmed, V_{DD33} = 3.3 V, T_A = 25°C	-1	—	+1	%
D_{HSI}	HSI Oscillator Duty cycle	V_{DD33} = 3.3 V, f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	HSI Oscillator Operating Current	V_{DD33} = 3.3 V, f_{HSI} = 8 MHz	—	0.92	—	mA
t_{SUHSI}	HSI Oscillator Startup time	V_{DD33} = 3.3 V, f_{HSI} = 8 MHz, HSIRCBL = 0 (HSI Ready Counter Bits Length 7 Bits)	—	17	—	μs

NOTE: HSIRCBL field is in PWRCU HSIRCR register

Table 11. Low Speed Internal Clock (LSI) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Low Speed Internal Oscillator Frequency(LSI)	V_{DD33} = V_{BAT} = 3.3 V, T_A = -40°C ~ +85°C	25	32	43	kHz
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD33} = V_{BAT} = 3.3 V, T_A = 25°C	—	1.0	2	μA
t_{SULSI}	LSI Oscillator Startup time	V_{DD33} = V_{BAT} = 3.3 V, T_A = 25°C	—	35	—	ms

PLL Characteristics

Table 12. PLL Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	$PLLV_{DD18}$ = 1.8 V	4	—	16	MHz
f_{PLL}	PLL output clock frequency	$PLLV_{DD18}$ = 1.8 V	8	—	144	MHz
t_{LOCK}	PLL lock time	$PLLV_{DD18}$ = 1.8 V	—	TBD	—	ms

Memory Characteristics

Table 13. Flash Memory Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{ENDU}	Number of guaranteed program /erase cycles before failure. (Endurance)	V_{DD18} =1.8 V, T_A= -40°C ~ +85°C	1	—	—	kcycles
T_{RET}	Data retention time	T_A = 25°C	100	—	—	Years
t_{PROG}	Word programming time	V_{DD18} = 1.8 V, T_A = -40°C ~ +85°C	40	—	—	μs
t_{ERASE}	Page erase time	V_{DD18} = 1.8 V, T_A = -40°C ~ +85°C	20	—	40	ms
t_{MERASE}	Mass erase time	V_{DD18} = 1.8 V, T_A = -40°C ~ +85°C	20	—	40	ms

I/O Port Characteristics

Table 14. I/O Port Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IL}	Low level input current	3.3 V IO	V_I = 0 V, On-chip pull-up resister disabled.	—	—	3	μA
		5 V-tolerant IO		—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High level input current	3.3 V IO	V_I = V_{DD33}, On-chip pull-down resister disabled.	—	—	3	μA
		5 V-tolerant IO		—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low level input voltage	3.3 V IO		-0.3	—	0.8	V
		5 V-tolerant IO		-0.3	—	0.8	V
		Reset pin		-0.3	—	0.8	V
V_{IH}	High level input voltage	3.3 V IO		2	—	3.6	V
		5 V-tolerant IO		2	—	5.5	V
		Reset pin		2	—	5.5	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V IO	—	400	—	mV
		5 V-tolerant IO	—	400	—	mV
		Reset pin	—	400	—	mV
I_{OL}	Low level output current (GPO Sink current)	3.3 V 4 mA drive IO, V_{OL} = 0.4 V	4	—	—	mA
		3.3 V 8 mA drive IO, V_{OL} = 0.4 V	8	—	—	mA
		5 V-tolerant 8 mA drive IO, V_{OL}=0.4V	8	—	—	mA
		5 V-tolerant 12 mA drive IO, V_{OL}=0.4V	12	—	—	mA
		Backup Domain IO drive @ V_{BAT} =3.3V, V_{OL} = 0.4 V, PB8, PB9, PB10.	—	—	1	mA
I_{OH}	High level output current (GPO Source current)	3.3V I/O 4 mA drive, V_{OH}=V_{DD33}-0.4V	4	—	—	mA
		3.3V I/O 8 mA drive, V_{OH}=V_{DD33}-0.4V	8	—	—	mA
		5 V-tolerant I/O 8 mA drive, V_{OH} = V_{DD33} - 0.4 V	8	—	—	mA
		5 V-tolerant I/O 12 mA drive, V_{OH} = V_{DD33} - 0.4 V	12	—	—	mA
		Backup Domain IO drive@V_{BAT}=3.3V, V_{OH} = V_{DD33} - 0.4 V, PB8, PB9, PB10.	—	—	1	mA
V_{OL}	Low level output voltage	3.3 V 4 mA drive IO, I_{OL} = 4 mA	—	—	0.4	V
		3.3 V 8 mA drive IO, I_{OL} = 8 mA	—	—	0.4	V
		5 V-tolerant 8 mA drive IO, I_{OL}=8mA	—	—	0.4	V
		5 V-tolerant 12 mA drive IO, I_{OL}=12mA	—	—	0.4	V
V_{OH}	High level output voltage	3.3 V 4 mA drive IO, I_{OH} = 4 mA	V_{DD33} - 0.4 V	—	—	V
		3.3 V 8 mA drive IO, I_{OH} = 8 mA	V_{DD33} - 0.4 V	—	—	V
		5 V-tolerant 8 mA drive IO, I_{OH}=8mA	V_{DD33} - 0.4 V	—	—	V
		5 V-tolerant 12 mA drive IO, I_{OH}=12mA	V_{DD33} - 0.4 V	—	—	V
R_{PU}	Internal pull-up resistor	3.3 V I/O	34	—	74	kΩ
		5 V-tolerant I/O	38	—	89	kΩ
R_{PD}	Internal pull-down resistor	3.3 V I/O	29	—	86	kΩ
		5 V-tolerant I/O	35	—	107	kΩ

ADC Characteristics

Table 15. ADC Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.7	3.3	3.6	V
V_{ADCIN}	A/D Converter input voltage range		0	—	V_{DDA}	V
I_{ADC}	Current consumption	V_{DDA} = 3.3 V	—	1	TBD	mA
I_{ADC_DN}	Power down current consumption	V_{DDA} = 3.3 V	—	1	10	uA
f_{ADC}	A/D Converter clock		0.7	—	14	MHz
f_S	Sampling rate		0.05	—	1	MHz
$f_{ADCCONV}$	A/D Converter conversion time		—	14	—	t_{ADC}
R_I	Input sampling switch resistance		—	—	1	kΩ
C_I	Input sampling capacitance	No pin/pad capacitance included	—	—	5	pF
t_{SU}	Startup time		—	—	1	us
N	A/D Converter Resolution		—	12	—	bits
INL	Integral Non-linearity error	f_S = 1 MHz, V_{DDA} = 3.3 V	-—	±2	±5	LSB
DNL	Differential Non-linearity error	f_S = 1 MHz, V_{DDA} = 3.3 V	—	—	±1	LSB
E_O	Offset error		—	—	±10	LSB
E_G	Gain error		—	—	±10	LSB

NOTES: 1. $t_{ADC} = 1/f_{ADC}$.

2. Guaranteed by design, not tested in production.

Operation Amplifier/Comparator Characteristics

Table 16. OPA/CMP Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.7	3.3	3.6	V
$I_{OPA/CMP}$	Typical operating current		—	230	—	uA
I_{OPA/CMP_DN}	Power down supply current	Assign registers OPAEN = 0 and EN_OPAOP = 0	—	—	0.1	uA
V_{IOS}	Input offset voltage	V_{DDA} = 3.3 V, AnOF[5:0] = '100000'	-15	—	15	mV
		V_{DDA} = 3.3 V, After calibration	-1	—	1	mV
GV	Voltage Gain		60	100		dB
U_t	Unit-Gain Bandwidth	RL=100KΩ		1,3		MHz
		RL=100KΩ, CL=100pF		1.24		
V_{CM}	Common mode voltage range	VDDA = 3.3 V	V_{SSA}	—	V_{DDA} – 0.6	V
t_{RT}	Comparator response time	VDDA = 3.3 V; Input Overdrive = ±10mV	—	1	—	us
SR	Slew Rate	VDDA = 3.3 V; Output capacitor load C_L=100pF		1.6		V/us

NOTE: Guaranteed by design, not tested in production.

GPTM Characteristics

Table 17. GPTM Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{GPTM}	Timer clock source	—	—	—	72	MHz
t_{RES}	Timer resolution time	—	1	—	—	$1/f_{GPTM}$
f_{EXT}	External signal frequency on channel 1 ~ 4	—	—	—	1/2	f_{GPTM}
RES	Timer resolution	—	—	—	16	bits

I²C Characteristics

Table 18. I²C Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	—	—	—	400	kHz
$t_{SCL(H)}$	SCL clock high time	—	600	—	—	ns
$t_{SCL(L)}$	SCL clock low time	—	1300	—	—	ns
t_{FALL}	SCL and SDA fall time	—	—	—	300	ns
t_{RISE}	SCL and SDA rise time	—	—	—	300	ns
$t_{SU(STA)}$	START condition setup time	—	600	—	—	ns
$t_{H(STA)}$	START condition hold time	—	600	—	—	ns
$t_{SU(SDA)}$	SDA data setup time	—	100	—	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0	—	—	ns
$t_{SU(STO)}$	STOP condition setup time	—	600	—	—	ns

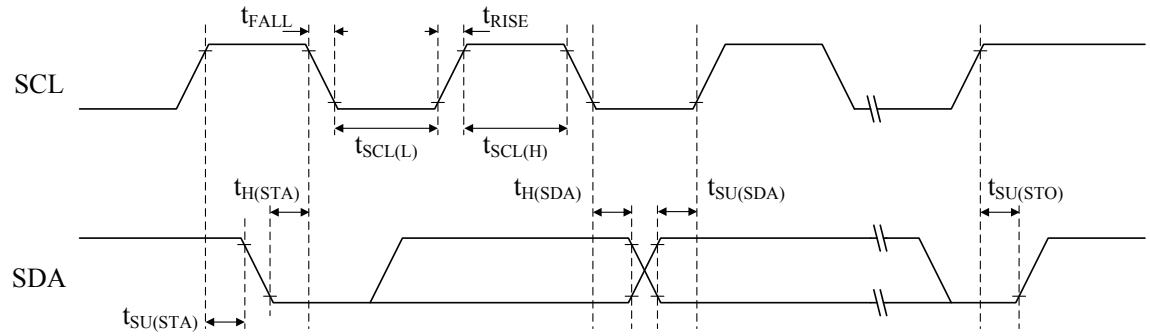


Figure 6. I²C Timing Diagram

SPI Characteristics

Table 19. SPI Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	$f_{PCLK}/4$	MHz
$t_{SCK(H)}$	SCK clock high time	—	$f_{PCLK}/8$	—	—	ns
$t_{SCK(L)}$	SCK clock low time	—	$f_{PCLK}/8$	—	—	ns
SPI Master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	5	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI Slave mode						
$t_{SU(SEL)}$	SEL enable setup time	—	4 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL enable hold time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data output disable time	—	—	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

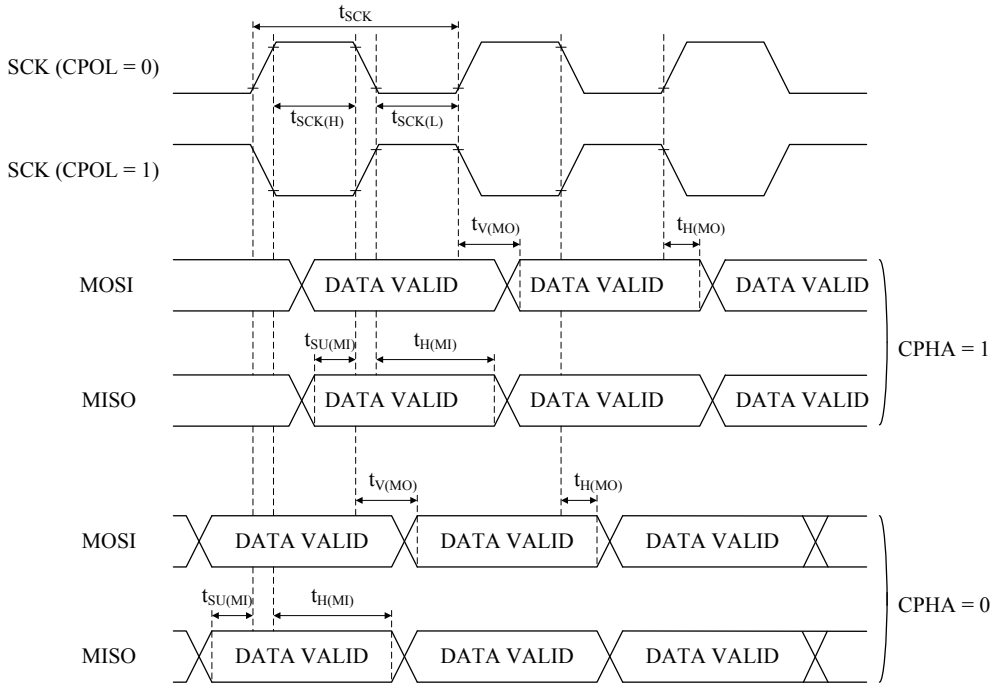


Figure 7. SPI Timing Diagram – SPI Master Mode

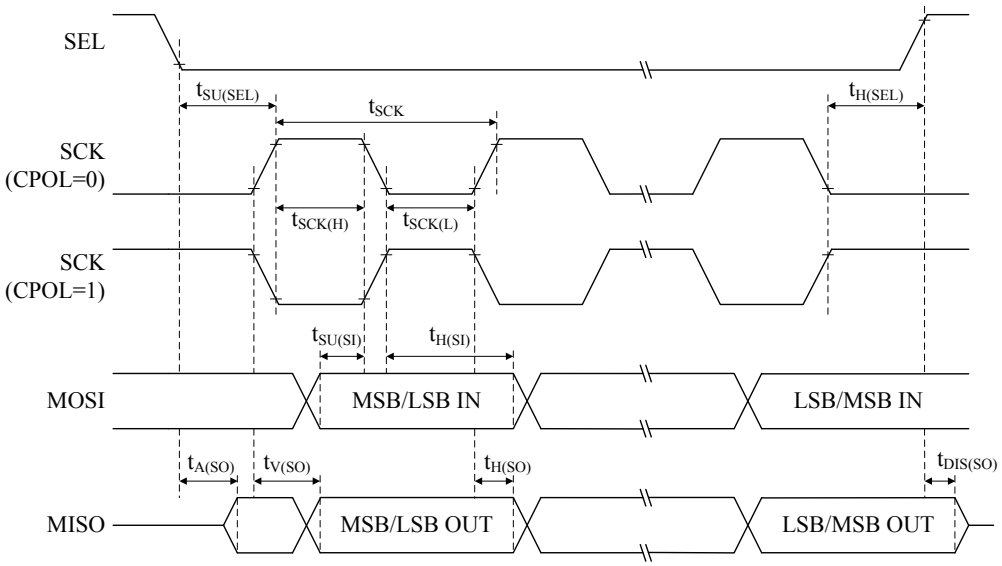
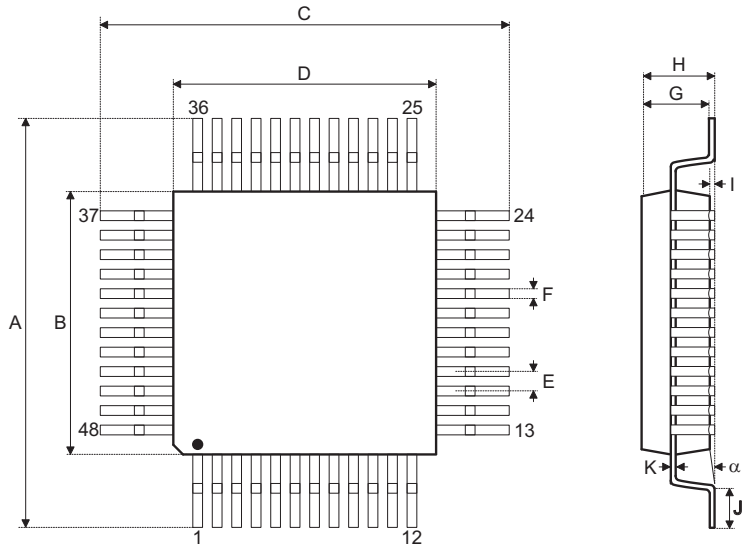


Figure 8. SPI Timing Diagram – SPI Slave Mode and CPHA=1

5 Package Information

48-pin LQFP (7mmx7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.020	—
F	—	0.008	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

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