TPS25810-Q1 具有负载检测功能的 USB Type-C DFP 控制器和电源开关

1 特性

- 兼容 USB Type-C 版本 1.2 的下行数据端口 (DFP) 控制器
- 连接器连接或断开检测
- 配置通道 (CC) STD、1.5A、3A 电流能力通告
- 超高速极性确定
- V_{BUS} 应用和放电
- V_{CONN} 应用于电子标记电缆
- 音频和调试附件识别
- 端口未连接时，I_{DDQ} 的典型值为 0.7μA
- 三个输入电源选项
  - IN1：USB 充电电源
  - IN2：V_{CONN} 电源
  - AUX：器件电源
- 电源唤醒可保证系统冬眠 (S4) 和关闭 (S5) 功耗状态下的低功耗
- 34mΩ（典型值）高侧金属氧化物半导体场效应晶体管 (MOSFET)
- 1.7A 或 3.4A 可编程 I_{LIM} (±7.1%)
- 端口功率管理可实现多端口功率资源优化
- 封装：20 引脚晶圆级四方扁平无引线 (WQFN) 封装 (3mm x 4mm) (1)

2 应用

- 汽车信息娱乐系统
- 汽车后座 USB 充电

(1) CC 引脚符合 IEC-61000-4-2 标准

3 说明

TPS25810-Q1 是一款 USB Type-C 下行数据端口 (DFP) 控制器，集成了一个额定电流为 3A 的 USB 电源开关。TPS25810-Q1 器件监测 Type-C 配置通道 (CC) 线路，确定 USB 设备何时与其相连。如果连接与上行数据端口 (UFP) 器件 相连，TPS25810-Q1 可将电源应用于 V_{BUS} 并将可选 V_{BUS} 拉电流能力通过 CC 线路传输至 UFP。如果使用以电气方式标记的电缆连接 UFP，TPS25810-Q1 器件也可以将 V_{CONN} 电源应用于电缆的 CC 引脚。TPS25810-Q1 器件还会识别何时连接了 Type-C 音频或调试附件。

TPS25810-Q1 器件在未连接器件时的电流消耗低于 0.7μA（典型值）。在未连接 UFP 时，S4 和 S5 系统电源使用 $\overline{\text{UFP}}$ 输出禁用 5V 高功率电源，从而进一步实现系统节能。在此模式下，器件能够由电压较低 (3.3V) 的辅助电源 (AUX) 供电运行，该电源通常在低功耗状态（S4 和 S5）下为系统微控制器供电。

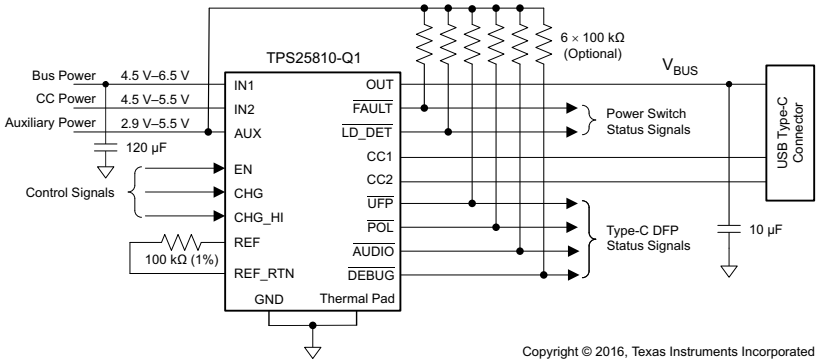
TPS25810-Q1 34mΩ 电源开关具备两种固定电流限值可供选择，对应于 Type-C 电流水平。$\overline{\text{FAULT}}$ 输出在开关处于过流和过热条件时发出信号。在所有端口无法同时提供高电流 (3A) 的环境下，$\overline{\text{LD_DET}}$ 输出可针对多个高电流 Type-C 端口的功率管理进行控制。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS25810-Q1	超薄四方扁平无引线 (WQFN) (20)	3.00mm x 4.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化电路原理图



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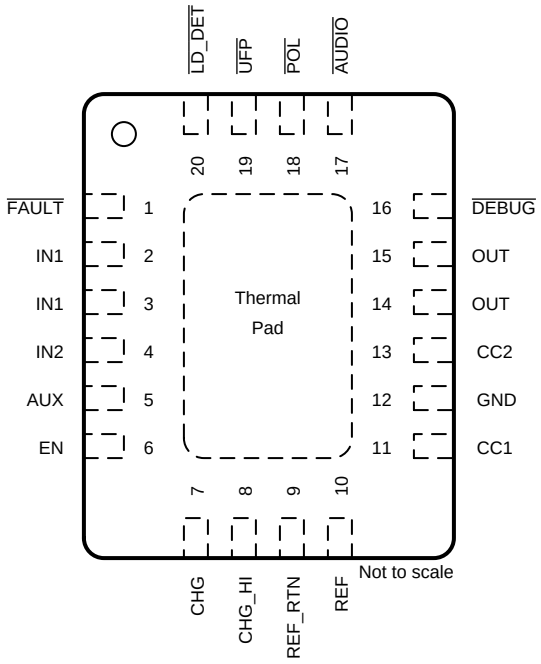
4 修订历史记录

日期	修订版本	注
2016 年 11 月	*	最初发布版本

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5 Pin Configuration and Functions

RVC Package
20-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{FAULT}}$	O	Fault event indicator. Open-drain logic output that asserts low to indicate a current-limit or thermal-shutdown event due to overtemperature.
2	IN1	I	V_{BUS} input supply. Internal power switch connects IN1 to OUT.
3	IN1	I	V_{BUS} input supply. Internal power switch connects IN1 to OUT.
4	IN2	I	V_{CONN} input supply. Internal power switch connects IN2 to CC1 or CC2. Short to IN1 if only one supply is used.
5	AUX	I	Auxiliary input supply. Connect to an always-alive system rail to use the power-wake feature. Short to IN1 and IN2 if only one supply is used.
6	EN	I	Enable logic input. Turns the device on and off
7	CHG	I	Charge-logic input to select between standard USB (500 mA for a Type-C receptacle supporting only USB 2.0, and 900 mA for Type-C receptacle supporting USB 3.1) or a Type-C current-sourcing ability.
8	CHG_HI	I	High-charge logic input to select between 1.5-A and 3-A Type-C current sourcing capability. Valid when CHG is set to Type-C current.
9	REF_RTN	I	Precision signal-reference return. Connect to the REF pin via a 100-kΩ, 1% resistor.
10	REF	I	Analog input used to generate the internal current reference. Connect a 1% or better, 100-ppm, 100-kΩ resistor between this pin and REF_RTN.
11	CC1	I/O	Analog input/output that connects to the Type-C receptacle CC1 pin
12	GND	—	Power ground
13	CC2	I/O	Analog input/output that connects to the Type-C receptacle CC2 pin.
14	OUT	O	Power switch output
15	OUT	O	Power switch output
16	$\overline{\text{DEBUG}}$	O	Open-drain logic output that asserts when a Type-C debug accessory is identified on the CC lines.
17	$\overline{\text{AUDIO}}$	O	Open-drain logic output that asserts when a Type-C audio accessory is identified on the CC lines.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
18	$\overline{\text{POL}}$	O	Polarity open-drain logic output that signals which Type-C CC pin is connected to the CC line. This gives the information needed to multiplex the super-speed lines. Asserted when the CC2 pin is connected to the CC line in the cable.
19	$\overline{\text{UFP}}$	O	Open-drain logic output that asserts when a Type-C UFP is identified on the CC lines.
20	$\overline{\text{LD_DET}}$	O	Load-detect open-drain logic output that signals when a device set to source Type-C 3-A current is sourcing over 1.95 A, nominal.
—	Thermal pad	—	Thermal pad on the bottom of the package. The thermal pad is internally connected to GND and is used to heat-sink the device to the circuit board. Connect the thermal pad to the GND plane.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, voltages are respect to GND (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage, V	IN1, IN2, AUX, EN, CHG, CHG_HI, REF, OUT, $\overline{\text{LD_DET}}$, $\overline{\text{FAULT}}$, CC1, CC2, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$	–0.3	7	V
	REF_RTN		Internally connected to GND	V
Pin positive source current, I_{SRC}	OUT, REF, CC1, CC2		Internally limited	A
Pin positive sink current, I_{SNK}	OUT (while applying V_{BUS})		5	A
	CC1, CC2 (while applying V_{CONN})		1	A
	$\overline{\text{LD_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$		Internally limited	mA
Operating junction temperature, T_J		–40	180	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per per AEC Q100-002 (2)	±2 000	V
		Charged-device model (CDM), per per AEC Q100-011	±500	
		61000-4-2 contact discharge, CC1 and CC2 (3) IEC	±8 000	
		IEC 61000-4-2 air discharge, CC1 and CC2 (3)	±15 000	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(3) Surges per IEC61000-402, 1999 applied between CC1/CC2 and output ground of the TPS25810EVM-745.

6.3 Recommended Operating Conditions

Voltages are with respect to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	IN1	4.5		6.5	V
		IN2	4.5		5.5	
		AUX	2.9		5.5	
V_I	Input voltage	EN, CHG, CHG_HI	0		5.5	V
V_{IH}	High-level input voltage	EN, CHG, CHG_HI	1.17			V
V_{IL}	Low-level voltage	EN, CHG, CHG_HI			0.63	V
V_{PU}	Pullup voltage	Used on $\overline{\text{LD_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$	0		5.5	V
I_{SRC}	Positive source current	OUT			3	A
		CC1 or CC2 when supplying VCONN			250	mA
I_{SNK}	Positive sink current (10 ms moving average)	$\overline{\text{LD_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$			10	mA
I_{SNK_PULSE}	Positive repetitive pulse sink current	$\overline{\text{LD_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$			Internally limited	mA
R_{REF}	Reference resistor		98	100	102	kΩ
T_J	Operating junction temperature		–40		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS25810-Q1 RVC (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT – POWER SWITCH						
$r_{DS(on)}$	On-resistance[1]	T_J = 25°C, I_{OUT} = 3 A		34	37	mΩ
		–40°C ≤ T_J ≤ 85°C, I_{OUT} = 3 A		34	46	
		–40°C ≤ T_J ≤ 125°C, I_{OUT} = 3 A		34	55	
I_{REV}	OUT to IN reverse leakage current	V_{OUT} = 6.5 V, V_{IN1} = V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C, I_{REV} is current out of IN1 pin		0	3	µA
OUT – CURRENT LIMIT						
I_{OS}	Short circuit current limit [1]	V_{CHG} = 0 V or V_{CHG} = V_{AUX} and V_{CHG_HI} = 0 V	1.58	1.7	1.82	A
			3.16	3.4	3.64	
		R_{REF} = 10 Ω			7	
OUT – DISCHARGE						
	Discharge resistance	V_{OUT} = 4 V, UFP signature removed from CC lines, time < t_{w_DCHG}	400	500	600	Ω
	Bleed discharge resistance	V_{OUT} = 4 V, No UFP signature on CC lines, time > t_{w_DCHG}	100	150	250	kΩ
REF						
V_O	Output voltage		0.78	0.8	0.82	V
I_{OS}	Short circuit current	R_{REF} = 10 Ω	9.5		15.3	µA
$\overline{\text{FAULT}}$						
V_{OL}	Output low voltage	$I_{\overline{FAULT}}$ = 1 mA			350	mV
I_{OFF}	Off-state leakage	$V_{\overline{FAULT}}$ = 5.5 V			1	µA
$\overline{\text{LD_DET}}$						
V_{OL}	Output low voltage	$I_{\overline{LD_DET}}$ = 1 mA			350	mV
I_{OFF}	Off-state leakage	$V_{\overline{LD_DET}}$ = 5.5 V			1	µA
I_{TH}	OUT sourcing, rising threshold current for load detect		1.8	1.95	2.1	A
	Hysteresis[2]			125		mA

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) These parameters are provided for reference only and do not constitute part of TI's published specifications for purposes of TI's product warranty.

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Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CC1, CC2 – V_{CONN} POWER SWITCH						
$r_{DS(on)}$	On-resistance	T_J = 25°C, I_{OUT} = 250 mA		365	420	mΩ
		–40°C ≤ T_J ≤ 85°C, I_{OUT} = 250 mA		365	530	
		–40°C ≤ T_J ≤ 125°C, I_{OUT} = 250 mA		365	600	
CC1, CC2 – V_{CONN} POWER SWITCH – CURRENT LIMIT						
I_{OS}	Short-circuit current limit(1)		300	355	410	mA
		R_{REF} = 10 Ω			800	
CC1, CC2 – CONNECT MANAGEMENT – DANGLING ELECTRONICALLY MARKED CABLE MODE						
I_{SRC}	Sourcing current on the pass-through CC Line	0 V ≤ V_{CCx} ≤ 1.5 V	64	80	96	µA
	Sourcing current on the Ra CC line	0 V ≤ V_{CCx} ≤ 1.5 V	64	80	96	
CC1, CC2 – CONNECT MANAGEMENT – ACCESSORY MODE						
I_{SRC}	CCx sourcing current (CC2 – audio, CC1-debug)	0 V ≤ V_{CCx} ≤ 1.5 V	64	80	96	µA
	CCx sourcing current (CC1 – audio, CC2-debug) (2)	0 V ≤ V_{CCx} ≤ 1.5 V		0		
CC1, CC2 – CONNECT MANAGEMENT – UFP MODE						
I_{SRC}	Sourcing current with either IN1 or IN2 in UVLO	0 V ≤ V_{CCx} ≤ 1.5 V V_{IN1} < $V_{TH_UVLO_IN1}$ or V_{IN2} < $V_{TH_UVLO_IN2}$	64	80	96	µA
I_{SRC}	Sourcing current	V_{CHG} = 0 V and V_{CHG_HI} = 0 V 0 V ≤ V_{CCx} ≤ 1.5 V	75	80	85	µA
		V_{CHG} = V_{AUX} and V_{CHG_HI} = 0 V 0 V ≤ V_{CCx} ≤ 1.5 V	170	180	190	
		V_{CHG} = V_{AUX} and V_{CHG_HI} = V_{AUX} 0 V ≤ V_{CCx} ≤ 2.45 V	312	330	348	
$\overline{UFP}$, $\overline{POL}$, $\overline{AUDIO}$, $\overline{DEBUG}$						
V_{OL}	Output low voltage	I_{SNK_PIN} = 1 mA			250	mV
I_{OFF}	Off-state leakage	V_{PIN} = 5.5 V			1	µA
EN, CHG, CHG_HI – LOGIC INPUTS						
V_{TH}	Rising threshold voltage			0.925	1.15	V
V_{TH}	Falling threshold voltage		0.65	0.875		V
	Hysteresis(2)			50		mV
I_{IN}	Input current	V_{EN} = 0 V or 6.5 V	–0.5		0.5	µA
OVERTEMPERATURE SHUTDOWN						
T_{TH_OTSD2}	Rising threshold temperature for device shutdown		155			°C
	Hysteresis(2)			20		°C
T_{TH_OTSD1}	Rising threshold temperature for OUT/ V_{CONN} switch shutdown in current limit		135			°C
	Hysteresis(2)			20		°C
IN1						
$V_{TH_UVLO_IN1}$	Rising threshold voltage for UVLO		3.9	4.1	4.3	V
	Hysteresis(2)			100		mV
$I_{IN1(DIS)}$	Disabled supply current	V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C			1	µA
$I_{IN1(CC_OPEN)}$	Enabled supply current with CC lines open	–40°C ≤ T_J ≤ 85°C			1	µA

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Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IN1(Ra)}$	Enabled supply current with accessory or dangling electronically marked cable signature on CC lines				2	µA
$I_{IN1(Rd)}$	Enabled supply current with UFP attached	V_{CHG} = 0 V, or V_{CHG} = V_{AUX} and V_{CHG_HI} = 0 V		75	100	µA
				85	110	
IN2						
$V_{TH_UVLO_IN2}$	Rising threshold voltage for UVLO		3.9	4.1	4.3	V
	Hysteresis(2)			100		mV
$I_{IN2(DIS)}$	Disabled supply current	V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C			1	µA
$I_{IN2(CC_OPEN)}$	Enabled supply current with CC lines open	–40°C ≤ T_J ≤ 85°C			1	µA
$I_{IN2(Ra)}$	Enabled supply current with accessory or dangling electronically marked cable signature on CC lines				2	µA
$I_{IN2(Rd)}$	Enabled supply current with UFP signature on CC lines (Includes IN current that provides the CC output current to the UFP Rd resistor)	V_{CHG} = 0 V, 0 V ≤ V_{CCx} ≤ 1.5 V		98	110	µA
		V_{CHG} = V_{IN} and V_{CHG_HI} = 0 V, 0 V ≤ V_{CCx} ≤ 1.5 V		198	215	
		0 V ≤ V_{CCx} ≤ 2.45 V		348	373	
AUX						
$V_{TH_UVLO_AUX}$	Rising threshold voltage for UVLO		2.65	2.75	2.85	V
	Hysteresis(2)			100		mV
$I_{AUX(DIS)}$	Disabled supply current	V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C			1	µA
$I_{AUX(CC_OPEN)}$	Enabled internal supply current with CC lines open	–40°C ≤ T_J ≤ 85°C		0.7	3	µA
$I_{AUX(Ra)}$	Enabled supply current with accessory or dangling active cable signature on CC lines			140	185	µA
$I_{AUX(Rd_noIN)}$	Enabled supply current with UFP termination on CC lines and with either IN1 or IN2 in UVLO	V_{IN1} < $V_{TH_UVLO_IN1}$ or V_{IN2} < $V_{TH_UVLO_IN2}$		145	190	µA
$I_{AUX(Rd)}$	Enabled supply current with UFP termination on CC lines			55	82	µA

6.6 Switching Characteristics

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT – POWER SWITCH						
t_r	Output-voltage rise time	V_{IN1} = 5 V, C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value)	1.2	1.8	2.5	ms
t_f	Output-voltage fall time		0.35	0.55	0.75	ms
t_{on}	Output-voltage turnon time	V_{IN1} = 5 V, C_L = 1 µF, R_L = 100 Ω	2.5	3.5	5	ms
t_{off}	Output-voltage turnoff time		2	3	4.5	ms
OUT – CURRENT LIMIT						
t_{ios}	Current-limit response time to short circuit	V_{IN1} – V_{OUT} = 1 V, R_L = 10 mΩ, see Figure 1		1.5	4	µs

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Switching Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN1} ≤ 6.5 V, 4.5 V ≤ V_{IN2} ≤ 5.5 V, 2.9 V ≤ V_{AUX} ≤ 5.5 V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{FAULT}}$						
t_{DEGA}	Asserting deglitch due to overcurrent		5.5	8.2	10.7	ms
$t_{DEGA(OC)}$	Asserting deglitch due to overtemperature in current limit(1)			0		ms
$t_{DEGA(OT)}$	Deasserting deglitch		5.5	8.2	10.7	ms
$\overline{\text{LD_DET}}$						
t_{DEGA}	Asserting deglitch		45	65	85	ms
t_{DEGD}	Deasserting deglitch		1.45	2.15	2.9	s
OUT – DISCHARGE						
	R_{DCHG} discharge time	V_{OUT} = 1 V, time I_{SNK_OUT} > 1 mA after UFP signature removed from CC lines	39	65	96	ms
CC1, CC2 - V_{CONN} POWER SWITCH						
t_r	Output voltage rise time	V_{IN2} = 5 V, C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value)	0.15	0.25	0.35	ms
t_f	Output voltage fall time		0.18	0.22	0.26	ms
t_{on}	Output voltage turnon time	V_{IN2} = 5 V, C_L = 1 µF, R_L = 100 Ω	1	1.5	2	ms
t_{off}	Output voltage turnoff time		0.3	0.4	0.55	ms
CC1, CC2 – V_{CONN} POWER SWITCH – CURRENT LIMIT						
t_{res}	Current limit response time to short circuit	V_{IN2} – V_{CONN} = 1 V, R = 10 mΩ, see Figure 1		1	3	µs
$\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$						
t_{DEGR}	Asserting deglitch		100	150	200	ms
t_{DEGF}	Deasserting deglitch		7.9	12.5	17.7	ms

(1) These parameters are provided for reference only and do not constitute part of TI's published specifications for purposes of TI's product warranty.

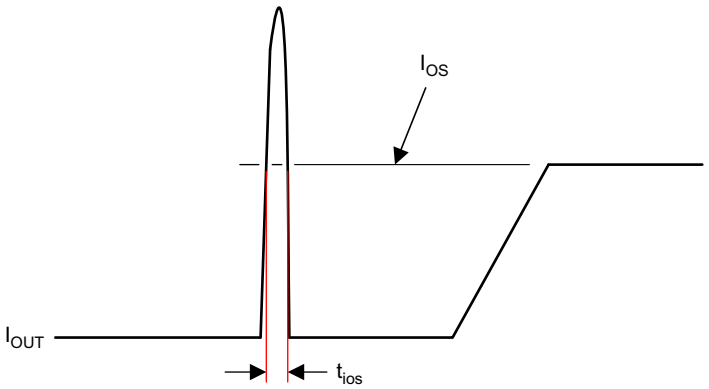


Figure 1. Output Short-Circuit Timing Diagram

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6.7 Typical Characteristics

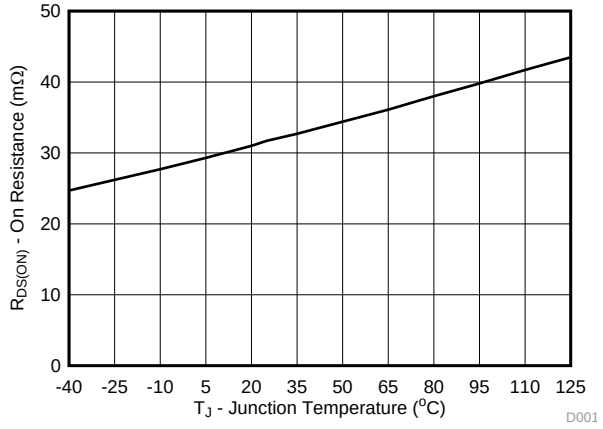


Figure 2. V_{BUS} Current-Limiting Switch On-Resistance vs Temperature

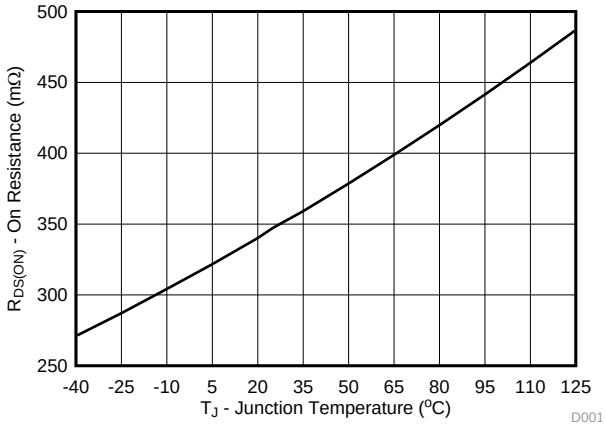
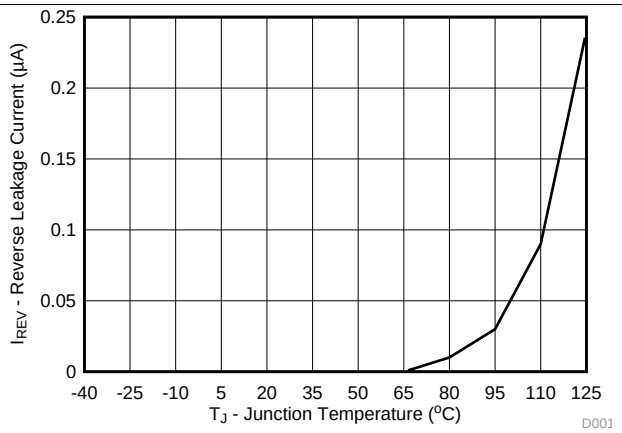


Figure 3. V_{CONN} Current-Limiting Switch On-Resistance vs Temperature



Device = Disabled; (V_{OUT} – V_{IN}) = 6. 5V

Figure 4. OUT Reverse Leakage Current vs Temperature

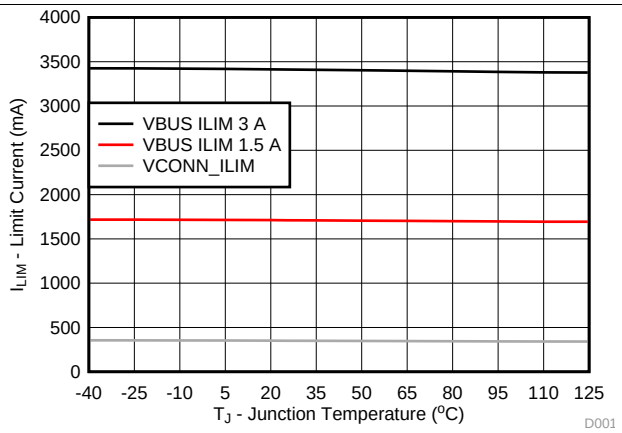


Figure 5. I_{LIM} for V_{BUS} and V_{CONN} vs Temperature

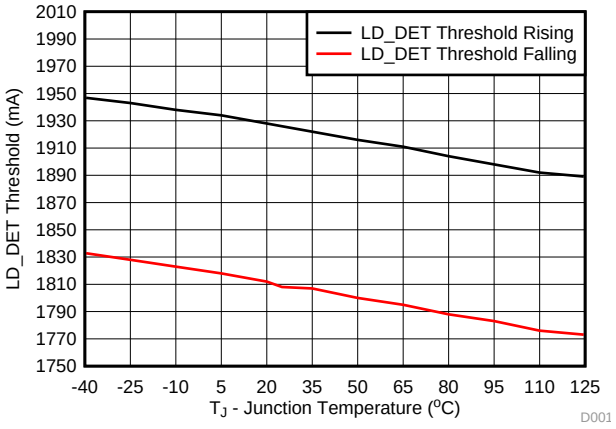


Figure 6. LD_DET Threshold vs Temperature

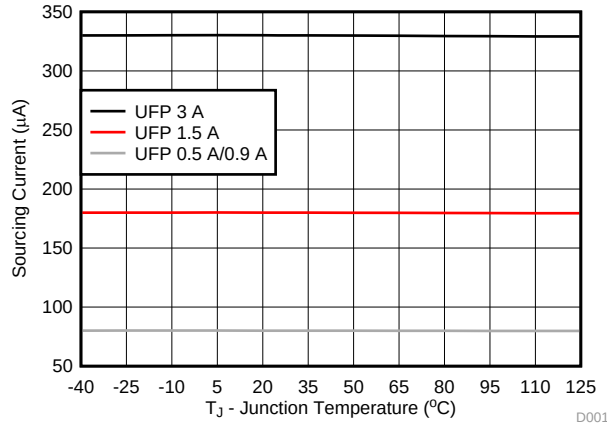


Figure 7. CC Sourcing Current to UFP vs Temperature

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Typical Characteristics (continued)

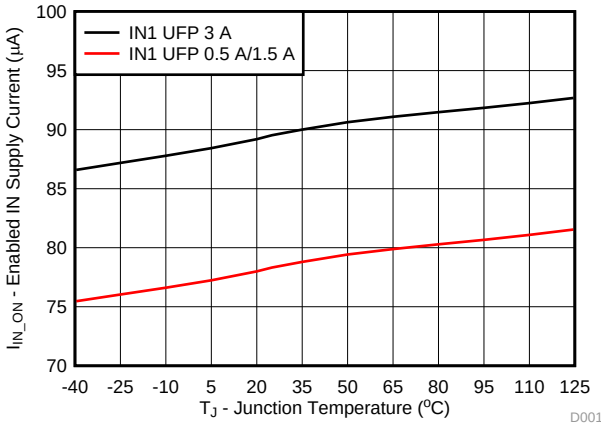


Figure 8. IN1 Current With UFP vs Temperature

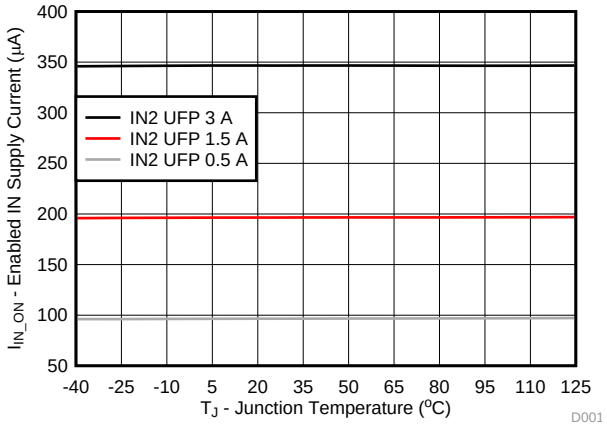
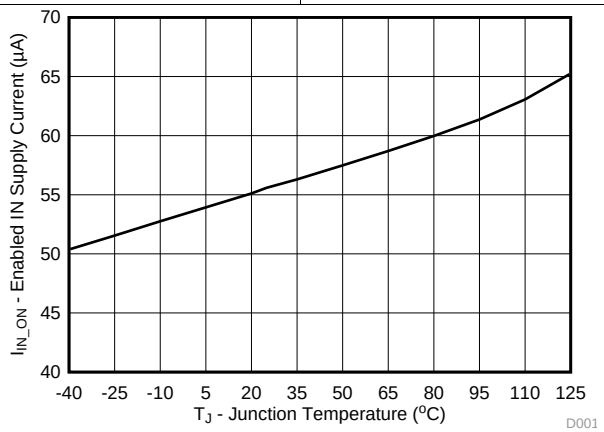


Figure 9. IN2 Current With UFP vs Temperature



V_{AUX} = 5 V

Figure 10. AUX Current With UFP vs Temperature

7 Detailed Description

7.1 Overview

The TPS25810-Q1 device is a highly integrated USB Type-C™ downstream-facing port (DFP) controller with built-in power switch developed for the new USB Type-C connector and cable. The device provides all of the functionality needed to support a USB Type-C DFP in a system where USB power delivery (PD) source capabilities (for example, V_{BUS} > 5 V) are not implemented. The device is designed to be compliant with the Type-C specification, revision 1.1.

7.1.1 USB Type-C Basic

For a detailed description of the Type-C specification, see the USB-IF Web site to download the latest released version. Some of the basic concepts of the Type-C specification that pertain to understanding the operation of the TPS25810-Q1 device (a DFP device) are described as follows.

USB Type-C removes the need for different plug and receptacle types for host and device functionality. The Type-C receptacle replaces both Type-A and Type-B receptacles because the Type-C cable is pluggable in either direction between host and device. A host-to-device logical relationship is maintained via the configuration channel (CC). Optionally, hosts and devices can be either providers or consumers of power when USB PD communication is used to swap roles.

All USB Type-C ports operate in one of the following three data modes:

- Host mode: the port can only be host (provider of power).
- Device mode: the port can only be device (consumer of power).
- Dual-role mode: the port can be either host or device.

Port types:

- DFP (downstream facing port): Host
- UFP (upstream facing port): Device
- DRP (dual-role port): Host or device

Valid DFP-to-UFP connections:

- Table 1 describes valid DFP-to-UFP connections.
- Host-to-host and device-to-device have no functions.

Table 1. DFP-to-UFP Connections

	HOST-MODE PORT	DEVICE-MODE PORT	DUAL-ROLE PORT
Host-mode port	No function	Works	Works
Device-mode port	Works	No function	Works
Dual-role port	Works	Works	Works(1)

(1) This may be automatic or manually driven.

7.1.2 Configuration Channel

The function of the configuration channel (CC) is to detect connections and configure the interface across the USB Type-C cables and connectors.

Functionally, the configuration channel serves the following purposes:

- Detect connection to the USB ports
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish DFP and UFP roles between two connected ports
- Discover and configure power: USB Type-C current modes or USB power delivery
- Discover and configure optional alternate and accessory modes
- Enhance flexibility and ease of use

Typical flow of DFP to UFP configuration is shown in Figure 11:

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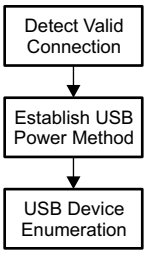


Figure 11. Flow of DFP to UFP Configuration

7.1.3 Detecting a Connection

DFPs and DRPs fulfill the role of detecting a valid connection over USB Type-C. Figure 12 shows a DFP-to-UFP connection made with Type-C cable. As shown in Figure 12, the detection concept is based on being able to detect terminations in the product that has been attached. A pullup and pulldown termination model is used. A pullup termination can be replaced by a current source.

- In the DFP-UFP connection, the DFP monitors both CC pins for a voltage lower than the unterminated voltage.
- A UFP advertises Rd on both its CC pins (CC1 and CC2).
- A powered cable advertises Ra on only one of the CC pins of the plug. Ra is used to inform the source to apply V_{CONN}.
- An analog audio device advertises Ra on both CC pins of the plug, which identifies it as an analog audio device. V_{CONN} is not applied on either CC pin in this case.

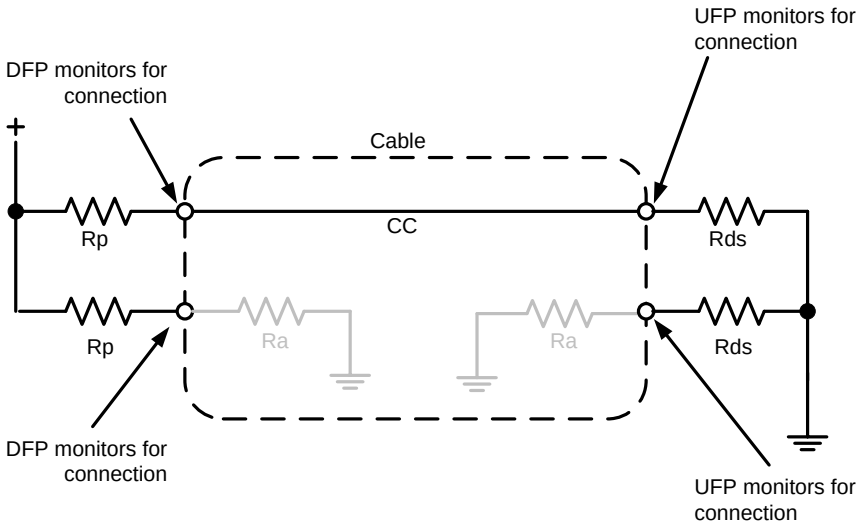
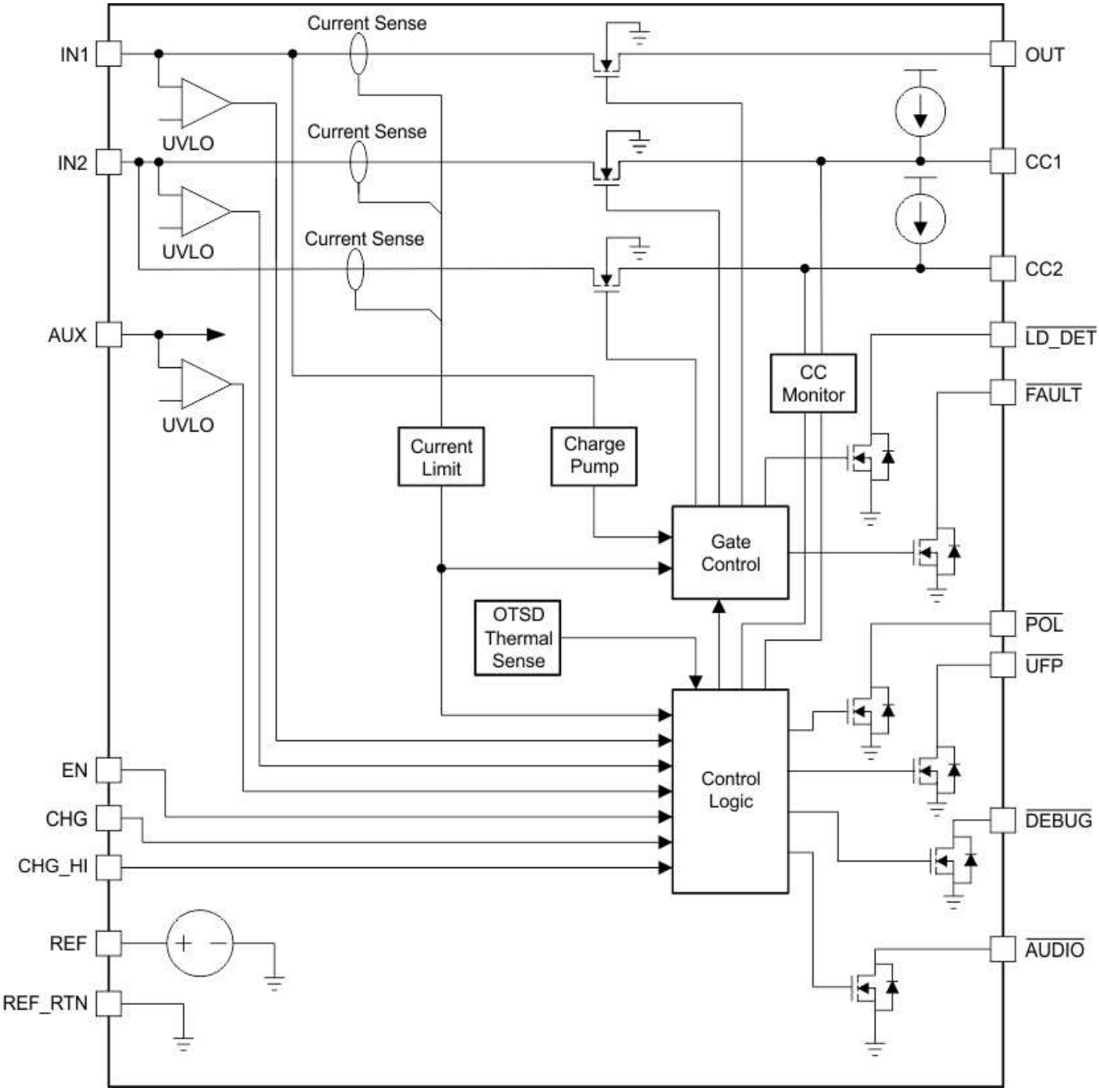


Figure 12. DFP-UFP Connection

7.2 Functional Block Diagram



7.3 Feature Description

The TPS25810-Q1 device is a DFP Type-C port controller with integrated power switches for V_{CONN} and V_{BUS}. The TPS25810-Q1 device does not support BC1.2 charging modes, because it does not interact with USB D+ and D– data lines. The TPS25810-Q1 device can be used in conjunction with a BC 1.2 device like the TPS2514A-Q1 to support BC1.2 and Type-C charging modes in a single Type-C DFP port. See the TPS25810 EVM user's guide (SLVUAI0) and *Application and Implementation* section of this data sheet for more details. The TPS25810-Q1 device can be used in a USB 2.0 only or in a USB 3.1 port implementation. When used in a USB 3.1 port, the TPS25810-Q1 device can control an external super-speed MUX to handle the Type-C flippable feature.

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Feature Description (continued)

7.3.1 Configuration Channel Pins CC1 and CC2

The TPS25810-Q1 device has two pins, CC1 and CC2, that serve to detect an attachment to the port and to resolve cable orientation. These pins are also used to establish the current broadcast to a valid UFP, configure V_{CONN}, and detect attachment of a debug or audio-adapter accessory.

Table 2 lists the TPS25810-Q1 response to various attachments to its port.

Table 2. TPS25810-Q1 Response

TPS25810-Q1 TYPE-C PORT	CC1	CC2	TPS25810-Q1 RESPONSE(1)					
			OUT	V_{CONN} on CC1 or CC2	$\overline{POL}$	$\overline{UFP}$	$\overline{AUDIO}$	$\overline{DEBUG}$
Nothing attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered cable, no UFP connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered cable, no UFP connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered cable, UFP connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered cable, UFP connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug accessory connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio-adapter accessory connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

(1) $\overline{POL}$, $\overline{UFP}$, $\overline{AUDIO}$, and $\overline{DEBUG}$ are open-drain outputs; pull high with 100 kΩ to AUX when used. Tie to GND or leave open when not used.

7.3.2 Current Capability Advertisement and Overload Protection

The TPS25810-Q1 device supports all three Type-C current advertisements as defined by the USB Type-C standard. Current broadcast to a connected UFP is controlled by the CHG and CHG_HI pins. For each broadcast level, the device protects itself from a UFP that draws current in excess of the USB Type-C current advertisement of that port by setting the current limit as shown in Table 3.

Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (TYP)	LOAD DETECT THRESHOLD (TYP)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

Under OUT overload conditions, an internal OUT current-limit regulator limits the output current to the selected I_{LIM} based on CHG and CHG_HI selection. In applications where V_{CONN} is supplied via CC1 or CC2, separate fixed current-limit regulators protect these pins from overload at the level indicated in the *Electrical Characteristics* table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (I_{OS} × R_{LOAD}). Two possible overload conditions can occur. The first overload condition occurs when either: 1) input voltage is first applied, enable is true, and a short circuit is present (load which draws I_{OUT} > I_{OS}), or 2) input voltage is present and the TPS25810-Q1 device is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the TPS25810-Q1 device ramps the output current to I_{OS}. The TPS25810-Q1 device limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in Figure 24 where the device was enabled into a short, and subsequently cycles current off and on as the thermal protection engages.

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The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within time t_{ios} (see Figure 1) when the specified overload (per *Electrical Characteristics*) is applied. The response speed and shape vary with the overload level, input circuit, and rate of application. The current-limit response varies between simply settling to I_{OS} or turnoff and controlled return to I_{OS}. Similar to the previous case, the TPS25810-Q1 device limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS25810-Q1 device thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [(V_{IN} – V_{OUT}) × I_{OS}] driving the junction temperature up. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C and then restarts. The TPS25810-Q1 current-limit profile is shown in Figure 13.

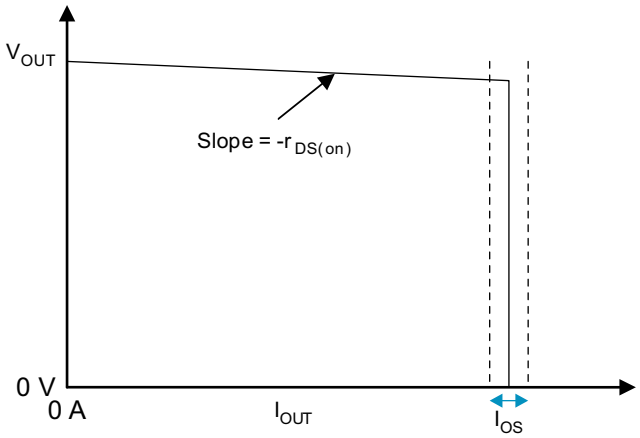


Figure 13. Current Limit Profile

7.3.3 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted on-off cycling due to input voltage droop during turnon.

7.3.3.1 Device Power Pins (IN1, IN2, AUX, OUT, and GND)

The device has multiple input power pins: IN1, IN2 and AUX. IN1 is connected to OUT by the internal power FET and serves the supply for the Type-C charging current. IN2 is the supply for V_{CONN} and ties directly between the V_{CONN} power switch on its input and CC1 or CC2 on its output. AUX, the auxiliary input supply, provides power to the device. See the *Functional Block Diagram*.

In the simplest implementation where multiple supplies are not available; IN1, IN2, and AUX can be tied together. However, in mobile systems (battery powered) where system power savings is paramount, IN1 and IN2 can be powered by the high-power dc-dc supply (>3-A capability), and AUX can be connected to the low-power supply that typically powers the system microcontroller when the system is in the hibernate or sleep power state. Unlike IN1 and IN2, AUX can operate directly from a 3.3-V supply commonly used to power the microcontroller when the system is put in low-power mode. Ceramic bypass capacitors close to the device from the INx and AUX pins to GND are recommended to alleviate bus transients.

The recommended operating voltage range for IN1 and IN2 is 4.5 V to 5.5 V, whereas AUX can be operated from 2.9 V to 5.5 V. However IN1, the high-power supply, can operate up to 6.5 V. This higher input voltage affords a larger IR loss budget in systems where a long cable harness is used, and results in high IR losses with 3-A charging current. Increasing IN1 beyond 5.5 V enables longer cable and board trace lengths between the device and the Type-C receptacle while meeting the USB specification for V_{BUS} ≥ 4.75 V at the connector.

Figure 14 illustrates the point. In this example IN1 is at 5 V, which restricts the IR loss budget from the dc-dc converter to the connector to 250 mV.

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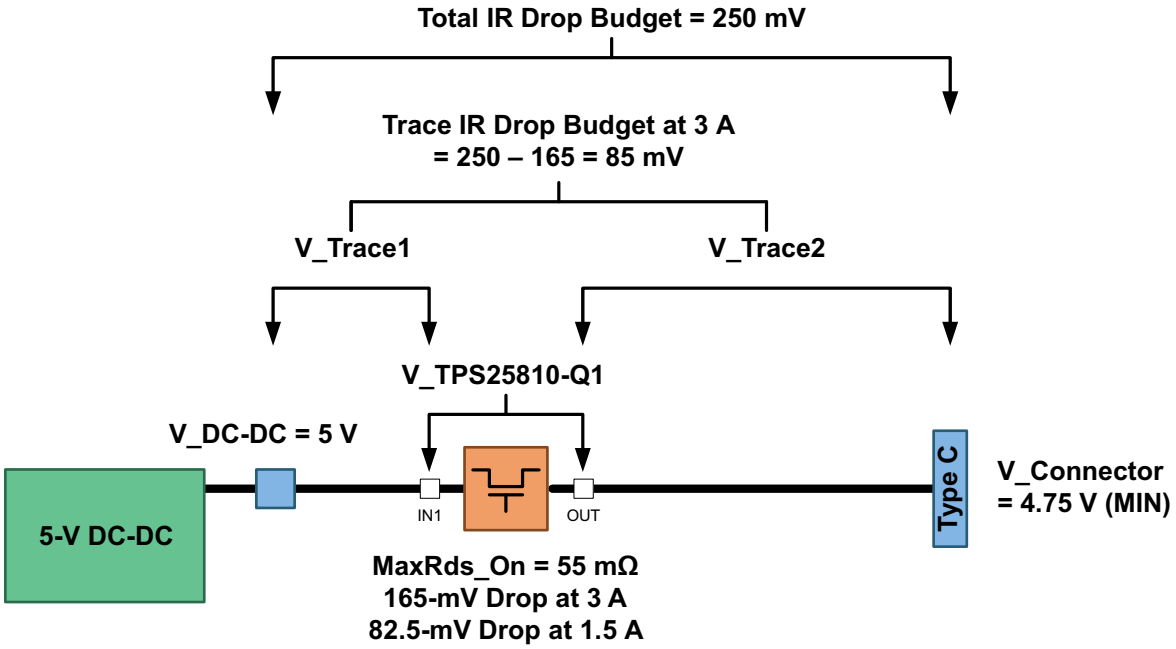


Figure 14. Total IR Loss Budget

7.3.3.2 FAULT Response

The $\overline{\text{FAULT}}$ pin is an open-drain output asserted low when the device OUT current exceeds its programmed value and the overtemperature threshold (T_{TH_OTSD1}) is crossed. See the *Electrical Characteristics* for overcurrent and overtemperature values. The $\overline{\text{FAULT}}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. The TPS25810-Q1 device is designed to eliminate false overcurrent fault reporting by using an internal deglitch circuit.

Connect $\overline{\text{FAULT}}$ with a pullup resistor to AUX. $\overline{\text{FAULT}}$ can be left open or tied to GND when not used.

7.3.3.3 Thermal Shutdown

The device has two internal overtemperature shutdown thresholds, T_{TH_OTSD1} and T_{TH_OTSD2}, to protect the internal FET from damage and assist with overall safety of the system. T_{TH_OTSD2} is greater than T_{TH_OTSD1}. $\overline{\text{FAULT}}$ is asserted low to signal a fault condition when the device temperature exceeds T_{TH_OTSD1} and the current-limit switch is disabled. However when T_{TH_OTSD2} is exceeded, all open-drain outputs are left open and the device is disabled such that minimum power and heat are dissipated. The device attempts to power up when the die temperature decreases by 20°C.

7.3.3.4 REF

A 100-kΩ (1% or better recommended) resistor is connected from this pin to REF_RTN. The REF pin sets the reference current required to bias the internal circuitry of the device. The overload current-limit tolerance and CC currents depend upon the accuracy of this resistor. Using a ±1% or better low-temperature-coefficient resistor yields the best current-limit accuracy and overall device performance.

7.3.3.5 Audio Accessory Detection

The USB Type-C specification defines an audio-adapter decode state which allows implementation of an analog USB Type-C to 3.5-mm headset adapter. The TPS25810-Q1 device detects an audio accessory device when both CC1 and CC2 pins detect V_{Ra} voltage (when pulled to ground by an Ra resistor). The device asserts the open-drain $\overline{\text{AUDIO}}$ pin low to indicate the detection of such a device.

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Table 4. Audio Accessory Detection

CC1	CC2	$\overline{\text{AUDIO}}$	STATE
Ra	Ra	Asserted (pulled low)	Audio-adapter accessory connected

Platforms supporting the audio accessory function can be triggered by the $\overline{\text{AUDIO}}$ pin to enable accessory mode circuits to support the audio function. When the Ra pulldown is removed from the CC2 pin, $\overline{\text{AUDIO}}$ is deasserted or pulled high. The TPS25810-Q1 device monitors the CC2 pin for audio device detach. When this function is not needed (for example in a data-less port), $\overline{\text{AUDIO}}$ can be tied to GND or left open.

7.3.3.6 Debug Accessory Detection

The Type-C spec supports an optional debug-accessory mode, used for debug only and not to be used for communicating with commercial products. When the TPS25810-Q1 device detects V_{Rd} voltage on both CC1 and CC2 pins (when pulled to ground by an Rd resistor), it asserts $\overline{\text{DEBUG}}$ low. With $\overline{\text{DEBUG}}$ asserted, the system can enter debug mode for factory testing or a similar functional mode. $\overline{\text{DEBUG}}$ deasserts or pulls high when Rd is removed from CC1. The TPS25810-Q1 device monitors the CC1 pin for debug-accessory detach.

If the debug-accessory mode is not used, tie $\overline{\text{DEBUG}}$ to GND or leave it open.

Table 5. Debug Accessory Detection

CC1	CC2	$\overline{\text{POL}}$	STATE
Rd	Rd	Asserted (pulled low)	Debug accessory connected

7.3.3.7 Plug Polarity Detection

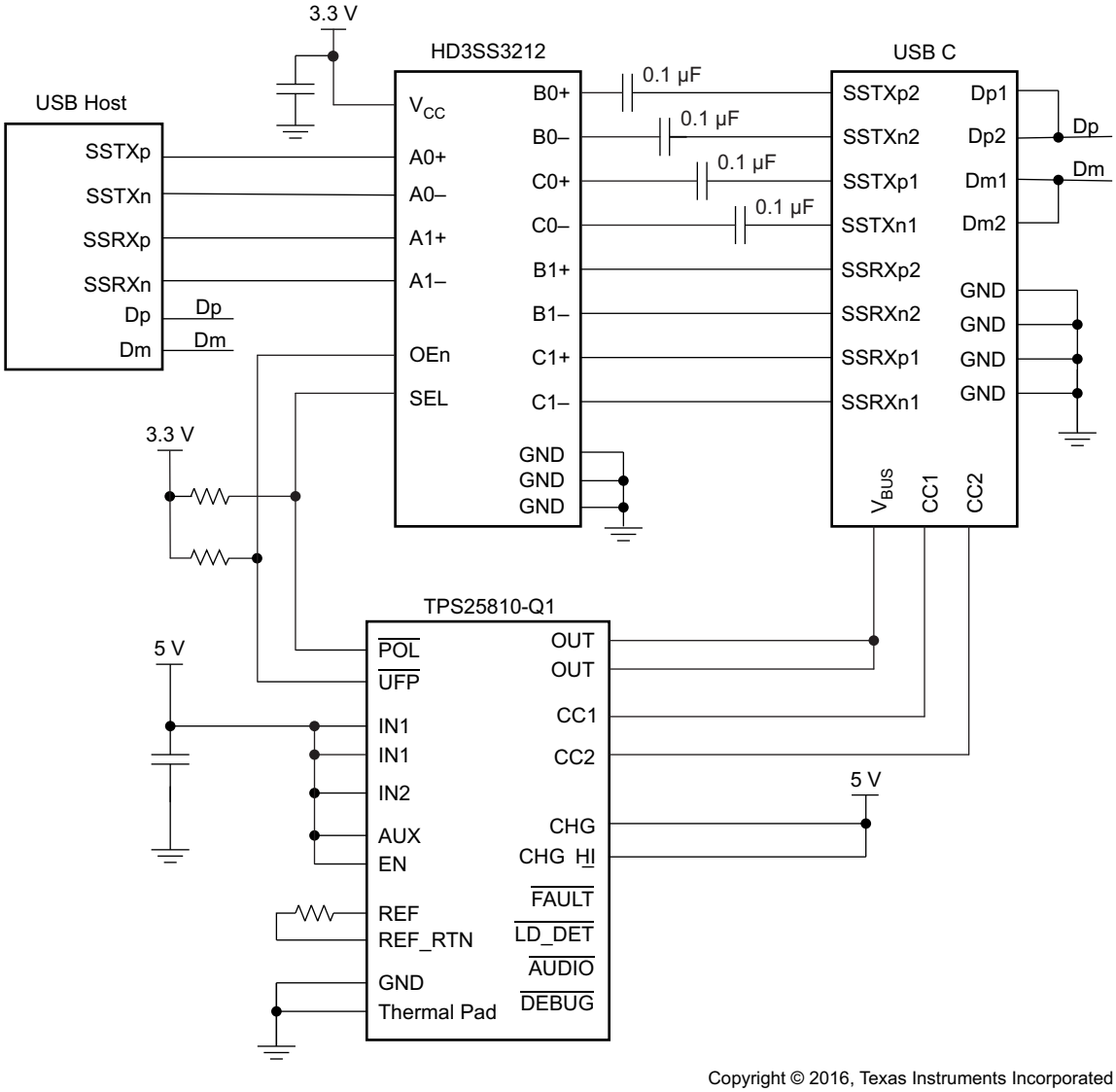
Reversible Type-C plug orientation is reported by the $\overline{\text{POL}}$ pin when a UFP is connected. However, when no UFP is attached $\overline{\text{POL}}$ remains deasserted, irrespective of cable plug orientation. Table 6 describes the $\overline{\text{POL}}$ state based on which of the device CC pins detects V_{Rd} from an attached UFP pulldown.

Table 6. Plug Polarity Detection

CC1	CC2	$\overline{\text{POL}}$	STATE
Rd	Open	Hi-Z	UFP connected
Open	Rd	Asserted (pulled low)	UFP connected with reverse plug orientation

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Figure 15 shows an example implementation which uses the $\overline{\text{POL}}$ terminal to control the SEL terminal on the HD3SS3212 device. The HD3SS3212 device provides switching on the differential channels between Port B and Port C to Port A, depending on cable orientation. For details on the HD3SS3212 device, see the HD3SS3212 data sheet (SLASE74).



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Figure 15. Example Implementation

7.3.3.8 Device Enable Control

The logic enable pin (EN) controls the power switch and device supply current. The supply current is reduced to less than 1 µA when a logic low is present on EN. The EN pin provides a convenient way to turn on or turn off the device while it is powered. The enable input threshold has built-in hysteresis. When this pin is pulled high, the device is turned on or enabled. When the device is disabled (EN pulled low) the internal FETs tied to IN1 and IN2 are disconnected, all open-drain outputs are left open (Hi-Z), and the monitor block for CC1 and CC2 is turned off. The EN terminal should not be left floating.

7.3.3.9 Load Detect

The load-detect function in the device is enabled when the device is set to broadcast high-current V_{BUS} charging (CHG = CHG_HI = High) on the CC pin. In this mode, the device monitors the OUT current to a UFP; if the current exceeds 1.95 A (typ), the $\overline{\text{LD_DET}}$ pin asserts. Because $\overline{\text{LD_DET}}$ is an open-drain output, pull it high with 100 kΩ to AUX when used; tie it to GND or leave it open when not used.

7.3.3.10 Power Wake

The power-wake feature supported in the TPS25810-Q1 device offers the mobile-systems designer a way to save on system power when no UFP is attached to the Type-C port. See Figure 16. To enable power wake, the $\overline{\text{UFP}}$ pins from device No. 1 and No. 2 are tied together (each with its own 100-kΩ pullup) to the enable pin of a 5-V, 6-A dc-dc buck converter. When no UFP is detected on both Type-C ports, the EN pin of the dc-dc converter is pulled high, thereby disabling it. Because both TPS25810-Q1 devices are powered by an always-on 3.3-V LDO, turning off the supply to IN1 and IN2 does not affect its operation in detach state. Anytime a UFP is detected on either port, the corresponding TPS25810-Q1 $\overline{\text{UFP}}$ pin is pulled low, enabling the dc-dc converter to provide charging current to the attached UFP. Turning off the high-power dc-dc converter when ports are unattached saves on system power. This method can save a significant amount of power, because the TPS25810-Q1 device only requires < 5 µA when no UFP device is connected.

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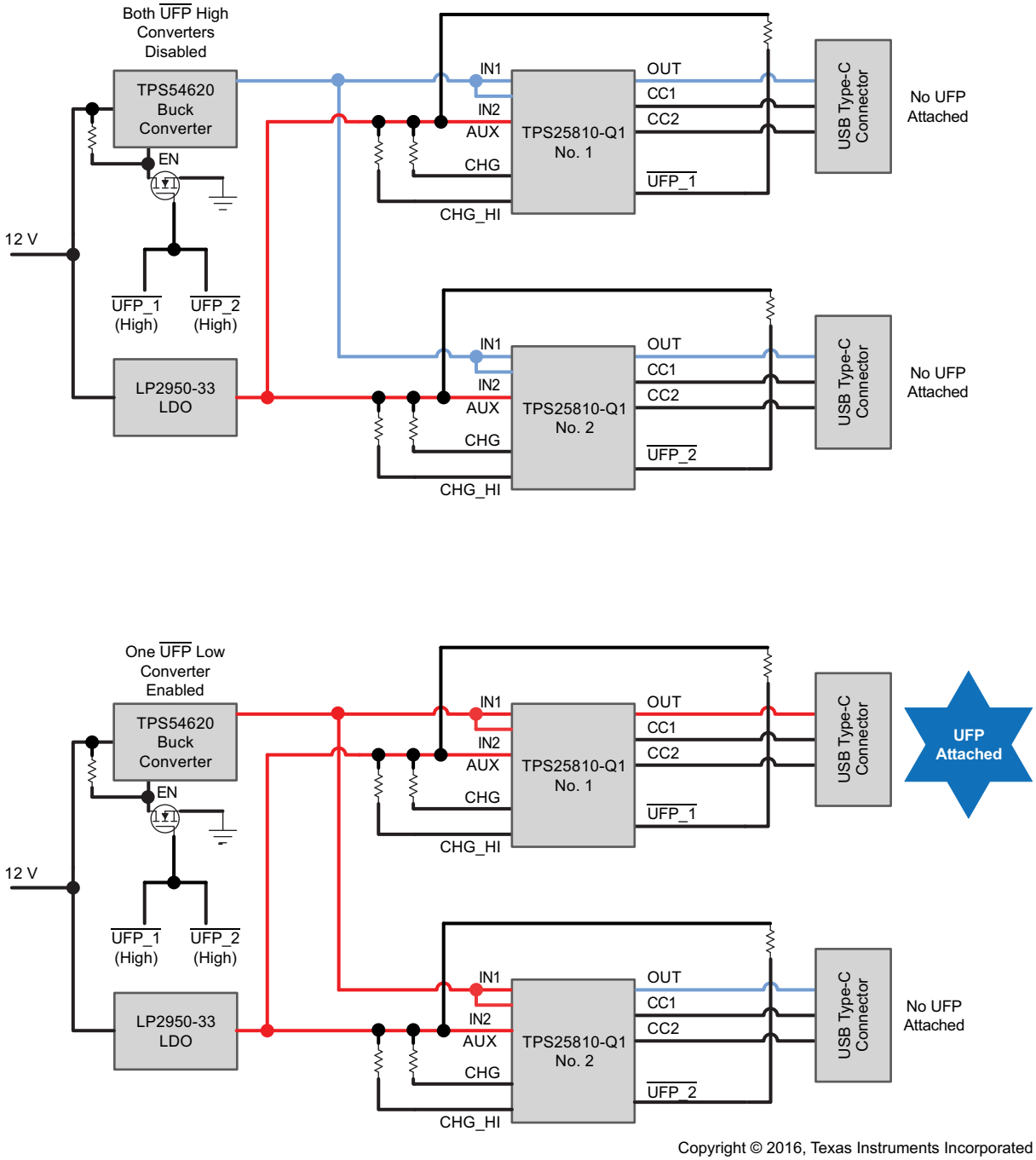


Figure 16. Power-Wake Implementation

7.3.3.11 Port Power Management (PPM)

PPM is the intelligent and dynamic allocation of power made possible with the use of the $\overline{\text{LD_DET}}$ pin. PPM is for systems that have multiple charging ports but cannot power them all at their maximum charging current simultaneously.

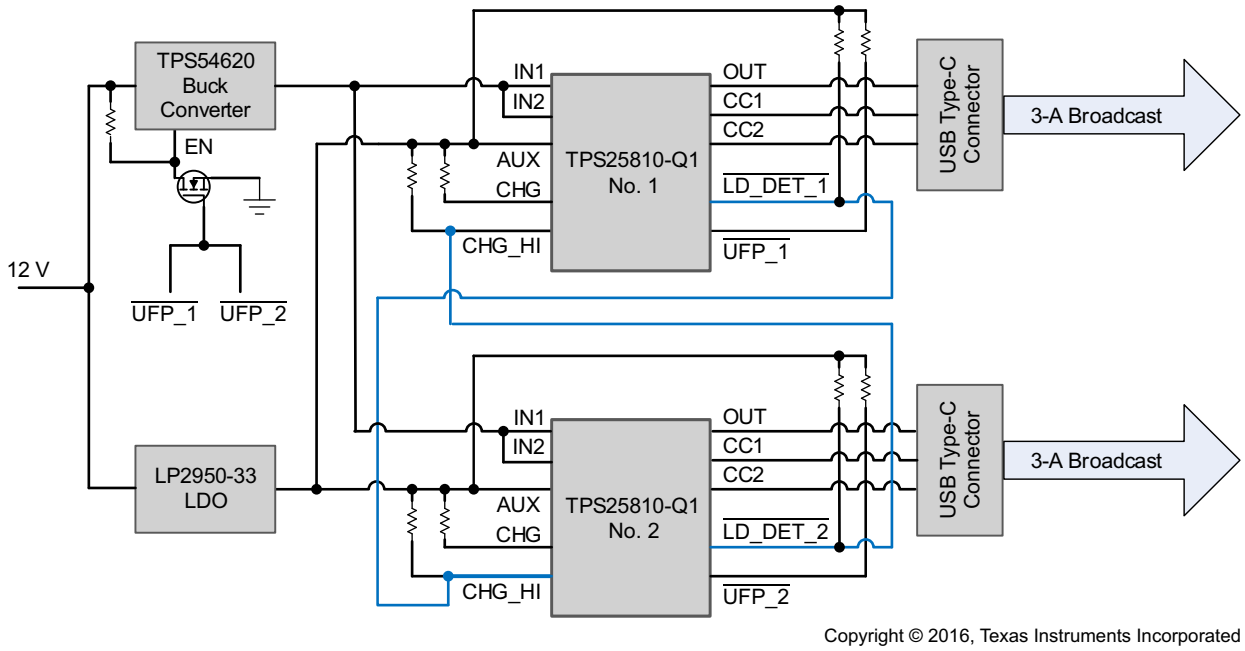
Goals of PPM are:

- Enhanced user experience, because the user needs not to search for a high-current charging port.
- Lowered cost and size of the power supply needed for implementing high-current charging in a multiport system.

7.3.3.12 Implementing PPM in a System With Two Type-C Ports

Figure 17 shows PPM and power wake implemented in a system with two Type-C ports, both initially set to broadcast high-current charging (3 A, CHG and CHG_HI pulled high via 100-kΩ resistors to AUX). To enable PPM, tie the LD_DET pin from TPS25810-Q1 device No. 1 to CHG_HI of TPS25810-Q1 device No. 2 and vice versa, as shown in Figure 17. Each device independently monitors the charging current drawn by its attached UFP.

IN1 and IN2 are connected to a TPS54620, a 6-A synchronous step-down converter. AUX is powered by an LP2950-33, a low-quiescent-current 3.3-V LDO. With no UFP attached to either Type-C port, the TPS25810-Q1 device is powered by the LP2950-33. This method saves a significant amount of power, because the TPS25810-Q1 device requires less than 2 µA when no USB device is connected.



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Figure 17. PPM and Power Wake Implemented

7.3.3.13 PPM Operation

When no UFP is attached, or either of the two attached UFPs is drawing current less than the LD_DET threshold (1.95 A typical), the LD_DET output for both devices is high (shown in blue in Figure 18). Now when a UFP is attached to device No. 1 that draws a charging current higher than the LD_DET threshold (1.95 A), this causes LD_DET to assert or pull low (shown in red in Figure 18). Because the LD-DET pins of the No. 1 and No. 2 devices are connected to the CHG_HI pins of each other, a high-current detection on device No. 1 forces device No. 2 to broadcast 1.5 A or medium charging-current capability on its CC pin. The Type-C specification requires a UFP to monitor the CC pins continuously and adjust its current consumption (within 60 ms) to remain within the value advertised by the DFP.

Figure 19 shows the case when a UFP attached to device No. 1 reduces its charging current below the LD_DET threshold, which causes LD-DET to de-assert, thereby toggling the device No. 2 CH_HI pin from low to high.

This scheme:

- Delivers a better user experience, as the user has no worry about the maximum charging current rating of the host ports. Both ports initially advertise high-current charging.
- Enables a smaller and lower-cost power supply, as the loading is controlled and never allowed to exceed 5 A.

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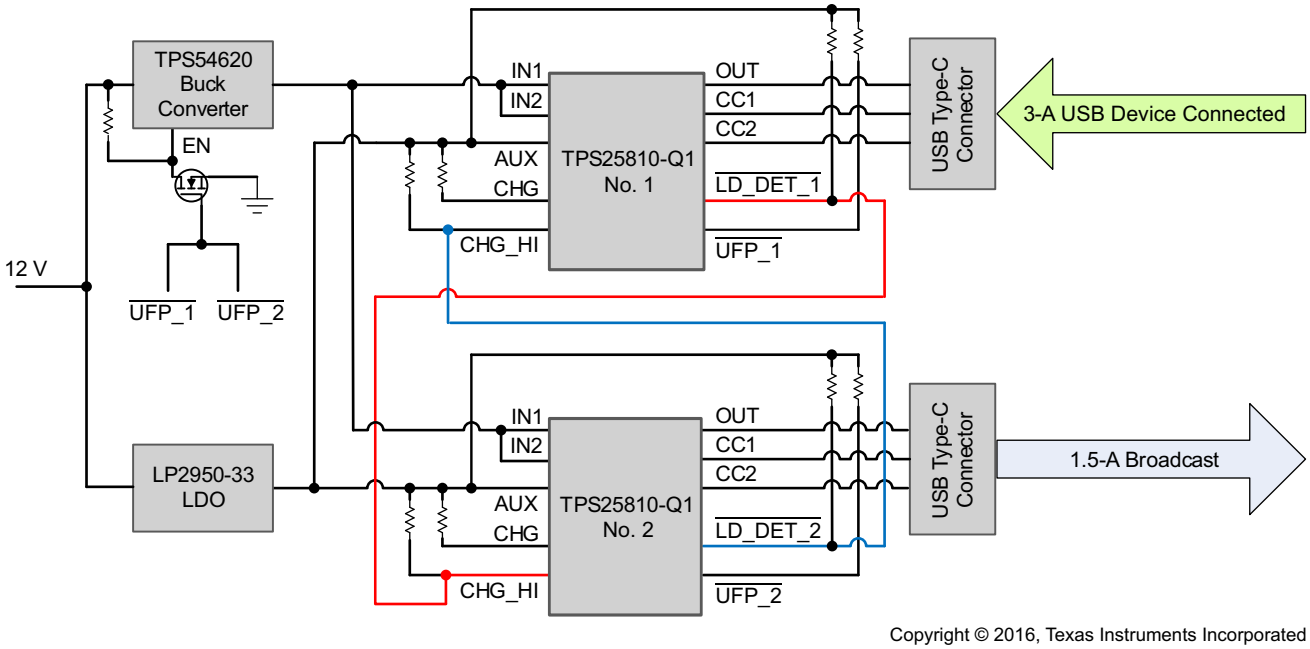


Figure 18. 3-A USB Device Connected

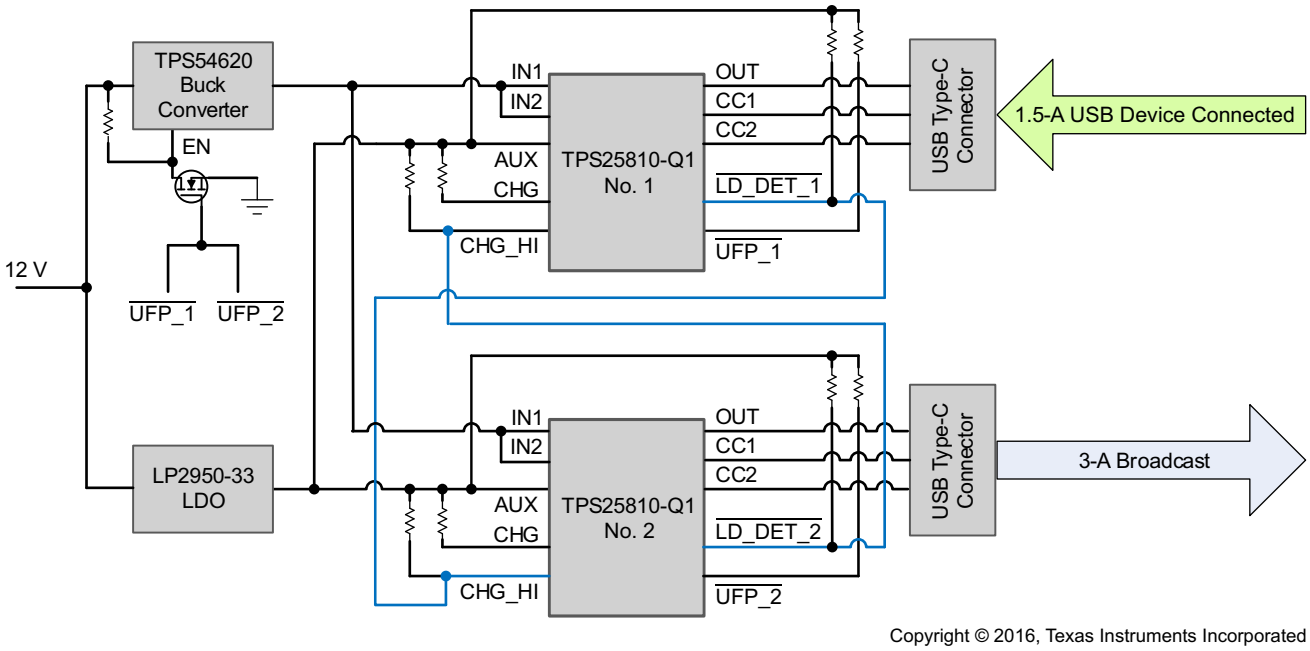


Figure 19. 1.5-A USB Device Connected

7.4 Device Functional Modes

The TPS25810-Q1 device is a Type-C controller with integrated power switch that supports all Type-C functions in a downstream facing port. The device is also used to manage current advertisement and protection for a connected UFP and active cable. The device starts its operation by monitoring the AUX bus. When V_{AUX} exceeds the undervoltage-lockout threshold, the device samples the EN pin. A high level on this pin enables the device, and normal operation begins. Having successfully completed its start-up sequence, the device now actively

Device Functional Modes (continued)

monitors its CC1 and CC2 pins for attachment to a UFP. When a UFP is detected on either the CC1 or CC2 pin, the internal MOSFET starts to turn on after the required debounce time is met. The internal MOSFET starts conducting and allows current to flow from IN1 to OUT. If Ra is detected on the other CC pin (not connected to the UFP), V_{CONN} is applied to allow current to flow from IN2 to the CC pin connected to Ra. For a complete listing of various device operational modes, see Table 2.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS25810-Q1 device is a Type-C DFP controller that supports all Type-C DFP required functions. The TPS25810-Q1 device only applies power to V_{BUS} when it detects that a UFP is attached and removes power when it detects the UFP is detached. The device exposes its identity via its CC pin, advertising its current capability based on CHG and CHG_HI pin settings. The TPS25810-Q1 device also limits its advertised current internally and provides robust protection to a fault on the system V_{BUS} power rail.

After a connection is established by the TPS25810-Q1 device, the device is capable of providing V_{CONN} to power circuits in the cable plug on the CC pin that is not connected to the CC wire in the cable. V_{CONN} is internally current limited and has its own supply pin IN2. Apart from providing charging current to a UFP, the TPS25810-Q1 device also supports audio and debug accessory modes.

The following design procedure can be used to implement a full-featured Type-C DFP.

NOTE

BC 1.2 is not supported in the TPS25810-Q1 device. To support BC1.2 with Type-C charging modes in a single Type-C connector, a device like a TPS2514A-Q1 must be used.

8.2 Typical Applications

8.2.1 Type-C DFP Port Implementation Without BC 1.2 Support

Figure 20 shows a minimal Type-C DFP implementation capable of supporting 5-V and 3-A charging.

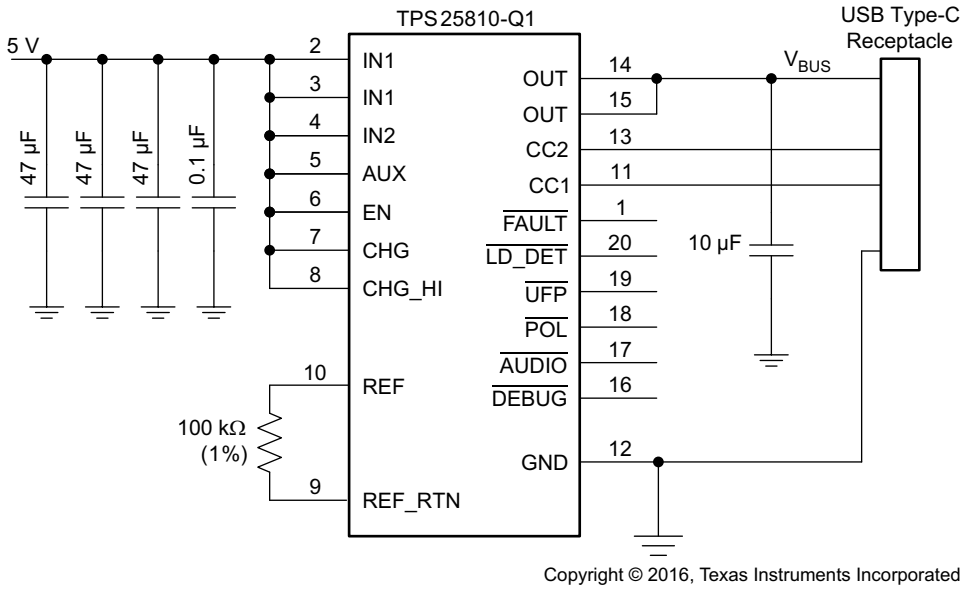


Figure 20. Type-C DFP Port Implementation Without BC 1.2 Support

Typical Applications (continued)

8.2.1.1 Design Requirements

8.2.1.1.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device. The actual capacitance should be optimized for the particular application. For all applications, a 0.1-μF or greater ceramic bypass capacitor between INx and GND is recommended as close to the device as possible for local noise decoupling.

All protection circuits, such as the TPS25810-Q1 device, have the potential for input voltage overshoots and output voltage undershoots. Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power-bus inductance and input capacitance when the INx pin is high-impedance (before turnon). Theoretically, the peak voltage is 2 times the applied voltage. The second cause is due to the abrupt reduction of output short-circuit current when the TPS25810-Q1 device turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPS25810-Q1 output is shorted. Applications with large input inductance (for instance, connecting the evaluation board to the bench power supply through long cables) may require large input capacitance to prevent the voltage overshoot from exceeding the absolute maximum voltage of the device.

The fast current-limit speed of the TPS25810-Q1 device to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1 μF to 22 μF adjacent to the TPS25810-Q1 input aids in both response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted. Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS25810-Q1 device has abruptly reduced the OUT current. Energy stored in the inductance drives the OUT voltage down, and potentially negative, as it discharges. An application with large output inductance (such as from a cable) benefits from the use of a high-value output capacitor to control voltage undershoot.

When implementing a USB-standard application, 120-μF minimum output capacitance is required. Typically, a 150-μF electrolytic capacitor is used, which is sufficient to control voltage undershoots. Because in Type-C applications, DFP is a cold socket when no UFP is attached, the output capacitance should be placed at the INx pin versus the OUT pin, as is done in USB Type-A ports. It is also recommended to put a 10-μF ceramic capacitor on the OUT pin for better voltage bypass.

8.2.1.2 Detailed Design Procedure

The TPS25810-Q1 device supports up to three different input voltages, based on the application. In the simplest implementation, all input pins are tied to a single voltage source set to 5 V, as shown in Figure 20. However, it is recommended to set a slightly higher (100 mV to 200 mV) input voltage, when possible, to compensate for IR loss from the source to the Type-C connector.

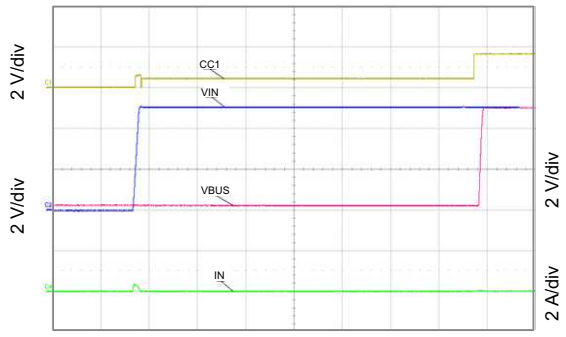
Other design considerations are listed as follows:

- Place at least 120 μF of bypass capacitance close to the INx pins versus the OUT pin, as Type-C is a cold-socket connector.
- A 10-μF bypass capacitor is recommended to be placed near a Type-C receptacle V_{BUS} pin to handle load transients.
- Depending on the maximum current-level advertisement supported by the Type-C port in the system, set the CHG and CHG_HI levels accordingly. Advertisement of 3 A is shown in Figure 20.
- EN, CHG, and CHG_HI pins can be tied directly to GND or V_{AUX} without a pullup resistor.
  - CHG and CHG_HI can also be dynamically controlled by a microcontroller to change the current advertisement level to the UFP.
- When an open-drain output of the TPS25810-Q1 device is not used, it can be left open or tied to GND.
- Use a 1% 100-kΩ resistor to connect between the REF and REF_RTN pins, placing it close to the device pin and isolated from switching noise on the board.

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Typical Applications (continued)

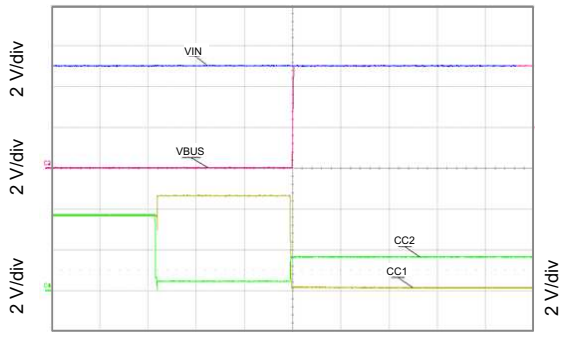
8.2.1.3 Application Curves



Time 20 ms/div

Basic start-up: IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = Rd, CC2 = open

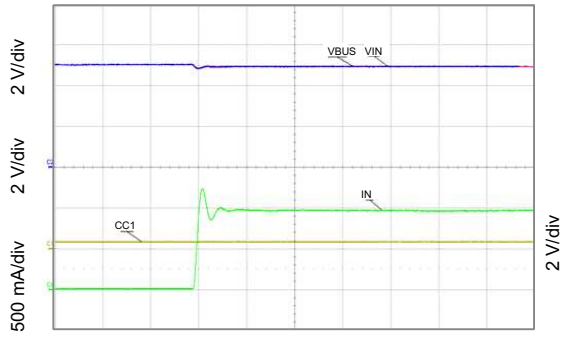
Figure 21. Basic Start-Up



Time 50 ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = open, CC2 = open → Rd

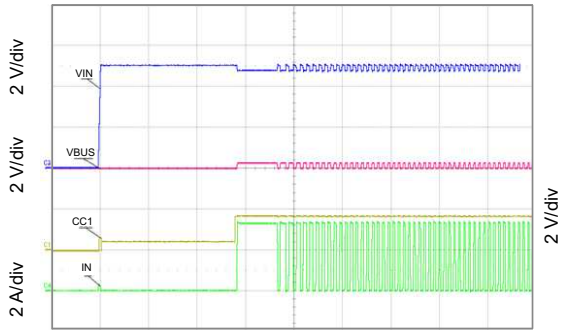
Figure 22. Start-Up



Time 200 µs/div

IN1 = IN2 = AUX = EN = 5 V; CHG = CHG_HI = 0 V, CC1 = open, CC2 = Rd, OUT = open → 5 Ω

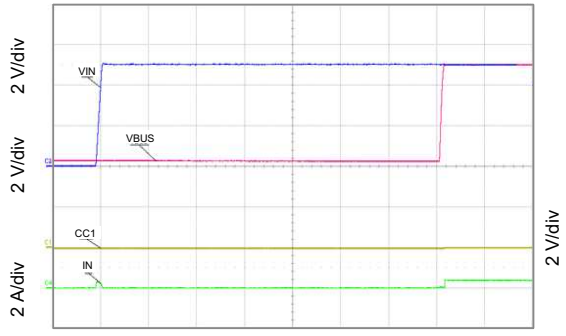
Figure 23. Load Step



Time 50 ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = Rd, CC2 = open, OUT = shorted

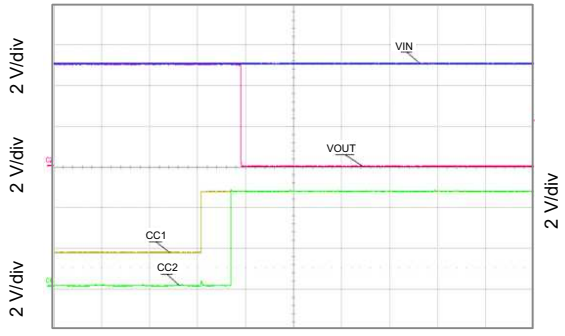
Figure 24. Hot-Plug to Short



Time 20 ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = short, CC2 = Rd

Figure 25. Short On CC1



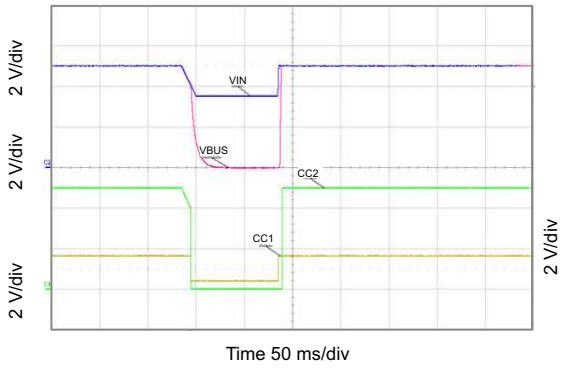
Time 20 ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V, CC1 = Rd → open, CC2 = open

Figure 26. Remove Rd

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Typical Applications (continued)



V_{IN} 5 V → 3.5 V (100 ms) → 5 V (1 V/ms),
IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5 V,
CC1 = Rd, CC2 = Ra

Figure 27. Brown-Out Test

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Typical Applications (continued)

8.2.2 Type-C DFP Port Implementation With BC 1.2 (DCP Mode) Support

Figure 28 shows a Type-C DFP implementation capable of supporting 5-V, 3-A charging in a Type-C port that is also able to support charging of legacy devices when used with a Type-C µB cable assembly for charging phones and handheld devices equipped with a µB connector.

This implementation requires the use of a TPS2514A-Q1, a USB dedicated charging-port (DCP) controller with auto-detect feature to charge not only BC1.2 compliant handheld devices but also popular phones and tablets that incorporate their own propriety charging algorithm. See the TPS2514A-Q1 datasheet for more details.

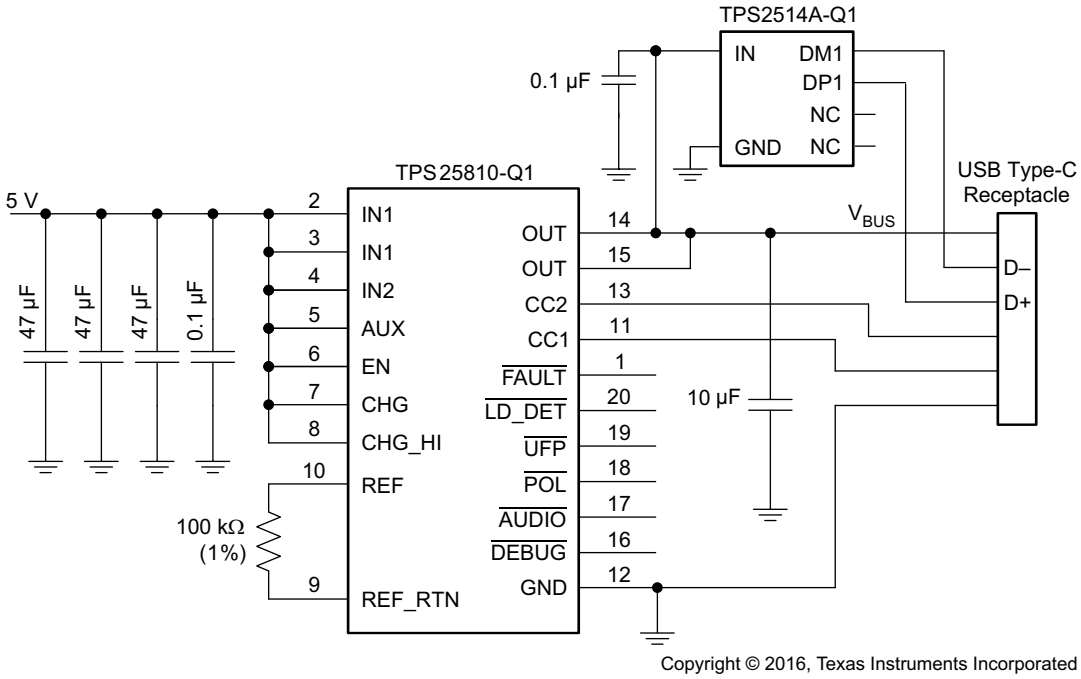


Figure 28. Type-C DFP Port Implementation With BC 1.2 (DCP Mode) Support

8.2.2.1 Design Requirements

See *Design Requirements* for the design requirements.

8.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure* for the detailed design procedure.

8.2.2.3 Application Curves

See *Application Curves* for the application curves.

9 Power Supply Recommendations

The device has three power supply inputs. IN1, which is directly connected to OUT via the power MOSFET, is tied to the V_{BUS} pin in the Type-C receptacle. IN2 also has a current-limiting switch and is multiplexed either to the CC1 or CC2 pin in the Type-C receptacle, depending on cable plug polarity. AUX is the device supply. In most applications, all three supplies are tied together. In a special implementation like power wake, IN1 and IN2 are tied to a single supply, whereas AUX is powered by a supply that is always ON and can be as low as 2.9 V.

USB Specification Revisions 2.0 and 3.1 require V_{BUS} voltage at the connector to be between 4.75 V and 5.5 V. Depending on layout and routing from the supply to the connector, the voltage drop on V_{BUS} must be tightly controlled. Locate the input supply close to the device. For all applications, a 10-μF or greater ceramic bypass capacitor between OUT and GND is recommended, located as close to the Type-C connector of the device as possible for local noise decoupling. The power supply should be rated higher than the current limit setting to avoid voltage droops during overcurrent and short-circuit conditions.

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10 Layout

10.1 Layout Guidelines

Layout best practices as they apply to the TPS25810-Q1 device are listed as follows.

- For all applications, a 10-µF ceramic capacitor is recommended near the Type-C receptacle and another 120-µF ceramic capacitor close to the IN1 pin.
  - The optimum placement of the 120-µF capacitor is closest to the IN1 and GND pins of the device.
  - Care must be taken to minimize the loop area formed by the bypass capacitor connection, the IN1 pin, and the GND pin of the IC. See Figure 29 for a PCB layout example.
- High-current-carrying power-path connections to the device should be as short as possible and should be sized to carry at least twice the full-load current.
  - Have the input and output traces as short as possible. The most common cause of voltage loss failure in USB power delivery is the resistance associated with the V_{BUS} trace. Trace length, maximum current being supplied for normal operation, and total resistance associated with the V_{BUS} trace must be taken into account while budgeting for voltage loss.
  - For example, a power-carrying trace that supplies 3 A, at a distance of 20 inches, 0.1-in. wide, with 2-oz. copper on the outer layer has a total resistance of approximately 0.046 Ω and voltage loss of 0.14 V. The same trace at 0.05 in. wide has a total resistance of approximately 0.09 Ω and voltage loss of 0.28 V.
  - Make power traces as wide as possible.
- The resistor attached to the REF pin of the device has several requirements:
  - It is recommended to use a 1% 100-kΩ low-temperature-cocoefficient resistor.
  - It should be connected to the REF and REF_RTN pins (pins 9 and pin 10, respectively).
  - The REF_RTN pin should be isolated from the GND plane. See Figure 29.
  - The trace routing between the REF and REF_RTN pins of the device should be as short as possible to reduce parasitic effects on current-limit and current-advertisement accuracy. These traces should not have any coupling to switching signals on the board.
- Locate all TPS25810-Q1 pullup resistors for open-drain outputs close to their connection pin. Pullup resistors should be 100 kΩ.
  - When a particular open-drain output is not used or needed in the system, leave the associated pin open or tied to GND.
- Keep the CC lines close to the same length.
- Thermal considerations:
  - When properly mounted, the thermal-pad package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the thermal pad must be soldered to the board GND plane directly under the device. The thermal pad is at GND potential and can be connected using multiple vias to inner-layer GND. Other planes, such as the bottom side of the circuit board, can be used to increase heat sinking in higher-current applications. See the *PowerPad™ Thermally Enhanced Package* technical report (SLMA002) and *PowerPAD™ Made Easy* application brief (SLMA004) for more information on using this thermal pad package.
  - The thermal via land pattern specific to the TPS25810-Q1 device can be downloaded from the device Web page at www.ti.com.
  - Obtaining acceptable performance with alternate layout schemes is possible; however, the layout example in the following section has been shown to produce good results and is intended as a guideline.
- ESD considerations:
  - The TPS25810-Q1 device has built-in ESD protection for CC1 and CC2. Keep trace length to a minimum from the Type-C receptacle to the TPS25810-Q1 device on CC1 and CC2.
  - A 10-µF output capacitor should be placed near the Type-C receptacle.
  - See the TPS25810EVM-745 evaluation module for an example of a double-layer board that passes IEC61000-4-2 testing.
  - Do not create stubs or test points on the CC lines. Keep the traces short if possible, and use minimal vias along the traces (1–2 inches or less).
  - See the *ESD Protection Layout Guide* application report (SLVA680) for additional information.
  - Have a dedicated ground plane layer, if possible, to avoid differential voltage buildup.

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10.2 Layout Example

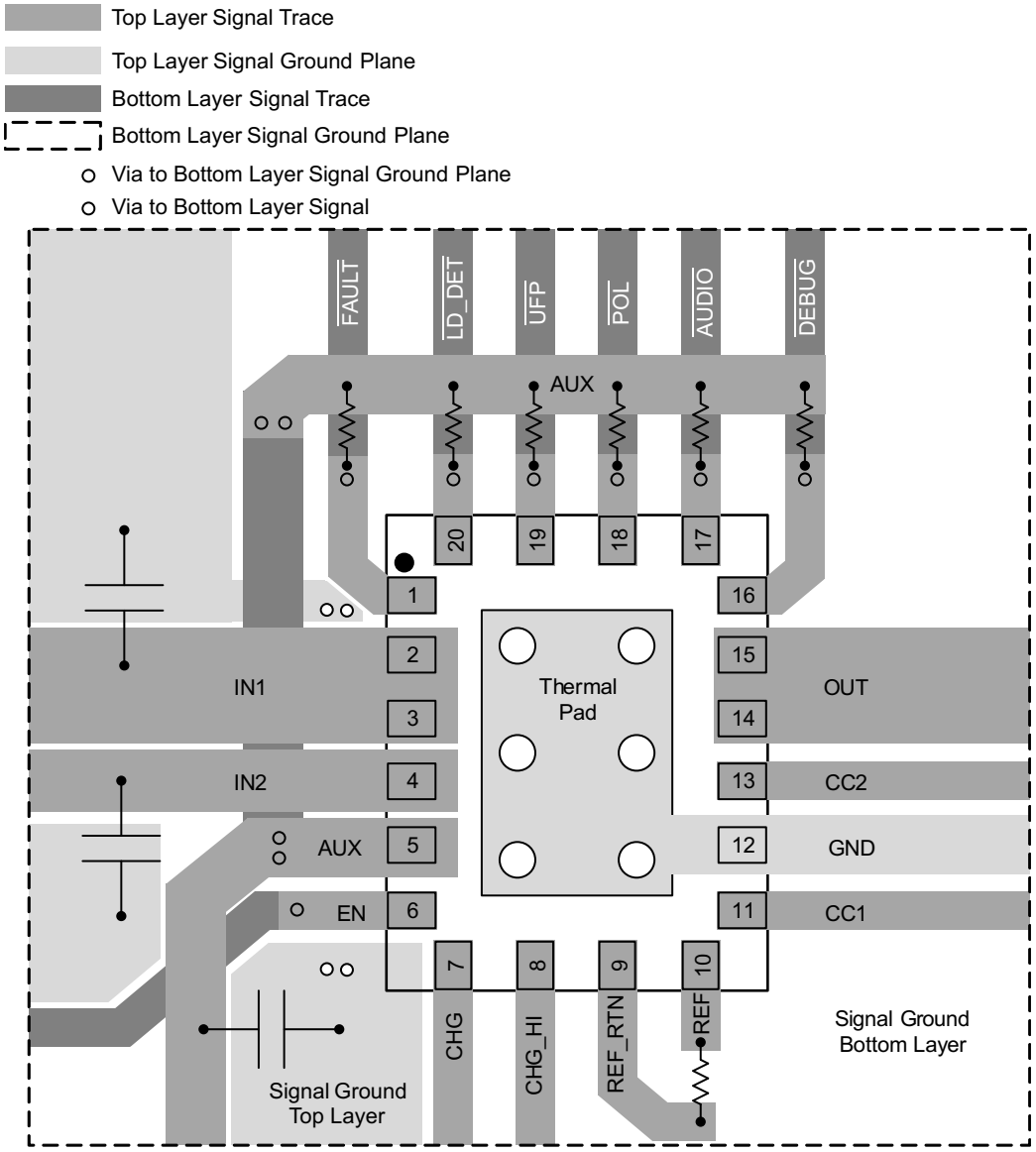


Figure 29. Layout Example

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《PowerPAD™ 速成》（文献编号：SLMA004）

《TPS25810EVM-745 用户指南》（文献编号：SLVUA0）

《TPS25810 高压 DFP 保护》（文献编号：SLVA751）

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18536KTT	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18536KTT	Samples
CSD18536KTTT	ACTIVE	DDPAK/ TO-263	KTT	3	50	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18536KTT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

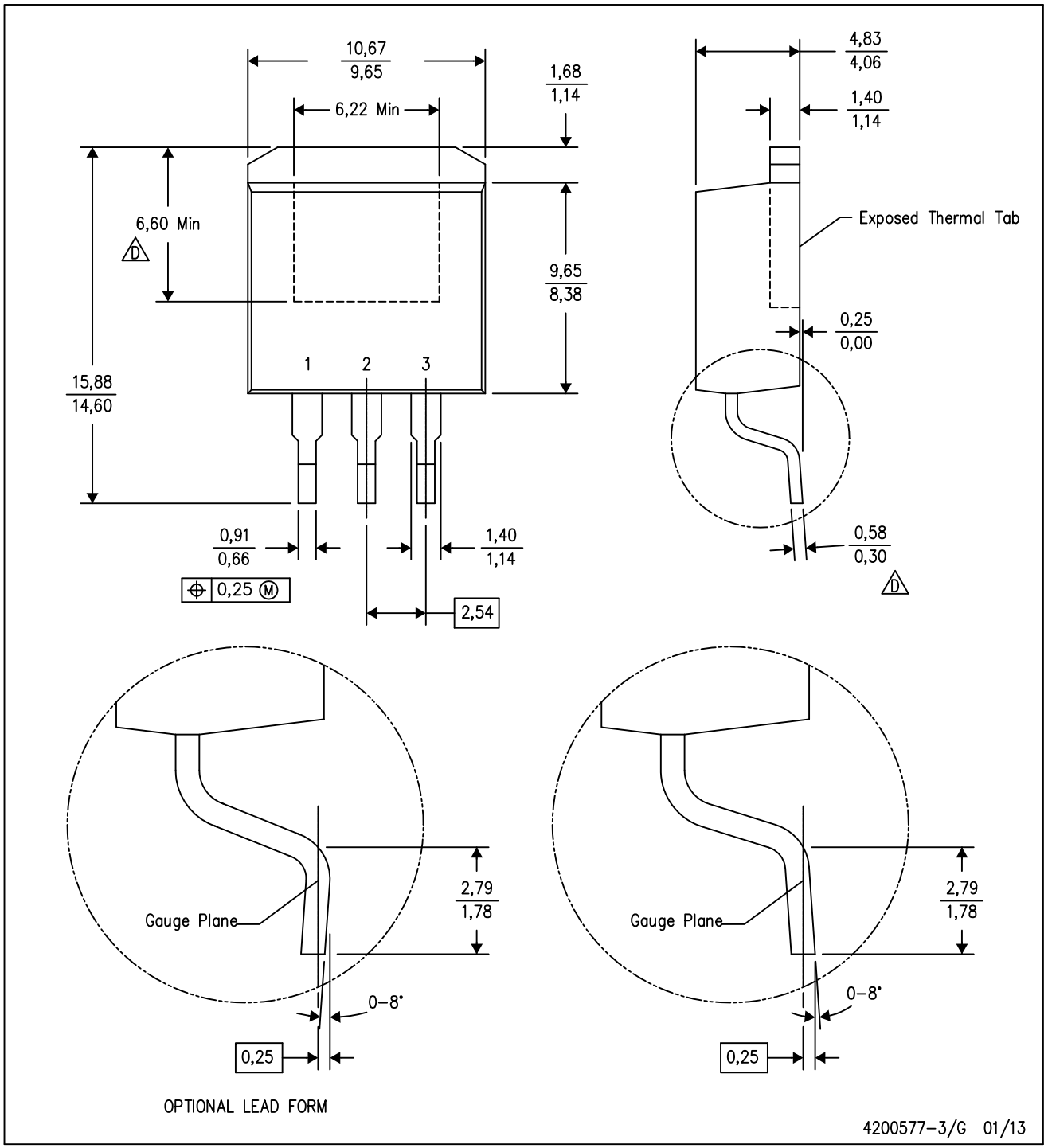
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

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