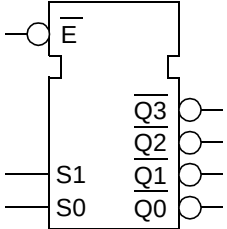


AMI5HG 0.5 micron CMOS Gate Array

Description

DC2x is a family of two-to-four line decoder/demultiplexers with active low enable.

Logic Symbol	Truth Table																																										
DC2x 	<table><tr><th>EN</th><th>S1</th><th>S0</th><th>Q0N</th><th>Q1N</th><th>Q2N</th><th>Q3N</th></tr><tr><td>H</td><td>X</td><td>X</td><td>H</td><td>H</td><td>H</td><td>H</td></tr><tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td></tr><tr><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td><td>H</td></tr><tr><td>L</td><td>H</td><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td></tr><tr><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td></tr></table>	EN	S1	S0	Q0N	Q1N	Q2N	Q3N	H	X	X	H	H	H	H	L	L	L	L	H	H	H	L	L	H	H	L	H	H	L	H	L	H	H	L	H	L	H	H	H	H	H	L
EN	S1	S0	Q0N	Q1N	Q2N	Q3N																																					
H	X	X	H	H	H	H																																					
L	L	L	L	H	H	H																																					
L	L	H	H	L	H	H																																					
L	H	L	H	H	L	H																																					
L	H	H	H	H	H	L																																					

HDL Syntax

Verilog DC2x *inst_name* (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

VHDL *inst_name*: DC2x port map (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

Pin Loading

Pin Name	Equivalent Loads	
	DC21	DC22
S0	3.2	3.2
S1	3.2	3.2
EN	1.0	4.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
DC21	8.0	TBD	17.8
DC22	10.0	TBD	20.7

a. See page 2-15 for power equation.

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Propagation Delays (ns)

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

DC21	Number of Equivalent Loads		1	2	4	6	8 (max)
	From: Sx	t _{PLH}	0.26	0.30	0.35	0.41	0.46
	To: QN	t _{PHL}	0.35	0.42	0.55	0.69	0.82
	From: EN	t _{PLH}	0.38	0.41	0.48	0.53	0.59
	To: QN	t _{PHL}	0.47	0.54	0.68	0.80	0.93
DC22	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Sx	t _{PLH}	0.23	0.33	0.45	0.60	0.71
	To: QN	t _{PHL}	0.42	0.57	0.73	0.90	1.02
	From: EN	t _{PLH}	0.27	0.37	0.50	0.64	0.76
	To: QN	t _{PHL}	0.52	0.67	0.82	0.99	1.11

Delay will vary with input conditions. See page 2-17 for interconnect estimates.