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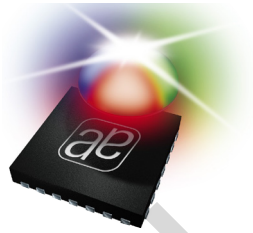
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AS3677

Triple Channel Lighting Management Unit with DCDC step/up, ALS, 2xDLS(=DBC) and RGB Driver



1 General Description

The AS3677 is a highly-integrated CMOS Power and Lighting Management Unit for mobile telephones, and other Li+ battery powered devices.

The AS3677 incorporates one Step Up DC/DC Converter for white backlight LEDs one Analog-to-Digital Converter, six current sinks, LED in-circuit function test, an I^2C serial interface, and control logic all onto a single device. It includes a charge pump to control e.g. an RGB together with an internal pattern generator for smooth blinking effects.

It supports **ambient light sensor** processing and **two** Dynamic Luminance Scaling (**DLS**) (also called Dynamic Backlight Control - DBC) input.

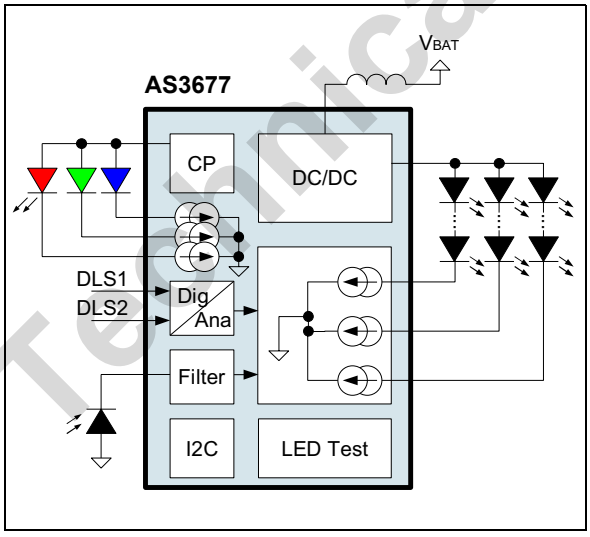
Internally the PWM signal for DLS can be used to change the analog current through the current sources (two channels can be used simultaneously). This avoids noise in the system as the changes of backlight control happen continuously without using the PWM modulation scheme.

Output voltages and output currents are fully programmable.

The AS3677 is part of the austriamicrosystems AS3675, AS3687/87XM, AS3688 and AS3689 lighting management unit family. It is software compatible to AS3675, AS3676, AS3687/87XM, AS3688 and AS3689.

The AS3677 is available in a space-saving WL-CSP package measuring only 2.2x2.2x0.6mm and operates over the -30ºC to +85ºC temperature range.

Figure 1. Function Diagram



2 Key Features

- High-Efficiency Step Up DC/DC Converter
  - Up to 25V, up to 50mA for White LEDs
  - Programmable Over voltage Protection (10V, 16V or 25V)
- 50mA Charge Pump
  - 1:1 and 1:2 Mode with automatic Up Switching
  - Only 2 External Capacitors Required
- 6 Current Sinks
  - Fully Programmable (8-bit) from: 0.1mA to 25.5mA
  - 3xHigh Voltage capable (up to 25V)
  - 3xLow voltage for use with the CP (up to 5.5V)
  - Selectively Enable/Disable Current Sinks
  - Dual Dynamic Luminance Scaling (DLS) support to improve backlight operating time (can adjust any current source)
  - Light Sensor input with internal hardware processing to control backlight according to ambient light using 3 groups
- Internal PWM Generation
  - 8 Bit resolution
  - Autonomous Logarithmic up/down dimming
- Led Pattern Generator
  - Autonomous driving of Fun RGB or indicator LEDs
- 10-bit Successive Approximation ADC
  - 27µs Conversion Time
  - Selectable Inputs: VANA, DLS1, DLS2, ALS/GPIO1, GPIO2, CURR1, CURR2, CURR6, VBAT, RGB1, RGB2 and RGB3
  - Internal Temp. Measurement
  - Light Sensor input with Java support (JSR-256): read ADC processed value
- Support for automatic LED testing (open and shorted LEDs can be identified)
- Programmable LDO
  - 1.8 to 3.35V, 10mA
  - Programmable via Serial Interface
- Wide Battery Supply Range: 3.0V to 5.5V
- I^2C Serial Interface Control with address control pin
- Over current and Thermal Protection
- Package
  WL-CSP25, 2.2x2.2x0.6mm, 0.4mm pitch

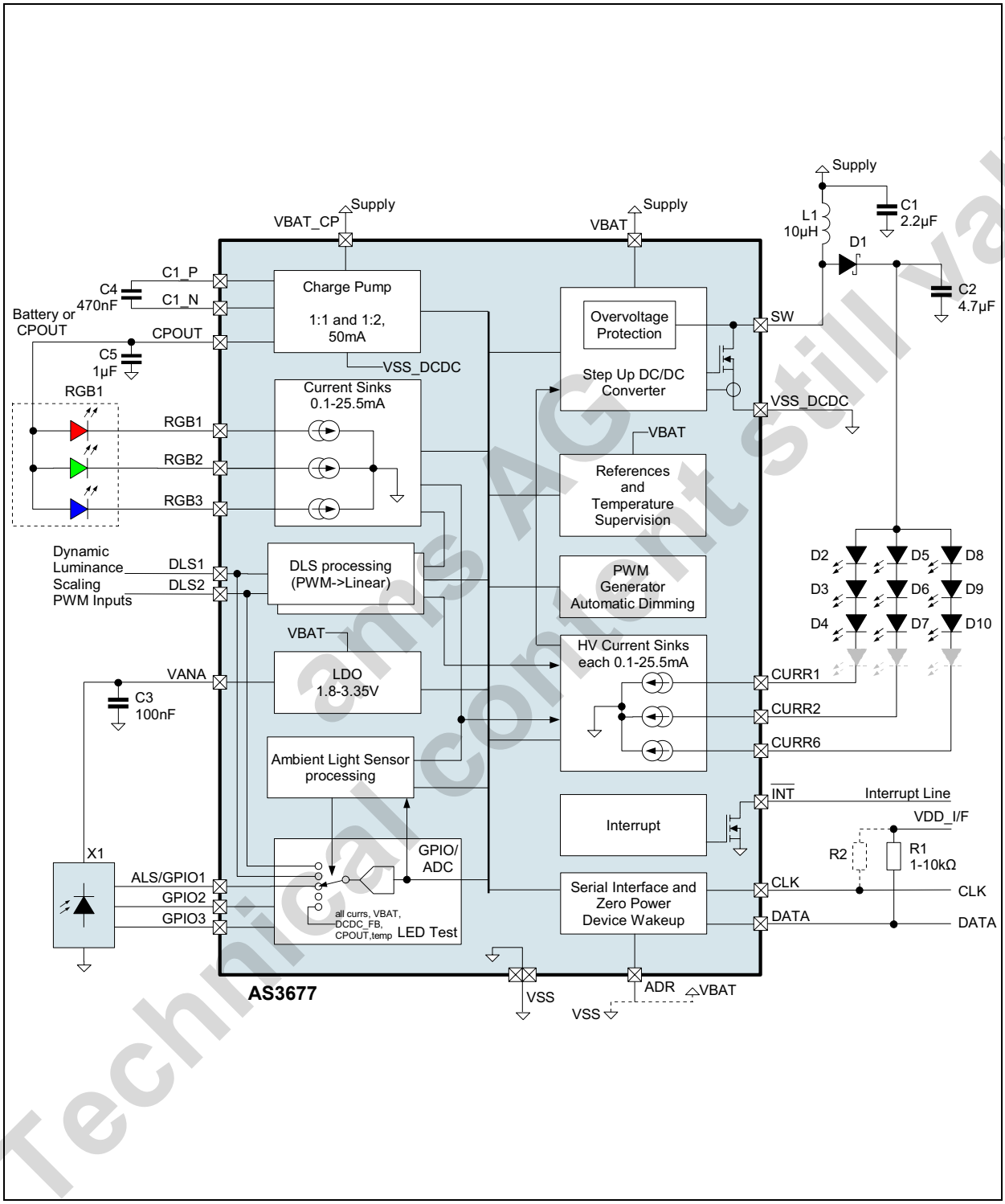
3 Applications

Lighting Management Unit for mobile phones, smartphones, PMP or PND

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The application circuit including all external components is shown in Figure 2:

Figure 2. Application Circuit AS3677

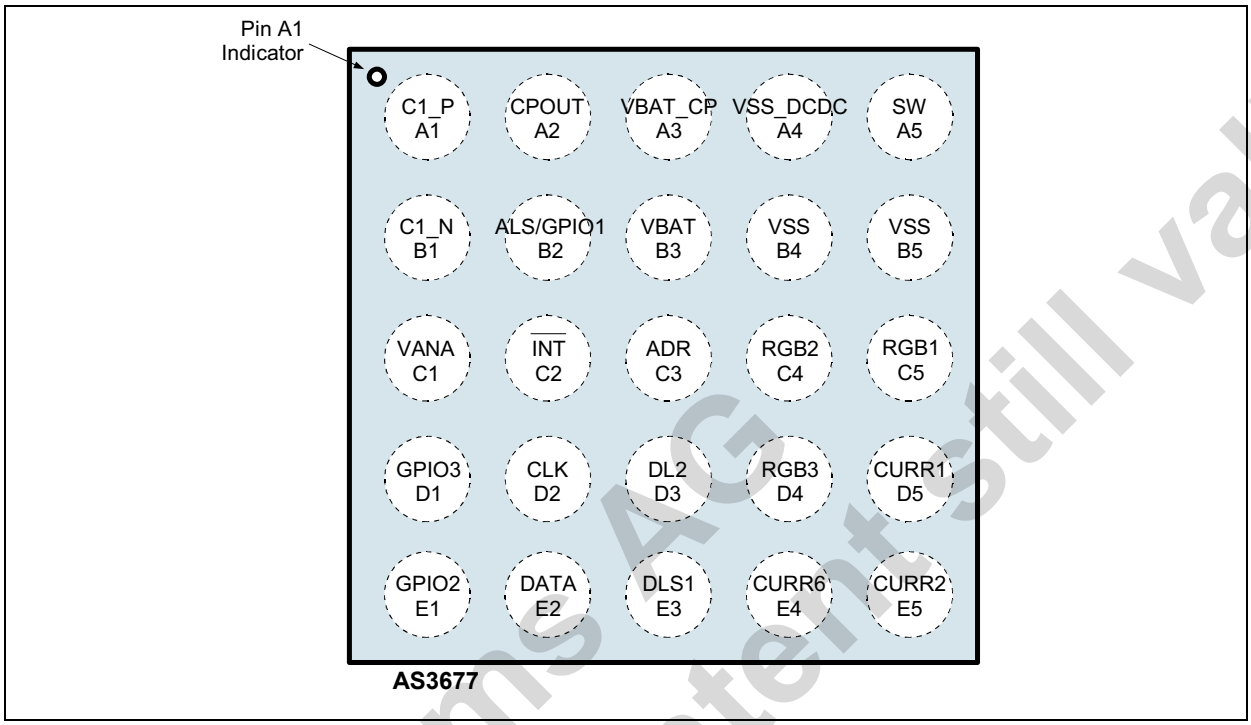


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4 Pinout

4.1 Pin Assignments

Figure 3. Pin Assignments (Top View)



4.2 Pin Description

Table 1. Pin Description

Pin Number	Pin Name	Description
A1	C1_P	Charge pump flying capacitor
A2	CPOUT	Charge pump output capacitor
A3	VBAT_CP	Charge pump supply voltage
A4	VSS_DCDC	DCDC and charge pump power ground pad - make a short connection to capacitor C1 and C2 (and C5)
A5	SW	Power pad - DCDC switch transistor output
B1	C1_N	Charge pump flying capacitor
B2	ALS/GPIO1	Ambient Light Sensor input and General Purpose Input Output 1
B3	VBAT	Positive supply pad - Connect to battery.
B4	VSS	ground pad
B5	VSS	ground pad
C1	VANA	LDO Output pad
C2	$\overline{INT}$	interrupt output - open drain active low
C3	ADR	I^2C address select input
C4	RGB2	Analog current sink input
C5	RGB1	Analog current sink input

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Table 1. Pin Description

Pin Number	Pin Name	Description
D1	GPIO3	General Purpose Input Output 3
D2	CLK	Digital input - Clock input for serial interface.
D3	DLS2	Digital Luminance Scaling PWM input2 (or General Input)
D4	RGB3	Analog current sink input
D5	CURR1	Analog current sink input
E1	GPIO2	General Purpose Input Output 2
E2	DATA	Digital input/output - Serial interface data
E3	DLS1	Digital Luminance Scaling PWM input1 (or General Input)
E4	CURR6	Analog current sink input
E5	CURR2	Analog current sink input

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5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3, “General Operating Conditions; typical values are at VBAT=3.7V and 25ºC,” on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
V_{IN_HV}	26V Pins	-0.3	26	V	Applicable for high-voltage current sink pins CURR1, CURR2, CURR6, SW
V_{IN_MV}	5V Pins	-0.3	7.0	V	Applicable for 5V pins VBAT, VBAT_CP, CLK, DATA, ADR, RGB1, RGB2, RGB3, CPOUT, C1_P, C1_N, INT
V_{IN_LV}	3.3V Pins	-0.3	5.0	V	Applicable for 3.3V pins ALS/GPIO1, GPIO2, GPIO3, DLS1, DLS2, VANA
	GND pins	0.0	0.0	V	2xVSS, VSS_DCDC
	Input Pin Current without causing latchup	-25	+25	mA	At 25ºC, Norm: EIA/JESD78
T_{strg}	Storage Temperature Range	-55	125	ºC	
I_{IN}	Humidity	5	85	%	Non-condensing
V_{ESD}	HBM	-2000	2000	V	Norm: JESD22-A114F
	CDM	-500	500	V	Norm: JEDEC JESD 22-C101E
	MM	-100	100	V	Norm: JEDEC JESD 22-A115-B
Pt	Total Power Dissipation		0.75	W	TA = 70 ºC, Tjunc_max = 125ºC; R_{THJU}=73 K/W
T_{BODY}	Peak Body Temperature		260	ºC	T = 20 to 40s, in accordance with IPC/JEDEC J-STD 020.
MSL	Moisture sensitivity level	1			Represents a max. floor life time of unlimited

6 Electrical Characteristics

Table 3. General Operating Conditions; typical values are at VBAT=3.7V and 25ºC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{HV}	High Voltage	Applicable for high-voltage current sink pins $CURR_1$, CURR2 and CURR6.	0.0		26.0	V
V_{BAT}	Battery Voltage	Pin VBAT, VBAT_CP	3.0	3.7	5.5	V
V_{PERI}	Periphery Supply Voltage	For serial interface pins.	1.5		5.5	V
T_{AMB}	Operating Temperature Range		-30	25	85	ºC
I_{ACTIVE}	Battery current	Normal Operating current (see Operating Modes on page 58)		110		µA
$I_{STANDBY}$	Standby Mode Current	Current consumption in standby mode. Interface active		10	15	µA

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Table 3. General Operating Conditions; typical values are at VBAT=3.7V and 25ºC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ISHUTDOWN	Shutdown Mode Current	interface inactive (CLK and DATA set to 0V)		0.1	3	µA

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7 Typical Operating Characteristics

Measured at VBAT=3.7V and TAMB=25ºC unless otherwise specified.

Figure 4. DCDC Efficiency vs. Load Current

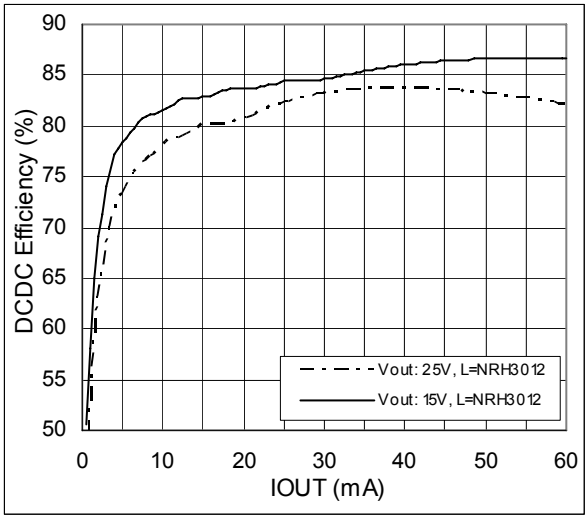


Figure 5. Charge Pump: Efficiency vs. VBAT

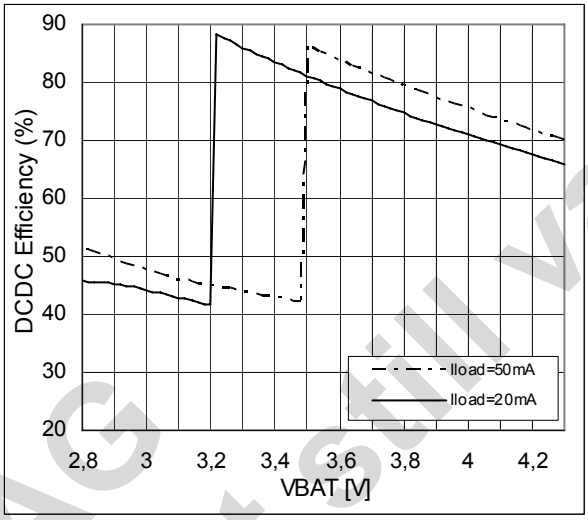


Figure 6. Charge Pump: Battery current vs. VBAT

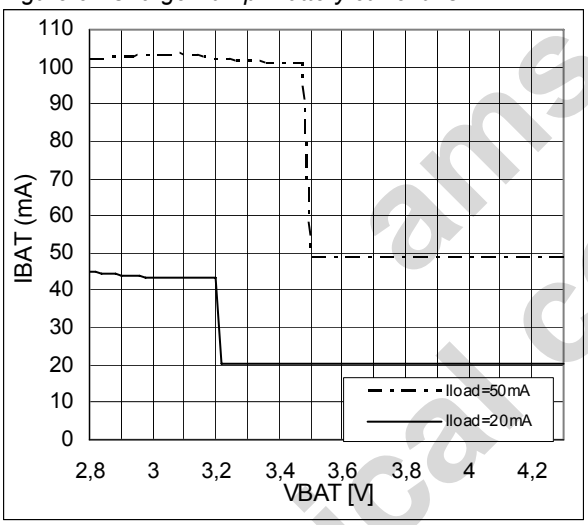


Figure 7. Current Sink CURR1 vs. V(CURRx)

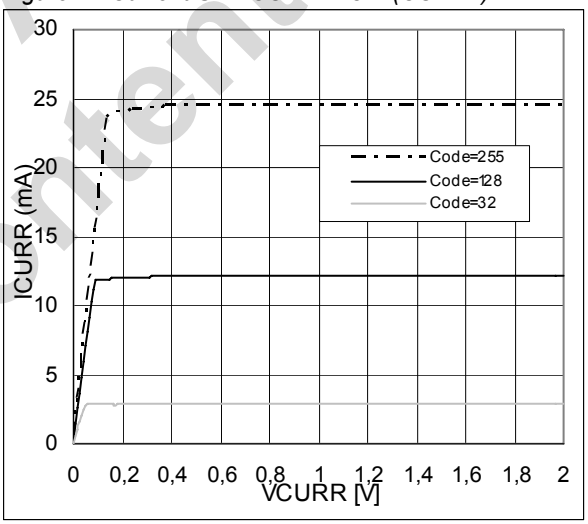


Figure 8. Current Sink RGB1 vs. V(CURRx)

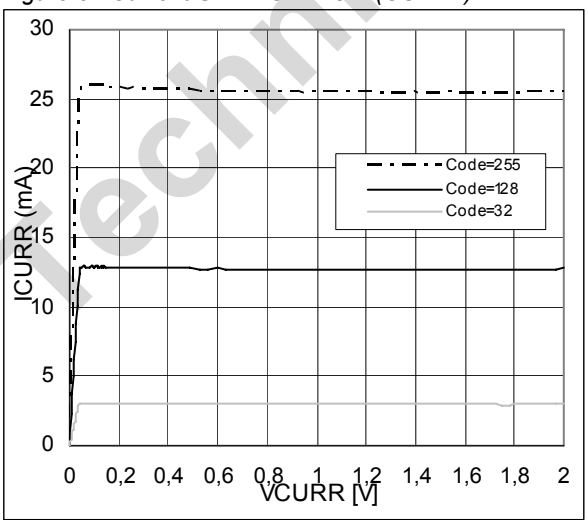
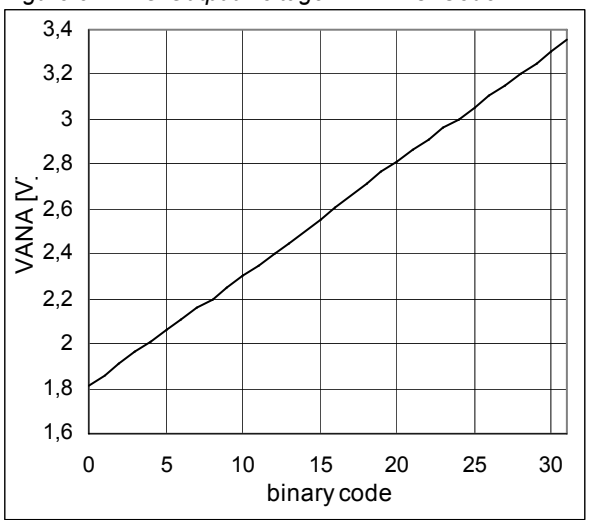


Figure 9. LDO Output Voltage VANA vs. Code



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Figure 10. LDO Output Voltage VANA vs. Load

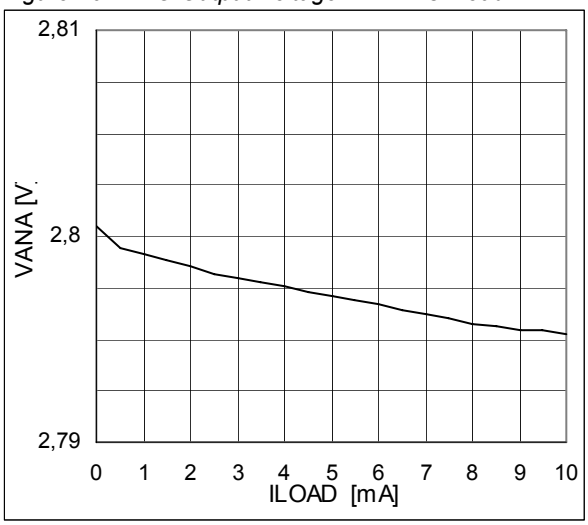
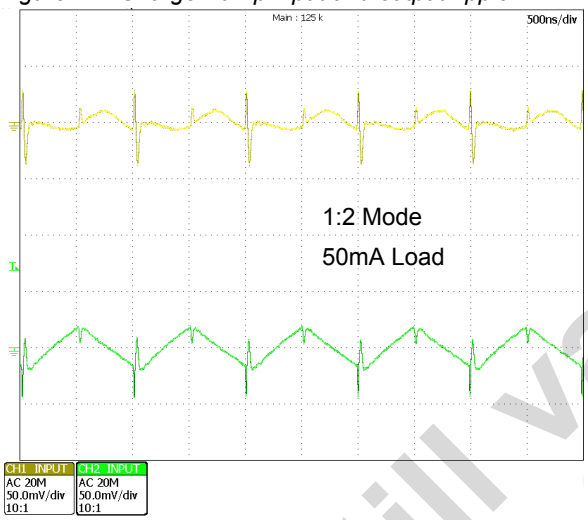


Figure 11. Charge Pump input and output ripple



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8 Detailed Description

8.1 LDO

The LDO is a general purpose LDO and the output pin connected to VANA and intended to power an external light sensor. Stability is guaranteed with ceramic output capacitors of 100nF ±20% (X5R).

The LDO is off by default after start-up.

Figure 12. LDO Block Diagram

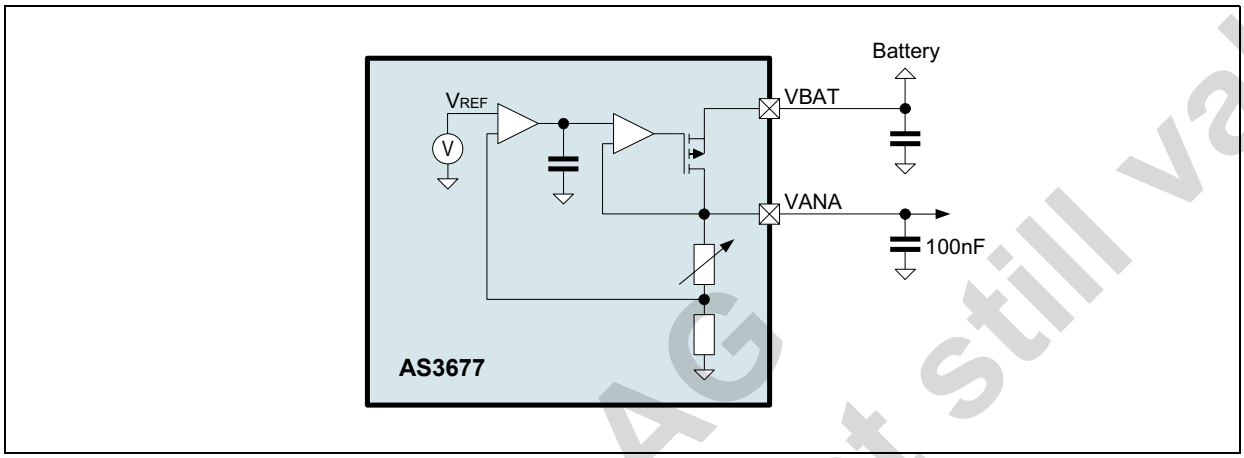


Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ILOAD	Output current		0		10	mA
RON	On Resistance			10	25	Ω
VDROPOUT	Dropout Voltage				250	mV
ION	Supply Current	Without load		19		µA
tstart	Start-up Time				200	µs
Vout_tol	Output Voltage Tolerance		-3		+3	%
VOUT	Output Voltage	VBAT > 3.0V	1.8		2.75	V
		Full Programmable Range	1.8		3.35	V

8.1.1 LDO Registers

Table 5. Reg control Register

Addr: 00		Reg control			
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter, and low-power mode.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	ldo_on	0	R/W	0	LDO is switched off
				1	LDO is switched on

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Table 6. LDO Voltage Register

Addr: 07h		LDO Voltage			
		This register sets the output voltage (VANA) for the LDO.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	ldo_voltage	00000b	R/W	Controls LDO voltage selection.	
				00000b	1.8V
				...	LSB=50mV
				11111b	3.35V

8.2 Step Up DC/DC Converter

The Step Up DC/DC Converter is a high-efficiency current mode PWM regulator, providing output voltage up to e.g. 25V/50mA. A constant switching-frequency results in a low noise on the supply and output voltages.

Figure 13. Step Up DCDC Converter Internal Block Diagram

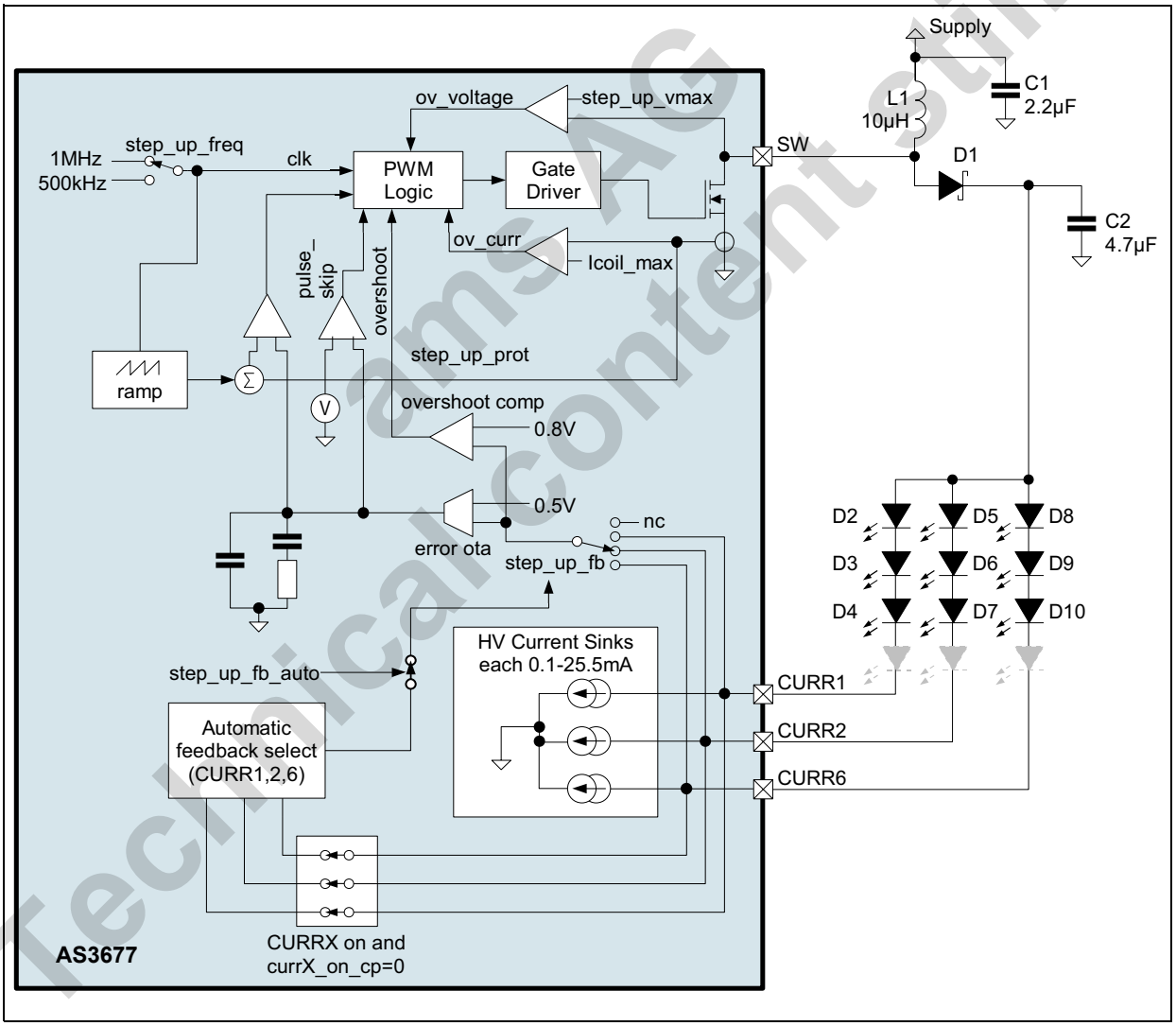


Table 7. Step Up DC/DC Converter Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{VDD}	Quiescent Current	Pulse skipping mode.		200		µA

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Table 7. Step Up DC/DC Converter Parameters (Continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{FB}	Feedback Voltage for Current Sink Regulation	on CURR1, CURR2 or CURR6 in regulation.		0.4	0.5	0.6	V
I_{COIL_MAX}	Coil current limit	step_up_lowcur=0			1200		mA
		step_up_lowcur=1			750		
		For fixed startup time of 500us	step_up_lowcur=0		600		
			step_up_lowcur=1		330		
R_{SW}	Switch Resistance	ON-resistance of external switching transistor.			0.42	1.0	Ω
I_{LOAD}	Load Current	At 25V output voltage		0		50	mA
f_{IN}	Switching Frequency	Internally trimmed		0.9	1	1.1	MHz
C_{OUT}	Output Capacitor	Ceramic, ±20%. Use nominal 4.7µF capacitors to obtain at least 0.7µF under all conditions (voltage dependence of capacitors)		0.7	4.7		µF
L	Inductor	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency.		7	10	13	µH
t_{MIN_ON}	Minimum on Time			90	140	190	ns
MDC	Maximum Duty Cycle			90			%
Vripple	Voltage ripple >20kHz	Cout=4.7µF,Iout=0..45mA, VBAT=3.0...4.2V				160	mV
	Voltage ripple <20kHz					40	mV
Efficiency	Efficiency	Iout=20mA,Vout=17V,VBAT=3.8V			85		%

To ensure soft startup of the dcdc converter, the over current limits are reduced for a fixed time after enabling the dcdc converter. The total startup time for an output voltage of e.g. 26V is less than 2ms.

8.2.1 Feedback Selection

Register DCDC control1 and DCDC control2 selects the type of feedback for the Step Up DC/DC Converter.

The feedback for the DC/DC converter can be selected to any of the current sinks (CURR1, CURR2, CURR6). If the register bit step_up_fb_auto is set, the feedback path is automatically selected between CURR1, CURR2 and CURR6 (the lowest voltage of these current sinks is used)[1]. The Step Up DC/DC Converter is regulated such that the required current at the feedback path can be supported.

Note: Always choose the path with the highest voltage drop as feedback to guarantee adequate supply for the other (unregulated) paths or enable the register bit step_up_fb_auto.

8.2.2 Over voltage Protection

The over voltage protection is controlled by the register step_up_vmax (can be programmed to 10V, 16V or 25V) to protect the external components (especially the output capacitor C1. If the voltage on the pin SW exceeds this voltage, the DCDC is immediately disabled and the register bit step_up_ov is set. To re-enable the DCDC set step_up_on=0 and afterwards step_up_on=1.

The voltage rating of the external components must be chosen to fit to the software setting of step_up_vmax[2].

Note: The voltage on CURR1, CURR2 and CURR6 must not exceed 26V (see page 20)

1. It is recommended to leave step_up_fb_auto=1 (default) all the times.
2. If the voltage is the DCDC overvoltage protection is chosen above the voltage ratings of the external components, permanent damage might result.

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8.2.3 PCB Layout Hints

To ensure good EMC performance of the DCDC converter, keep its external power components C1, L1, D1 and C2 close together. Connect the ground of C1, C2 locally together and connect this with a short path to AS3677 VSS. This ensures that local high-frequency currents will not flow to the battery.

8.2.4 Step up Registers

Table 8. Reg control Register

Addr: 00		Reg control			
		This register enables/disables the Charge Pump and the Step Up DC/DC Converter.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3	step_up_on	0	R/W	Enable the step up converter	
				0b	Disable the Step Up DC/DC Converter
				1b	Enable the Step Up DC/DC Converter

Table 9. DCDC control1 Register

Addr: 21h		DCDC control1			
		This register controls the Step Up DC/DC Converter.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	step_up_frequ	0	R/W	Defines the clock frequency of the Step Up DC/DC Converter.	
				0	1MHz
				1	500kHz
2:1	step_up_fb	01	R/W	Controls the feedback source if step_up_fb_auto = 0	
				00	no feedback selected - don't use
				01	CURR1 feedback enabled (default)
				10	CURR2 feedback enabled
				11	CURR6 feedback enabled
4:3	step_up_vmax	00	R/W	Overvoltage protection for the DCDC step up	
				00	16V
				01	10V
				10	25V
				11	don't use (15.5V)

Table 10. DCDC control2 Register

Addr: 22h		DCDC control2			
		This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1	skip_fast	0	R/W	Step Up DC/DC Converter output voltage at low loads, when pulse skipping is active	
				0	Accurate output voltage, more ripple
				1	Elevated output voltage, less ripple

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Table 10. DCDC control2 Register (Continued)

Addr: 22h		DCDC control2			
		This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3	step_up_lowcur	1	R/W	Step Up DC/DC Converter coil current limit	
				0	Normal current limit
				1	Current limit reduced by approx. 33%
4	step_up_ov	0	R	Step Up DC/DC overvoltage triggered	
				0	No overvoltage triggered
				1	Overvoltage triggered; this bit is automatically reset by step_up_on=0
7	step_up_fb_auto	1	R/W	0	step_up_fb select the feedback of the DCDC converter
				1	The feedback is automatically chosen within the current sinks CURR1, CURR2 and CURR6 (never DCDC_FB). Only those are used for this selection, which are enabled (currX_mode must not be 00) and not connected to the charge pump (currX_on_cp must be 0).

8.3 Charge Pump

The Charge Pump uses the external flying capacitor C4 to generate output voltages higher than the battery voltage. There are two different operating modes of the charge pump itself:

- 1:1 Bypass Mode
  - Battery input and output are connected by a low-impedance switch
  - battery current = output current.
- 1:2 Mode
  - The output voltage is up to 2 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  - battery current = 2 times output current

As the battery voltage decreases, the Charge Pump must be switched from 1:1 mode to 1:2 mode in order to provide enough supply for the current sinks. Depending on the actual current the mode with best overall efficiency can be automatically or manually selected:

The charge pump mode switching can be done manually or automatically with the following possible software settings:

- Automatic
  - Start with 1:1 mode
  - Switch up automatically to 1:2 mode
- Manual
  - Set modes 1:1 and 1:2 by software

The Charge Pump requires the external components listed in the following table:

Table 11. Charge Pump External Components

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_4	External Flying Capacitor	Ceramic low-ESR capacitor between pins C1_P and C1_N		470		nF
C_5	External Storage Capacitor	Ceramic low-ESR capacitor between pins CPOUT and VSS, pins CPOUT and VSS_CP		1.0		µF

Note: The connections of the external capacitors C4 and C5 should be kept as short as possible.

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The maximum voltage on the flying capacitor C4 is VBAT.

Table 12. Charge Pump Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICPOUT	Output Current Continuous	Depending on PCB layout	0.0		50	mA
VCPOUTmax	Output Voltage	Internally limited, Including output ripple			5.6	V
η	Efficiency	Including current sink loss; ICPOUT < 50mA.		80		%
ICP1_2	Power Consumption without Load, fclk = 1 MHz	1:2 Mode		2.15		mA
Rcp1_1	Effective Charge Pump Output Resistance (Open Loop, fclk = 1MHz)	1:1 Mode; VBAT = 3V		8.8		Ω
Rcp1_2		1:1.2 Mode; VBAT = 3V		31		
fclk Accuracy	Accuracy of Clock Frequency		-10		10	%
currhv_switch	CURR1, 2, 6 minimum voltage	If the voltage drops below this threshold, the charge pump will use the next available mode (1:1 -> 1:2)			0.45	V
currlv_switch	RGB1-3 minimum voltage				0.2	V
t_{deb}	CP automatic up-switching debounce time	cp_start_debounce=0		240		µsec
		After switching on CP (cp_on set to 1), if cp_start_debounce=1		2000		µsec

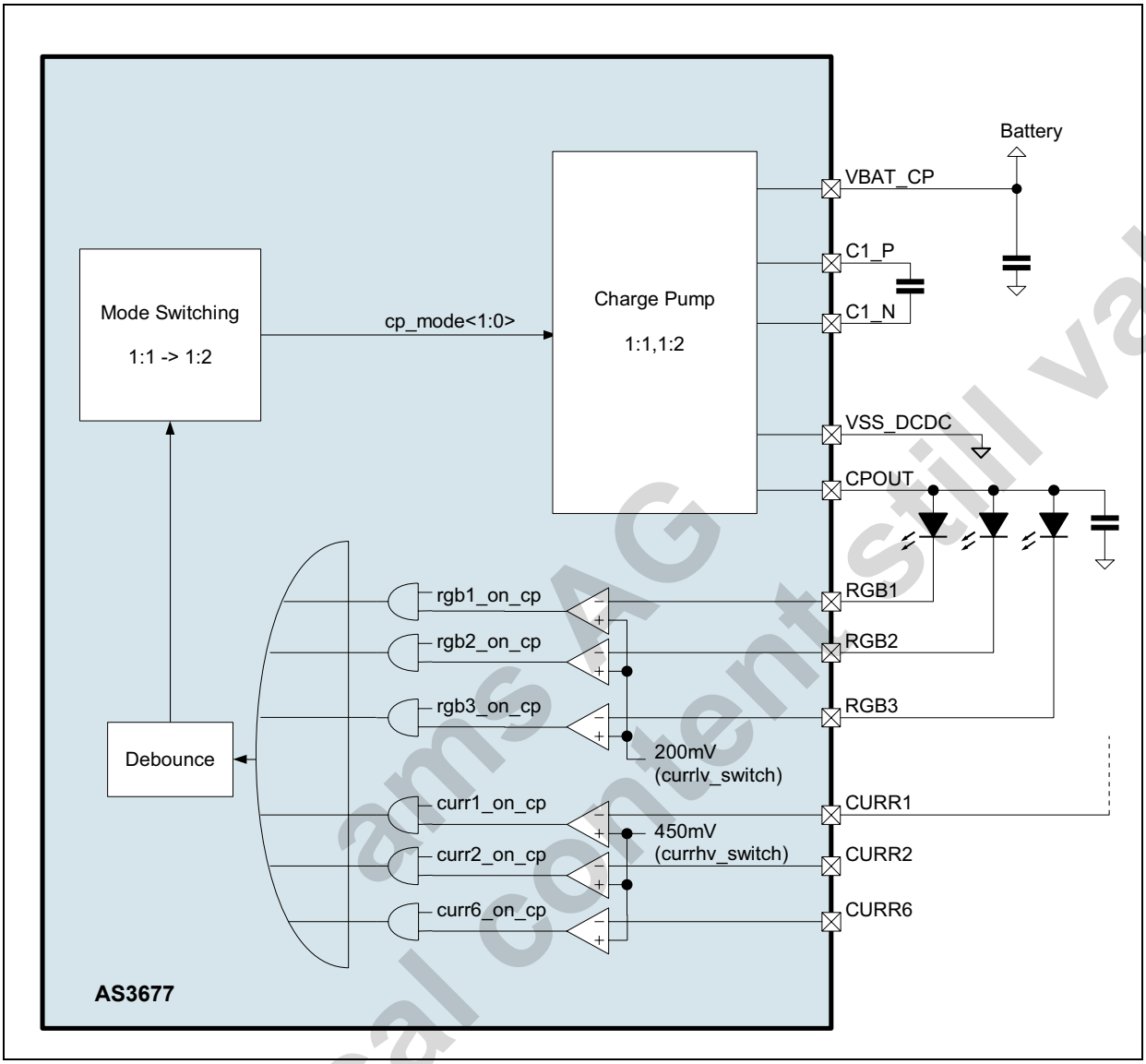
8.3.1 Charge Pump Mode Switching

If automatic mode switching is enabled (cp_mode_switching (see page 16) = 00 or cp_mode_switching = 01) the charge pump monitors the current sinks, which are connected via a led to the output CPOUT. To identify these current sources (sinks), the registers CP mode Switch1 and CP mode Switch2 (register bits rgb1_on_cp … rgb3_on_cp, curr1_on_cp, curr2_on_cp and curr6_on_cp) should be setup before starting the charge pump (cp_on (see page 16) = 1). If any of the voltage on these current sources drops below the threshold (currlv_switch, currhv_switch), the next higher mode is selected after the debounce time.

If the currX_on_cp=0 and the according current sink is connected to the charge pump, the current sink will be functional, but there is no up switching of the charge pump, if the voltage compliance is too low for the current sink to supply the specified current.

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Figure 14. Automatic Mode Switching



8.3.2 Soft Start

An implemented soft start mechanism reduces the inrush current. Battery current is smoothed when switching the charge pump on and also at each switching condition. This precaution reduces electromagnetic radiation significantly.

8.3.3 Unused Charge Pump

If the charge pump is not used, capacitors C4 and C5 (not C2) can be removed. The pins C1_P, C1_N and CPOUT should be left open and keep register cp_on and cp_auto_on at 0 (default value).

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8.3.4 Charge Pump Registers

Table 13. Reg control Register

Addr: 00h		Reg control			
		This register controls the Charge Pump.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2	cp_on	0	R/W	0	Set Charge Pump into 1:1 mode (off state) unless cp_auto_on is set
				1	Enable manual or automatic mode switching

Table 14. CP control Register

Addr: 23h		CP control			
		This register enables/disables the Charge Pump and the Step Up DC/DC Converter.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	cp_clk	0	R/W	Clock frequency selection.	
				0	1 MHz
				1	500 kHz
2:1	cp_mode	00b	R/W	Charge Pump mode (in manual mode sets this mode, in automatic mode reports the actual mode used)	
				00	1:1 mode
				01	
				10	1:2 mode
				11	
4:3	cp_mode_switching	00b	R/W	Set the mode switching algorithm	
				00	Automatic Mode switching
				01	
				10	Manual Mode switching; register cp_mode defines the actual charge pump mode used
				11	
5	cp_start_debounce	0	R/W	0	Mode switching debounce timer is always 240µs
				1	Upon startup (cp_on set to 1) the mode switching debounce time is first started with 2ms then reduced to 240µs
6	cp_auto_on	1	R/W	0	Charge Pump is switched on/off with cp_on
				1	Charge Pump is automatically switched on if a current sink, which is connected to the charge pump (defined by registers CP Mode Switch 1 & 2) is switched on

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Table 15. CP mode Switch1 Register

Addr: 24h		CP mode Switch1			
		Setup which current sinks are connected (via leds) to the charge pump; if set to '1' the correspond current source (sink) is used for automatic mode selection of the charge pump			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	rgb1_on_cp	1	R/W	0	current Sink RGB1 is not connected to charge pump
				1	current sink RGB1 is connected to charge pump
5	rgb2_on_cp	1	R/W	0	current Sink RGB2 is not connected to charge pump
				1	current sink RGB2 is connected to charge pump
6	rgb3_on_cp	1	R/W	0	current Sink RGB3 is not connected to charge pump
				1	current sink RGB3 is connected to charge pump

Table 16. CP mode Switch2 Register

Addr: 25h		CP mode Switch2			
		Setup which current sinks are connected (via LEDs) to the charge pump; if set to '1' the correspond current source (sink) is used for automatic mode selection of the charge pump			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr1_on_cp	0	R/W	0	current Sink CURR1is not connected to charge pump
				1	current sink CURR1 is connected to charge pump
1	curr2_on_cp	0	R/W	0	current Sink CURR2 is not connected to charge pump
				1	current sink CURR2 is connected to charge pump
7	curr6_on_cp	0	R/W	0	current Sink CURR6 is not connected to charge pump
				1	current sink CURR6 is connected to charge pump

Table 17. Curr low voltage status1 Register

Addr: 2Ah		Curr low voltage status1			
		Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	rgb1_low_v	NA	R	0	voltage of current Sink RGB1 >currlv_switch
				1	voltage of current Sink RGB1 <currlv_switch
5	rgb2_low_v	NA	R	0	voltage of current Sink RGB2 >currlv_switch
				1	voltage of current Sink RGB2 <currlv_switch
6	rgb3_low_v	NA	R	0	voltage of current Sink RGB3 >currlv_switch
				1	voltage of current Sink RGB31 <currlv_switch
7	curr6_low_v	NA	R	0	voltage of current Sink CURR6 >currlv_switch
				1	voltage of current Sink CURR6 <currlv_switch

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Table 18. Curr low voltage status2 Register

Addr: 2Bh		Curr low voltage status2			
		Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr1_low_v	NA	R	0	voltage of current Sink CURR1 >currhv_switch
				1	voltage of current Sink CURR1 <currhv_switch
1	curr2_low_v	NA	R	0	voltage of current Sink CURR2 >currhv_switch
				1	voltage of current Sink CURR2 <currhv_switch

8.4 Current Sinks

The AS3677 contains three general purpose current sinks intended to control backlight LEDs.

CURR1, CURR2 and CURR6 are used as feedback for the Step Up DC/DC Converter (regulated to 0.5V in this configuration) see Feedback Selection on page 11.

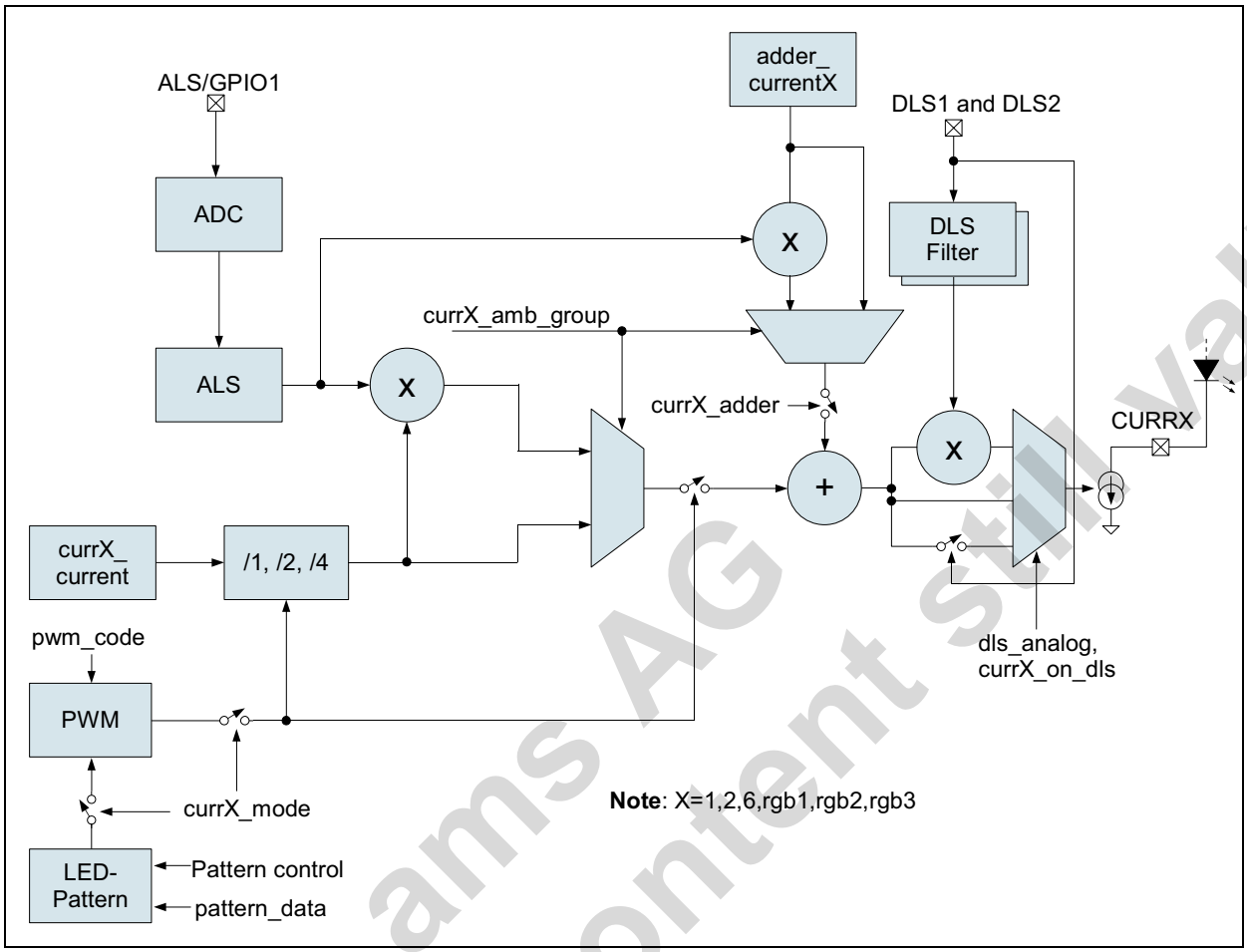
Table 19. Current Sink Function Overview

Current Sink	Max. Voltage (V)	Max. Current (mA)	Resolution		Software Current Control	Hardware On/Off Control
			(Bits)	(mA)		
RGB1	5.5	25.5	8	0.1	Separate	Internal PWM; external PWM at DLS1, Pattern generator
RGB2						
RGB3						
CURR1	26.0	25.5	8	0.1	Separate	Internal PWM; external PWM at DLS1, Pattern generator
CURR2						Internal PWM; external PWM at DLS1 or DLS2, Pattern generator
CURR6						

The processing inside the AS3677 is shown in Figure 15 (shown for one current source only):

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Figure 15. Internal processing of the different signals



8.4.1 Unused Current Sinks

Unused current sinks can be left open or used as ADC inputs (see Analog-to-Digital Converter on page 50).

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8.4.2 High Voltage Current Sinks CURR1, CURR2, CURR6

The high voltage current sinks have a resolution of 8 bits.

Table 20. HV Current Sinks Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{BIT7}	Current sink if Bit7 = 1	For V(CURRx) > 0.45V		12.8		mA
I_{BIT6}	Current sink if Bit6 = 1			6.4		
I_{BIT5}	Current sink if Bit5 = 1			3.2		
I_{BIT4}	Current sink if Bit4 = 1			1.6		
I_{BIT3}	Current sink if Bit3 = 1			0.8		
I_{BIT2}	Current sink if Bit2 = 1			0.4		
I_{BIT1}	Current sink if Bit1 = 1			0.2		
I_{BIT0}	Current sink if Bit0 = 1			0.1		
Δm	matching Accuracy	CURR1,CURR2,CURR6	-7		+7	%
Δ	absolute Accuracy		-15		+15	%
$V_{CURR1,2,6x}$	Voltage compliance		0.45		25	V
$I_{QCURR1,2,6}$	Quiescent current			165		µA

High Voltage Current Sinks CURR1, CURR2, CURR6 Registers

Table 21. Curr1 current Register

Addr: 09h		Curr1 current			
		This register controls the High voltage current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr1_current	0	R/W	Defines current into current sink curr1	
				00h	0 mA
				01h	0.1 mA
				....	....
				FFh	25.5 mA

Table 22. Curr2 current Register

Addr: 0Ah		Curr2 current			
		This register controls the High voltage current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr2_current	0	R/W	Defines current into current sink curr2	
				00h	0 mA
				01h	0.1 mA
				....	....
				FFh	25.5 mA

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Table 23. Curr6 current Register

Addr: 2Fh		Curr6 current			
		This register controls the High voltage current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr6_current	0	R/W	Defines current into current sink CURR6	
				00h	0 mA
				01h	0.1 mA
				....	....
				FFh	25.5 mA

Table 24. curr12 control Register

Addr: 01h		curr12 control			
		This register select the mode of the current sinks controls High voltage current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	curr1_mode	0	R/W	Select the mode of the current sink curr1	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled
3:2	curr2_mode	0	R/W	Select the mode of the current sink curr2	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled

Table 25. curr rgb control Register

Addr: 02h		curr rgb control			
		This register select the mode of the current sinks CURR6.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:6	curr6_mode	0	R/W	Select the mode of the current sink CURR6	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled

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8.4.3 Current Sinks RGB1, RGB2, RGB3

These current sinks have a resolution of 8 bits and can sink up to 25.5mA.

Table 26. Current Sinks RGB1, RGB2, RGB3 Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{BIT7}	Current sink if Bit7 = 1	For V(RGBx) > 0.2V		12.8		mA
I_{BIT6}	Current sink if Bit6 = 1			6.4		
I_{BIT5}	Current sink if Bit5 = 1			3.2		
I_{BIT4}	Current sink if Bit4 = 1			1.6		
I_{BIT3}	Current sink if Bit3 = 1			0.8		
I_{BIT2}	Current sink if Bit2 = 1			0.4		
I_{BIT1}	Current sink if Bit1 = 1			0.2		
I_{BIT0}	Current sink if Bit0 = 1			0.1		
Δm	matching Accuracy	RGB1, RGB2, RGB3	-10		+10	%
Δ	absolute Accuracy		-15		+15	%
V_{RGBX}	Voltage compliance		0.2		CPOUT	V
$I_{QRGB1,2,3}$	Quiescent current			165		µA

RGB Current Sinks Registers

Table 27. curr rgb control Register

Addr: 02h		curr rgb control			
		This register select the mode of the current sinks RGB1, RGB2, RGB3			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	rgb1_mode	0	R/W	Select the mode of the current sink RGB1	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled
3:2	rgb2_mode	0	R/W	Select the mode of the current sink RGB2	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled
5:4	rgb3_mode	0	R/W	Select the mode of the current sink RGB3	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled

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Table 28. Rgb1 current Register

Addr: 0Bh		Rgb1 current			
		This register controls the RGB current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	rgb1_current	0	R/W	Defines current into Current sink RGB1	
				00h	0 mA
				01h	0.1 mA
				....	....
				FFh	25.5 mA

Table 29. Rgb2 current Register

Addr: 0Ch		Rgb2 current			
		This register controls the RGB current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	rgb2_current	0	R/W	Defines current into Current sink RGB2	
				00h	0 mA
				01h	0.1 mA
				....	....
				FFh	25.5 mA

Table 30. Rgb3 current Register

Addr: 0Dh		Rgb3 current			
		This register controls the RGB current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	rgb3_current	0	R/W	Defines current into Current sink RGB3	
				00h	0 mA
				01h	0.1 mA
				....	....
				FFh	25.5 mA

8.4.4 LED Pattern Generator

The LED pattern generator is capable of producing a pattern with 32 bits length and 1 second duration (31.25ms for each bit). The pattern itself can be started every second, every 2nd, 3rd up to 7th second[3].

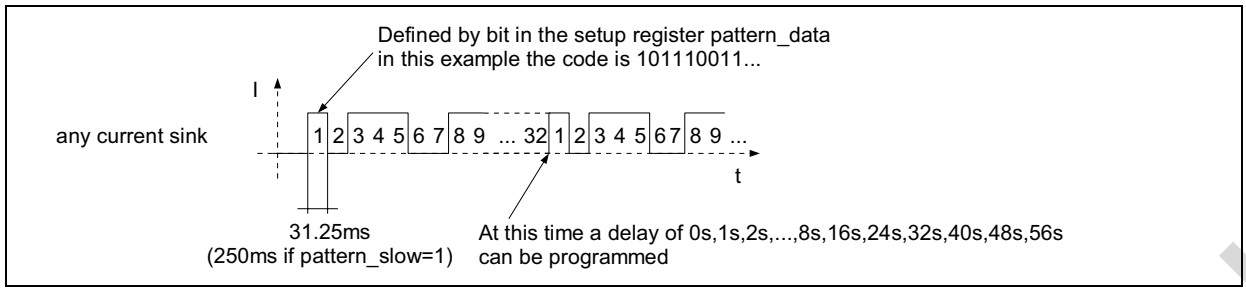
With this pattern all current sinks can be controlled. The pattern itself switches the configured current sources between 0 and their programmed current.

If everything else is switched off, the current consumption in this mode is I_{ACTIVE}. (excluding current through switched on current source) and the charge pump, if required. The charge pump can be automatically switched on/off depending on the pattern (set register cp_auto_on on page 16=1) to reduce the overall current consumption.

3. All times can be extended by a factor of 8 by setting pattern_slow=1 (this result in a delay of up to 56s)

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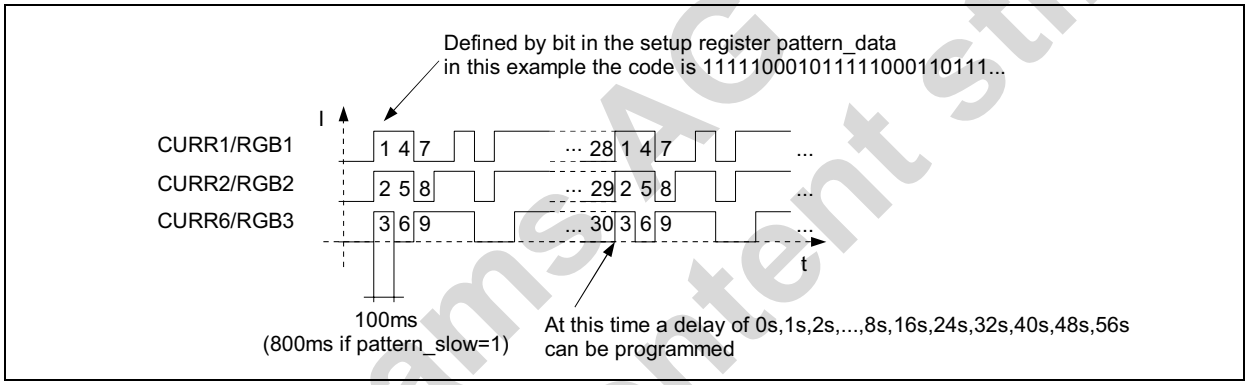
Figure 16. LED Pattern Generator AS3677 *for pattern_color = 0*



To select the different current sinks to be controlled by the LED pattern generator, see the 'xxxx'_mode registers (where 'xxxx' stands for the to be controlled current sink, e.g. curr1_mode for CURR1 current sink). See also the description of the different current sinks.

To allow the generator of a color patterns set the bit pattern_color to '1'. Then the pattern can be connected to CURRx as follows:

Figure 17. LED Pattern Generator AS3677 *for pattern_color = 1*



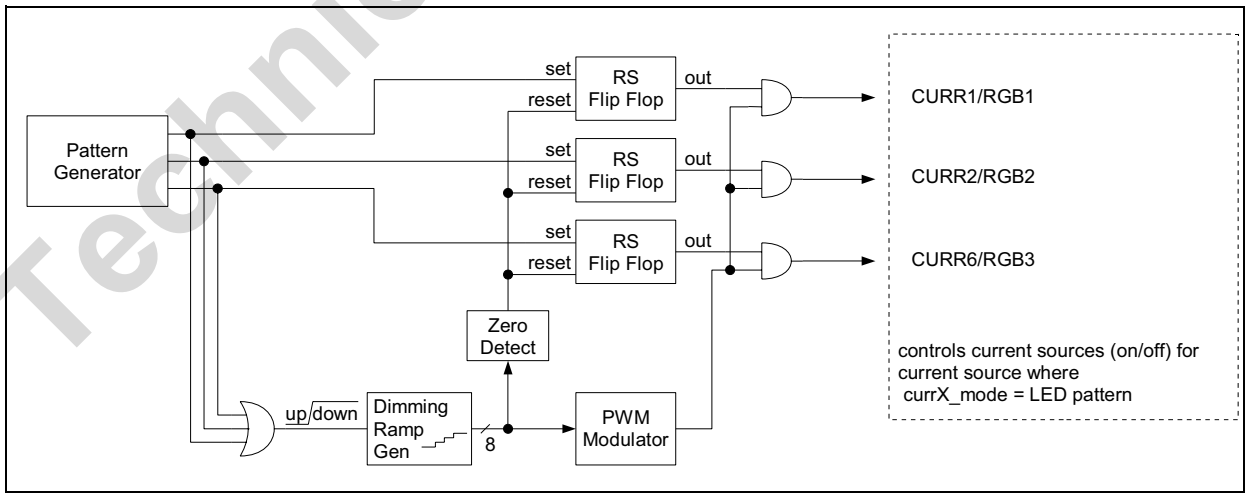
Only those current sinks will be controlled, where the 'xxxx'_mode register is configured for LED pattern.

If the register bit pattern_slow is set, all pattern times are increased by a factor of eight. (bit duration: 250ms if pattern_color=0 / 800ms if pattern_color=1, delays between pattern up to 56s).

Soft Dimming for Pattern

The internal pattern generator can be combined with the internal pwm dimming modulator to obtain as shown in the following figure:

Figure 18. Soft dimming Architecture for the AS3677 *(softdim_pattern=1 and pattern_color = 1)*

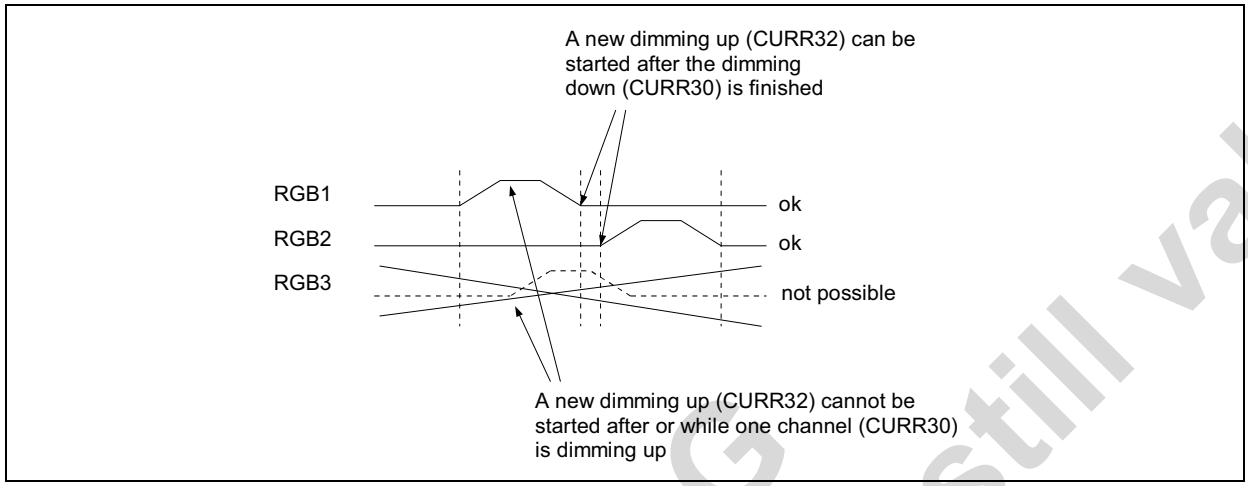


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With the AS3677 smooth fade-in and fade-out effects can be automatically generated.

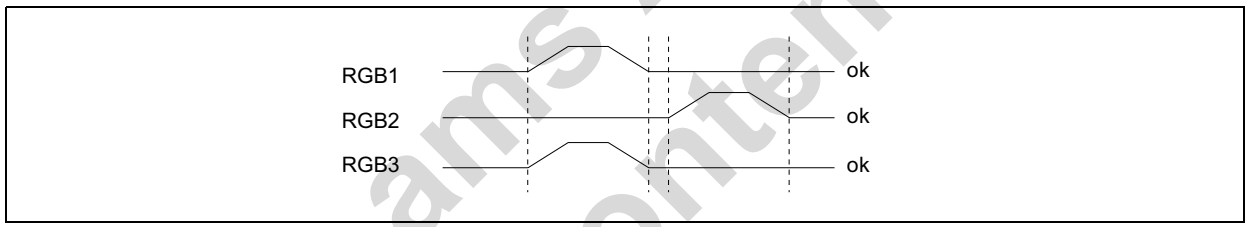
As there is only one dimming ramp generator and one pwm modulator following constraints have to be considered when setting up the pattern (applies only if pattern_color=1):

Figure 19. Soft dimming example Waveform for CURR30-32



However using the identical dimming waveform for two channels is possible as shown in the following figure:

Figure 20. Soft dimming example Waveform for CURR30-32



LED Pattern Registers

Table 31. Pattern data0...Pattern data3 Registers

Addr: 19h,1Ah,1Bh,1Ch		Pattern data0, Pattern data1, Pattern data2, Pattern data3		
		This registers contains the pattern data for the current sinks.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	pattern_data_0[1]	0	R/W	Pattern data0
7:0	pattern_data_1	0	R/W	Pattern data1
7:0	pattern_data_2	0	R/W	Pattern data2
7:0	pattern_data_3	0	R/W	Pattern data3

1. Update any of the pattern register only if none of the current sources is connected to the pattern generator ('xxxx'_mode must not be 11b). The pattern generator is automatically started at the same time when any of the current sources is connected to the pattern generator

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Table 32. Pattern control Register

Addr: 18h		Pattern control			
		This register controls the LED pattern			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	pattern_color	0	R/W	Defines the pattern type for the current sinks	
				0b	single 32 bit pattern (also set currX_mode = 11)
				1b	RGB pattern with each 10 bits (set all currX_mode = 11)
2:1	pattern_delay	00b	R/W	Delay between pattern, details (see Table 35); together with pattern_delay2 sets the delay time between patterns	
3	softdim_pattern	0b	R/W	Enable the 'soft' dimming feature for the pattern generator	
				0	Pattern generator directly control current sources
				1	'Soft Dimming' is performed (see page 24)

Table 33. Gpio current Register

Addr: 2Ch		Gpio current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	pattern_delay2	0	R/W	Delay between pattern (see Table 35 on page 26); together with pattern_delay sets the delay time between patterns	
6	pattern_slow	0	R/W	Pattern timing control	
				0b	normal mode
				1b	slow mode (all pattern times are increased by a factor of eight)

Table 34. Pattern End Register

Addr: 54h		Pattern End		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	pattern_end	0	R	pattern_end is toggled from 0 to 1 (or from 1 to 0) at each end of the pattern just before restarting of the internal pattern generator at the first bit of the pattern data (can be used to synchronize the baseband software to the pattern generator)[1]

1. pattern_end toggles whenever the AS3677 is in active mode (see Section 8.11 Operating Modes on page 58) even if no pattern data has been setup.

Table 35. LED Pattern timing

pattern_slow	pattern_delay2	pattern_delay[1..0]	bit duration [ms]		delay [s] between patterns	pattern duration [s] (total cycle time: pattern + delay)
	delay between patterns		pattern_color=0	pattern_color=1		
0	0	00	31	100	0[1]	1
0	0	01	31	100	1	2
0	0	10	31	100	2	3
0	0	11	31	100	3	4

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Table 35. LED Pattern timing

pattern_slow	pattern_delay2	pattern_delay[1..0]	bit duration [ms]		delay [s] between patterns	pattern duration [s] (total cycle time: pattern + delay)
	delay between patterns		pattern_color=0	pattern_color=1		
0	1	00	31	100	4	5
0	1	01	31	100	5	6
0	1	10	31	100	6	7
0	1	11	31	100	7	8
1	0	00	250	800	0	8
1	0	01	250	800	8	16
1	0	10	250	800	16	24
1	0	11	250	800	24	32
1	1	00	250	800	32	40
1	1	01	250	800	40	48
1	1	10	250	800	48	56
1	1	11	250	800	56	64

1. Even by setting 000 for pattern delay, there is a small delay before the new patterns starts.

8.4.5 PWM Generator

The PWM generator can be used for any current sink. The setting applies for all current sinks, which are controlled by the pwm generator (e.g. CURR1 is pwm controlled if curr1_mode = 10). The pwm modulated signal can switch on/off the current sinks and therefore depending on its duty cycle change the brightness of an attached LED.

Internal PWM Generator

The internal PWM generator uses the 2MHz internal clock as input frequency and its dimming range is 6 bits digital (2MHz / 2^6 = 31.3kHz pwm frequency) and 2 bits analog. Depending on the actual code in the register pwm_code the following algorithm is used:

If pwm_code bit 7 = 1

Then the upper 6 bits (Bits 7:2) of pwm_code are used for the 6 bits PWM generation, which controls the selected currents sinks directly

If pwm_code bit 7 =0 and bit 6 = 1

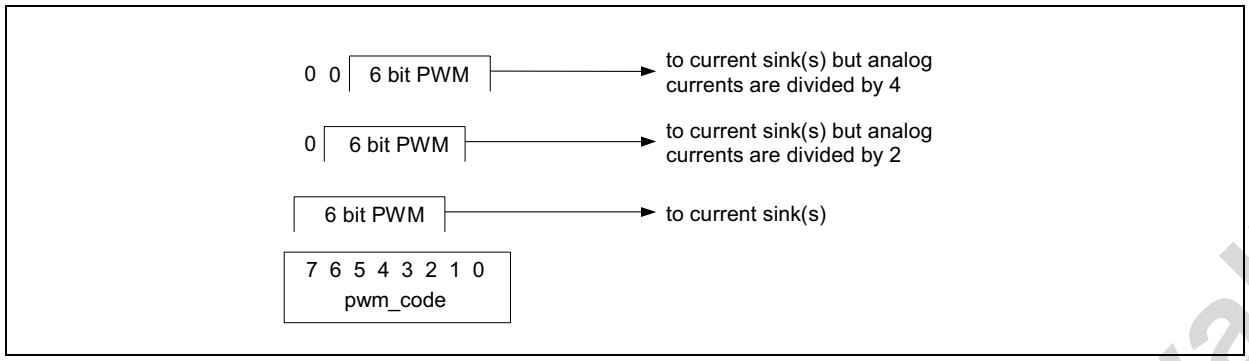
Then bits 6:1 of pwm_code are used for the 6 bits PWM generation. This signal controls the selected current sinks, but the analog current of these sinks is divided by 2

If pwm_code bit 7 and bit 6 = 0

Then bits 5:0 of pwm_code are used for the 6 bits PWM generation. This signal controls the selected current sinks, but the analog current of these sinks is divided by 4

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Figure 21. PWM Control

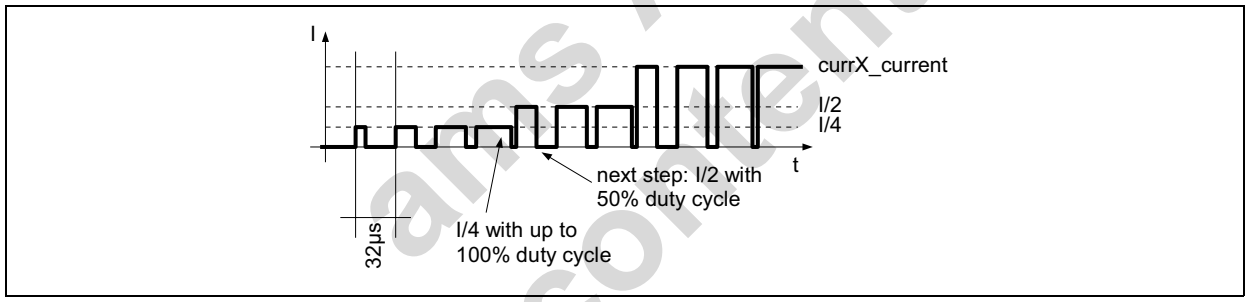


Automatic Up/Down Dimming

If the register pwm_dim_mode is set to 01 (up dimming) or 10 (down dimming) the value within the register pwm_code is increased (up dimming) or decreased (down dimming) every time and amount (either 1/4th or 1/8th) defined by the register pwm_dim_speed. The maximum value of 255 (completely on) and the minimum value of 0 (off) is never exceeded. It is used to smoothly and automatically dim the brightness of the LEDs connected to any of the current sinks. The PWM code is readable all the time (also during up and down dimming).

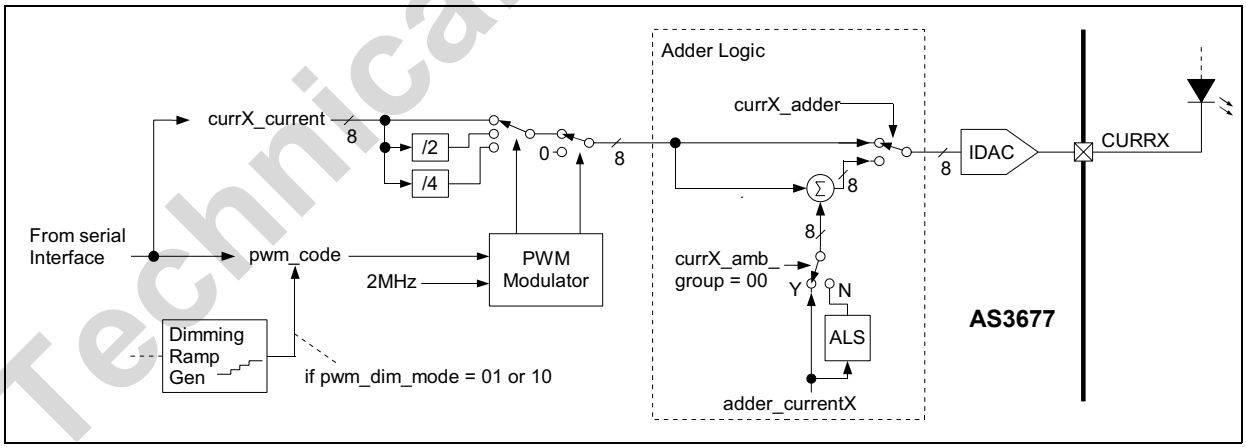
The waveform for up dimming looks as follows (cycles omitted for simplicity):

Figure 22. PWM Dimming Waveform for up dimming (pwm_dim_mode = 01); currX_mode = PWM controlled (not all steps shown)



The internal pwm modulator circuit controls the current sinks as shown in the following figure:

Figure 23. PWM Control Circuit (currX_mode = 10b (PWM controlled)); X = any current sink



The adder logic (available for all current sinks) is intended to allow dimming not only from 0% to 100% (or 100% to 0%) of currX_current, but also e.g. from 10% to 110% (or 110% to 10%) of currX_current. The starting current for up dimming is defined by 0 + currX_adder and the end current is defined by currX_current + currX_adder.

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An overflow of the internal bus (8 Bits wide to the IDAC) has to be avoided by the register settings (currX_current + currX_adder must not exceed 255).

Note: The adder logic operates independent of the currX_mode setting, but its main purpose is to work together with the pwm modulator (improved up/down dimming)

If the adder logic is not used anymore, set the bit currX_adder to 0. (Setting adder_currentX to 0 is not sufficient)

At the end of up/down dimming, the pwm_code register keeps its final value (for up-dimming 255 and for down-dimming 0). This can be used to identify the exact time, when up/down dimming is finished.

Table 36. PWM Dimming Table

	Decrease by 1/4th every step		Decrease by 1/8th every step		Seconds	Seconds	Seconds	Seconds
Step	%Dimming	PWM	%Dimming	PWM	50msec/ Step	25msec/ Step	5msec/ Step	2.5msec/ Step
1	100,0	255	100,0	255	0,00s	0,00s	0,000s	0,000s
2	75,3	192	87,8	224	0,05s	0,03s	0,005s	0,003s
3	56,5	144	76,9	196	0,10s	0,05s	0,010s	0,005s
4	42,4	108	67,5	172	0,15s	0,08s	0,015s	0,008s
5	31,8	81	59,2	151	0,20s	0,10s	0,020s	0,010s
6	23,9	61	52,2	133	0,25s	0,13s	0,025s	0,013s
7	18,0	46	45,9	117	0,30s	0,15s	0,030s	0,015s
8	13,7	35	40,4	103	0,35s	0,18s	0,035s	0,018s
9	10,6	27	35,7	91	0,40s	0,20s	0,040s	0,020s
10	8,2	21	31,4	80	0,45s	0,23s	0,045s	0,023s
11	6,3	16	27,5	70	0,50s	0,25s	0,050s	0,025s
12	4,7	12	24,3	62	0,55s	0,28s	0,055s	0,028s
13	3,5	9	21,6	55	0,60s	0,30s	0,060s	0,030s
14	2,7	7	19,2	49	0,65s	0,33s	0,065s	0,033s
15	2,4	6	16,9	43	0,70s	0,35s	0,070s	0,035s
16	2,0	5	14,9	38	0,75s	0,38s	0,075s	0,038s
17	1,6	4	13,3	34	0,80s	0,40s	0,080s	0,040s
18	1,2	3	11,8	30	0,85s	0,43s	0,085s	0,043s
19	0,8	2	10,6	27	0,90s	0,45s	0,090s	0,045s
20	0,4	1	9,4	24	0,95s	0,48s	0,095s	0,048s
21	0,0	0	8,2	21	1,00s	0,50s	0,100s	0,050s
22			7,5	19	1,05s	0,53s	0,105s	0,053s
23			6,7	17	1,10s	0,55s	0,110s	0,055s
24			5,9	15	1,15s	0,58s	0,115s	0,058s
25			5,5	14	1,20s	0,60s	0,120s	0,060s
26			5,1	13	1,25s	0,63s	0,125s	0,063s
27			4,7	12	1,30s	0,65s	0,130s	0,065s
28			4,3	11	1,35s	0,68s	0,135s	0,068s
29			3,9	10	1,40s	0,70s	0,140s	0,070s

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Table 36. PWM Dimming Table

	Decrease by 1/4th every step		Decrease by 1/8th every step		Seconds	Seconds	Seconds	Seconds
Step	%Dimming	PWM	%Dimming	PWM	50msec/ Step	25msec/ Step	5msec/ Step	2.5msec/ Step
30			3,5	9	1,45s	0,73s	0,145s	0,073s
31			3,1	8	1,50s	0,75s	0,150s	0,075s
32			2,7	7	1,55s	0,78s	0,155s	0,078s
33			2,4	6	1,60s	0,80s	0,160s	0,080s
34			2,0	5	1,65s	0,83s	0,165s	0,083s
35			1,6	4	1,70s	0,85s	0,170s	0,085s
36			1,2	3	1,75s	0,88s	0,175s	0,088s
37			0,8	2	1,80s	0,90s	0,180s	0,090s
38			0,4	1	1,85s	0,93s	0,185s	0,093s
39			0,0	0	1,90s	0,95s	0,190s	0,095s

PWM Generator Registers

Table 37. Pwm control Register

Addr: 16h		Pwm control			
		This register controls PWM generator			
Bit	Bit Name	Default	Access	Description	
2:1	pwm_dim_mode	00b	R/W	Selects the dimming mode	
				00b	no dimming; actual content of register pwm_code is used for pwm generator
				01b	logarithmic up dimming (codes are increased). Start value is actual pwm_code
				10b	logarithmic down dimming (codes are decreased). Start value is actual pwm_code; switch off the dimmed current source after dimming is finished to avoid unnecessary quiescent current
				11b	NA
5:3	pwm_dim_speed	000b	R/W	Defines dimming speed by increase/decrease pwm_code	
				000b	by 1/4th every 50 msec (total dim time 1.0s)
				001b	by 1/8th every 50 msec (total dim time 1.9s)
				010b	by 1/4th every 25 msec (total dim time 0.5s)
				011b	by 1/8th every 25 msec (total dim time 0.95s)
				100b	by 1/4th every 5 msec (total dim time 100ms)
				101b	by 1/8th every 5 msec (total dim time 190ms)
				110b	by 1/4th every 2.5 msec (total dim time 50ms)
				111b	by 1/8th every 2.5 msec (total dim time 95ms)

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Table 38. Pwm code Register

Addr: 17h		Pwm code			
		This register controls the Pwm code.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	pwm_code	00b	R/W	Selects the PWM code	
				00h	0% duty cycle
				....	....
				FFh	100% duty cycle

Table 39. Adder Current 1 Register

Addr: 30h		Adder Current 1			
		This register defines the current which can be added to CURR1, CURR30, CURR41, RGB1			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	adder_current1	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text)	
				00h	0 (represents 0mA)
				....	....
				FFh	255 (represents 25.5mA)

Table 40. Adder Current 2 Register

Addr: 31h		Adder Current 2			
		This register defines the current which can be added to CURR2, CURR31, CURR42, RGB2			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	adder_current2	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text)	
				00h	0 (represents 0mA)
				....	....
				FFh	255 (represents 25.5mA)

Table 41. Adder Current 3 Register

Addr: 32h		Adder Current 3			
		This register defines the current which can be added to CURR6, CURR32, CURR43, RGB3			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	adder_current3	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text)	
				00h	0 (represents 0mA)
				....	....
				FFh	255 (represents 25.5mA)

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Table 42. Adder Enable 2 Register

Addr: 34h		Adder Enable 2			
		Enables the adder circuit for the selected current sources			
Bit	Bit Name	Default	Access	Description	
0	curr1_adder	0	R/W	Enables adder circuit for current source CURR1	
				0	Normal Operation of the current source
				1	adder_current1 gets added to the current source current; if curr1_amb_group is not 00, the adder current is multiplied by the ALS group selected by curr1_amb_group
1	curr2_adder	0	R/W	Enables adder circuit for current source CURR2	
				0	Normal Operation of the current source
				1	adder_current2 gets added to the current source current; if curr2_amb_group is not 00, the adder current is multiplied by the ALS group selected by curr2_amb_group
2	curr6_adder	0	R/W	Enables adder circuit for current source CURR6	
				0	Normal Operation of the current source
				1	adder_current3 gets added to the current source current; if curr6_amb_group is not 00, the adder current is multiplied by the ALS group selected by curr6_amb_group

Table 43. Adder Enable 1 Register

Addr: 33h		Adder Enable 1			
		Enables the adder circuit for the selected current sources			
Bit	Bit Name	Default	Access	Description	
0	rgb1_adder	0	R/W	Enables adder circuit for current source RGB1	
				0	Normal Operation of the current source
				1	adder_current1 gets added to the current source current
1	rgb2_adder	0	R/W	Enables adder circuit for current source RGB2	
				0	Normal Operation of the current source
				1	adder_current2 gets added to the current source current
2	rgb3_adder	0	R/W	Enables adder circuit for current source RGB3	
				0	Normal Operation of the current source
				1	adder_current3 gets added to the current source current

8.4.6 ALS - Ambient Light Sensing

The ADC converts every 1ms the ambient light sensor signal from pin ALS/GPIO1[4]. This signal is pre-processed with a offset defined by amb_offset and a gain defined by amb_gain (1/4, 1/2, 1, 2). Then it is low-pass filtered with a programmable cut-off frequency going from 0.25Hz to 32Hz. Increasing signals and decreasing signal can have individual cut-off frequencies adjustable from 0.25Hz to 32Hz (amb_filter_up and amb_filter_down).

This filtered signal can be readout from the register amb_result<7:0>.

4. adc_select=02h (select ALS/GPIO1 input)

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Each of the available three channels (N=1 or 2) has six 8-bit registers:

- groupN_y0: define current multiplier for values below groupN_X1
- groupN_y3: define current multiplier for high values (actual starting point defined by groupN_x1,groupN_k1 and groupN_x2,groupN_k2)
- groupN_x1, groupN_k1: If ADC reading is > groupN_x1 then groupN_k1 divided by 32 defines the slope of the first ramp
- groupN_x2, groupN_k2: If ADC reading is > groupN_x2 then groupN_k2 divided by 32 defines the slope of the second ramp

Each current sources has a 2 bit register (currX_amb_group) to select None, Group1 or Group2 of ambient light sensing.

The calculations are done every 1ms resulting in a flicker-free 1000Hz update rate of the current sources.

Note: The ADC is switched off between conversion to save power.

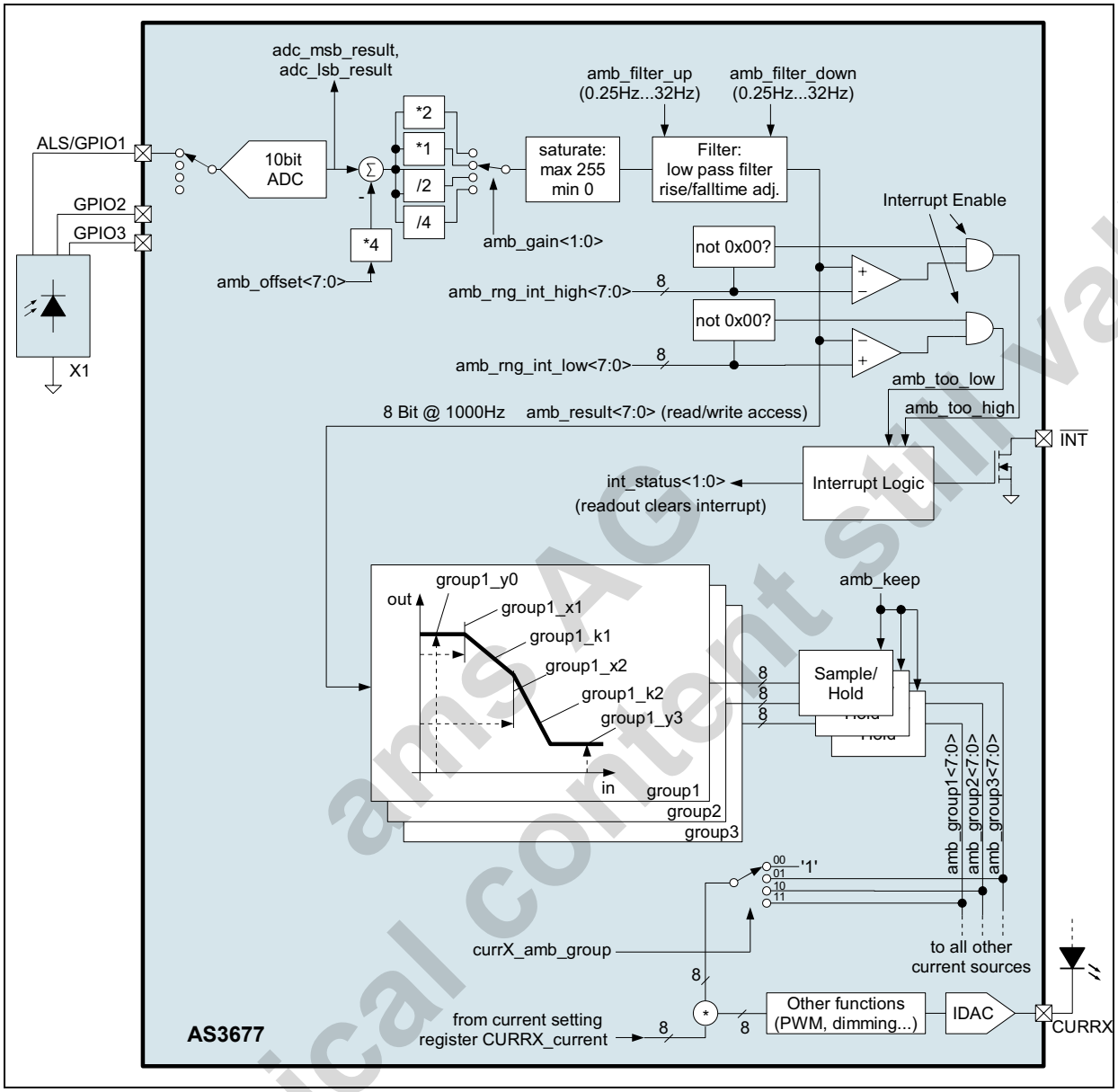
All groupN_k1 and groupN_k2 values are divided by 32 except group3_k1 (see page 39), which is divided by 1. This allows a step response to a small change in the input signal (e.g. for keyboard backlight).

Table 44. ALS Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{ALSON}	ALS operating current	averaged; excluding LDO supplying external sensor - see LDO on page 9		19		µA

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Figure 24. Ambient Light Sensor and Interrupt Logic internal circuit



Ambient Light Sensor Registers

Table 45. ALS control Register

Addr: 90h		ALS control			
		control ambient light sensing			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	amb_on	0	R/W	Enables the ambient light sensing feature	
				0	ambient light sensor disabled
				1	ambient light sensor enabled

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Table 45. ALS control Register (Continued)

Addr: 90h		ALS control		
		control ambient light sensing		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:1	amb_gain	0	R/W	Control Ambient Light Sensor preprocessing gain
				00 gain = 1/4
				01 gain = 1/2
				10 gain = 1
				11 gain = 2
3	amb_keep	0	R/W	Enable S/H of group tables output - see Figure 24 on page 34
				0 Group output is enabled (S/H = sampling)
				1 Groups outputs on hold (S/H = hold)

Table 46. ALS filter Register

Addr: 91h		ALS filter		
		control for ambient light sensor filtering		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	amb_filter_up	000	R/W	Controls the filter cut off (-3dB) frequency (increasing)
				000 0.25Hz
				001 0.5Hz
				010 1Hz
				011 2Hz
				100 4Hz
				101 8Hz
				110 16Hz
				111 32Hz
6:4	amb_filter_down	000	R/W	Controls the filter cut off (-3dB) frequency (decreasing)
				000 0.25Hz
				001 0.5Hz
				010 1Hz
				011 2Hz
				100 4Hz
				101 8Hz
				110 16Hz
				111 32Hz

Table 47. ALS offset Register

Addr: 92h		ALS offset		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	amb_offset	00h	R/W	Controls the offset of the ambient light sensor

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Table 48. ALS result Register

Addr: 93h		ALS result		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	amb_result	00h	R	Filtered result of the ambient light sensor value
			W	Pre-set the value of the ALS filter (especially useful when doing gain switching of the ALS sensor)

Table 49. ALS curr12 group Register

Addr: 94h		ALS curr12 group			
		controls the group mapping for CURR1 and CURR2			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	curr1_amb_group	00	R/W	CURR1 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
3:2	curr2_amb_group	00	R/W	CURR2 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3

Table 50. ALS rgb group Register

Addr: 95h		ALS rgb group			
		controls the group mapping for RGB1, RGB2, RGB3 and CURR6			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	rgb1_amb_group	00	R/W	RGB1 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
3:2	rgb2_amb_group	00	R/W	RGB2 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
5:4	rgb3_amb_group	00	R/W	RGB3 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3

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Table 50. ALS rgb group Register (Continued)

Addr: 95h		ALS rgb group			
		controls the group mapping for RGB1, RGB2, RGB3 and CURR6			
Bit	Bit Name	Default	Access	Description	
7:6	curr6_amb_group	00	R/W	CURR6 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3

Group1

Table 51. ALS group 1 Y0 Register

Addr: 98h		ALS group 1 Y0		
Bit	Bit Name	Default	Access	Description
7:0	group1_y0	00h	R/W	Group 1 y0 value - divided by 256

Table 52. ALS group 1 Y3 Register

Addr: 99h		ALS group 1 Y3		
Bit	Bit Name	Default	Access	Description
7:0	group1_y3	00h	R/W	Group 1 y3 value - divided by 256

Table 53. ALS group 1 X1 Register

Addr: 9Ah		ALS group 1 X1		
Bit	Bit Name	Default	Access	Description
7:0	group1_x1	00h	R/W	Group 1 x1 value

Table 54. ALS group 1 K1 Register

Addr: 9Bh		ALS group 1 K1		
Bit	Bit Name	Default	Access	Description
7:0	group1_k1	00h	R/W	Group 1 k1 value - divided by 32 defines first slope

Table 55. ALS group 1 X2 Register

Addr: 9Ch		ALS group 1 X2		
Bit	Bit Name	Default	Access	Description
7:0	group1_x2	00h	R/W	Group 1 x2 value

Table 56. ALS group 1 K2 Register

Addr: 9Dh		ALS group 1 K2		
Bit	Bit Name	Default	Access	Description
7:0	group1_k2	00h	R/W	Group 1 k2 value- value divided by 32 defines second slope

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Group2

Table 57. ALS group 2 Y0 Register

Addr: 9Eh		ALS group 2 Y0		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_y0	00h	R/W	Group 2 y0 value - divided by 256

Table 58. ALS group 2 Y3 Register

Addr: 9Fh		ALS group 2 Y3		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_y3	00h	R/W	Group 2 y3 value - divided by 256

Table 59. ALS group 2 X1 Register

Addr: A0h		ALS group 2 X1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_x1	00h	R/W	Group 2 x1 value

Table 60. ALS group 2 K1 Register

Addr: A1h		ALS group 2 K1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_k1	00h	R/W	Group 2 k1 value - divided by 32 defines first slope

Table 61. ALS group 2 X2 Register

Addr: A2h		ALS group 2 X2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_x2	00h	R/W	Group 2 x2 value

Table 62. ALS group 2 K2 Register

Addr: A3h		ALS group 2 K2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_k2	00h	R/W	Group 2 k2 value- value divided by 32 defines second slope

Group3

Table 63. ALS group 3 Y0 Register

Addr: A4h		ALS group 3 Y0		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_y0	00h	R/W	Group 3 y0 value - divided by 256

Table 64. ALS group 3 Y3 Register

Addr: A5h		ALS group 3 Y3		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_y3	00h	R/W	Group 3 y3 value - divided by 256

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Table 65. ALS group 3 X1 Register

Addr: A6h		ALS group 3 X1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_x1	00h	R/W	Group 3 x1 value

Table 66. ALS group 3 K1 Register

Addr: A7h		ALS group 3 K1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_k1	00h	R/W	Group 3 k1 value - divided by ***1*** defines first slope

Table 67. ALS group 3 X2 Register

Addr: A8h		ALS group 3 X2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_x2	00h	R/W	Group 3 x2 value

Table 68. ALS group 3 K2 Register

Addr: A9h		ALS group 3 K2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_k2	00h	R/W	Group 3 k2 value- value divided by 32 defines second slope

The output of the group selection circuit (after the S/H circuit) can be observed with following registers:

Table 69. ALS group output 1 Register

Addr: AAh		ALS group output 1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	amb_group1	00h	R	Ambient Light Sensor Group 1 output register

Table 70. ALS group output 2 Register

Addr: ABh		ALS group output 2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	amb_group2	00h	R	Ambient Light Sensor Group 2 output register

Table 71. ALS group output 3 Register

Addr: ACh		ALS group output 3		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	amb_group3	00h	R	Ambient Light Sensor Group 3 output register

The range selection interrupt threshold and interrupt enable is defined by following registers amb_range_int_high and amb_range_int_low:

Table 72. ALS range high interrupt threshold Register

Addr: ADh		ALS range high interrupt threshold		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	amb_range_int_high	00h	R/W	If the filter output amb_result >= amb_range_int_high then an amb_too_high interrupt is asserted If amb_range_int_high=0, the interrupt is disabled

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Table 73. ALS range low interrupt threshold Register

Addr: AEh		ALS range low interrupt threshold		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	amb_range_int_low	00h	R/W	If the filter output amb_result <= amb_range_int_low then an amb_too_low interrupt is asserted If amb_range_int_low=0, the interrupt is disabled

The range selection generates an interrupt by pulling the pin $\overline{INT}$ low (if any of the register bit of Interrupt Status are set, $\overline{INT}$ is pulled low(. When the register Interrupt Status is readout, the interrupt is automatically cleared:

Table 74. Interrupt Status Register

Addr: AFh		Interrupt Status			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	amb_too_high	0	R/sC[1]	Comparator for amb_result >= amb_range_int_high	
				0	not triggered
				1	triggered
1	amb_too_low	0	R/sC[1]	Comparator for amb_result <= amb_range_int_low	
				0	not triggered
				1	triggered

1. Read - self clear. The register automatically clears it content after readout. This avoids any lost interrupts.

8.4.7 DLS(=DBC) - Dynamic Luminance Scaling Input

The pins DLS1 and DLS2 can be used for dynamic backlight scaling input. Dynamic backlight scaling is used to reduce the power of the backlight especially when showing dark picture contents on the display. The control unit to operate DLS is the display processor sending a PWM signal to the AS3677 and in parallel changing the display content to compensate for a reduced brightness backlight.

The AS3677 can use the DLS (Dynamic Luminance Scaling) (also called DBC = Dynamic Backlight Control) in two different operating modes:

1. Digital DLS Mode - selected by dls_analog=0: The input signal from pins DLS1 and DLS2 are controlling the current source directly. A logic 'L' switches off the selected current source and a logic 'H' enables the current source with the configured current. This operating mode is compatible to the AS3676 processing of DLS.
2. Analog DLS Mode - selected by dls_analog=1: In this operating mode, the input signals form DLS1 and DLS2 are digitally filtered (two parallel filters are possible!) and smoothly controls the current through the selected

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current source(s). Therefore the output signal does not show any PWM signal and therefore reduces the noise in noise sensitive systems - especially if the connection to the LED used long wires.

Note: For any current source, do not use DLS and the internal PWM generator (see PWM Generator on page 27) at the same time.

Table 75. DLS Input Parameters

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{DLS}	DLS input frequency range	pins DLS1 and DLS2 if used for DLS (any bit set: curr1_on_dls, curr2_on_dls or curr6_on_dls); pin DLS1 if used for RGB1, RGB2 and RGB3 (only 'digital' DLS)	dls_analog=0	25		1000	kHz
			dls_analog=1	300[1]		25000[1]	Hz
f_{DLS_FILTER}	DLS internal filter 3dB cutoff frequency	dls_analog=1, low pass filter 4th order			2		kHz
V_{IHDLS}	High Level Input Voltage	pins DLS1 and DLS2		1.38		VBAT	V
V_{ILDLS}	Low Level Input Voltage					0.52	V
I_{LEAK}	Input Leakage Current	to VBAT or VSS		-5		5	µA

1. For duty cycles >5%

Note: If using dls_analog=1, the minimum PWM ratio is limited by the LED performance. If the analog current is reduced too much, it might result in unevenness of the display backlight (as the LEDs are usually not specified at very low current operation).

RGB1, RGB2 and RGB3 can only use 'digital' DLS - the register dls_analog does have no influence.

The analog processing of the DLS signal works as follows (dls_analog=1):

1. The input signal from pins DLS1 and DLS2 are feed into the digital filter. A logic 'L' is converted into '0.000' and a logic 'H' is converted into '1.000'.
2. The digital filter processes this signal. The filter itself is implemented as a 4th order low pass filter with fixed coefficients. Its 3dB cut-off frequency is set to f_{DLS_FILTER}.
3. The output signal (fixed comma binary 8 bit signal) is multiplied by the individual current setting.
4. From this 8 x 8 multiplication (16bit result), the 8 MSBs are used.

This value is converted with a current DAC into a current, which controls the LED.

8.4.8 Unused DLS Input Pins

The pins DLS1 and DLS2 should be connected to VSS if not used.

8.4.9 DLS Internal Processing

The internal processing is shown in Figure 25:

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Figure 25. DLS (Dynamic Luminance Scaling) internal circuit shown for a single current sink

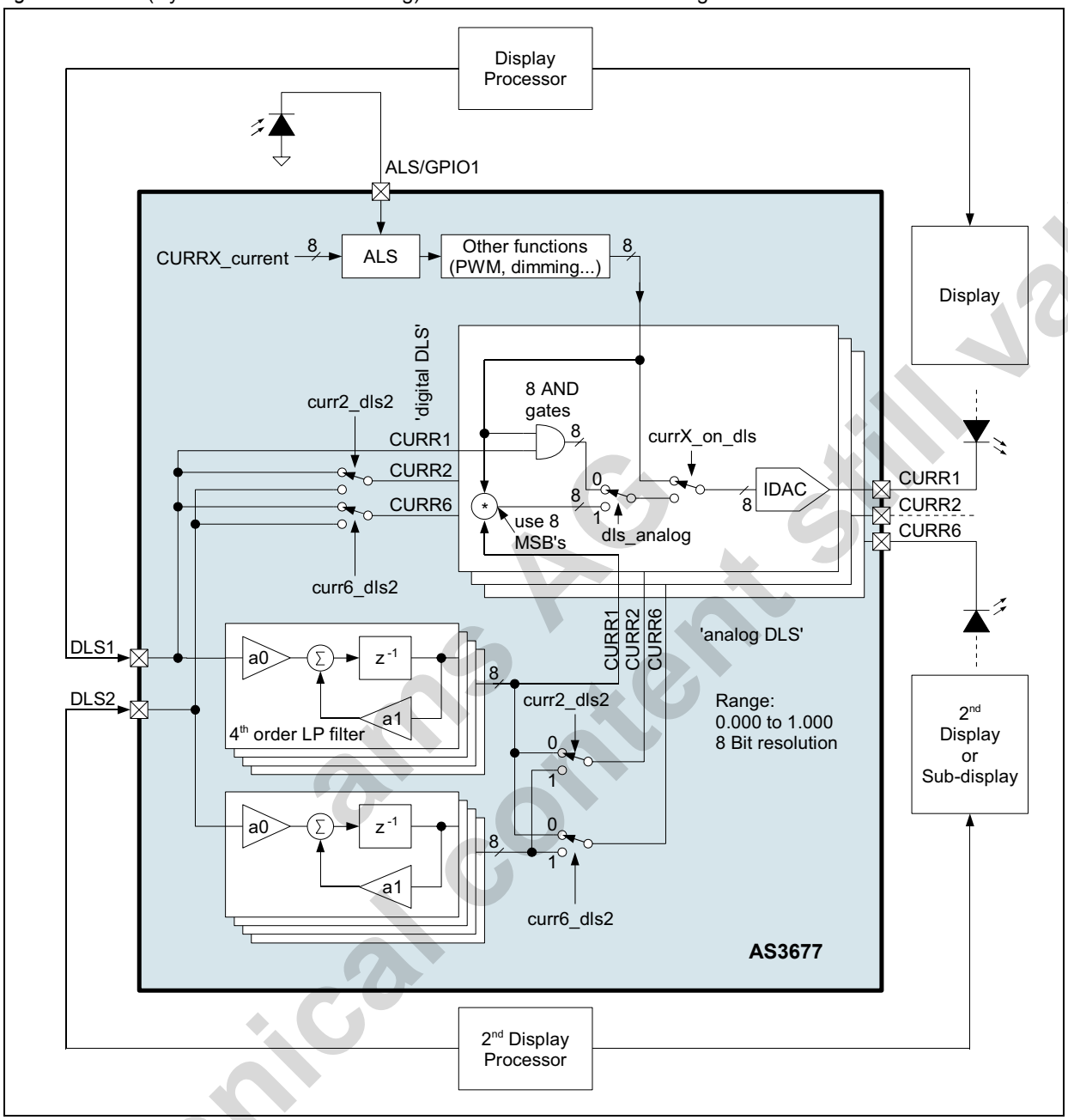


Table 76. DLS mode control1 Register

Addr: 56h		DLS mode control1			
		Setup which current sinks are connected to the DLS; if set to '1' the correspond current source (sink) is combined with the DLS input			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	rgb1_on_dls	0	R/W	0	RGB1 current sink is not combined with DLS
				1[1]	RGB1 current sink is combined with DLS (only 'digital' DLS with input pin DLS1)

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Table 76. DLS mode control1 Register (Continued)

Addr: 56h		DLS mode control1			
		Setup which current sinks are connected to the DLS; if set to '1' the correspond current source (sink) is combined with the DLS input			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5	rgb2_on_dls1	0	R/W	0	RGB2 current sink is not combined with DLS
				1[1]	RGB2 current sink is combined with DLS (only 'digital' DLS with input pin DLS1)
6	rgb3_on_dls	0	R/W	0	RGB3 current sink is not combined with DLS
				1[1]	RGB3 current sink is combined with DLS (only 'digital' DLS with input pin DLS1)
7	dls_analog	0	R/W	0	'digital' DLS for all current sinks
				1	'analog' DLS for CURR1, CURR2 and CURR6 if enabled

1. When this bit is set, do not use the internal PWM generator for this current source at the same time.

Table 77. DLS mode control2 Register

Addr: 57h		DLS mode control2			
		Setup which current sinks are connected to the DLS; if set to '1' the correspond current source (sink) is combined with the DLS input			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr1_on_dls	0	R/W	0	CURR1 current sink is not combined with DLS
				1[1]	CURR1 current sink is combined with DLS
1	curr2_on_dls	0	R/W	0	CURR2 current sink is not combined with DLS
				1[1]	CURR2 current sink is combined with DLS
5	curr2_dls2	0	R/W	0	CURR2 uses DLS1 as input
				1	CURR2 uses DLS2 as input
6	curr6_dls2	0	R/W	0	CURR6 uses DLS1 as input
				1	CURR6 uses DLS2 as input
7	curr6_on_dls	0	R/W	0	CURR6 current sink is not combined with DLS
				1[1]	CURR6 current sink is combined with DLS

1. When this bit is set, do not use the internal PWM generator for this current source at the same time.

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8.5 General Purpose Input / Output

The pin DLS1, DLS2 are digital input, $\overline{INT}$ is an open drain output and ALS/GPIO1, GPIO2 and GPIO3 are a highly-configurable general purpose input/output pins which can be used for the following functionality:

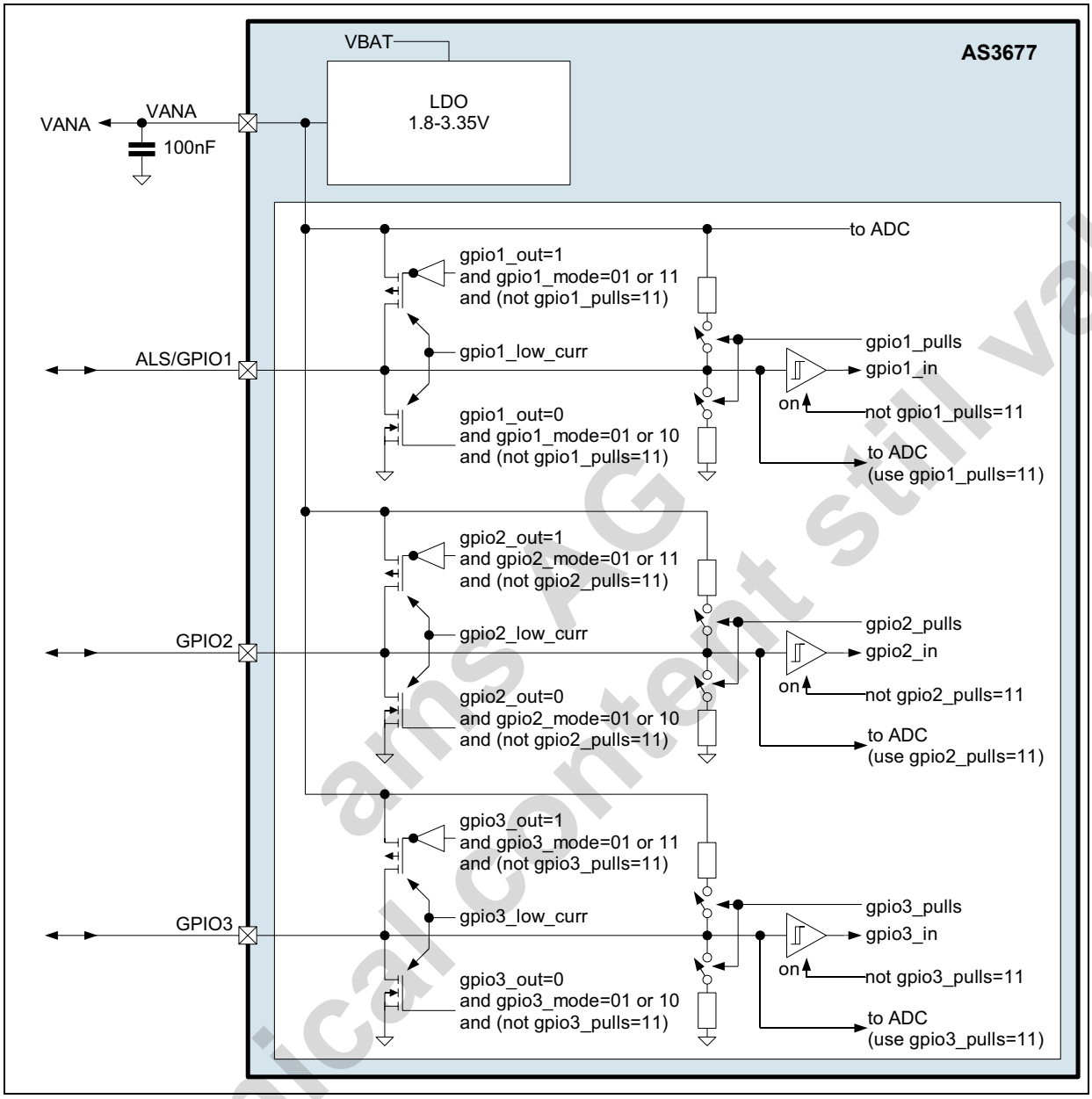
- DLS1 and DLS2 primary function is a DLS input - see DLS(=DBC) - Dynamic Luminance Scaling Input on page 40
- ALS/GPIO1 primary function is ALS input - see ALS - Ambient Light Sensing on page 32
- Digital Schmitt Trigger Input
- Digital Output with 4mA Driving Capability at 2.8V Supply (VANA)
- Tristate Output
- Analog Input to the ADC
- Default Mode for ALS/GPIO1 is ADC input (as required for the ALS function), GPIO2 and GPIO3 is Input with Pull-Down

Table 78. GPIO *Pin Function Summary*

GPIO3 Pin	Configuration	Additional Function
ALS/GPIO1	Digital Input, Totem-Pole Output (Push/Pull), Open Drain (PMOS or NMOS), High-Z, Pull-Down or Pull-Up Resistor	ADC Input, ALS - light sensor input (see page 32)
GPIO2, GPIO3		ADC Input
DLS1, DLS2	Digital Input	ADC Input, PWM Input, DLS input (see page 40)
$\overline{INT}$	Open Drain Output	ADC Input

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Figure 26. GPIOs and VANA Blockdiagram



8.5.1 Unused GPIO and digital Input Pins

If the pins ALS/GPIO1, GPIO2 or GPIO3 are not used, they can be left open (an internal pulldown, which is enabled by default, will pull them to GND, ALS/GPIO1 is configured as ADC input). The pins DLS1 and DLS2 should be connected to VSS, $\overline{INT}$ can be left open.

8.5.2 GPIO and Digital Inputs Characteristics

Table 79. GPIO and digital inputs DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Rpull	Pull up/Pull down Resistance	enabled by gpio1_pulls, gpio2_pulls and gpio3_pulls	30		75	kΩ
V_{GPIO}	Supply Voltage	=VANA	1.8		3.35	V

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Table 79. GPIO and digital inputs DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIHGPIO	High Level Input Voltage	pins ALS/GPIO1, GPIO2 and GPIO3	1.38		VANA	V
VILGPIO	Low Level Input Voltage				0.52	V
VHYS	Hysteresis			0.1		V
ILEAK	Input Leakage Current	to VANA or VSS	-5		5	µA
VOHGPIO	High Level Output Voltage	at Iout	0.8·VANA			V
VOLGPIO	Low Level Output Voltage				0.2· VANA	V
VOLINT	Low Level Output voltage	Pin $\overline{INT}$ at 4mA			0.2	V
IOUT	Driving Capability	VANA = 2.8V, gpio1_low_curr or gpio2_low_curr or gpio3_low_curr= 1	4			mA
		VANA = 2.8V, gpio1_low_curr or gpio2_low_curr or gpio3_low_curr= 0	10[1]			
CLOAD	Capacitive Load				50	pF

1. Limited by LDO driving capability - see LDO on page 9

8.5.3 GPIO Registers

Table 80. GPIO output 2 Register

Addr: 50h		GPIO output 2		
		This register controls GPIO3 outputs.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio1_out	0	R/W	Writes a logic signal to pin ALS/GPIO1; this is independent of any other bit setting e.g., gpio1_mode Table 82.
1	gpio2_out	0	R/W	Writes a logic signal to pin GPIO2; this is independent of any other bit setting e.g., gpio2_mode Table 82
2	gpio3_out	0	R/W	Writes a logic signal to pin GPIO3; this is independent of any other bit setting e.g., gpio3_mode Table 83

Table 81. GPIO signal 2 Register

Addr: 51h		GPIO signal 2		
		This register controls GPIO3 outputs.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio1_in	N/A	R	Reads a logic signal from pin ALS/GPIO1; this is independent of any other setting e.g.,Table 82 except gpio1_pulls=11
1	gpio2_ in	N/A	R	Reads a logic signal from pin GPIO2; this is independent of any other setting e.g.,Table 82 except gpio2_pulls=11
2	gpio3_ in	N/A	R	Reads a logic signal from pin GPIO3; this is independent of any other setting e.g.,Table 83 except gpio3_pulls=11

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Table 82. GPIO control Register

Addr: 1Eh		GPIO control		
		This register controls GPIO3 and GPIO31 pin functions.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	gpio1_mode	00	R/W	Defines the direction for pin ALS/GPIO1
				00 Input only
				01 Output (push and pull)
				10 Output (open drain, only push; only NMOS is active)
				11 Output (open drain, only pull; only PMOS is active)
3:2	gpio1_pulls	11	R/W	Adds the following pullup/pulldown to pin ALS/GPIO1; this is independent of setting of bits gpio1_mode
				00 None
				01 Pulldown
				10 Pullup
				11 ADC input (gpio1_mode = XX); recommended for analog signals
5:4	gpio2_mode	00	R/W	Defines the direction for pin GPIO2
				00 Input only
				01 Output (push and pull)
				10 Output (open drain, only push; only NMOS is active)
				11 Output (open drain, only pull; only PMOS is active)
7:6	gpio2_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO2; this is independent of setting of bits gpio2_mode
				00 None
				01 Pulldown
				10 Pullup
				11 ADC input (gpio2_mode = XX); recommended for analog signals

Table 83. GPIO control 3 Register

Addr: 1Fh		GPIO control 3		
		This register enables low current mode for GPIO3s.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	gpio3_mode	00	R/W	Defines the direction for pin GPIO3
				00 Input only
				01 Output (push and pull)
				10 Output (open drain, only push; only NMOS is active)
				11 Output (open drain, only pull; only PMOS is active)

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Table 83. GPIO control 3 Register (Continued)

Addr: 1Fh		GPIO control 3			
		This register enables low current mode for GPIO3s.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:2	gpio3_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO3; this is independent of setting of bits gpio3_mode	
				00	None
				01	Pulldown
				10	Pullup
				11	ADC input (gpio3_mode = XX); recommended for analog signals

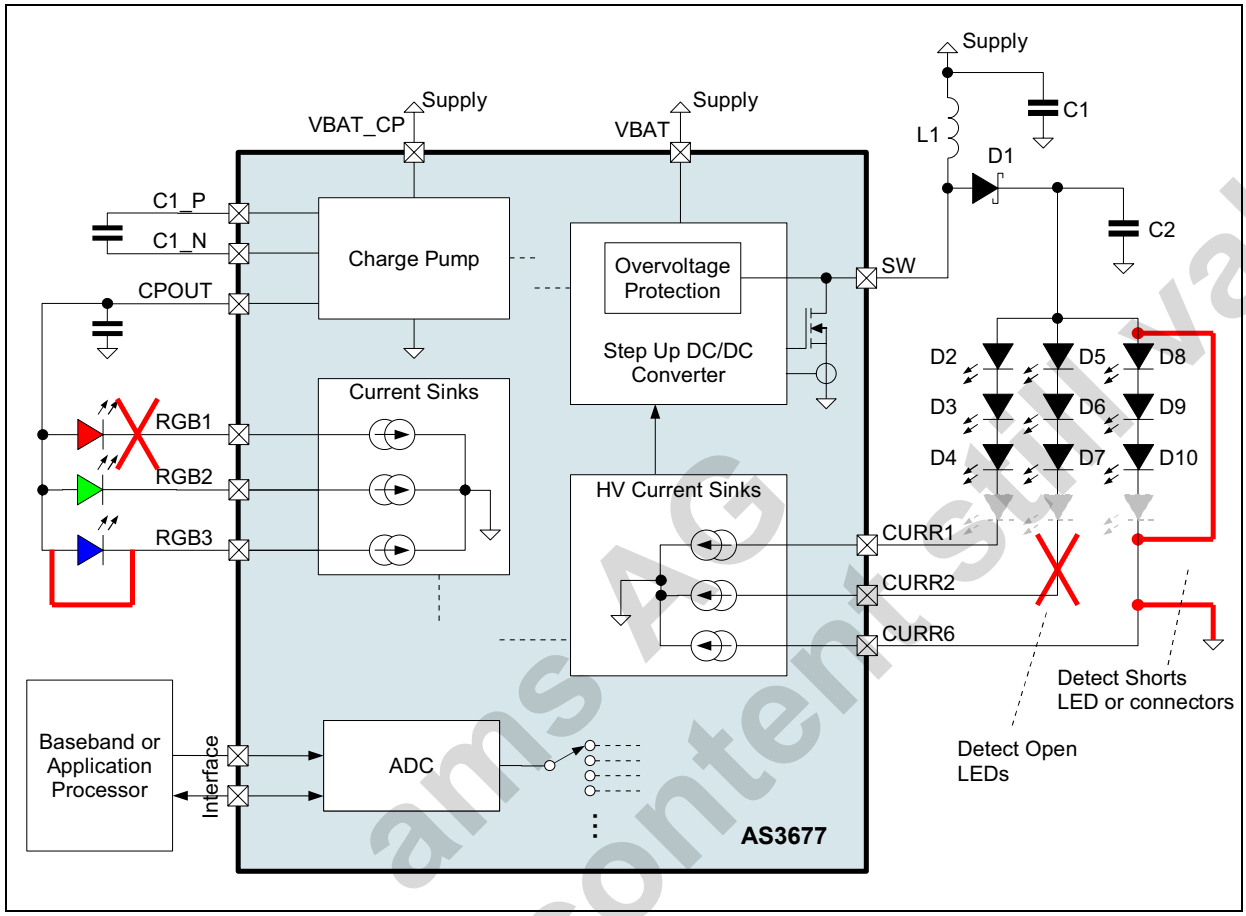
Table 84. GPIO driving cap Register

Addr: 20h		GPIO driving cap			
		This register enables low current mode for GPIO3s.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	gpio1_low_curr	0	R/W	Defines the driving capability of pin ALS/GPIO1	
				0	Iout
				1	Iout /4
1	gpio2_low_curr	0	R/W	Defines the driving capability of pin GPIO2	
				0	Iout
				1	Iout /4
2	gpio3_low_curr	0	R/W	Defines the driving capability of pin GPIO3	
				0	Iout
				1	Iout /4

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8.6 LED Test

Figure 27. LED Function Testing



The AS3677 supports the verification of the functionality of all the connected LEDs (open and shorted LEDs and short to VSS can be detected). This feature is especially useful in production test to verify the correct assembly of the LEDs, all its connectors and cables. It can also be used in the field to verify if any of the LEDs is damaged. A damaged LED can then be disabled (to avoid unnecessary currents).

The current sources, dcdc converter, charge pump and the internal ADC are used to verify correct operation of each LED string.

8.6.1 Function Testing for single LEDs connected to the Charge Pump

For any current source connected to the charge pump (CURR30-33) where only one LED is connected between the charge pump and the current sink (see Figure 27) use:

Table 85. Function Testing for LEDs connected to the Charge Pump

Step	Action	Example Code
1	Switch on the charge pump and set it into manual 1:2 mode (to avoid automatic mode switching during measurements)	Reg 23h ≤ 14h (cp_mode = 1:2, manual) Reg 00h ≤ 04h (cp_on = 1)
2	Switch on the current sink for the LED to be tested	e.g. for register CURR31set to 9mA use Reg 0Dh ≤ 5Ah (rgb1_current = 9mA) Reg 02h ≤ 01h (rgb1_mode = on)
3	Measure with the ADC the voltage on CPOUT	Reg 26h ≤ 95h (adc_select=CPOUT,start ADC) Fetch the ADC result from Reg 27h and 28h

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Table 85. Function Testing for LEDs connected to the Charge Pump

Step	Action	Example Code
4	Measure with the ADC the voltage on the switched on current sink	Reg 26h ≤ 85h (adc_select=RGB1,start ADC) Fetch the ADC result from Reg 27h and 28h
5	Switch off the current sink for the LED to be tested	Reg 02h ≤ 00h (rgb1_mode = off)
6	Compare the difference between the ADC measurements (which is the actual voltage across the tested LED) against the specification limits of the tested LED	Calculation performed in baseband uProcessor
7	Do the same procedure for the next LED starting from point 2	Jump to 2. If not all the LEDs have been tested
8	Switch off the charge pump set charge pump automatic mode	Reg 00h ≤ 00h (cp_on = 0) Reg 23h ≤ 00h

8.6.2 Function Testing example for LEDs connected to the DCDC

Use following procedure as an example:

Table 86. Function Testing procedure for LEDs connected to the DCDC

Step	Action	Example Code
1	Switch on one current sink (only one!) for the LED string to be tested (CURR1,2 or 6) - this example uses CURR1	e.g. Test LEDs on CURR1: Reg 01h ≤ 01h (curr1_mode=on) Reg 09h ≤ 3ch (curr1_current = 9mA)
2	Select the feedback path for the LED string to be tested (e.g. step_up_fb = 01 for LED string on CURR1) and disable automatic feedback	Reg 21h ≤ 02h (step_up_fb=CURR1) Reg 22h <- 04h (step_up_fb_auto=off)
3	Set step_up_vmax to fit the external components used (e.g. max 16V)	Reg 21h <- 00h (for 16V maximum output voltage)
4	Switch on the DCDC converter	Reg 00h ≤ 08h
5	Wait 2ms (dcdc startup time and some margin)	
6	Measure the voltage on CURR1	Reg 26h ≤ 98h (adc_select=CURR1, start ADC; Fetch the ADC result from Reg 27h and 28h)
7	If the voltage on CURR1 is below 1.0V but above 0.1V, this LED string is working fine (typical value will be at 0.5V)	For a proper working LED result must be below <199h (1.0V) and above >29h (0.1V)
8	Switch off current sink CURR1	Reg 01h ≤ 00h (curr1_mode=off)
9	Repeat whole procedure for each used LED string (replace CURR1 with CURR2 or CURR6)	

Note: With the above described procedures electrically open and shorted LEDs can be automatically detected

8.7 Analog-to-Digital Converter

The AS3677 has a built-in 10-bit successive approximation analog-to-digital converter (ADC). It is internally supplied which is also the full-scale input range (0V defines the ADC zero-code). For input signals exceeding 2.5V a resistor divider with a gain of 0.5 (Ratioprescaler) is used to scale the input of the ADC converter. Consequently the resolution is:

Table 87. ADC Input Ranges, Compliances and Resolution

Channels (Pins)	Input Range	V_{LSB}	Note
ALS/GPIO1, GPIO2, GPIO3 and VANA, DLS1, DLS2	0V-2.5V	2.44mV	V_{LSB}=2.5/1024
ADC_{TEMP_CODE}	-30°C to 125°C	1 / ADC_{TC}	junction temperature

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Table 87. ADC Input Ranges, Compliances and Resolution

Channels (Pins)	Input Range	VLSB	Note
VBAT, CPOUT, RGB1, RGB2, RGB3	0V-5V	4.88mV	VLSB=(2.5/1024)/0.4; internal resistor divider used
CURR1, CURR2, CURR6	0V-1.0V	2.44mV	VLSB=2.5/1024

Table 88. ADC Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Resolution		10			Bit
VIN	Input Voltage Range	VSUPPLY = 2.5V	VSS		see Table 87	V
DNL	Differential Non-Linearity			± 0.25		LSB
INL	Integral Non-Linearity			± 0.5		LSB
Vos	Input Offset Voltage			± 0.25		LSB
Rin	Input Impedance		100			MΩ
Cin	Input Capacitance				9	pF
VSUPPLY	Power Supply Range	± 2%, internally trimmed.		2.5		V
Idd	Power Supply Current	During conversion only.		286		µA
TTOL	Temperature Sensor Accuracy	@ 25 °C	-10		+10	°C
ADCTOFFSET	ADC temperature measurement offset value			375		°C
ADCTC	Code temperature coefficient	Temperature change per ADC LSB		1.2939		°C/ Code
RatioPRESCALER	Ratio of Prescaler	For all low voltage current sinks, CPOUT and VBAT		0.4		
Transient Parameters (2.5V, 25 ºC)						
Tc	Conversion Time	All signals are internally generated and triggered by start_conversion		27		µs
fc	Clock Frequency			1.0		MHz
ts	Settling Time of S&H			16		µs

The junction temperature (TJUNCTION) can be calculated with the following formula (ADCTEMP_CODE is the adc conversion result for channel 17h selected by register adc_select = 010111):

$$T_{JUNCTION}\,[°C] = ADC_{TOFFSET} - ADC_{TC} \cdot ADC_{TEMP_CODE} \qquad \text{(EQ 1)}$$

ADC Registers

Table 89. ADC_MSB result Register

Addr: 27h		ADC_MSB result		
		Together with Register 27h, this register contains the results (MSB) of an ADC cycle.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
6:0	adc_result_msb	N/A	R	ADC results register.

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Table 89. ADC_MSB result Register (Continued)

Addr: 27h		ADC_MSB result			
		Together with Register 27h, this register contains the results (MSB) of an ADC cycle.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7	result_not_ready	N/A	R	Indicates end of ADC conversion cycle	
				0	Result is ready
				1	Conversion is running

Table 90. ADC_LSB result Register

Addr: 28h		ADC_LSB result		
		Together with Register 28h, this register contains the results (LSB) of an ADC cycle		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	adc_result_lsb	N/A	R	ADC result register

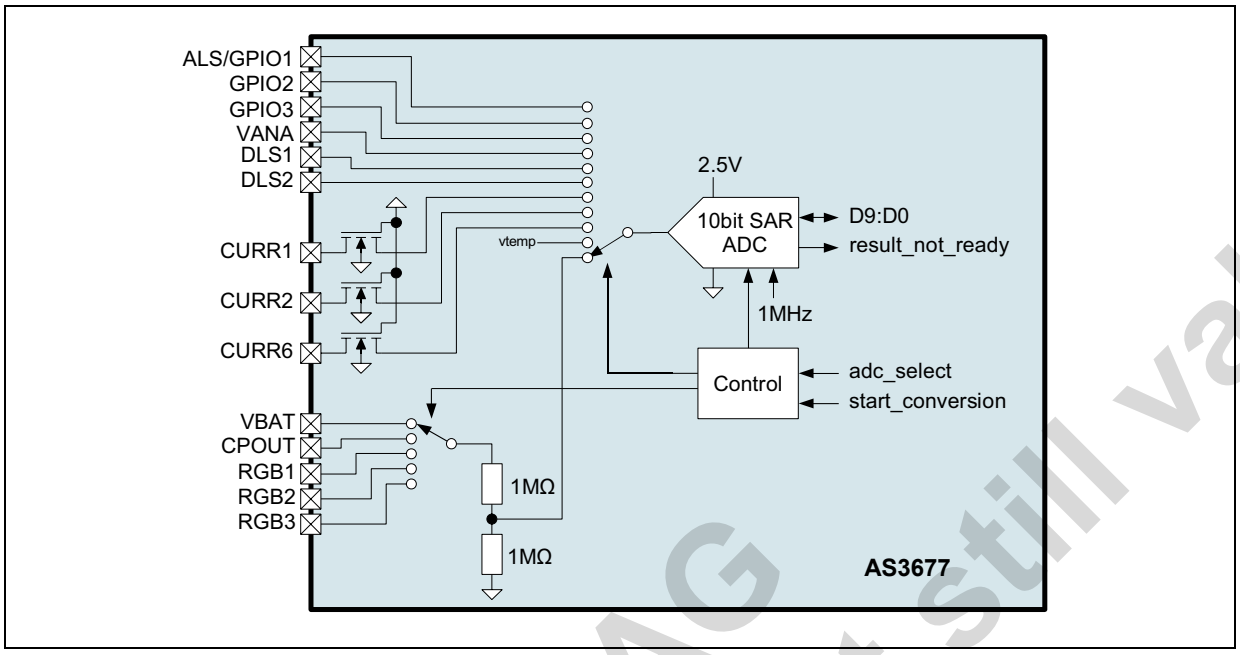
Table 91. ADC_control Register

Addr: 26h		ADC_control			
		This register input source selection and initialization of ADC			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:0	adc_select[1]	02h	R/W	Selects input source as ADC input	
				000000 (00h)	GPIO2
				000001 (01h)	VANA
				000010 (02h)	ALS/GPIO1
				000100 (04h)	GPIO3
				000101 (05h)	RGB1
				000110 (06h)	RGB2
				000111 (07h)	RGB3
				001000 (08h)	CURR1
				001001 (09h)	CURR2
				010001 (11h)	DLS1
				010010(12h)	DLS2
				010011 (13h)	CURR6
				010100 (14h)	VBAT
				010101 (15h)	CPOUT
				010111 (17h)	ADCTEMP_CODE (junction temperature)
				other codes	reserved
7	start_conversion	N/A	W	Writing a 1 into this bit starts one ADC conversion cycle.	

1. See Table Table 87 for ADC ranges and resolution.

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Figure 28. ADC Circuit



8.8 Power-On Reset

The internal reset is controlled by two sources:

- VBAT Supply
- Serial interface state (CLK, DATA)

The internal reset is forced if VBAT is low or if both interface pins (CLK, DATA) are low for more than t_{POR_DEB} (typ. 100ms)[5]. Then device enters shutdown mode. For details see section Operating Modes on page 58.

The reset levels control the state of all registers. As long as VBAT and CLK/DATA are below their reset thresholds, the register contents are set to default. Access by serial interface is possible once the reset thresholds are exceeded.

5. Only if shutdwn_enab=1

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Figure 29. Zero Power Device Wakeup block diagram

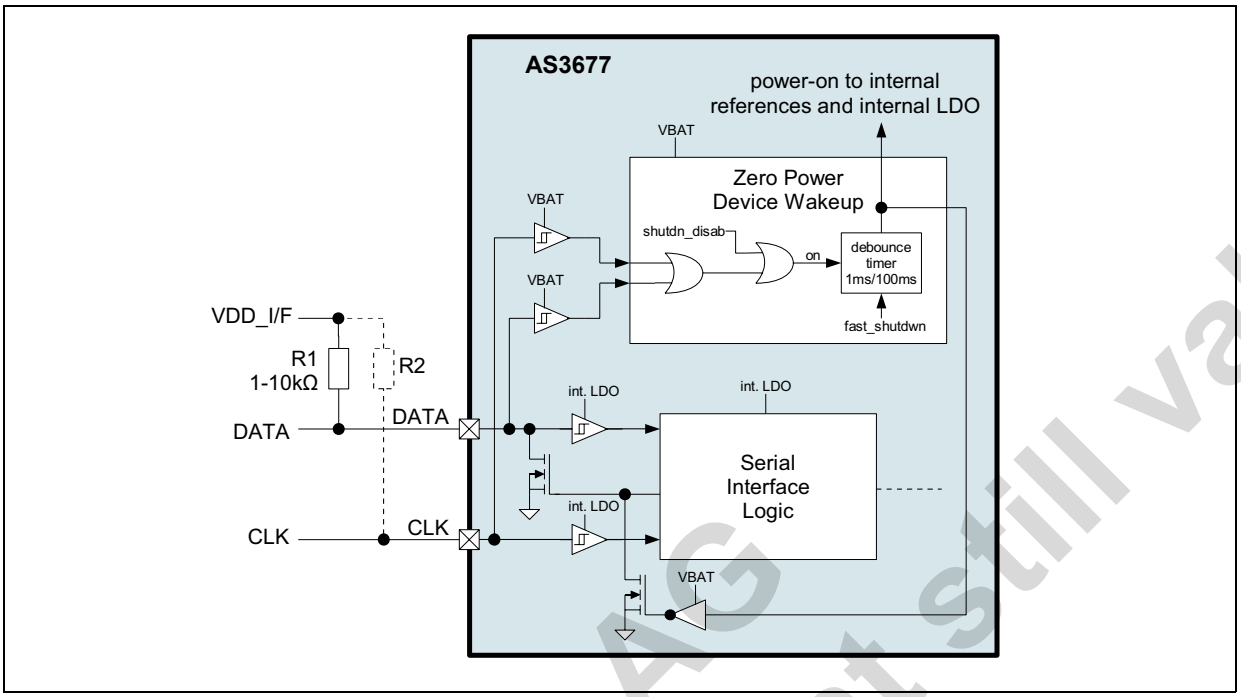


Table 92. Power On Reset Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{POR_VBAT}	Overall Power-On Reset	Monitor voltage on VBAT; power-on reset for all internal functions.		2.0		V
V_{POR_PERI}	Reset Level for pins CLK, DATA	Monitor voltage on pins CLK, DATA		1.0		V
t_{POR_DEB}	Reset debounce time for pins CLK, DATA			100		ms
t_{start}	Interface Startup Time			6		ms

8.8.1 Reset control register

Table 93. Overtemp control Register

Addr: 29h		Overtemp control			
		This register reads and resets the overtemperature flag.			
Bit	**Bit Name**	**Default**	**Access**	Description	
4	shutdwn_enab	1	R/W	Enable Shutdown mode and serial interface reset.	
				0	Serial Interface reset disabled. Device does not enter Shutdown mode
				1	Serial Interface reset enabled, device enters shutdown when SCL and SDA remain low for min. 100ms

8.9 Temperature Supervision

An integrated temperature sensor provides over-temperature protection for the AS3677. This sensor generates a flag if the device temperature reaches the overtemperature threshold of 140°. The threshold has a hysteresis to prevent oscillation effects.

If the device temperature exceeds the T_{140} threshold all current sources, the charge pump and the dcdc converter is disabled and the ov_temp flag is set. After decreasing the temperature by T_{HYST} operation is resumed.

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The ov_temp flag can only be reset by first writing a 1 and then a 0 to the register bit rst_ov_temp.

Bit ov_temp_on = 1 activates temperature supervision Table 95. It is recommend to leave this bit set (default state).

Table 94. Overtemperature Detection

Symbol	Parameter	Condition		Min	Typ	Max	Unit
T_{140}	ov_temp Rising Threshold				140		°C
T_{HYST}	ov_temp Hysteresis				5		°C

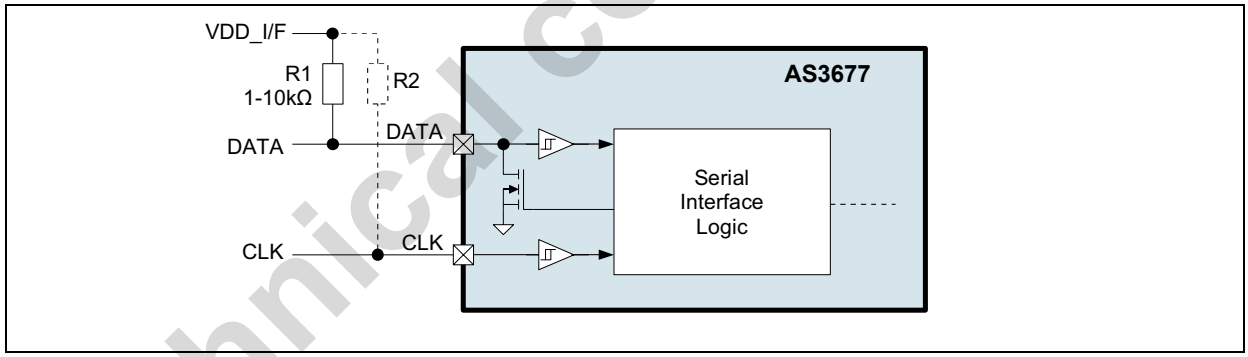
Table 95. Overtemp control Register

Addr: 29h		Overtemp control			
		This register reads and resets the overtemperature flag.			
Bit	Bit Name	Default	Access	Description	
0	ov_temp_on	1	W	Activates/deactivates device temperature supervision. Default: Off - all other bits are only valid if this bit is set to 1	
				0	Temperature supervision is disabled. No reset will be generated if the device temperature exceeds 140°C
				1	Temperature supervision is enabled
1	ov_temp	N/A	R	1	Indicates that the overtemperature threshold has been reached; this flag is not cleared by an overtemperature reset. It has to be cleared using rst_ov_temp
2	rst_ov_temp	0	R/W	The ov_temp flag is cleared by first setting this bit to 1, and then setting this bit to 0.	

8.10 Serial Interface

The AS3677 is controlled using serial interface pins CLK and DATA:

Figure 30. Serial interface block diagram



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The clock line CLK is never held low by the AS3677 (as the AS3677 does not use clock stretching of the bus).

Table 96. Serial Interface Voltages and Timings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IHI/F}$	High Level Input Voltage	Pins DATA and CLK	1.38		VBAT	V
$V_{ILI/F}$	Low Level Input Voltage		0.0		0.52	V
$V_{HYSTI/F}$	Hysteresis			0.1		V
t_{RISE}	Rise Time		0		1000	ns
t_{FALL}	Fall Time		0		300	ns
V_{OL}	Low Level Output voltage	Pin DATA at 4mA			0.2	V
t_{CLK_FILTER}	Spike Filter on CLK			100		ns
t_{DATA_FILTER}	Spike Filter on DATA			300		ns

The AS3677 is compatible to the NXP two wire specification http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf, Version 2.1, January 2000 for standard and fast mode (no high speed mode).

8.10.1 Serial Interface Features

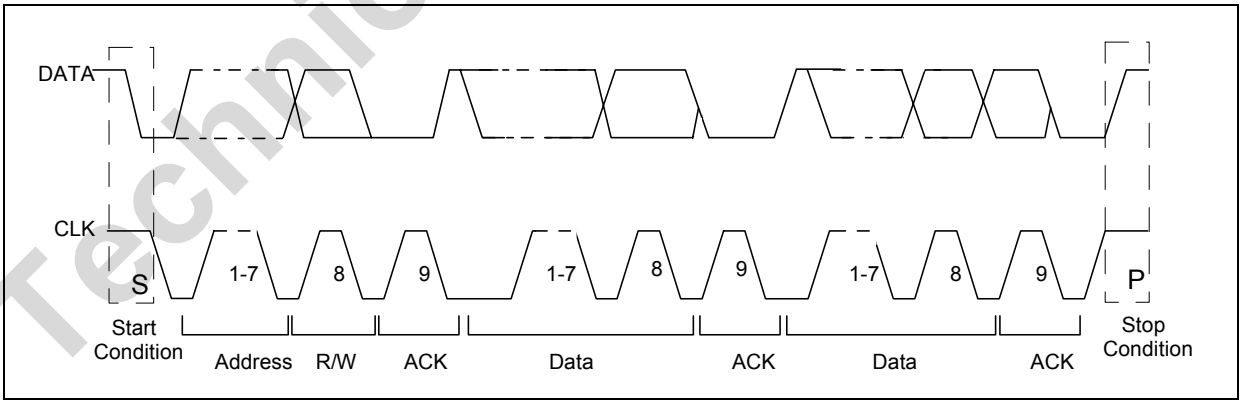
- Fast Mode Capability (Maximum Clock Frequency is 400 kHz)
- 7-bit Addressing Mode
- Write Formats
  - Single-Byte Write
  - Page-Write
- Read Formats
  - Current-Address Read
  - Random-Read
  - Sequential-Read
- DATA Input Delay and CLK spike filtering by integrated RC components

8.10.2 Device Address Selection

The serial interface address of the AS3677 has the following address:

- If ADR is connected to VSS: 80h – Write Commands, 81h – Read Commands
- If ADR is connected to VBAT: 82h – Write Commands, 83h – Read Commands

Figure 31. Complete Serial Data Transfer



Serial Data Transfer Formats

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Definitions used in the serial data transfer format diagrams are listed in the following table:

Table 97. Serial Data Transfer Byte Definitions

Symbol	Definition	R/W (AS3677 Slave)	Note
S	Start Condition after Stop	R	1 bit
Sr	Repeated Start	R	1 bit
DW	Device Address for Write	R	10000000b (80h) ADR=VSS 10000010b (82h) ADR=VBAT
DR	Device Address for Read	R	10000001b (81h) ADR=VSS 10000011b (83h) ADR=VBAT
WA	Word Address	R	8 bits
A	Acknowledge	W	1 bit
N	Not Acknowledge	R	1 bit
reg_data	Register Data/Write	R	8 bits
data (n)	Register Data/read	R	1 bit
P	Stop Condition	R	8 bits
WA++	Increment Word Address Internally	R	During Acknowledge

Figure 32. Serial Interface Byte Write

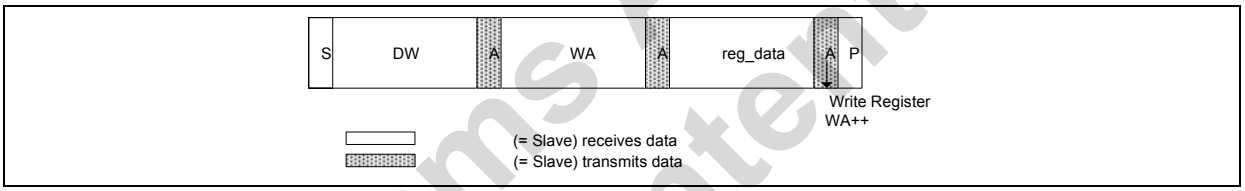
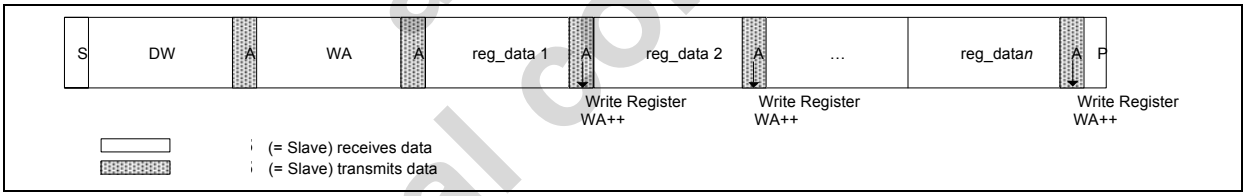


Figure 33. Serial Interface Page Write



Byte Write and Page Write formats are used to write data to the slave.

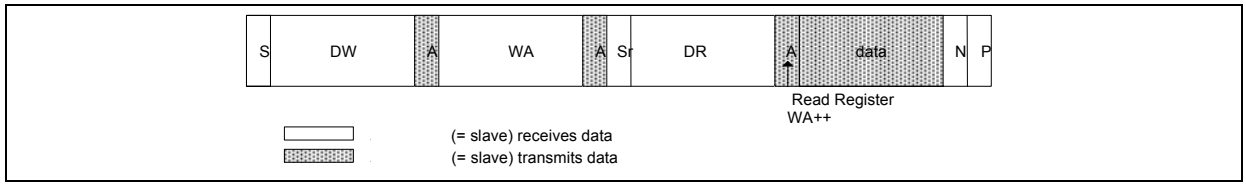
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

The following diagrams show the serial read formats supported by the AS3677.

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Figure 34. Serial Interface Random Read

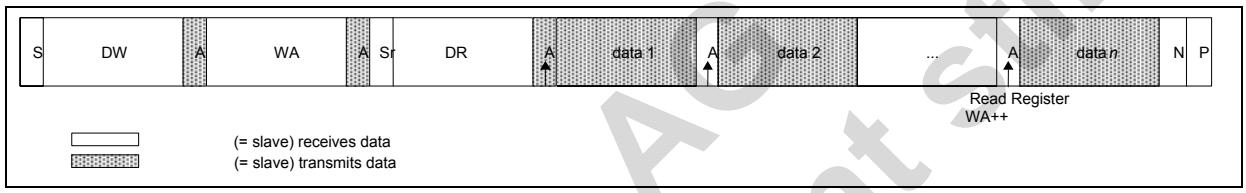


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st CLKpulse after the ACKNOWLEDGE bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a NOT ACKNOWLEDGE, and issues a STOP condition on the bus.

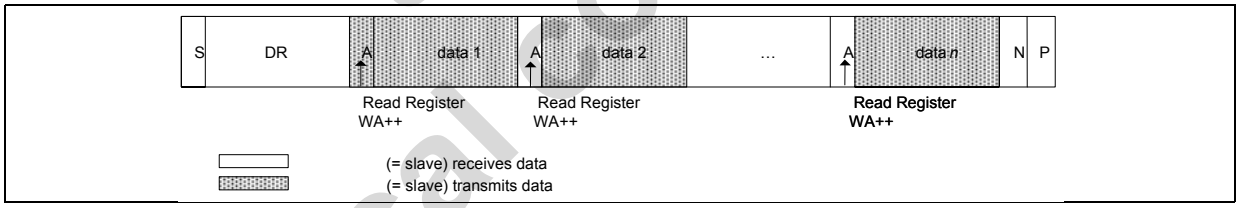
Figure 35. Serial Interface Sequential Read



Sequential Read is the extended form of Random Read, as multiple register-data bytes are subsequently transferred.

In contrast to the Random Read, in a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a NOT ACKNOWLEDGE following the last data byte and subsequently generate the STOP condition.

Figure 36. Serial Interface Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address.

Analogous to Random Read, a single byte transfer is terminated with a NOT ACKNOWLEDGE after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes must be responded to with an ACKNOWLEDGE from the master.

For termination of the transmission the master sends a NOT ACKNOWLEDGE following the last data byte and a subsequent STOP condition.

8.11 Operating Modes

If the voltages on CLK and DATA is less than V_{POR_PERI} for > t_{POR_DEB} (see Table 92 on page 54), the AS3677 is in shutdown mode and its current consumption is minimized (I_{BAT} = $I_{SHUTDOWN}$) and all internal registers are reset to their default values.

If the voltage at CLK or DATA rises above V_{POR_PERI}, the AS3677 serial interface is enabled and the AS3677 and the standby mode is selected. The AS3677 is switched automatically from standby mode (I_{BAT} = I_{STANBY}) into active mode (I_{BAT} = I_{ACTIVE}) and back, if one of the following blocks are activated:

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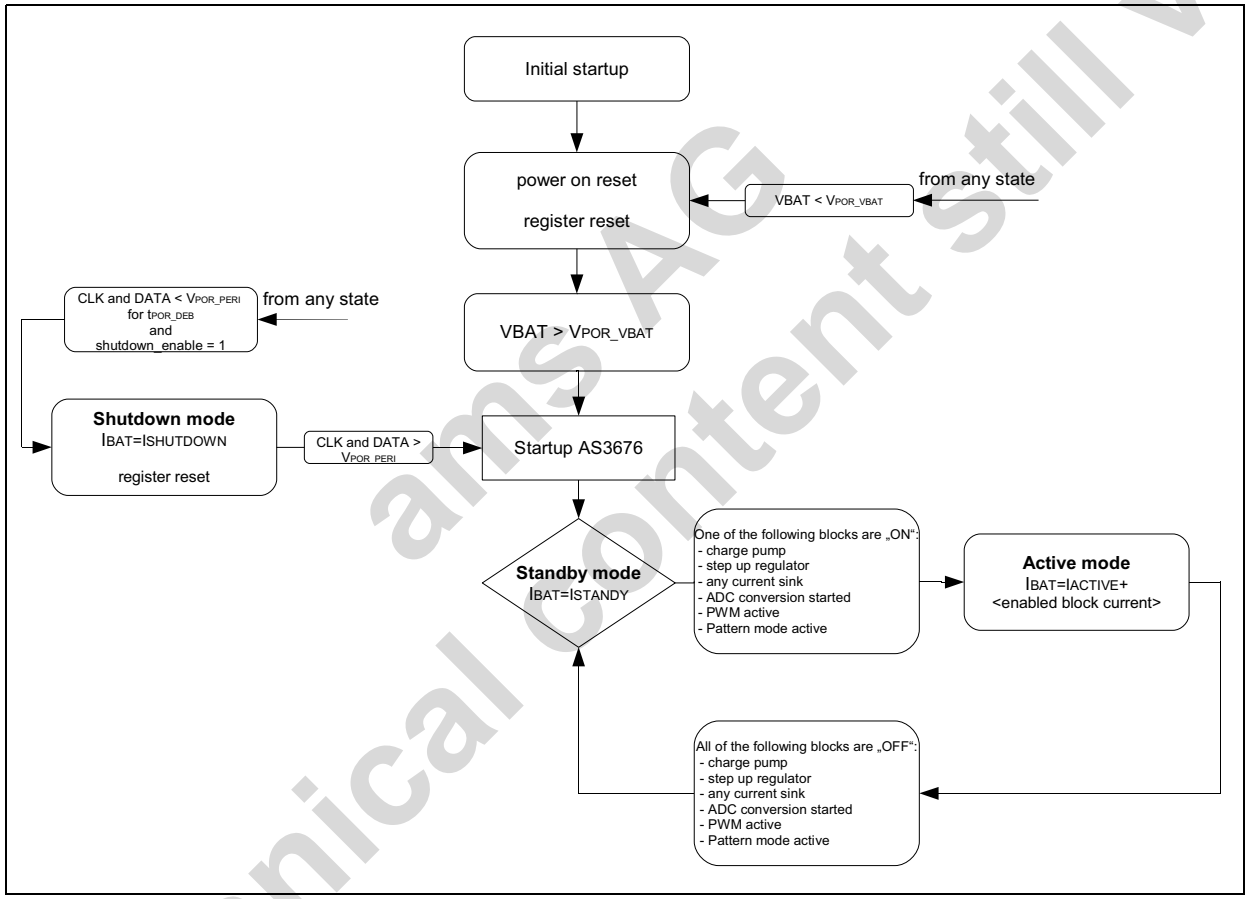
- Charge pump
- Step up regulator
- Any current sink
- ADC conversion started
- PWM active
- Pattern mode active.

If any of these blocks are already switched on the internal oscillator is running and a write instruction to the registers is directly evaluated within 1 internal CLK cycle (typ. 1µs)

If all these blocks are disabled, a write instruction to enable these blocks is delayed by 64 CLK cycles (oscillator will startup, within max 200µs).

The mode switching is shown in Figure 37:

Figure 37. Startup and Operating Mode Selection



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9 Register Map

Table 98. Registermap

Register Definition	Addr	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Reg control	00h	00					step_up_on	cp_on		ldo_on
curr12 control	01h	00h					curr2_mode		curr1_mode	
curr rgb control	02h	00h	curr6_mode		rgb3_mode		rgb2_mode		rgb1_mode	
LDO Voltage	07h	00h				ldo_voltage				
Curr1 current	09h	00h	curr1_current							
Curr2 current	0Ah	00h	curr2_current							
Rgb1 current	0Bh	00h	rgb1_current							
Rgb2 current	0Ch	00h	rgb2_current							
Rgb3 current	0Dh	00h	rgb3_current							
Pwm control	16h	00h			pwm_dim_speed			pwm_dim_mode		
Pwm code	17h	00h	pwm_code							
Pattern control	18h	00h					softdim_pattern	pattern_delay		pattern_color
Pattern data0	19h	00h	pattern_data_0							
Pattern data1	1Ah	00h	pattern_data_1							
Pattern data2	1Bh	00h	pattern_data_2							
Pattern data3	1Ch	00h	pattern_data_3							
GPIO control	1Eh	4Ch	gpio2_pulls		gpio2_mode		gpio1_pulls		gpio1_mode	
GPIO control 3	1Fh	04h					gpio3_pulls		gpio3_mode	
GPIO driving cap	20h	00h						gpio3_low_curr	gpio2_low_curr	gpio1_low_curr
DCDC control1	21h	02h				step_up_vmax		step_up_fb		step_up_frequ
DCDC control2	22h	88h	step_up_fb_auto			step_up_ov	step_up_lowcur		skip_fast	
CP control	23h	40h		cp_auto_on	cp_start_debounce	cp_mode_switching		cp_mode		cp_clk
CP mode Switch1	24h	70h		rgb3_on_cp	rgb2_on_cp	rgb1_on_cp				
CP mode Switch2	25h	00h	curr6_on_cp						curr2_on_cp	curr1_on_cp
ADC_control	26h	02h	start_conversion		adc_select					
ADC_MSB result	27h	NA	result_not_ready	adc_result_msb						
ADC_LSB result	28h	NA						adc_result_lsb		
Overtemp control	29h	11h				shutdwn_enab		rst_ov_temp	ov_temp	ov_temp_on
Curr low voltage status1	2Ah	NA	curr6_low_v	rgb3_low_v	rgb2_low_v	rgb1_low_v				

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Table 98. Registermap

Register Definition	Addr	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Curr low voltage status2	2Bh	NA							curr2_low_v	curr1_low_v
Gpio current	2Ch	80h		pattern_slow		pattern_delay2				
Curr6 current	2Fh	00h	curr6_current							
Adder Current 1	30h	00h	adder_current1 (can be enabled for CURR1)							
Adder Current 2	31h	00h	adder_current2 (can be enabled for CURR2)							
Adder Current 3	32h	00h	adder_current3 (can be enabled for CURR6)							
Adder Enable 1	33h	00h						rgb3_adder	rgb2_adder	rgb1_adder
Adder Enable 2	34h	00h						curr6_adder	curr2_adder	curr1_adder
ASIC ID1	3Eh	A6h	1	0	1	0	0	1	1	0
ASIC ID2	3Fh	5Xh	0	1	0	1	revision			
GPIO output 2	50h	00h						gpio3_out	gpio2_out	gpio1_out
GPIO signal 2	51h	00h						gpio3_ in	gpio2_ in	gpio1_in
Pattern End	54h	00h								pattern_end
DLS mode control1	56h	00h	dls_analog	rgb3_on_dls	rgb2_on_dls1	rgb1_on_dls				
DLS mode control2	57h	00h	curr6_on_dls	curr6_dls2	curr2_dls2				curr2_on_dls	curr1_on_dls
ALS control	90h	00h					amb_keep	amb_gain		amb_on
ALS filter	91h	00h		amb_filter_down				amb_filter_up		
ALS offset	92h	00h	amb_offset							
ALS result	93h	00h	amb_result							
ALS curr12 group	94h	00h					curr2_amb_group		curr1_amb_group	
ALS rgb group	95h	00h	curr6_amb_group		rgb3_amb_group		rgb2_amb_group		rgb1_amb_group	
ALS group 1 Y0	98h	00h	group1_y0							
ALS group 1 Y3	99h	00h	group1_y3							
ALS group 1 X1	9Ah	00h	group1_x1							
ALS group 1 K1	9Bh	00h	group1_k1							
ALS group 1 X2	9Ch	00h	group1_x2							
ALS group 1 K2	9Dh	00h	group1_k2							
ALS group 2 Y0	9Eh	00h	group2_y0							
ALS group 2 Y3	9Fh	00h	group2_y3							
ALS group 2 X1	A0h	00h	group2_x1							

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Table 98. Registermap

Register Definition	Addr	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
ALS group 2 K1	A1h	00h	group2_k1							
ALS group 2 X2	A2h	00h	group2_x2							
ALS group 2 K2	A3h	00h	group2_k2							
ALS group 3 Y0	A4h	00h	group3_y0							
ALS group 3 Y3	A5h	00h	group3_y3							
ALS group 3 X1	A6h	00h	group3_x1							
ALS group 3 K1	A7h	00h	group3_k1							
ALS group 3 X2	A8h	00h	group3_x2							
ALS group 3 K2	A9h	00h	group3_k2							
ALS group output 1	AAh	00h	amb_group1							
ALS group output 2	ABh	00h	amb_group2							
ALS group output 3	ACh	00h	amb_group3							
ALS range high interrupt threshold	ADh	00h	amb_range_int_high							
ALS range low interrupt threshold	AEh	00h	amb_range_int_low							
Interrupt Status	AFh	00h							amb_too_low	amb_too_high

Note: If writing to register, write 0 to unused bits

Write to read only bits will be ignored

yellow color = read only

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10 Application Information

10.1 External Components

Table 99. External Components List

Part Number	Min	Value Typ	Max	tol. (min.)	Rating (max)	Notes	Package (min.)[1]
C1		2.2µF		±20%	6.3V	Ceramic, X5R (Vana1 output) (e.g. Taiyo Yuden JMK107BJ225MA-T or LMK107BJ225MA) only required if LDO is used	0603
C2		4.7µF		±20%	25V	Ceramic, X5R, X7R (Step Up DCDC output) (e.g. Taiyo Yuden TMK316BJ475KD)	1206 (0805) 3.2x1.6x0.85mm
C3		100nF		±20%	6.3V	Ceramic, X5R (LDO output capacitor) (e.g. Taiyo Yuden JMK063BJ104KP-F)	0402
C4		470nF		±20%	6.3V	Ceramic, X5R (Charge Pump flying capacitor) (e.g. Taiyo Yuden JMK105BJ474KV-F)	0402
C5		1µF		±20%	6.3V	Ceramic, X5R (Charge Pump output) (e.g. Taiyo Yuden JMK105BJ105KV-F)	0402
R1		1-10kΩ				DATA Pullup resistor – usually already inside master	0201
R2						CLK Pullup resistor – usually already inside master	0201
L1		10µH		±20%		Recommended Type: Murata LQH3NPN100NJ0 or Panasonic ELLSFG100MA or TDK VLF3012A or Taiyo Yuden NRH3012T100MN (7µH min. at 600mA)	3x3x 1.2mm (H is max)
D1	PMEG4010BEA					Schottky diode	SOT666 1.6x1.6x0.6mm
X1	Light Sensor					e.g. Rohm BH1620FVC or Toshiba TPS856	1.6x1.6x 0.55mm
D2:D10	LED					As required by application	

1. in 1/100 inch (unless otherwise specified)

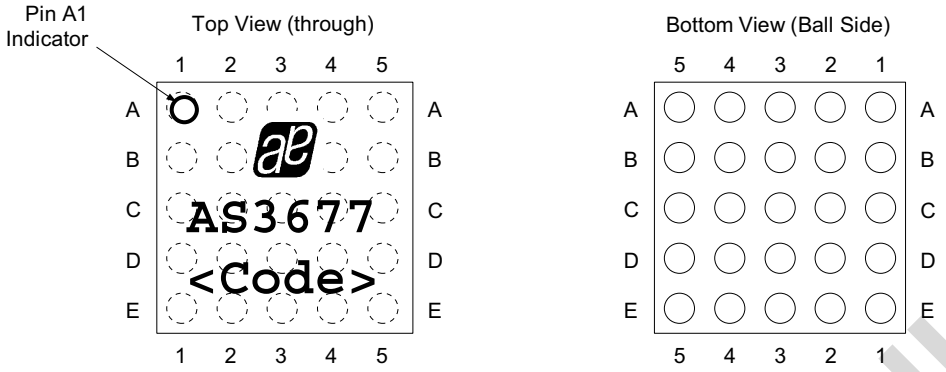
10.2 Layout Recommendations

1. GND Planes: Connect the VSS pins (B4, B5) to the low noise GND-plane.
   VSS_DCDC (A4) should be connected to a separated GND-plane. Connect also the charge pump output capacitor (C5) and the DCDC-caps (C1, C2) to this separated GND-plane. Connect all other blocking caps to the low noise GND-plane. Keep the area of the separated GND plane as small as possible and connect it to the star point of the low noise GND plane. Do not connect VSS (B4, B5) directly to VSS_DCDC (A4).
2. Supplies: The pins VBAT (B3) and VBAT_CP (A3) can be connected directly together. Put a blocking Cap close to VBAT_CP.
3. DCDC: Put L1, D1, C1 and C2 close together and also close to the pins SW (A5) and VSS_DCDC (A4).
4. LDO: Put C3 close to pin VANA (C1)

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11 Package Drawings and Markings

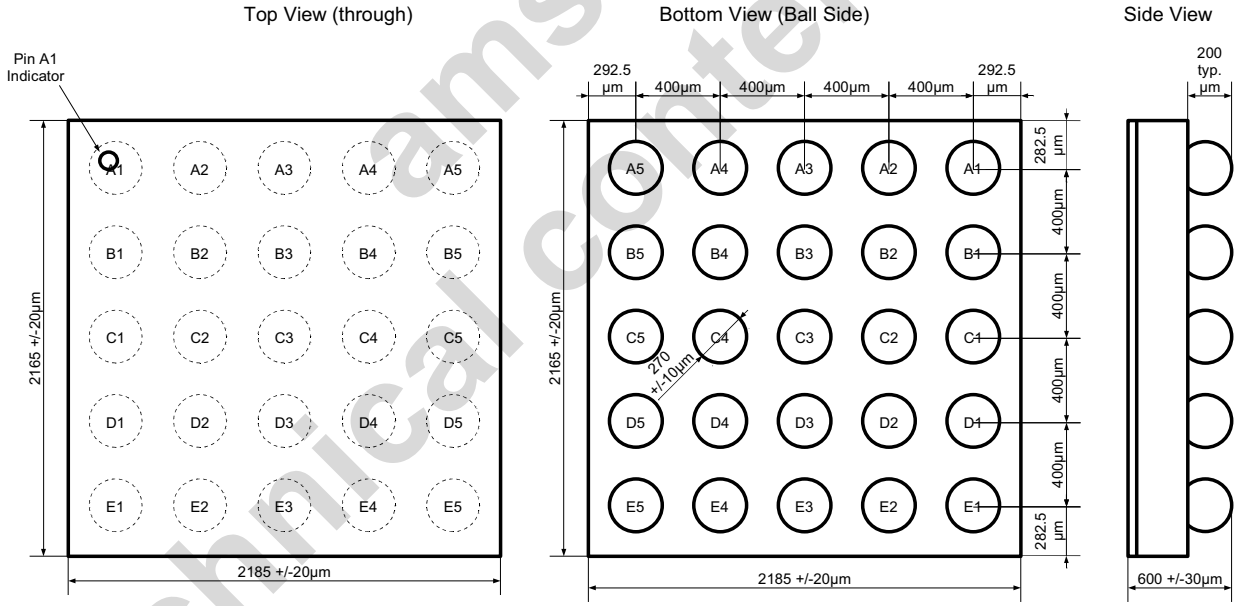
Figure 38. WL-CSP25 2.2x2.2x0.6mm 5x5 Balls Package Drawing



Note:

Line 1: austriamicrosystems logo
Line 2: AS3677
Line 3: <Code>
Encoded datecode 4 characters

Figure 39. WL-CSP25 2.2x2.2x0.6mm 5x5 Balls Detail Dimensions

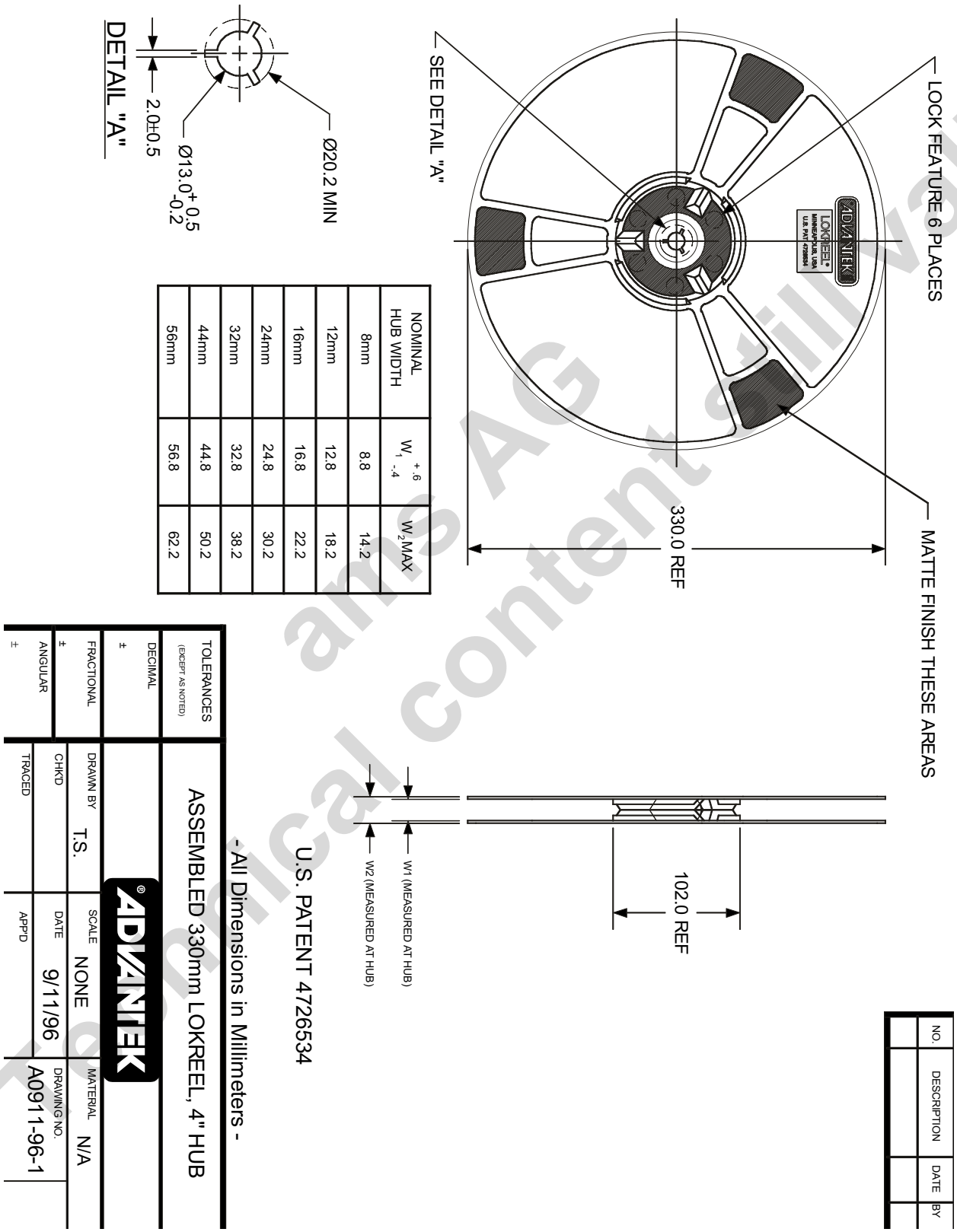


The coplanarity of the balls is 40µm.

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11.1 Tape & Reel Information

Figure 40. Tape & Reel Dimensions



NOMINAL HUB WIDTH	W_1 +.6 -.4	W_2 MAX
8mm	8.8	14.2
12mm	12.8	18.2
16mm	16.8	22.2
24mm	24.8	30.2
32mm	32.8	38.2
44mm	44.8	50.2
56mm	56.8	62.2

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12 Ordering Information

The devices are available as the standard products shown in Table 100.

Table 100. Ordering Information

Model	Description	Delivery Form	Package
AS3677-ZWLT	AS3677 Wafer Level Chip Scale Package, size 2.2x2.2x0.6mm, 5x5 balls, 0.4mm pitch, Green, Pb-Free	Tape & Reel	25pin WL-CSP (2.2x2.2x0.6mm) RoHS compliant / Pb-Free

Note: AS3677-ZWLT

AS3677-
- Z Temperature Range: -30ºC - 85ºC
- WL Package: Wafer Level Chip Scale Package (WL-CSP) 2.2x2.2x0.6mm
- T Delivery Form: Tape & Reel

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