

Improved Current Mode PWM Controller

FEATURES

- Pin-for-Pin Compatible With the UC3846
- 65ns Typical Delay From Shutdown to Outputs, and 50ns Typical Delay From Sync to Outputs
- Improved Current Sense Amplifier With Reduced Noise Sensitivity
- Differential Current Sense with 3V Common Mode Range
- Trimmed Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1V Shutdown Threshold
- High Current Dual Totem Pole Outputs (1.5A peak)
- TTL Compatible Oscillator SYNC Pin Thresholds
- 4kV ESD Protection

DESCRIPTION

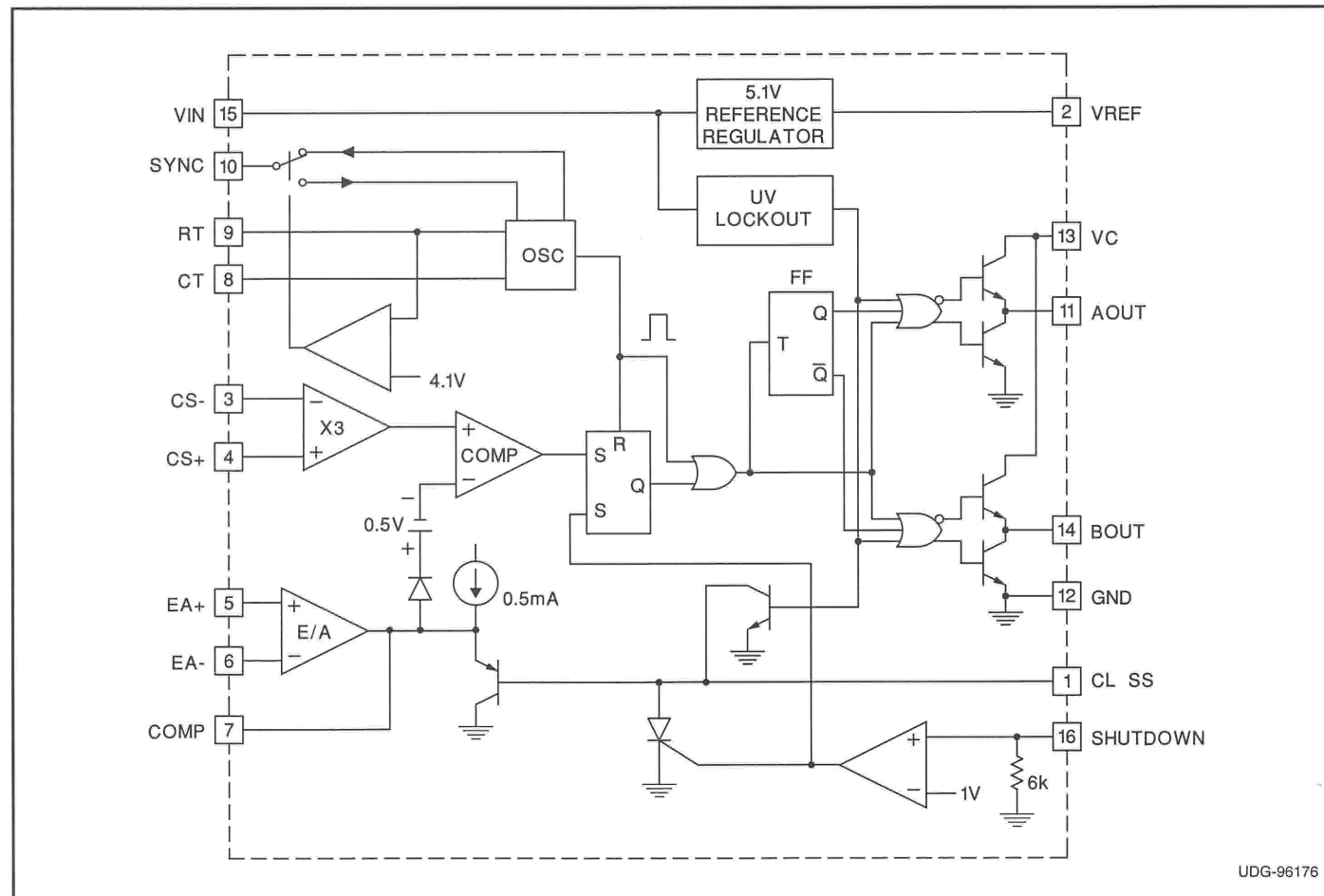
The UC3856 is a high performance version of the popular UC3846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the current sense output is slew rate limited to reduce noise sensitivity. Fast 1.5A peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a tri-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal "noise" caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1V, 5% shutdown threshold; and 4kV minimum ESD protection on all pins.

BLOCK DIAGRAM



UDG-96176

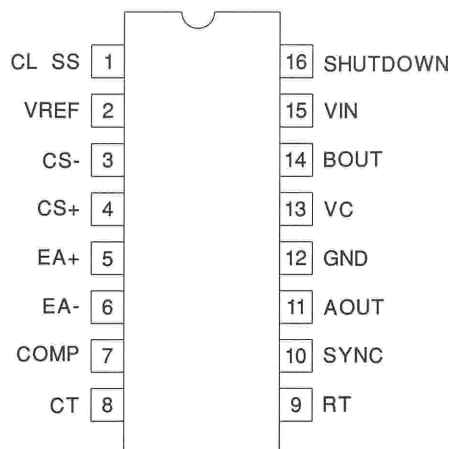
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+40V
Collector Supply Voltage	+40V
Output Current, Source or Sink	
DC	0.5A
Pulse (0.5μs)	2.0A
Error Amp Inputs	−0.3V to +V _{IN}
Shutdown Input	−0.3V to +10V
Current Sense Inputs	−0.3V to +3V
SYNC Output Current	±10mA
Error Amplifier Output Current	−5mA
Soft Start Sink Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at T _A = 25°C (Note 2)	1000mW
Power Dissipation at T _C = 25°C (Note 2)	2000mW
Junction Temperature	−55°C to +150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

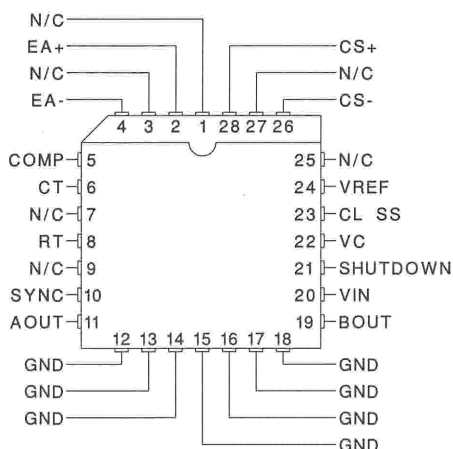
All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

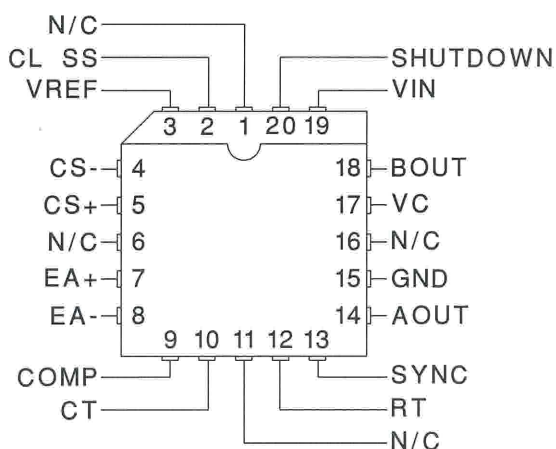
**DIL-16, SOIC-16 (Top View)
J or N, DW PACKAGE**



**PLCC-28 (Top View)
QP PACKAGE**



**PLCC-20 (Top View)
Q PACKAGE**



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for UC1856; −40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, V_{IN} = 15V, R_T = 10k, C_T = 1nF, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T _J = 25°C, I _O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V _{IN} = 8V to 40V			20			20	mV
Load Regulation	I _O = −1mA to −10mA			15			15	mV
Total Output Variation	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz < f < 10kHz, T _J = 25°C		50			50		μV
Long Term Stability	T _J = 125°C, 1000 Hrs (Note 2)		5	25		5	25	mV
Short Circuit Current	VREF = 0V	−25	−45	−65	−25	−45	−65	mA
Oscillator Section								
Initial Accuracy	T _J = 25°C	180	200	220	180	200	220	kHz
	Over Operating Range	170		230	170		230	kHz

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PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (cont.)								
Voltage Stability	VIN = 8V to 40V			2			2	%
Discharge Current	TJ = 25°C, VCT = 2V	7.5	8.0	8.8	7.5	8.0	8.8	mA
	VCT = 2V	6.7	8.0	8.8	6.7	8.0	8.8	mA
Sync Output High Level	IO = −1mA	2.4	3.6		2.4	3.6		V
Sync Output Low Level	IO = +1mA		0.2	0.4		0.2	0.4	V
Sync Input High Level	CT = 0V, RT = VREF	2.0	1.5		2.0	1.5		V
Sync Input Low Level	CT = 0V, RT = VREF		1.5	0.8		1.5	0.8	V
Sync Input Current	CT = 0V, RT = VREF VSYNC = 5V		1	10		1	10	μA
Sync Delay to Outputs	CT = 0V, RT = VREF VSYNC = 0.8V to 2V		50	100		50	100	ns
Error Amplifier Section								
Input Offset Voltage	VCM = 2V			5			10	mV
Input Bias Current				−1			−1	μA
Input Offset Current				500			500	nA
Common Mode Range	VIN = 8V to 40V	0		VIN-2	0		VIN-2	V
Open Loop Gain	VO = 1.2V to 3V	80	100		80	100		dB
Unity Gain Bandwidth	TJ = 25°C	1	1.5		1	1.5		MHz
CMRR	VCM = 0V to 38V, VIN = 40V	75	100		75	100		dB
PSRR	VIN = 8V to 40V	80	100		80	100		dB
Output Sink Current	VID = −15mV, VCOMP = 1.2V	5	10		5	10		mA
Output Source Current	VID = 15mV, VCOMP = 2.5V	−0.4	−0.5		−0.4	−0.5		mA
Output High Level	VID = 50mV, RL (COMP) = 15k	4.3	4.6	4.9	4.3	4.6	4.9	V
Output Low Level	VID = −50mV, RL (COMP) = 15k		0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	VCS− = 0V, CL SS Open (Notes 3,4)	2.5	2.75	3.0	2.5	2.75	3.0	V/V
Maximum Differential Input Signal (VCS+ - VCS−)	CL SS Open (Note 3) RL (COMP) = 15k	1.1	1.2		1.1	1.2		V
Input Offset Voltage	VCL SS = 0.5VCOMP Open (Note 3)		5	35		5	35	mV
CMRR	VCM = 0V to 3V	60			60			dB
PSRR	VIN = 8V to 40V	60			60			dB
Input Bias Current	VCL SS = 0.5V, COMP Open (Note 3)	−1		1	−1		1	μA
Input Offset Current	VCL SS = 0.5V, COMP Open (Note 3)	−1		1	−1		1	μA
Input Common Mode Range		0		3	0		3	V
Delay to Outputs	VEA+ = VREF, EA− = 0V CS+ − CS− = 0V to 1.5V		120	250		120	250	ns
Current Limit Adjust Section								
Current Limit Offset	VCS− = 0V VCS+ = 0V, COMP = Open (Note 3)	0.43	0.5	0.57	0.43	0.5	0.57	V
Input Bias Current	VEA+ = VREF, VEA− = 0V		−10	−30		−10	−30	μA
Shutdown Terminal Section								
Threshold Voltage		0.95	1.00	1.05	0.95	1.00	1.05	V
Input Voltage Range		0		5	0		5	V

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PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Shutdown Terminal Section (cont.)								
Minimum Latching Current (I _{CL SS})	(Note 5)	3	1.5		3	1.5		mA
Maximum Non-Latching Current (I _{CL SS})	(Note 6)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	V _{SHUTDOWN} = 0 to 1.3V		65	110		65	110	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Off-State Bias Current	V _C = 40V			250			250	μA
Output Low Level	I _{OUT} = 20mA		0.1	0.5		0.1	0.5	V
	I _{OUT} = 200mA		0.5	2.6		0.5	2.6	V
Output High Level	I _{OUT} = -20mA	12.5	13.2		12.5	13.2		V
	I _{OUT} = -200mA	12	13.1		12	13.1		V
Rise Time	C1 = 1nF		40	80		40	80	ns
Fall Time	C1 = 1nF		40	80		40	80	ns
UVLO Low Saturation	V _{IN} = 0V, I _{OUT} = 20mA		0.8	1.5		0.8	1.5	V
PWM Section								
Maximum Duty Cycle		45	47	50	45	47	50	%
Minimum Duty Cycle				0			0	%
Undervoltage Lockout Section								
Startup Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.7			0.7		V
Total Standby Current								
Supply Current			18	23		18	23	mA

Note 1: All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

Note 2: This parameter, although guaranteed over the recommended operating conditions is not 100% tested in production.

Note 3: Parameter measured at trip point of latch with $V_{EA+} = V_{REF}$, $V_{EA-} = 0\text{V}$.

Note 4: Amplifier gain defined as:

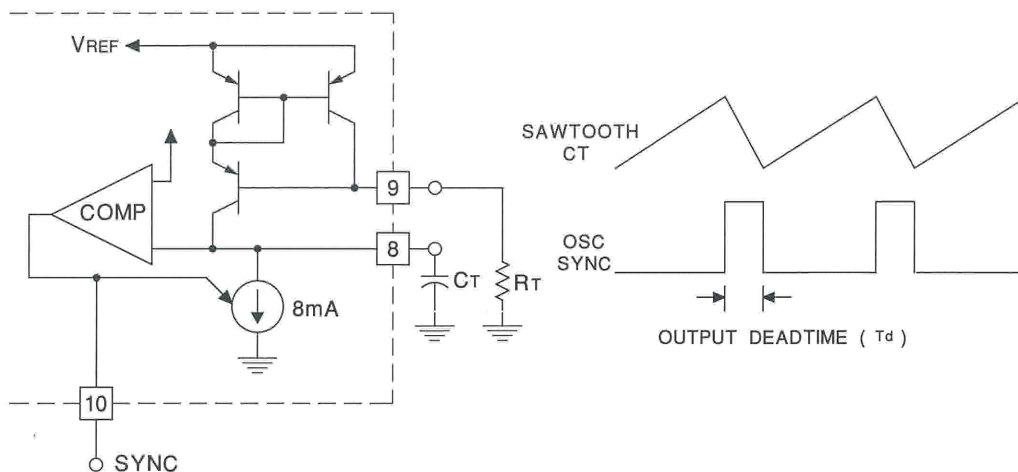
$$G = \frac{\Delta V_{COMP}}{\Delta V_{CS+}}; \quad \Delta V_{CS-} = 0\text{V TO } 1.0\text{V}$$

Note 5: Current into CL SS guaranteed to latch circuit into shutdown state.

Note 6: Current into CL SS guaranteed not to latch circuit into shutdown state.

APPLICATIONS INFORMATION

Oscillator Circuit



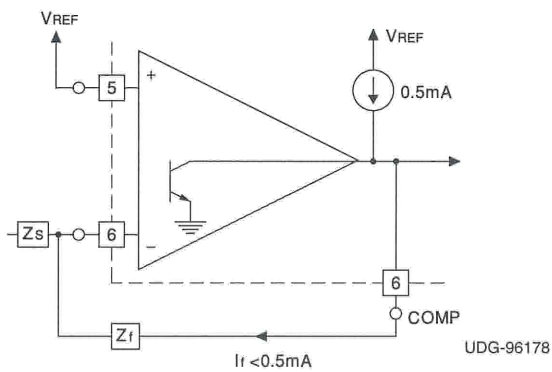
Output deadtime is determined by size of the external capacitor, C_T , according to the formula: $T_d = \frac{2C_T}{8mA - \frac{3.6}{R_T}}$

For large values of R_T : $T_d = 250C_T$

Oscillator frequency is approximated by the formula: $f_T = \frac{2}{R_T C_T}$

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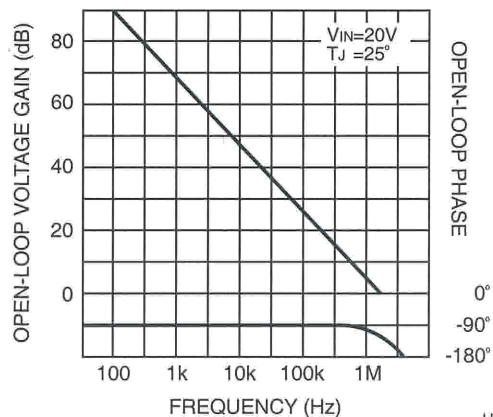
Error Amplifier Output Configuration



Error Amplifier can source up to 0.5mA.

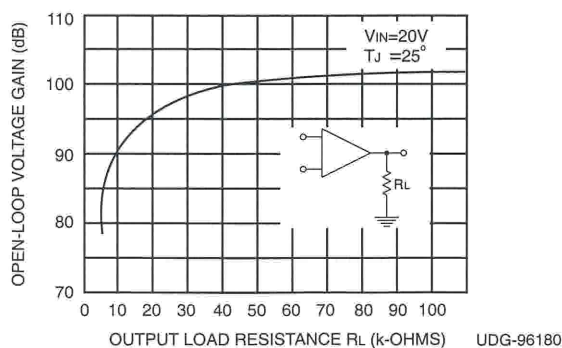
UDG-96178

Error Amplifier Gain and Phase vs Frequency



UDG-96179

Error Amplifier Open-Loop D.C. Gain vs Load Resistance

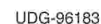


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Slaving allows parallel operation of two or more units with equal current sharing.

The schematic diagram shows a current source circuit with current limiting and feedback. A reference voltage V_{REF} is applied to a divider of resistors R_1 and R_2 . The output of this divider is connected to block 1, which is labeled "CURRENT LIMIT". The output of block 1 is connected to the base of a BJT transistor. The emitter of the transistor is grounded. The collector of the transistor is connected to a 0.5mA current source (represented by a circle with a downward arrow) and a diode (represented by a triangle pointing down). The diode is connected to a 0.5V voltage source (represented by a battery symbol). The output of the current source and diode is connected to block 7, which is labeled "COMP". The output of block 7 is connected to the non-inverting input of an operational amplifier (represented by a triangle with a circle). The inverting input of the operational amplifier is connected to a feedback network consisting of a resistor R_s and a diode (represented by a triangle pointing up). The output of the operational amplifier is connected to block 3, which is labeled "COMP". Block 3 is also connected to the non-inverting input of a multiplier block (represented by a triangle with "X3"). The multiplier block is connected to block 4, which is labeled "COMP". Block 4 is connected to the inverting input of the operational amplifier. The output of the operational amplifier is connected to block 7, which is labeled "COMP".

$$\text{Peak current (Is) is determined by the formula: } I_s = \frac{\left(\frac{R_2 V_{REF}}{R_1 + R_2} \right) - 0.5}{3R_S}$$



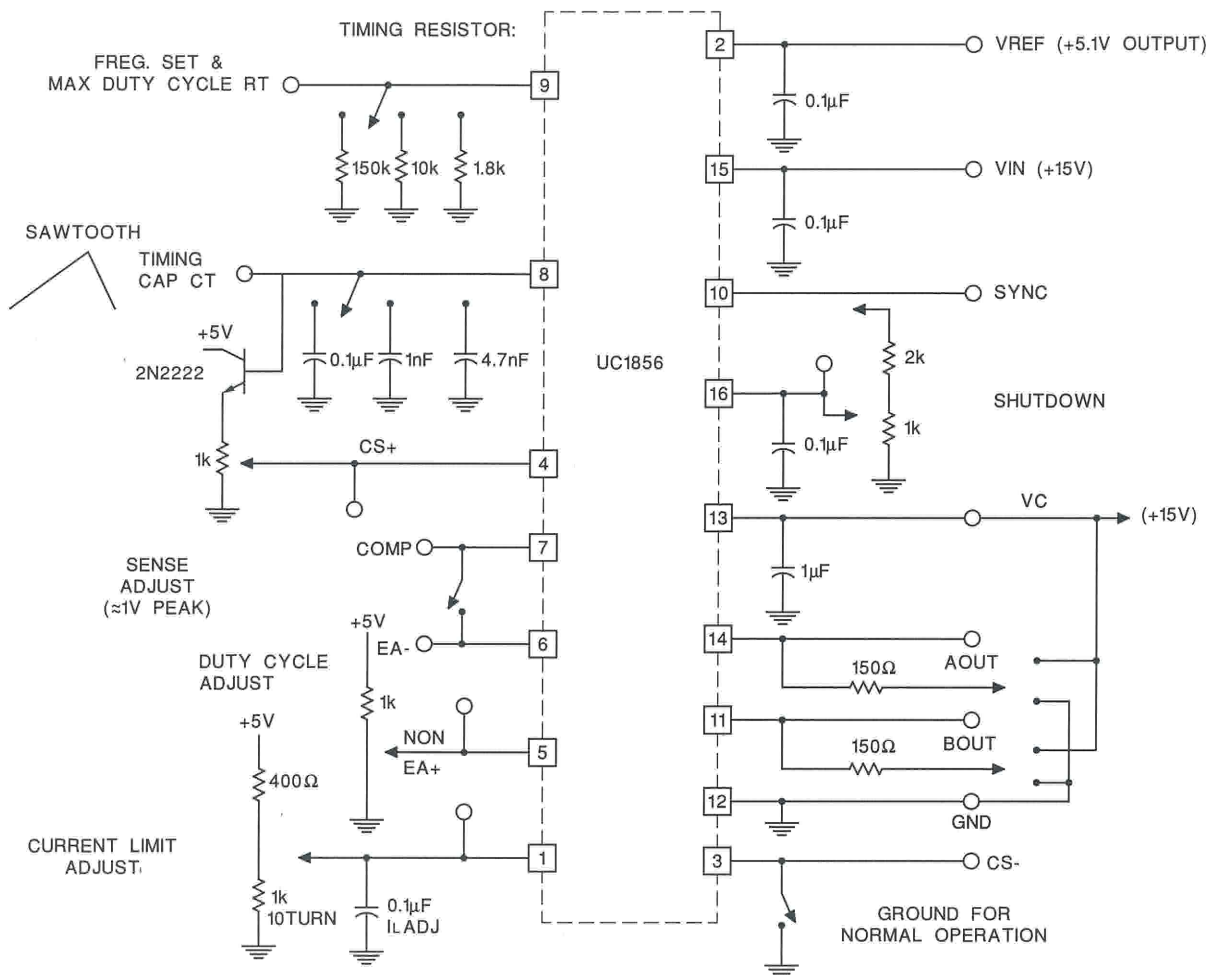
If $\frac{V_{REF}}{R1} > 3\text{mA}$, the device will latch off until power is recycled.

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APPLICATIONS INFORMATION (cont.)

UC1856 Open Loop Test Circuit



- BYPASS CAPS SHOULD BE LOW ESR & ESL TYPE
 - SHORT E/A- & COMP FOR UNITY GAIN TESTING
- THE USE OF A GROUND PLANE IS HIGHLY RECOMMENDED**

UDG-96186

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9453001M2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9453001MEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
UC1856J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
UC1856J883B	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
UC1856L	OBSOLETE	TO/SOT	L	28		TBD	Call TI	Call TI	
UC1856L20	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1856L20883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1856L883B	OBSOLETE	TO/SOT	L	28		TBD	Call TI	Call TI	
UC2856DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2856DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2856DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2856DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2856J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
UC2856N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2856NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3856DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3856DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3856DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3856DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3856N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3856NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UC3856Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	
UC3856QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF UC1856, UC2856, UC2856M, UC3856 :

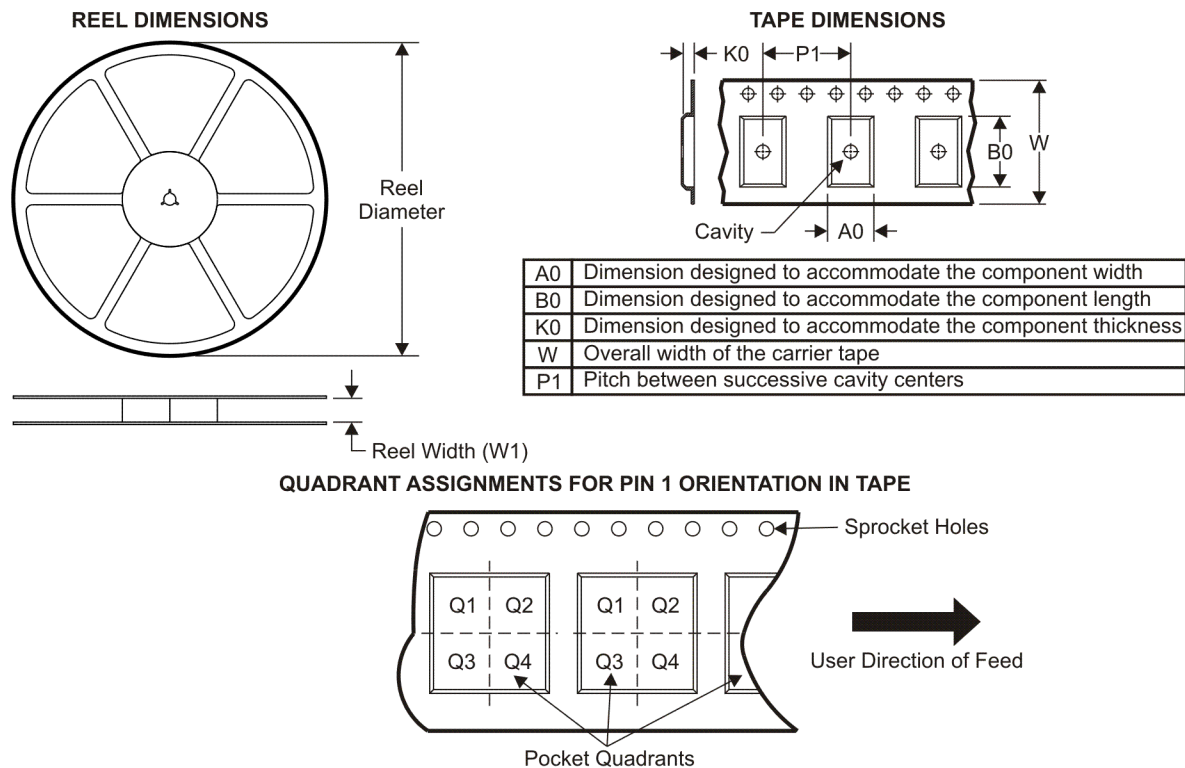
● Catalog: [UC3856](#), [UC2856](#)

● Automotive: [UC2856-Q1](#), [UC2856-Q1](#)

● Military: [UC2856M](#), [UC1856](#)

NOTE: Qualified Version Definitions:

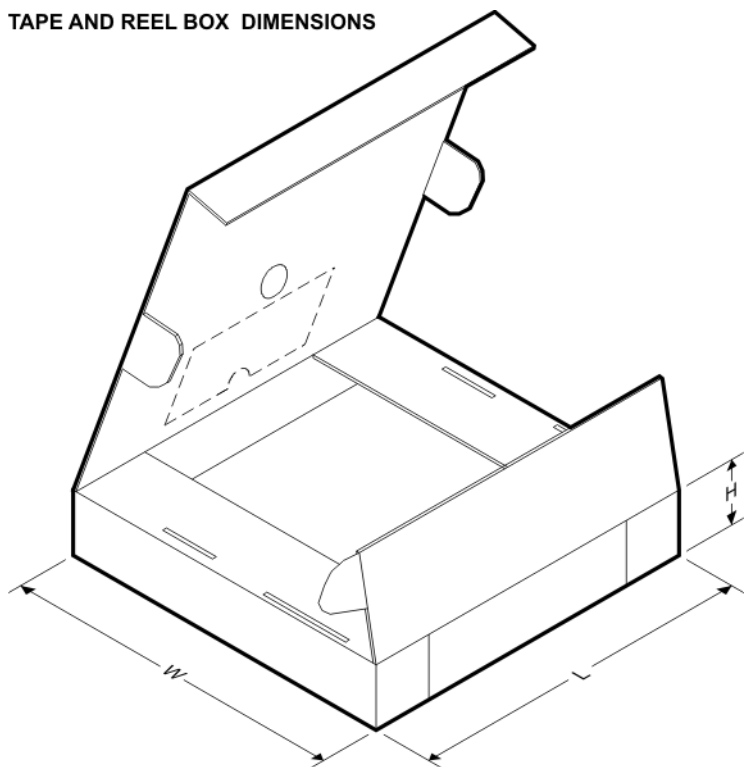
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2856DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC3856DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2856DWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC3856DWTR	SOIC	DW	16	2000	346.0	346.0	33.0

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