NBA3N012C

3.3 V Automotive Grade LVDS Line Receiver

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Description

The NBA3N012C is a single LVCMOS Output Differential Line Receiver for Low Power and high data rate Automotive applications. The device is optimized to support data rate higher than 400 Mbps (200 MHz). The NBA3N012C accept directly LVDS signal as an input and translate it to LVCMOS output levels. The device includes an input termination resistor minimizing number of the external components for point to point interface.

The NBA3N012C is offered in 5 lead SOT23 package and it is shipping in 3000 pcs tape & reel.

Features

- Compatible with TIA/EIA−644A Standard
- Automotive Grade AECQ−100 Grade 1
- > 400 Mbps (200 MHz) Data Rate
- Operating Range: V_{DD} = 3.3 V ± 0.3 V
- Typical 100 ps Differential Skew
- Maximum Propagation Delay of 3.5 ns
- Low Power Dissipation (Typical 20 mW @ 3.3 V)
- SOT23−5 Lead Package with Pinout optimized for easy PCB Layout
- Integrated Line Termination Resistor of 100 Ω
- Power Down High Impedance on LVDS Pins
- Inputs Accept LVDS/CML/LVPECL Signals
- Temperature Operating Range −40°C to +125°C
- These are Pb−Free Devices

Typical Applications:

- Automotive: Head Lamp Lighting for Cars
- Telecom: Wireless, Microwave and Optical

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	I/O Type	Description
1	V_{DD}		Power Supply Pin
2	GND		Ground Pin
3	IN	Input	Non−Inverting Input Pin
4	$\overline{IN}$	Input	Inverting Input Pin
5	Q	Output	Output Pin

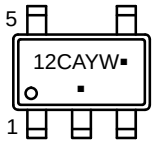
Table 2. TRUTH TABLE

Inputs	Output
[IN] – [$\overline{IN}$]	**Q**
V_{ID} ≥ +0.1 V	H
V_{ID} ≤ −0.1 V	L
Full Fail Safe OPEN/SHORT or terminated	H or L



SOT23−5
DT SUFFIX
CASE 527AH

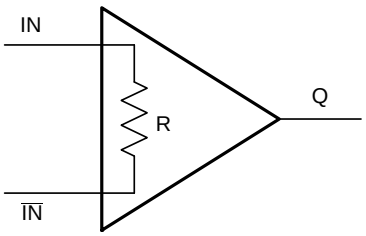
MARKING DIAGRAM



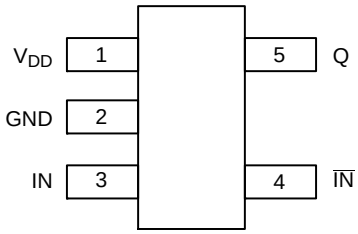
12C	= Specific Device Code
A	= Assembly Code
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

LOGIC DIAGRAM



PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NBA3N012CSNT1G	SOT23−5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 3. ATTRIBUTES (Note 1)

Characteristics			Value
ESD Protection	Human Body Model (JEDEC Standard 22, Method A114−E)	All Pins	≥ 8 kV
	Charge Device Model (JEDEC Standard 22, Method C101D)	All Pins	≥ 1.25 kV
Moisture Sensitivity (Note 1)			Level 1
Flammability Rating	Oxygen Index: 28 to 34		UL 94 Code V−0 A 0.125 in 28 to 34

1. For additional information, see Application Note AND8003/D

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply voltage	$-0.30 \le V_{DD} \le +4.0$	V
V_{IN}	Input Voltage (IN, $\overline{IN}$) LVDS	−0.30 to +3.90	V
V_Q	Output Voltage (Pin Q) LVCMOS	−0.30 to (V_{DD} + 0.30)	V
I_{OS}	Output Short Circuit Current (Pin Q)	−100	mA
Tj	Maximum Junction Temperature	135	°C
Tstg	Storage Temperature Range	−65 to +150	°C
θ_{JC}	Thermal resistance (Junction−to−Case) – (Note 3)	107	°C/W
θ_{JA}	Thermal resistance (Junction−to−Ambient) – (Note 3)	138.5	°C/W
T_{sol}	Lead Temperature Soldering (4 Seconds) – SOLDERRM/D	260	°C
PD	Package Power Dissipation @ 25°C − Derating of 7.22 mW/°C above 25°C	794	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. The maximum ratings applied are individual stress limit values and not valid simultaneously.
3. JEDEC standard multilayer board −2S2P (2 signal 2 power)

Table 5. DC CHARACTERISTICS V_{DD} = 3.3 V ± 0.3 V, GND = 0 V, T_A −40°C to +125°C (Note 4)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	No Load Supply Current	Pin: V_{DD}; Inputs Open		5.4	9	mA
V_{OH}	Output High Voltage	Pin: Q; I_{OH} = −0.4 mA, Inputs shorted or terminated, V_{ID} = +200 mV	2.4	3.1		V
V_{OL}	Output Low Voltage	Pin: Q; I_{OL} = 2 mA, V_{ID} = −200 mV		0.3	0.5	V
I_{OS}	Output Short Circuit Current	Pin: Q; V_Q = 0 V	−15	−50	−100	mA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.7		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. − minus sign indicated only direction. Current into the device is defined as positive. I_{OS} is specified as magnitude only.

Table 6. ELECTRICAL CHARACTERISTICS V_{DD} = 3.3 V ± 0.3 V, GND = 0 V, T_A −40°C to +125°C, Pin: IN/$\overline{IN}$ (Note 5)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{TH}	Differential Input High Threshold	V_{CM} dependent on V_{DD}			+30	+100	mV
V_{TL}	Differential Input Low Threshold			−100	−30		mV
V_{CM}	Offset Voltage			0.1		2.35	V
I_{IN}	Input Current	V_{IN} = +2.8 V	V_{DD} = 0 V or 3.6 V	−10	±1	+10	μA
		V_{IN} = 0 V		−10	±1	+10	μA
		V_{IN} = +3.6 V	V_{DD} = 0 V	−20		+20	μA
I_{IND}	Differential Input Current	V_{IN} = +0.4 V, $V_{\overline{IN}}$ = +0 V		3.0	3.9	4.4	mA
		V_{IN} = +2.4 V, $V_{\overline{IN}}$ = +2.0 V					
R_T	Integrated Termination Resistor				100		Ω
C_{IN}	Input Capacitance	IN = $\overline{IN}$ = GND			3		pF

5. − minus sign indicated only direction. Current into the device is defined as positive.

Table 7. SWITCHING CHARACTERISTICS
V_{DD} = 3.3 V ± 0.3 V, GND = 0 V, T_A −40°C to +125°C, F = 1 MHz, Z_O = 50 Ω, t_r, t_f ≤ 3 ns (0% to 100%) − (Note 6)

Symbol	Parameters	Min	Typ	Max	Unit
t_{pHLD}	High to Low Differential Propagation Delay	1.0	1.8	3.5	ns
t_{pLHD}	Low to High Differential Propagation Delay	1.0	1.7	3.5	ns
t_r	Rise Time – Transition Low to High		350	800	ps
t_f	Fall Time – Transition High to Low		175	800	ps
$t_{SKD(P)}$	Differential Pulse Skew $\|t_{pHLD} - t_{pLHD}\|$ (Note 7)	0	100	400	ps
$t_{SKD(PP)1}$	Part to Part Skew – (Note 8)	0	0.3	1.0	ns
$t_{SKD(PP)2}$	Part to Part Skew – (Note 9)	0	0.4	2.5	ns
f_{MAX}	Maximum Operating Frequency – (Note 10)		250		MHz

6. Test Conditions for the above − V_{ID} = 200 mV, C_L = 15 pF (includes Load & Jig Capacitance), Figures 1 and 2
7. $|t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
8. Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
9. Part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD2} is defined as |Max − Min| differential propagation delay.
10. f_{MAX} Input Conditions: $t_r = t_f$ < 1 ns (0% to 100%), Duty Cycle 50%, differential (1.05 V to 1.35 V Peak to Peak). f_{MAX} Output Conditions: V_{OL} (Max 0.4 V), V_{OH} (min 2.4 V), Load = 15 pF (stray + probe), Duty Cycle 60%/40%

PARAMETER MEASUREMENT:

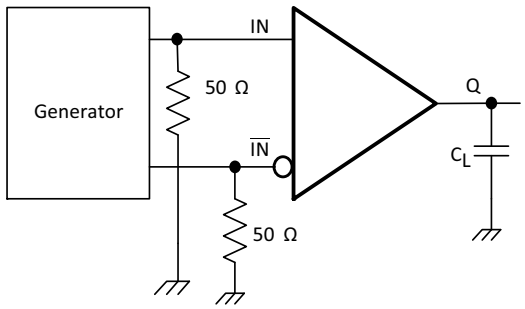


Figure 1. Receiver Propagation Delay & Transition Time Test Circuit

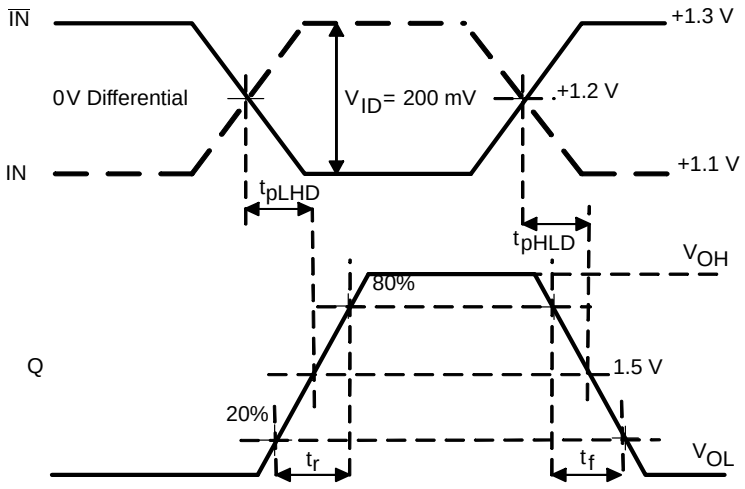
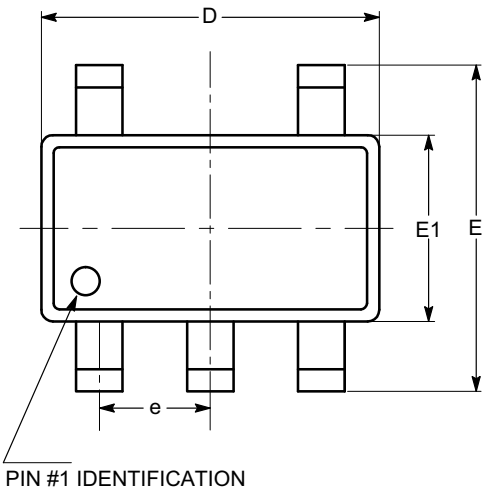


Figure 2. Receiver Propagation Delay & Transition Time Waveforms

NBA3N012C

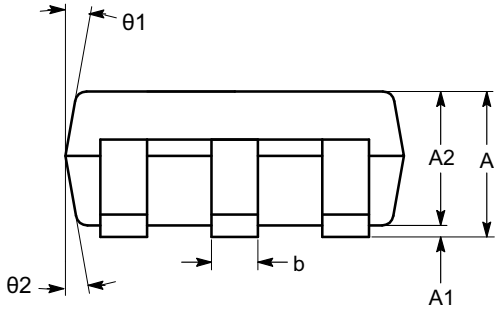
PACKAGE DIMENSIONS

SOT−23, 5 Lead
CASE 527AH
ISSUE O

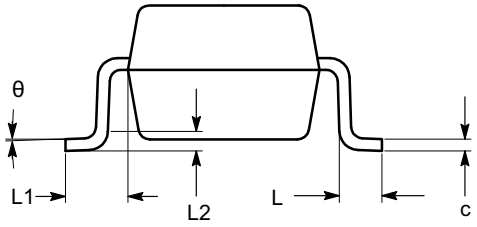


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.15	1.30
b	0.30		0.50
c	0.08		0.22
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 BSC	
L	0.30	0.45	0.60
L1		0.60 REF	
L2		0.25 REF	
θ	0°	4°	8°
θ1	5°	10°	15°
θ2	5°	10°	15°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.

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