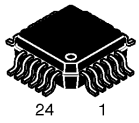
Technical Data

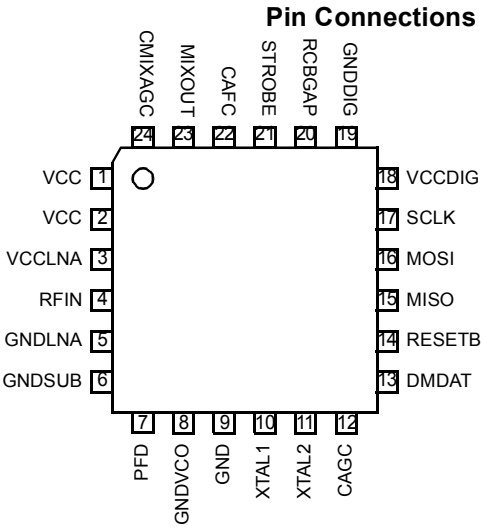
Romeo2
MC33591/D
Rev. 7.1, 7/2002

PLL Tuned UHF Receiver for Data Transfer Applications

MOTOROLA intelligence everywhere™ | digital dna™



FTA SUFFIX
PLASTIC PACKAGE
CASE 977
(LQFP–24)



FEATURES

- 315MHz, 434MHz Bands
- OOK and FSK Demodulation
- Low Current Consumption: 5mA Typ. in Run Mode
- Internal or External Strobing
- Fast Wake-Up Time (1ms)
- -105dBm RF Sensitivity (at 4.8kBd Data Rate)
- Fully Integrated VCO
- Image Cancelling Mixer
- Integrated IF Bandpass Filter at 660kHz
- IF Bandwidth: 500kHz
- ID Byte and Tone Detection
- Data Rate: 1 to 11kBd
- Manchester Coded Data Clock Recovery
- Fully Configurable by SPI Interface
- Few External Components, no RF Adjustment

Figure 1: Simplified block diagram

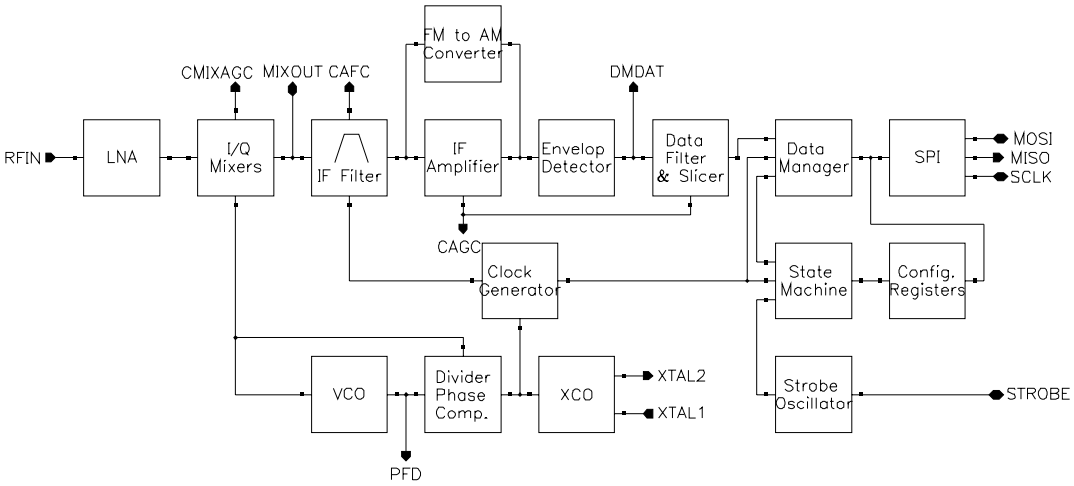


Table 1: Ordering Information

Device	RF frequency/ IF filter bandwidth	Ambiant Temperature Range	Package
MC33591FTA	434MHz / 500kHz	-40°C to +85°C	LQFP24

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PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	VCC	5V power supply
2	VCC	5V power supply
3	VCCLNA	5V LNA power supply
4	RFIN	RF input
5	GNDLNA	LNA ground
6	GNDSUB	Ground
7	PFD	Access to VCO control voltage
8	GNDVCO	VCO ground
9	GND	Ground
10	XTAL1	Reference oscillator crystal
11	XTAL2	Reference oscillator crystal
12	CAGC	IF AGC capacitor for OOK Reference for FSK
13	DMDAT	Demodulated data (OOK & FSK modulation)
14	RESETB	State Machine Reset
15	MISO	SPI interface I/O
16	MOSI	SPI interface I/O
17	SCLK	SPI interface clock
18	VCCDIG	5V digital power supply
19	GNDDIG	Digital ground
20	RCBGAP	Reference voltage output
21	STROBE	Strobe oscillator control Stop/Run external control input
22	CAFC	AFC capacitor
23	MIXOUT	Mixer output
24	CMIXAGC	Mixer AGC capacitor

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{CCLNA}	V_{GND} - 0.3 to 5.5	V
Voltage Allowed on Each Pin		V_{GND} - 0.3 to V_{CC} + 0.3	V
ESD HBM Voltage Capability on Each Pin (note 1)		±2000	V
ESD MM Voltage Capability on Each Pin (note 2)		±200	V
Solder Heat Resistance Test (10 s)		260	°C
Storage Temperature	Ts	-65 to +150	°C
Junction Temperature	Tj	150	°C

Notes:
1 Human Body model, AEC-Q100-002 Rev. C.
2 Machine Model, AEC-Q100-003 Rev. E.

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RECEIVER FUNCTIONAL DESCRIPTION

The basic functionality of the ROMEO2 receiver may be seen by reference to the accompanying block diagram (see figure 1). It is fully compatible with the TANGO3 transmitter.

The RF section comprises a mixer with image cancelling, followed by an IF band-pass filter at 660kHz, an AGC controlled gain stage and OOK/FSK demodulators, the desired modulation type being selectable by the SPI interface. The data output from the circuit may either be the data comparator output, or, if Data Manager is enabled, the SPI port.

The local oscillator is controlled with a PLL referenced to the crystal oscillator. The received channel is defined by the choice of the crystal frequency.

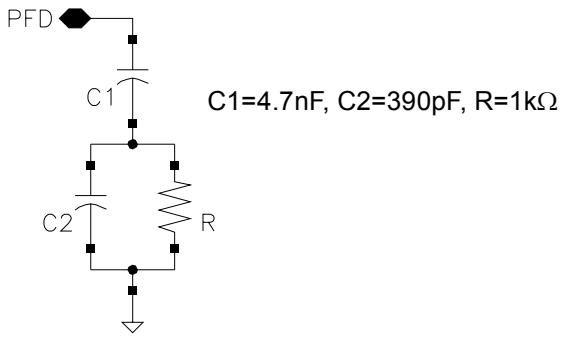
An SPI bus permits programming the modulation type, data rate, UHF frequency, ID word etc., though to accomodate applications where no bus interface is available the circuit defaults at power-on to a standard operating mode.

Depending upon the configuration, the circuit can be either externally strobed by the STROBE input or internally wait-and-sleep cycled to reduce the power consumption. At any time, a high level on STROBE overrides the internal timer output and wakes up ROMEO2. When the circuit is switched into sleep mode its current consumption is approximately 100µA. The circuit configuration which has previously been programmed is retained.

THE LOCAL OSCILLATOR PLL

The PLL is tuned by comparing the local oscillator frequency, after suitable division, with that of the crystal oscillator reference. The loop filter has been integrated in the IC. Practical limits upon the values of components which may be integrated mean that the local oscillator performance may be slightly improved by using an external PFD filter, shown in Figure 2. In this way the user may choose to have optimum performance with the addition of external filter components. The PLL gain may be programmed by bit PG: it is recommended that this bit be set to 1, corresponding to low loop gain.

Figure 2 : External loop filter



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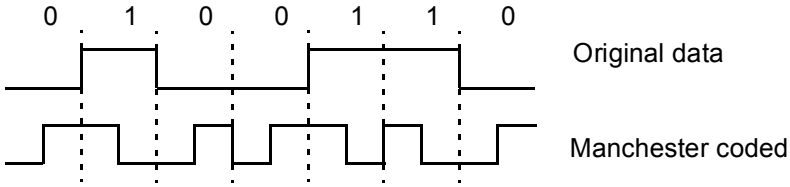
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COMMUNICATION PROTOCOL

MANCHESTER CODING DESCRIPTION

Manchester coding is defined as follows: data is sent during the first half-bit, complementary data is sent during the second half-bit.

Figure 3: Manchester coding example



The signal average value is constant. This allows clock recovery from the data stream itself. In order to achieve a correct clock recovery, Manchester coded data must have a duty cycle between:

- 48% and 52% in OOK,
- 45% and 55% in FSK.

PREAMBLE, ID, HEADER WORDS AND MESSAGE DESCRIPTION

The following description applies if the Data Manager is enabled (DME=1).

The ID word is a Manchester coded byte whose content has been previously loaded in the Configuration Register 2. The complement of the ID word is recognized as an ID word. ID word is sent at the same data rate as data.

A preamble is required:

- before ID,
- before Header if HE=1,
- before data if HE=0.

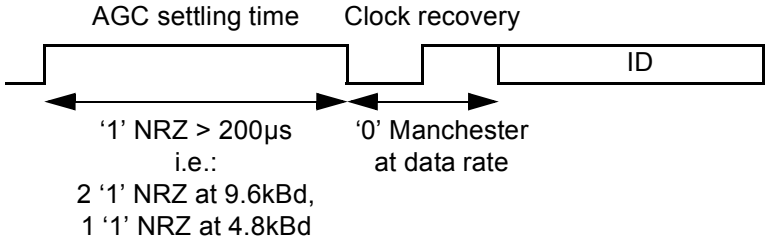
It enables:

- in case of OOK modulation, AGC to settle,
- in case of FSK modulation, data slicer reference voltage to settle,
- in any case, clock recovery.

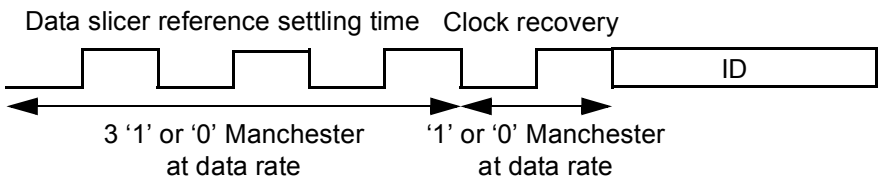
Figure 4 defines the Preamble word in OOK and FSK modulation. Preamble content must be carefully defined in order not to be decoded as an ID or Header word.

Figure 4: Preamble definition

OOK Modulation:



FSK Modulation:



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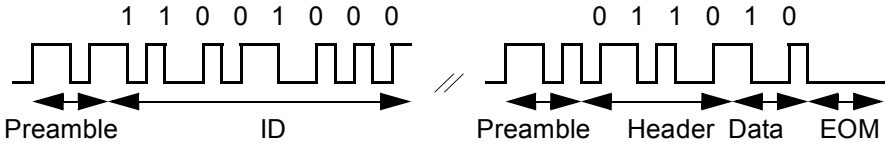
COMMUNICATION PROTOCOL

The Header word is a 4 bit Manchester coded message '0110' or its complement sent at the selected data rate. **This bit sequence and its complement must not be found in the sequence preamble and ID word.** Data must follow the Header without any delay.

Data are completed by a End-of-Message (EOM) word, consisting of 2 NRZ consecutive ones or zeroes. Even in case of FSK modulation, the data must be completed by a EOM and not by simply stopping the RF telegram. If the complement of the Header word is received, output data are complemented too.

The following example shows a complete message with Preamble, ID, Header words followed by 2 data bits, and an EOM. The preamble is placed at the beginning of both ID and Header words.

Figure 5: Complete message example



MESSAGE PROTOCOL

If the receiver is continuously Sleep/Run cycling, the ID word has to be recognized to stay in Run mode. Consequently, the transmitted ID burst has to be long enough to include two consecutive receiver Run cycles.
If the Strobe oscillator is enabled (SOE=1), the circuit is in Sleep mode during SR $\times$ T_{Strobe} and in Run mode during T_{Strobe} (where T_{Strobe} is the Strobe oscillator period and SR is the Strobe Ratio, see Table 5).

Therefore, the sleep/run cycle period is equal to (SR+1) $\times$ T_{Strobe}.
If SOE=0, these timings constraints must be respected by the external control applied on pin STROBE.

Figure 6: Complete telegram with ID detection

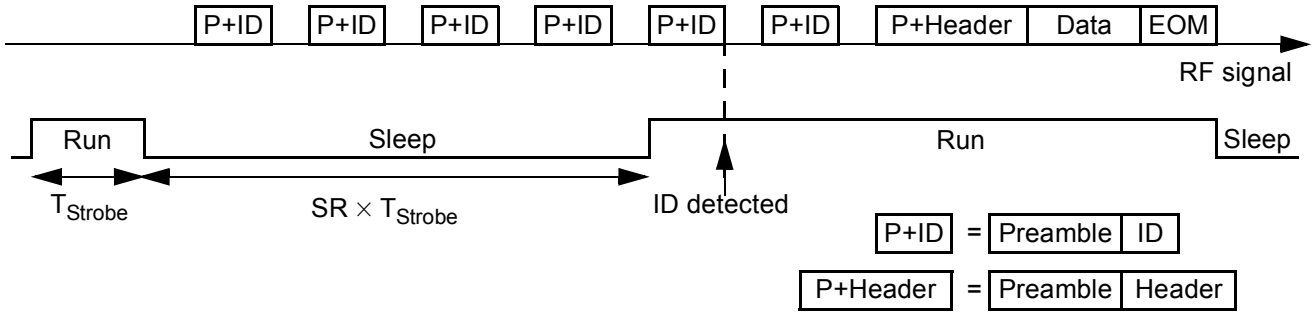
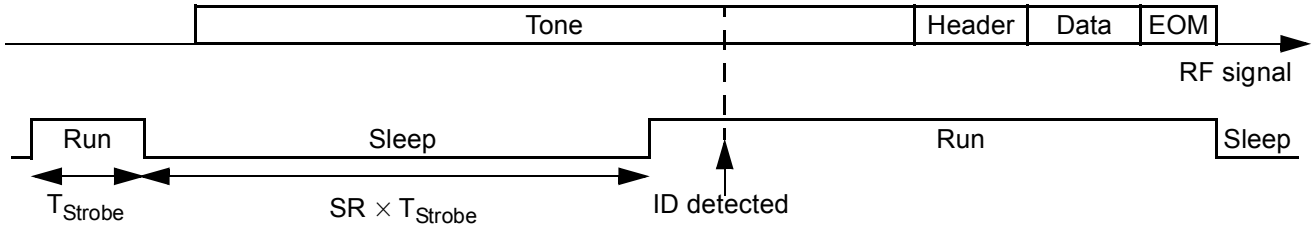


Figure 7: Complete telegram with tone detection



Figures 8 & 9 detail RF signals and the processing done by the receiver in several configuations.

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Figure 8: Telegrams with ID

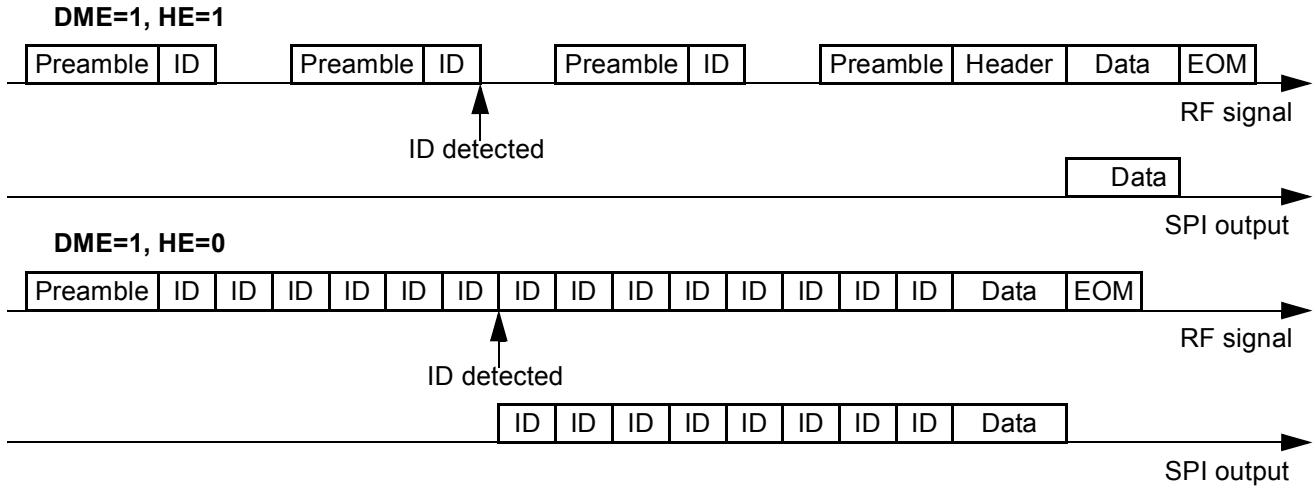
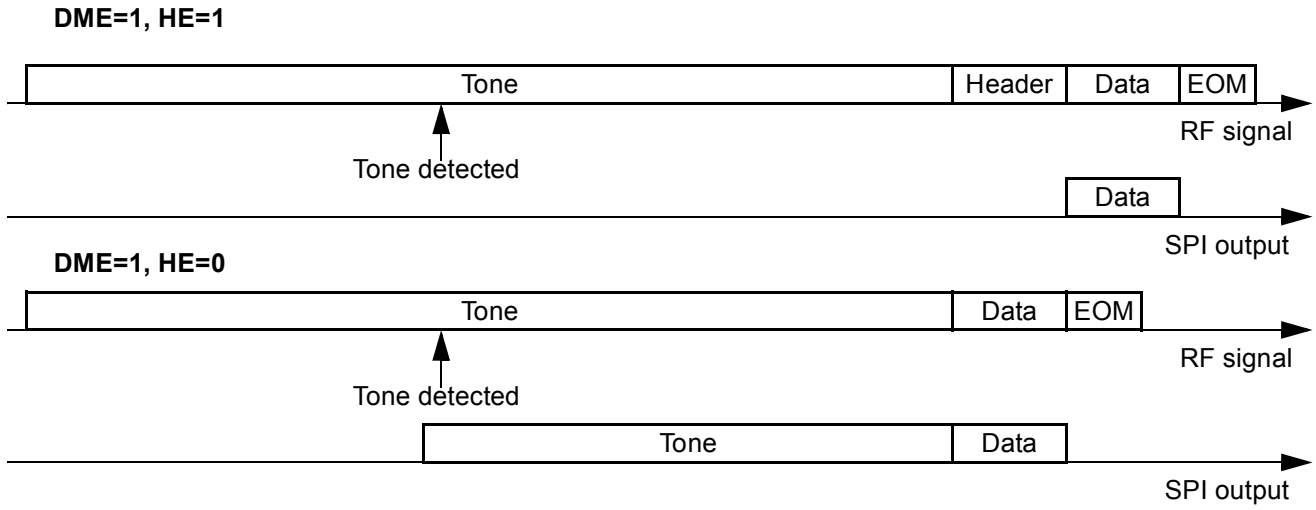


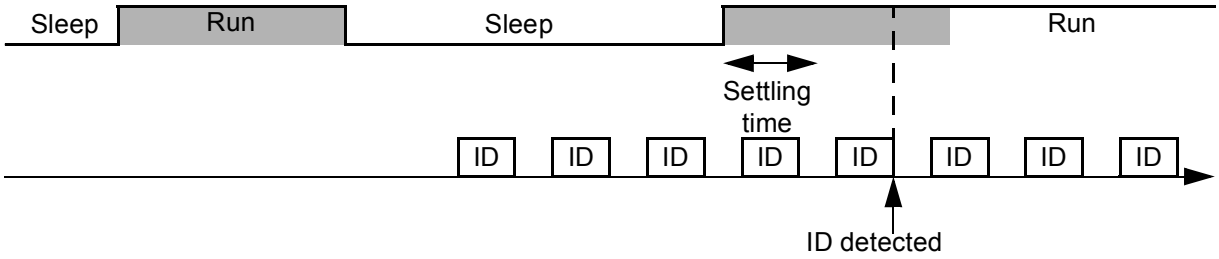
Figure 9: Telegrams with tone



RECEIVER START-UP DELAY

A settling time (1ms typ.) is required when entering into Wait mode. figure 10.

Figure 10: Wait usable window



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DATA MANAGER

This block has five purposes:
- ID detection,
- Header recognition,
- Clock recovery,
- Output data and recovered clock on SPI port,
- End-of-Message detection.

Table 2 details some ROMEO2 features versus the bits DME and SOE values.

Table 2: ROMEO2 features versus DME and SOE

DME	SOE	Timer	ROMEO2 kept in Run mode by	Microcontroller woken-up by
0	0	External control by STROBE pin	STROBE pin	Raw data
	1	Internal and external control by STROBE pin		
1	0	External control by STROBE pin	STROBE pin	Message Detection word
	1	Internal and external control by STROBE pin	ID detection and STROBE pin	Data clock

Table 3 details some ROMEO2 features versus DME values.

Table 3: ROMEO2 features versus DME

DME	SPI status	Data format	Output
0	Disabled	Bitstream No clock	MOSI -
1	Master when RESETB=1	Data bytes Recovered clock	MOSI SCLK

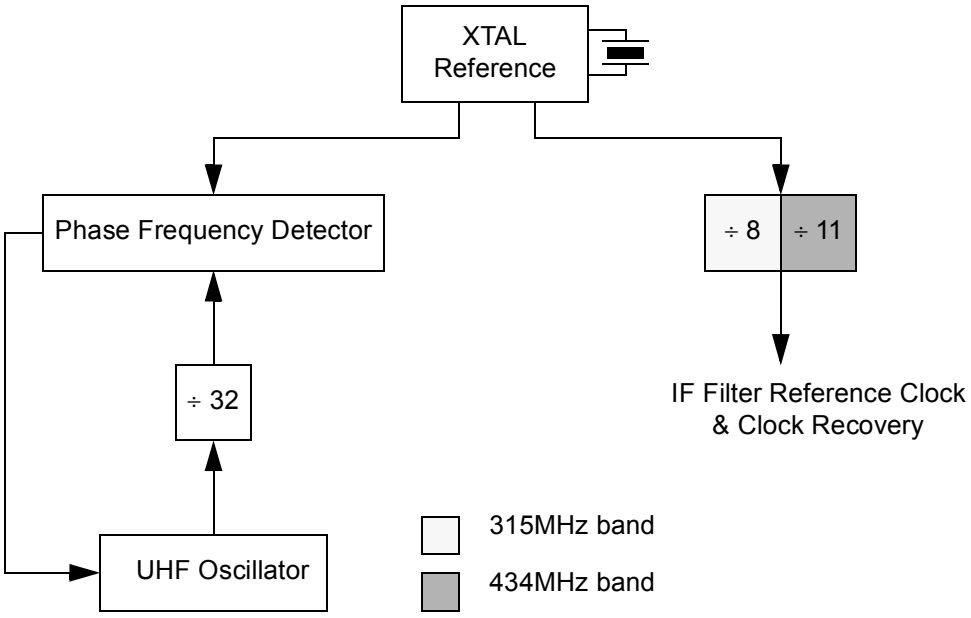
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CLOCK GENERATOR

Typical crystal frequencies are:
- 9.864375MHz for 315MHz band,
- 13.580625MHz for 434MHz band.

Figure 11: Clock generation diagram



SERIAL INTERFACE

ROMEO2 and the microcontroller communicate through a Serial Peripheral Interface (SPI). It enables:
- the microcontroller to set and check ROMEO2 configuration,
- ROMEO2 to send the received data.

If the SPI is not used, a Power On Reset (POR) sets ROMEO2 to operate correctly in a default configuration.

The interface is operated by the 3 following input/output pins:
- Serial Clock SCLK,
- Master Output Slave Input MOSI,
- Master Input Slave Output MISO.

The master clock is used to synchronise data movement both in and out of the device through its MOSI and MISO lines. The master and slave devices are capable of exchanging a byte of information during a sequence of eight clock cycles. Since SCLK is generated by the master device, this line is an input on a slave device.
The MISO line is configured as an input in a master device and as an output in a slave device. The MOSI line is configured as an output in a master device and as an input in a slave device. The MISO and MOSI lines transfer serial data in one direction with the most significant bit sent first. Data are captured on falling edges of SCLK. Data are shifted out on rising edge of SCLK. When no data are output, SCLK and MOSI force a low level. Using Motorola acronyms, this means that the clock phase and polarity control bits of the microcontroller SPI have to be CPOL= 0 and CPHA=1.

In configuration mode, as long as a low level is applied on RESETB (see state machine on figure 14 page 13), the microcontroller is the master node providing clock information on SCLK input, control and configuration bits on the MOSI line. If the default configuration is not the desired one, the microcontroller (MCU) can change it by writing into the configuration registers. The configuration registers can also be read back to check their contents. Configuration registers cannot be addressed separately, the whole configuration has to be sent as a 3x8 bitstream. The contents are written out as a 24-bit serial data stream. Transmissions which are not multiple of 24

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bits may lead to unexpected configurations. The first bit transmitted on MOSI does not change the content of the configuration registers. Note that a low level applied on RESETB does not affect the configuration register content.

When RESETB is set to a high level, if Data Manager is enabled (DME=1), ROMEO2 becomes master and sends received data on the MOSI line and the recovered clock on SCLK. It is then recommended that the MCU SPI is set as slave. If the data received does not fit in an entire number of bytes, the data manager will fill the last byte. If the data received constitute an whole number of bytes, the data manager may generate and send an extra byte whose content is irrelevant. If DME=0, the SPI is disabled. Raw data is sent on the MOSI line.

When ROMEO2 SPI is changed from master (run mode) to slave (configuration mode) or from slave to master, it is recommended that the MCU SPI is set as slave before the mode transition.

At power-on, the POR resets the internal registers. This defines the receiver default configuration (see gray rows on tables 4, 7 & 8). In this configuration, the SPI is disabled and ROMEO2 sends raw data on the MOSI line. This default configuration enables the circuit to operate as a standalone receiver without any external control. After POR, RESETB forces a low level. Therefore an external pull-up resistor should be used in order to avoid entering configuration mode.

Figure 12: Writing into configuration registers

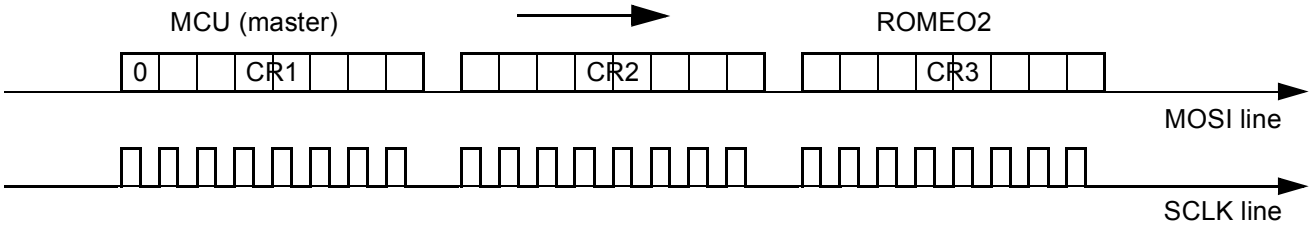
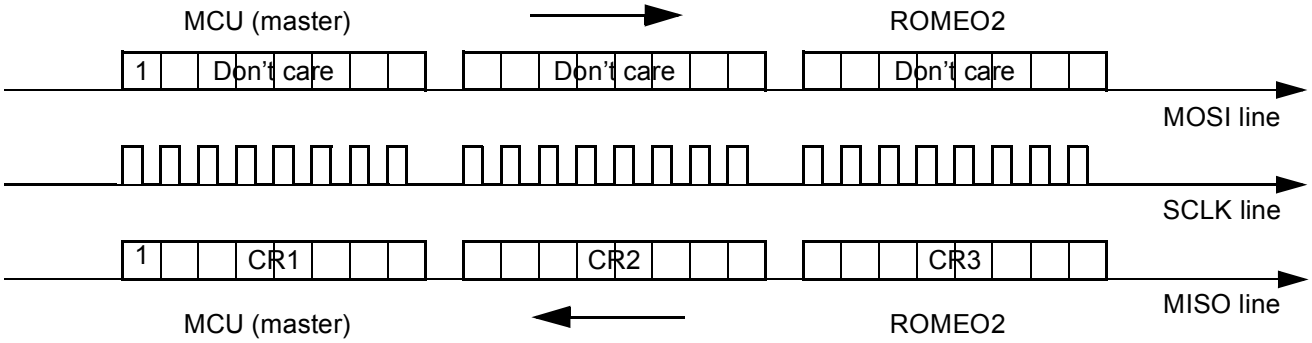


Figure 13: Reading configuration registers



CONFIGURATION REGISTERS

Table 4 describes the **Configuration Register 1** (CR1).

Table 4: Configuration Register 1

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Bit name	R/W	CF	MOD	SOE	SR1	SR0	DME	HE
Reset value	1	1	0	1	0	1	0	0

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- R/$\overline{W}$ controls the 3 registers access (read or write):

0 = Write CR1, CR2 ,CR3,
1 = Read CR1, CR2, CR3.

- CF defines the Carrier Frequency as shown onTable 5.

Table 5: Carrier Frequency selection

CF	Selected Frequency
0	315MHz
1	434MHz

- MOD sets the data Modulation type:

0 = On/Off Keying (OOK) modulation,
1 = Frequency Shift Keying (FSK) modulation.

- SOE enables the Strobe Oscillator:

0 = Disabled,
1 = Enabled,

Whatever SOE value has been programmed, a high level on STROBE sets the circuit into run mode.

- SR0/SR1 define the Strobe Ratio (SR) as shown on Table 6. SR is the ratio Sleep time over Run time and Run time=T_{Strobe} (where T_{Strobe} is the Strobe oscillator period).

Table 6: Strobe Ratio selection

SR1	SR0	Strobe Ratio
0	0	3
0	1	7
1	0	15
1	1	31

- DME enables the Data Manager:

0 = Disabled,
1 = Enabled.

Data are output on MOSI and the associated clock on SCLK.

- HE defines if a Header word is present (the bit HE is only active if DME=1):

0 = No header,
1 = Header.

Configuration Register 2 (CR2) defines the Identifier (ID) word content. The bits will be Manchester coded.

Table 7: Configuration Register 2

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Bit name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset value	0	0	0	0	0	0	0	0

Table 8 describes the **Configuration Register 3** (CR3).

Table 8: Configuration Register 3

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Bit name	DR1	DR0	MG	MS	PG	-	-	-
Reset value	1	0	0	0	0	0	0	0

- DR0/DR1 define the Data Rate (before Manchester coding) as shown onTable 9.

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Table 9: Data Rate selection

DR1	DR0	Selected Ratio
0	0	1.0 - 1.4 kBd
0	1	2 - 2.7 kBd
1	0	4 - 5.3 kBd
1	1	8.6 - 10.6 kBd

- MG sets the mixer gain:
  - 0 = Normal,
  - 1 = -17dB (typical).
- MS switches the MIXOUT pin:
  - 0 = To the mixer output,
  - 1 = To the IF input.

Table 10: Mixer and MIXOUTconfiguration

MG	MS	Mixer Gain	MIXOUT
0	0	Normal	Mixer output
0	1	Normal	IF input
1	0	Reduced	Mixer output
1	1	Forbidden, mixer test mode only	

The combination MG=1, MS=1 is forbidden in any application. It configures the receiver in a test mode where the mixer runs at $f_{VCO}/4$.

- PG sets the phase comparator gain (see “The local oscillator PLL” chapter, page 4):
  - 0 = High gain mode,
  - 1 = Low gain mode.

STATE MACHINES

AFTER POR RESET STATE MACHINE

There are 3 different modes for the receiver.

Sleep mode corresponds to the low power consumption mode:
- if SOE=0, the whole receiver is shutdown,
- if SOE=1, the strobe oscillator remains active.

Configuration mode is used for writing or reading the internal registers. In this mode, the SPI is slave and the receiver is enabled. The crystal oscillator is running and generates the clock for the SPI. This implies that before the circuit is in sleep mode, a delay corresponding to the crystal oscillator wake-up time must be inserted between the falling edge on RESETB and the start of the transmission on the SPI lines. The local oscillator is running as well. This means that demodulated data can be read on DMDAT but are not sent by the SPI.

In **Run mode**, the receiver is enabled (crystal and local oscillators are running). It is either waiting for an RF telegram or receiving one.

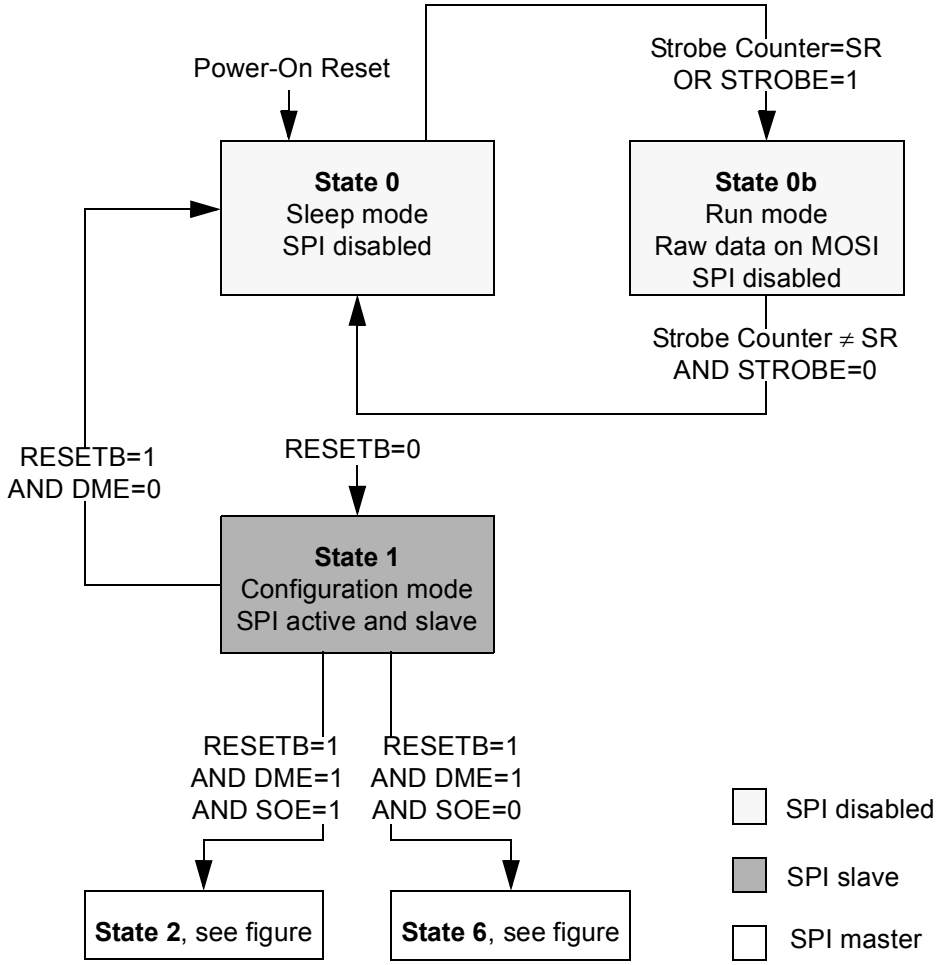
Figure 14 details the state machine after Power On Reset (POR). The state machine is synchronized by a sampling clock at 615kHz (sampling period Ts=1.6µs), derivated from the crystal oscillator. The transition time between state 1 and states 2 or 6 is less than $3 \times$ Ts.

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After POR, the circuit is in **state 0** and configuration registers' content is set to the reset value. This enables to use ROMEO2 in a standalone configuration without any external control.
As long as a low level is applied on RESETB, the circuit stays in **state 1**. This configuration mode enables to write or read the internal registers through the SPI interface.

Figure 14: After POR state machine



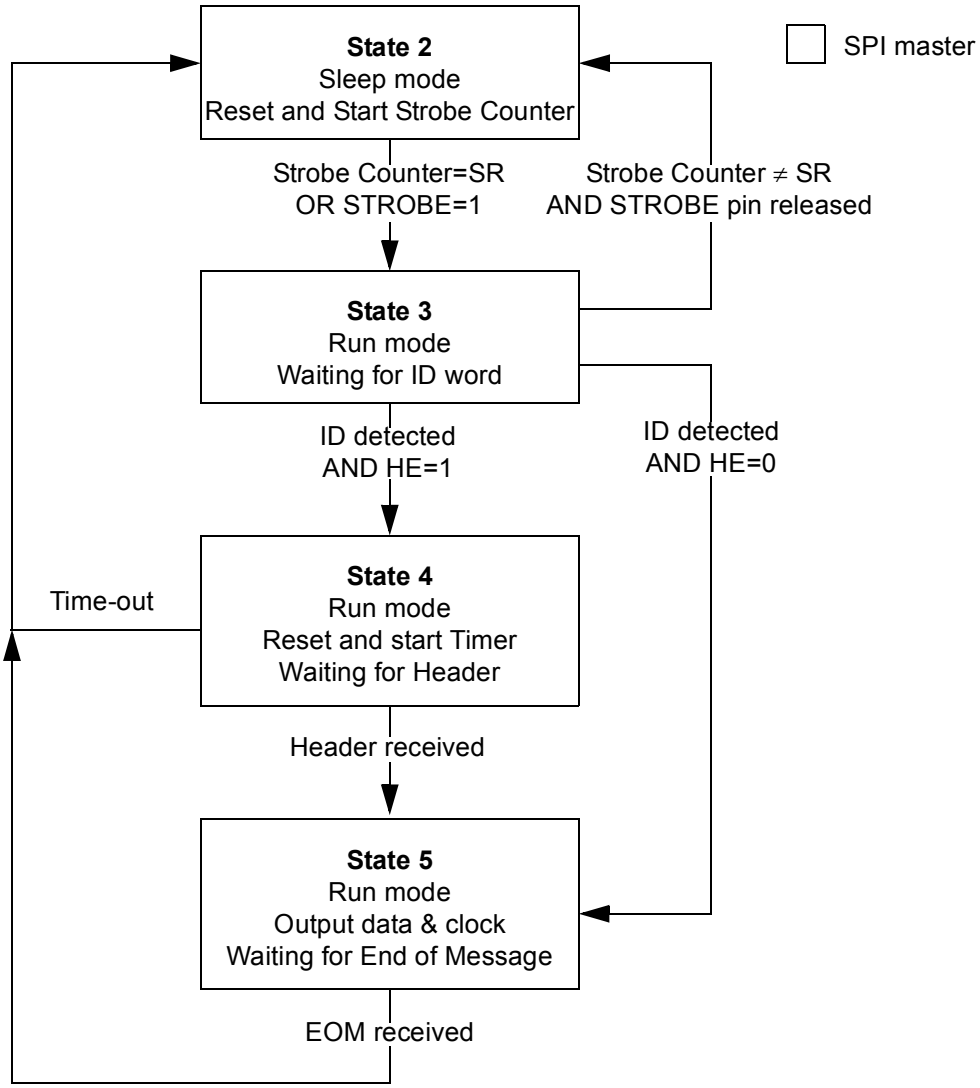
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STATE MACHINE WITH STROBE OSCILLATOR CONTROL

Figure 15 details the state machine when the strobe oscillator is enabled (SOE=1).

Figure 15: State machine with strobe oscillator control



State 2:
The circuit is in Sleep mode, except for the Strobe oscillator and the Strobe counter.

State 3:
The circuit is waiting for a valid ID word. If ID or its complement is detected, the state machine advances to state 4. If not, it will go back into sleep mode (state 2) at the end of the Strobe period.

State 4:
ID or its complement has been detected, Data Manager is waiting for Header or its complement. Time-out counter is running. This counter will count up to 66 (± 1) times the strobe oscillator period (T_{Strobe}).

State 5:
If Header has been received, data and clock signals are output on the SPI port until End of Message indicates the data sequence end. If the complement of Header has been received, output data are complemented too.

For all states:
At any time, a low level applied on RESETB during more than one Ts forces the state machine to state 1. When

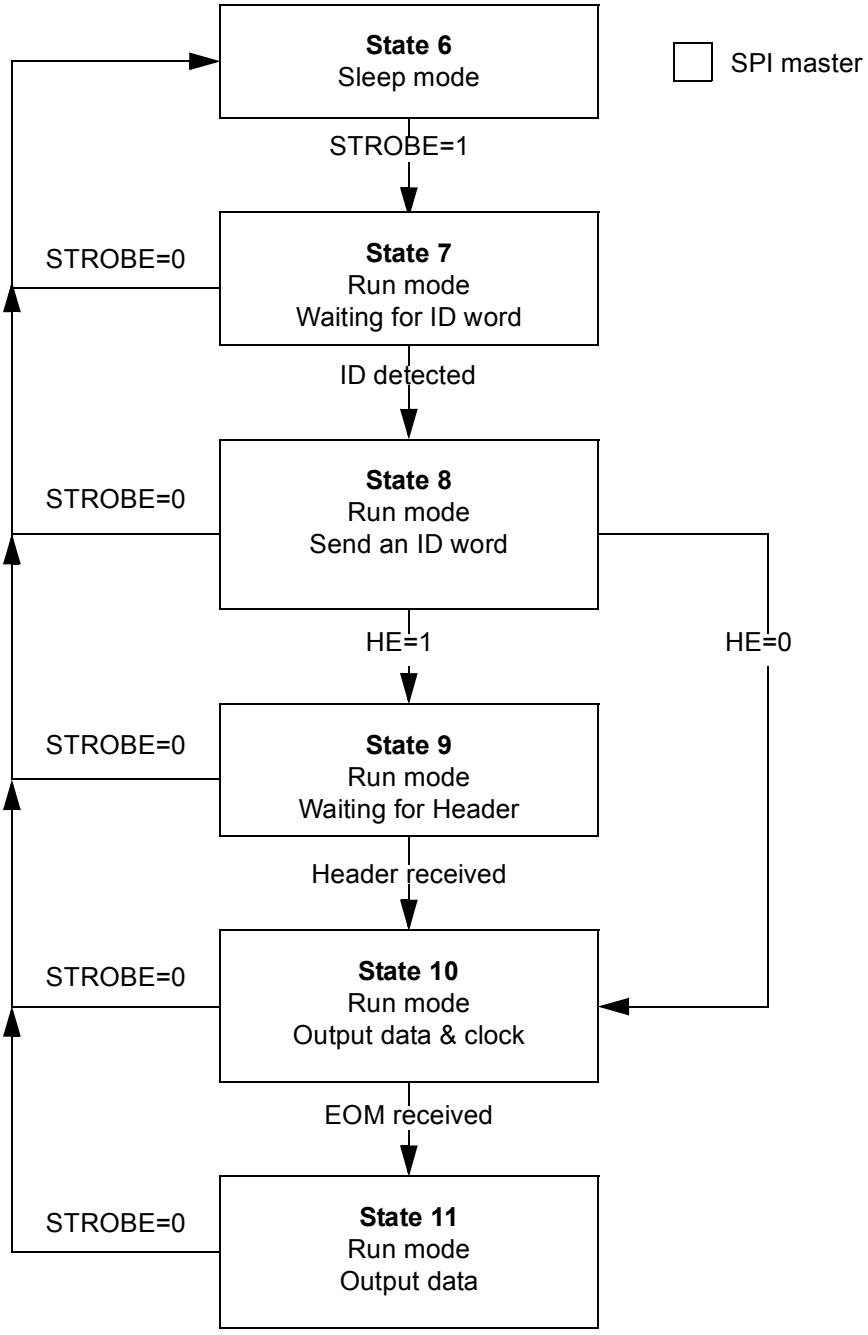
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the transition condition from one state to the next one is fulfilled, the transition time is one Ts (except for reaching state 2). The transition time to state 2 is 2 × Ts (+ duration of the dummy byte if it is shifted out, only for transition coming from state 5).

STATE MACHINE WITH STROBE PIN CONTROL

Figure 16 details the state machine when the strobe oscillator is disabled (SOE=0).

Figure 16: State machine with STROBE pin control



State 6:

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Programming SOE=0 sets ROMEO2 to state 6. The circuit is in Sleep mode.

State 7:
A high level applied on STROBE sets the circuit into state 7. If an ID or its complement is detected, the state machine advances to state 8. If not, it will stay in state 7 as long as STROBE is high.

State 8:
After ID or its complement detection, ID byte is sent to the microcontroller on MOSI line at 310kBd. This warns the microcontroller that data are received which means that an high level has to be maintained on STROBE. At any time a low level applied on STROBE sets the circuit into state 6.

State 9:
If Header or its complement is detected, the state machine advances to state 10. If not, it will stay in state 9 as long as STROBE is high.

State 10:
If Header has been received, data and clock signals are output on the SPI port. If the complement of Header has been received, output data are complemented too. At any time a low level applied on STROBE sets the circuit into state 6, after the current byte is fully transmitted.

State 11:
If data are received after a End of Message they are output on the MOSI pin without clock recovery.

For all states:
At any time, a low level applied on RESETB for more than one Ts forces the state machine to state 1. When the transition condition from one state to the next one is fulfilled, the transition time is one Ts except reaching state 6. The transition time for reaching state 6 is 2 $\times$ Ts (+ time needed to shift out a full byte if STROBE pin is forced to low when in state 10).

STROBE OSCILLATOR

The Strobe Oscillator is a relaxation oscillator in which an external capacitor C5 is charged by an external resistance R2 (refer to figure 17 and table 11). When a threshold is reached or exceeded C5 is discharged and the cycle restarts. The period is: $T_{Strobe}=0.12 \times R2 \times C5$.

The circuit may be forced into states 0b, 3, 7 etc. (see State Machine Diagrams) by setting the STROBE pin to V_{CC}. As V_{CC} is above the oscillator threshold voltage referred to in the previous paragraph, the condition in which the STROBE pin is set to V_{CC} is internally detected and the oscillator pull-down circuitry disabled to limit the current which must be supplied.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC}=[4.5V;5.5V], operating temperature range T_A=[-40°C;+85°C]. Values refer to the circuit in recommended in the application schematic (see figure 17), unless otherwise specified. Typical values reflect average measurement at V_{CC}=5V, T_A=25°C, using MC33591.

	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
1	**General Parameters**					
1.1	Mean Supply Current	315 & 434MHz bands, Strobe Ratio=7, PG=0, see note 1	-	815	1100	µA
1.3	Supply Current in Run & Configuration Modes	315 & 434MHz bands, PG=0	-	5.7	7.4	mA
1.5	Supply Current in Sleep Mode	Strobe oscillator enabled	-	115	250	µA
1.6		Strobe oscillator disabled	-	90	200	µA
1.7	Supply Current in Run & Configuration Modes	315 & 434MHz bands, PG=1	-	5.4	7.0	mA
1.9	Sleep Mode to Run Mode Delay	Circuit ready to receive, OOK modulation	-	1.0	1.8	ms
1.10	" "	Circuit ready to receive, FSK modulation, f_{data} is the data rate in kBd	-	0.7 + 3 / f_{data}	1.4 + 3 / f_{data}	ms
1.11	Run Mode to Sleep Mode Delay	Measured between falling edge on STROBE and supply current reduced to 10%	-	0.1	-	ms
Note 1: If I_{Run} and I_{Sleep} are the supply currents in Run and Sleep modes and SR is the Strobe Oscillator Ratio, the Mean Supply Current I_{Mean} is given by: $I_{Mean}=(I_{Run} + SR \times I_{Sleep}) / (SR + 1)$.						

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC}=[4.5V;5.5V], operating temperature range T_A=[-40°C;+85°C]. Values refer to the circuit in recommended in the application schematic (see figure 17), unless otherwise specified. Typical values reflect average measurement at V_{CC}=5V, T_A=25°C, using MC33591.

	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
2	**RF Parameters** General and Front End parameters assume a 50Ω resistor in parallel with the D.U.T. except where the use of a matching network is specified.					
2.1.1	Sensitivity in OOK at nominal transmitter center frequency	DME=0, with matching network, see notes 2, 3, 5, 6	-	-105	-96	dBm
2.1.2	" "	DME=1, with matching network, see notes 2, 4, 5, 6	-	-103	-94	dBm
2.1.3	" "	DME=0, see notes 2, 3, 6	-	-96	-87	dBm
2.1.4	" "	DME=1, see notes 2, 4, 6	-	-94	-85	dBm
2.2.1	Sensitivity in OOK at nominal transmitter center frequency Operating temperature range -20°C to +85°C	DME=0, with matching network, see notes 2, 3, 5, 6	-	-105	-98	dBm
2.2.2	" "	DME=1, with matching network, see notes 2, 4, 5, 6	-	-103	-96	dBm
2.2.3	" "	DME=0, see notes 2, 3, 6	-	-96	-89	dBm
2.2.4	" "	DME=1, see notes 2, 4, 6	-	-94	-87	dBm
2.3.1	Sensitivity in FSK at nominal transmitter center frequency	DME=0, with matching network, see notes 3, 5, 6	-	-105	-99	dBm
2.3.2		DME=1, with matching network, see notes 4, 5, 6	-	-103	-97	dBm
2.3.3		DME=0, see notes 3, 6	-	-96	-90	dBm
2.3.4		DME=1, see notes 4, 6	-	-94	-88	dBm
2.6.1	Sensitivity in FSK	Transmitter frequency shift at +/-40kHz 500kHz IF bandwidth DME=1, see notes 4, 6	-	-	-86	dBm
2.6.2	" "	Transmitter frequency shift at +/-80kHz 500kHz IF bandwidth DME=1, see notes 4, 6	-	-	-84	dBm
2.8.2	Variation of DMDAT level, FSK modulation	500kHz IF bandwidth, see note 7	-6	-	6	dB
2.9	Image Frequency Rejection	315MHz band	17	25	-	dB
2.10		434MHz band	20	29	-	dB

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	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
2.12	IP3	315 MHz band, measured at MIXOUT, min. value for 2 pairs of frequencies (MHz): (340.00, 365.00), (500.00, 685.00)	-	-17	-	dBm
2.13		434MHz band, measured at MIXOUT, min. value for 2 pairs of frequencies (MHz): (455.00, 476.08), (550.00, 666.08)	-	-19	-	dBm
2.15	Max. Detectable Input Signal Level of a NRZ 1	OOK modulation, TX modulation depth: 97.5%	-	-14	-	dBm
2.27	Out-of-Band Jammer desensitization for OOK & FSK modulation 434MHz band, PG=1, sensitivity reduced by 6dB	CW jammer at RF ±500kHz, see note 4	-	16	-	dBc
2.28		CW jammer at RF ±1MHz, see note 4	-	24	-	dBc
2.29		CW jammer at RF ±2MHz, see note 4	-	33	-	dBc
2.39	In-Band Jammer desensitization 434MHz band sensitivity reduced by 6dB	OOK modulation, CW jammer at RF ±50kHz, see note 4	-	-10	-	dBc
2.40	“ “	FSK modulation, ±35kHz deviation, CW jammer at RF ±50kHz, see note 4	-	-7	-	dBc
2.43	Input Impedance: // Resistance	315MHz, level on RFIN□□□ ≤ -50dBm	-	1.1	-	kΩ
2.44		434MHz, level on RFIN□□□ ≤ -50dBm	-	1.1	-	kΩ
2.46	Input Impedance: // Capacitance	315MHz band	-	1.4	-	pF
2.47		434MHz band	-	1.4	-	pF
2.51	Mixer Conversion Gain	315 & 434MHz bands, from RFIN to MIXOUT	-	48	-	dB
2.53	Mixer Gain Reduction	315 & 434MHz bands, when setting MG=1	-	18	-	dB
2.55	Mixer Input Gain reduced by 1dB	315 & 434MHz bands	-	-49	-	dBm
2.57	Mixer AGC Settling Time	RF rise time < 400ns, 10 to 90% rise time	-	4	-	µs
2.58	Mixer AGC Gain Decay Rate		-	5	-	dB/ ms

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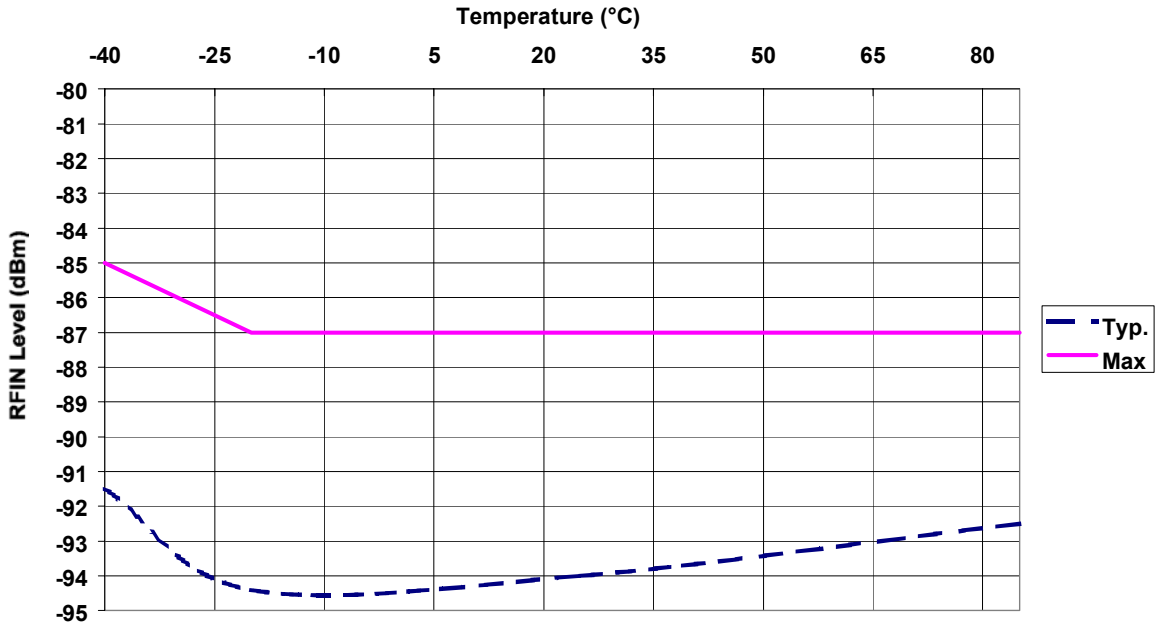
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	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
2.59	Local Oscillator Leakage	315 & 434MHz bands, at matching network input, see note 5	-	-102	-70	dBm

Note 2: OOK Sensitivity vs Temperature characteristic (shown for parameters 2.1.4 & 2.2.4)



Parameters 2.1.1 to 2.1.3 and 2.2.1 to 2.2.3 characteristics vs temperature are similar.

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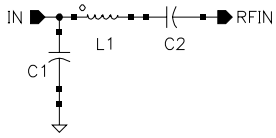
Unless otherwise specified, V_{CC}=[4.5V;5.5V], operating temperature range T_A=[-40°C;+85°C]. Values refer to the circuit in recommended in the application schematic (see figure 17), unless otherwise specified. Typical values reflect average measurement at V_{CC}=5V, T_A=25°C, using MC33591.

	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	

Note 3: **Sensitivity measurement method with Data Manager disabled (DME=0)**
A continuous Manchester coded 0 sequence (4.8kBd, OOK modulation depth: 100%, FSK modulation deviation: 35kHz, 50% duty cycle) is applied at RFIN. The mean value of the frequency of the output signal on MOSI is measured over 200 cycles. The sensitivity is defined as the lowest input level during an NRZ one corresponding to a mean output frequency deviation lower than 5% of the expected data rate.

Note 4: **Sensitivity measurement method with Data Manager enabled (DME=1, HE=0)**
A complete telegram (4.8kBd, OOK modulation depth: 100%, FSK modulation deviation: 35kHz, 50% duty cycle) including preamble, ID word and data (80 random bits without Header) is applied at RFIN. The sensitivity is defined as the lowest input level during an NRZ one necessary to achieve 0 Bit Error Rate (BER).

Note 5: **50Ω matching networks**
434MHz band: C1=1.5pF, C2=100pF, L1=68nH.



Tolerances: +/-10% for capacitances; +/-2% for inductor

Note 6: **Sensitivity measurement conditions**
* OOK & FSK Modulation (+/-35kHz) at 4.8kBd (50% duty cycle)
* 315MHz & 434MHz bands (500kHz IF bandwidth)
* Performances include receiver crystal tolerance of +/-80ppm over temperature range i.e. +/-35kHz @ 434MHz

Note 7: **FSK variation measurement conditions**
A frequency modulated signal, carrier = 660kHz with ±35kHz deviation is injected at MIXOUT
Measure the DMDAT voltage swing at 660kHz, this will be DMDAT(Ref) in actual temperature/Vcc conditions
Measure the DMDAT voltage swing from Freq[1] = 660kHz - 120kHz to Freq[2] = 660kHz + 120kHz
DMDAT(Ref) / DMDAT(Freq[x]) is measured over the whole range Freq[1] to Freq[2]

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	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
3	**IF filter, IF Amplifier, FM to AM Converter and Envelope Detector** The IF filter operates at approximately 660kHz, with a 500kHz bandwidth.					
3.2	IF High Cut Off Frequency at -3dB	IF bandwidth: 500kHz	850	940	-	kHz
3.4	IF Low Cut Off Frequency at -3dB	IF bandwidth: 500kHz	-	460	520	kHz
3.7	IF Cut Off Low Freq. at -30dB	IF bandwidth: 500kHz	-	290	-	kHz
3.8	IF Cut Off High Freq. at -30dB		-	1260	-	kHz
3.10		IF bandwidth: 500kHz	-	480	580	kHz
3.12	Total filter gain variation within -3dB Bandwidth	IF bandwidth: 500kHz	-3	-	3	dB
3.13	IF Amplifier Gain	From MIXOUT to DMDAT	-	55	-	dB
3.14	IF AGC Dynamic Range	OOK modulation	-	55	-	dB
3.15	IF AGC Gain Decay Rate		-	2.5	-	dB/ ms
3.16	IF Amplifier AGC Settling Time		-	75	200	µs
3.17	Detector Output Signal Amplitude	OOK modulation, measured at DMDAT	-	260	-	mV_{pk-pk}
3.19	Carrier Deviation	FSK modulation, IF bandwidth 500kHz	±35	-	±80	kHz

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	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
4	**PLL Divider & Crystal Oscillator**					
4.1	Maximum Crystal Series Resistance		-	-	200	Ω
5	**Data Filter & Slicer, Data Manager, SPI**					
5.1	Data Frequency	OOK and FSK modulations, DME=0	1	-	11	kHz
5.2	Low pass filter delay 2nd order Butterworth response	DR1=0, DR0=0, 1200 bauds	51	73	102	µs
5.3		DR1=0, DR0=1, 2400 bauds	30	42	57	µs
5.4		DR1=1, DR0=0, 4800 bauds	19	25	34	µs
5.5		DR1=1, DR0=1, 9600 bauds	12	16	22	µs
5.6	Data Rate Range for Clock Recovery	DR1=0, DR0=0	1.0	-	1.4	kBd
5.7		DR1=0, DR0=1	2	-	2.7	kBd
5.8		DR1=1, DR0=0	4	-	5.3	kBd
5.9		DR1=1, DR0=1	8.6	-	10.6	kBd
5.10	Input Low Voltage	Pins MOSI, SCLK, RESETB	0	-	$0.3 \times V_{CC}$	V
5.11	Input High Voltage		$0.7 \times V_{CC}$	-	V_{CC}	V
5.13	Input Pull Down Current	Pins MOSI, SCLK, RESETB, $V_{IN}=V_{CC}$	-	2	-	µA
5.14	Output Low Voltage	Pins MOSI, MISO, SCLK, $\|I_{LOAD}\|$ =10µA	0	0.02	$0.2 \times V_{CC}$	V
5.15	Output High Voltage		$0.8 \times V_{CC}$	4.97	V_{CC}	V
5.16	Fall/Rise Time	Pins MOSI, MISO, SCLK, C_{LOAD} = 5pF, from 10% to 90% of the output swing	-	-	100	ns
5.17	Input Low Voltage	Pin STROBE used as digital input	0	-	0.5	V
5.18	Input High Voltage		4.4	-	V_{CC}	V
5.19	Input Pull Down Current	Pin STROBE used as digital input, $V_{IN}=V_{CC}$	-	-	50	µA
5.20	SPI data rate	On MOSI, MISO & SCLK, SPI master or slave, see note 8	-	-	310	kBd

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ELECTRICAL CHARACTERISTICS

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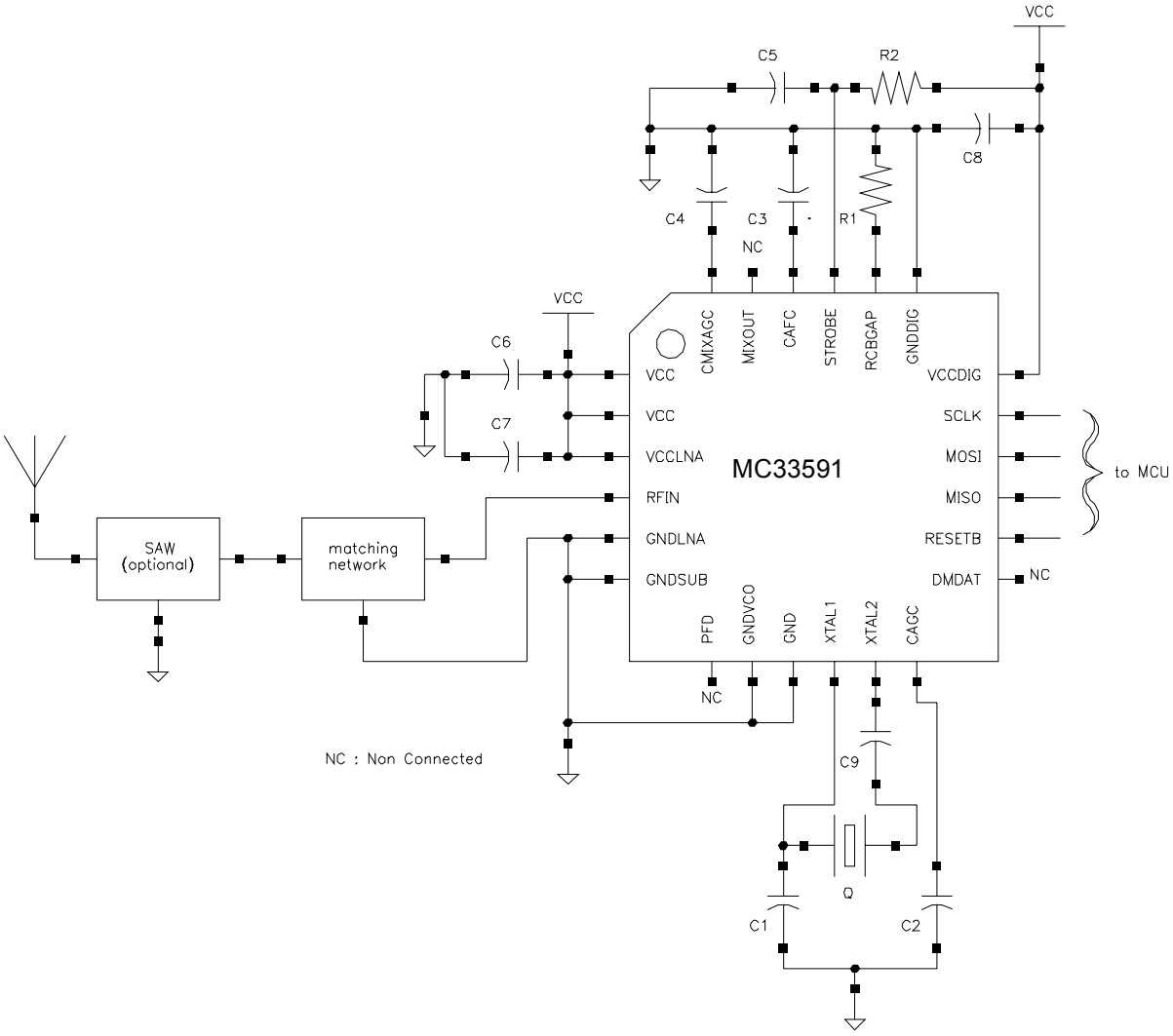
	Parameter	Test Conditions, Comments	Limits			Unit
			Min.	Typ.	Max.	
5.21	SPI interface source current $V_{OH}=0.8 \times V_{CC}$	MOSI, MISO, SCLK pins	60	170	-	µA
5.22	SPI interface sink current $V_{OL}=0.2 \times V_{CC}$		60	220	-	µA
Note 8: As well as the state machine, the SPI interface is synchronized by a sampling clock at 615kHz derivated from the crystal oscillator. The maximum speed is then half this synchronization clock.						
6	**Strobe Oscillator (SOE=1)**					
6.1	Strobe Oscillator Period (T_{Strobe}) Range	$T_{Strobe}=0.12 \times R2 \times C5$, see figure 17	2	3.8	87	ms
6.9	External Capacitor (C5)		-	68	330	nF
6.10	External Resistor (R2)		-	470	2200	kΩ
6.2	Strobe Oscillator Period Accuracy	T_J=25°C, V_{CC}=5V, external components R2 & C5 fixed	-5	-	5	%
6.3	Strobe Oscillator Period Temperature Coefficient		-	0.05	-	%/°C
6.4	Strobe Oscillator Period Supply Voltage Coefficient	$(\Delta T_{Strobe}/T_{Strobe})/(\Delta V_{CC}/V_{CC})$	-	0.2	-	-
6.5	Sink Output Resistance	Pin STROBE	-	6	-	kΩ
6.7	High Threshold Voltage		-	1.0	-	V
6.8	Low Threshold Voltage		-	0.45	-	V

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APPLICATION SCHEMATIC

Figure 17: Application schematic



Component description: see tables 11, 12, 13.

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APPLICATION SCHEMATIC

Table 11: Component description

Component	Function	Value	Unit
Q	Reference oscillator crystal	315MHz band: 9.864375	MHz
		434MHz band: 13.580625	MHz
R1	Current reference resistor	180 ± 1%	kΩ
R2	Strobe oscillator resistor	470	kΩ
C1	Crystal load capacitor	10	pF
C2	- OOK modulation - IF amplifier AGC capacitor	100 ± 10%	nF
	- FSK modulation - Low pass filter capacitor	See table 13	
C3	AFC capacitor	100 ± 10%	pF
C4	Mixer AGC capacitor	10 ± 10%	nF
C5	Strobe oscillator capacitor	68	nF
C6	Power supply decoupling capacitor	100	nF
C7		100	pF
C8		1	nF
C9	Crystal DC decoupling capacitor	10	nF

R2 and C5 values correspond to a strobe oscillator period T_{Strobe}=3.8ms.

Exemples of crystal references are given below

Table 12: Typical crystal characteristics (SMD package)

Parameter	**NDK LN-G102-952 (for 315MHz)**	**NDK LN-G102-877 (for 434MHz)**	**Unit**
Crystal frequency	9.864375	13.580625	MHz
Load capacitance	12	12	pF
Motional capacitance	3.71	4.81	fF
Static capacitance	1.22	1.36	pF
Max loss resistance	100	50	Ω

CAGC capacitor is data rate related in FSK modulation.

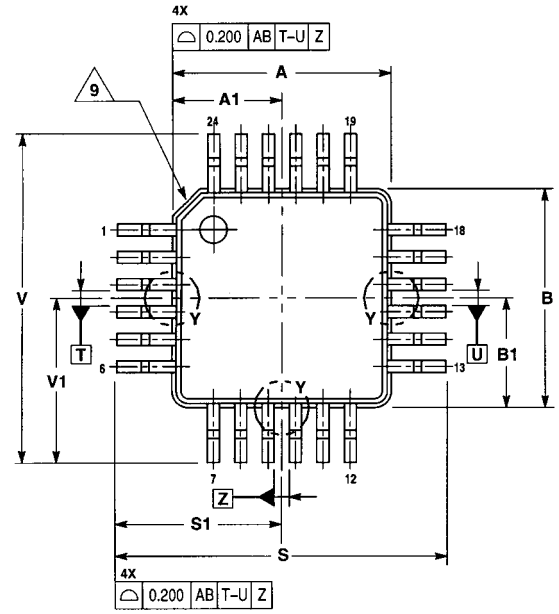
Table 13: C2 value versus data rate in FSK modulation

	Data Rate				Unit
	1.2	2.4	4.8	9.6	kBd
C2	100 ± 10%	47 ± 10%	22 ± 10%	12/10 ± 10%	nF

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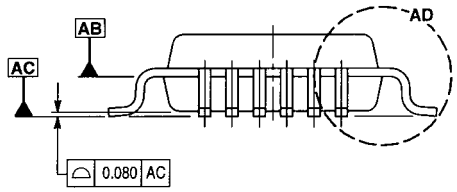
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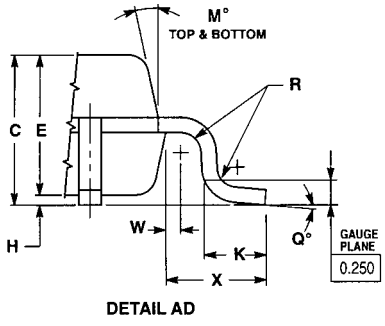
CASE OUTLINE DIMENSIONS



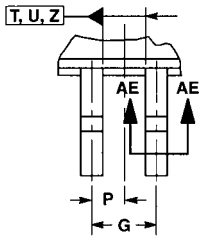
NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

DIM	MILLIMETERS MIN	MAX
A	4.000 BSC	
A1	2.000 BSC	
B	4.000 BSC	
B1	2.000 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
Q	0°	7°
R	0.150	0.250
S	6.000 BSC	
S1	3.000 BSC	
V	6.000 BSC	
V1	3.000 BSC	
W	0.200 REF	
X	1.000 REF	

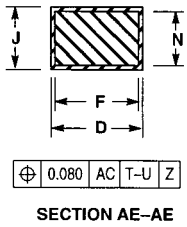




DETAIL AD



DETAIL Y



SECTION AE–AE

CASE 977–02
ISSUE A

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