High Speed CMOS Logic – 54HC241

Octal 3-State Non-Inverting Buffer / Line Driver / Line Receiver in bare die form

Rev 1.0
30/11/21

Description

The 54HC241 is produced on a 2.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device can be used as two 4-bit buffers or one 8-bit buffer & features non-inverting inputs with two output enables, each controlling four of the 3-state outputs. The device improves performance & density in clock drivers, 3-state memory address drivers & bus orientated transmitters and receivers. Device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. All inputs are equipped with protection circuits against static discharge & transient excess voltage.

Features:

- Output Drive Capability: 15 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS241
- Lower power alternative to Bipolar or BiCMOS logic
- Full military temperature range.

Ordering Information

The following part suffixes apply:

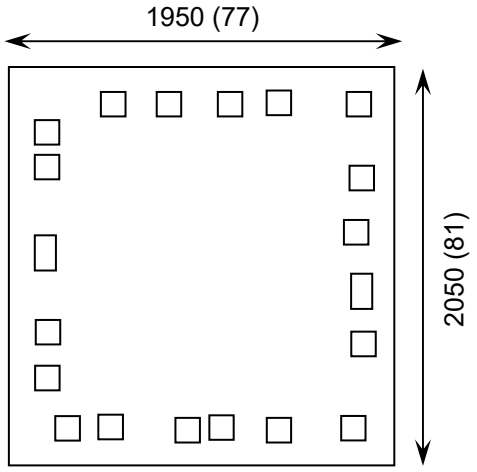
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

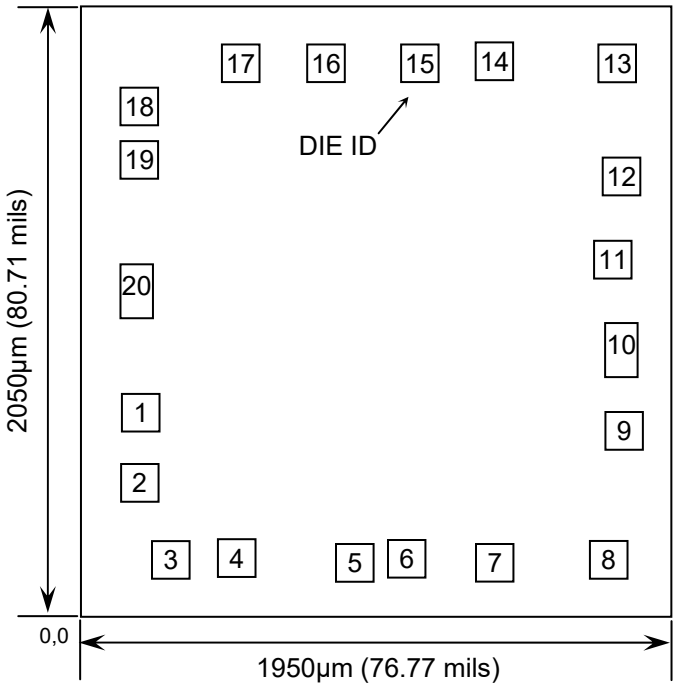
Mechanical Specification

Die Size (Unsawn)	1950 x 2050 77 x 81	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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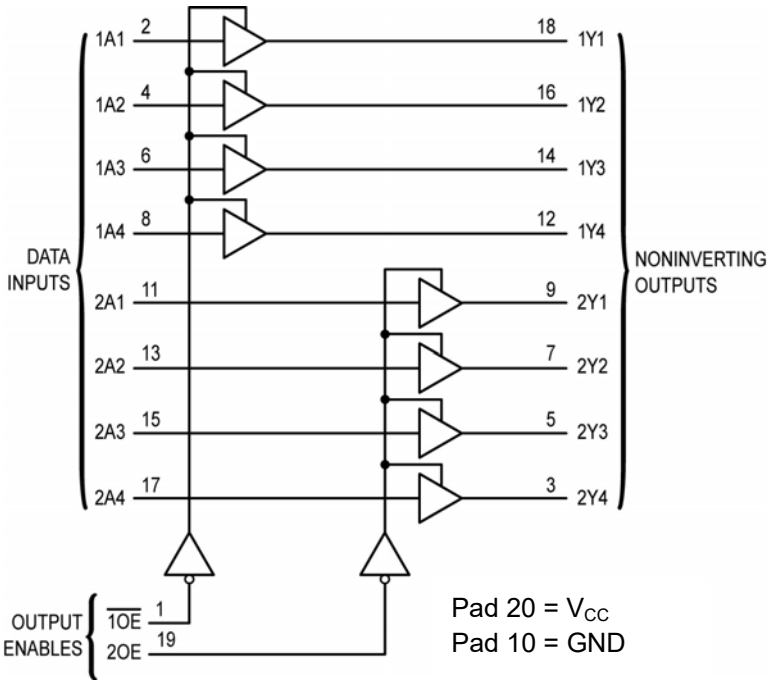
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Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{1OE}$	0.152	0.636
2	1A1	0.152	0.396
3	2Y4	0.300	0.142
4	1A2	0.470	0.152
5	2Y3	0.868	0.132
6	1A3	1.038	0.152
7	2Y2	1.330	0.132
8	1A4	1.709	0.142
9	2Y1	1.729	0.578
10	GND	1.729	0.812
11	2A1	1.699	1.149
12	1Y4	1.729	1.438
13	2A2	1.719	1.804
14	1Y3	1.301	1.824
15	2A3	1.062	1.804
16	1Y2	0.758	1.804
17	2A4	0.468	1.804
18	1Y1	0.142	1.662
19	2OE	0.142	1.489
20	V_{CC}	0.142	1.005
CONNECT CHIP BACK TO V_{CC}			

Logic Diagram



Pad 20 = V_{CC}
Pad 10 = GND

Truth Table

INPUT		OUTPUT	INPUT		OUTPUT
$\overline{1OE}$	1A	1Y	2OE	2A	2Y
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

H = High level (steady state)
L = Low level (steady state)
X = Don't care, Z = High impedance

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Pad Descriptions

ADDRESS INPUTS
1A1, 1A2, 1A3, 1A4, 2A1, 2A2, 2A3, 2A4
(Pads 2, 4, 6, 8, 11, 13, 15, 17)
Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROL INPUTS
$\overline{1OE}$, (Pad 1)
Output enable active–low. When a low level is applied to this pin, the outputs are enabled and the devices function as non-inverting buffers. When a high level is applied, the outputs assume the high impedance state.
2OE, (Pad 19)
Output enable active–high. When a high level is applied to this pin, the outputs are enabled and the devices function as non-inverting buffers. When a low level is applied, the outputs assume the high impedance state.

OUTPUTS
1Y1, 1Y2, 1Y3, 1Y4, 2Y1, 2Y2, 2Y3, 2Y4
(Pads 18, 16, 14, 12, 9, 7, 5, 3)
Device outputs. Depending upon the state of the output enable pins, these outputs are either non-inverting outputs or high–impedance outputs.

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pin	I_{IN}	±20	mA
DC Output Current, per pin	I_{OUT}	±35	mA
DC V_{CC} or GND Current, per pin	I_{CC}	±75	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Input Rise or Fall rate	V_{CC} = 4.5V	t_r, t_f	0	1000	ns
	V_{CC} = 5.5V		0	500	
	V_{CC} = 6.0V		0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	$V_{OUT} = V_{CC}$ -0.1V $\|I_{OUT}\| \leq 20\mu A$	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	$V_{OUT} = 0.1V$ $\|I_{OUT}\| \leq 20\mu A$	0.5	0.5	0.5	V
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	
Minimum High-Level Output Voltage	V_{OH}	2.0V	$V_{IN} = V_{IH}$ $\|I_{OUT}\| \leq 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		4.5V	$V_{IN} = V_{IH}$ $\|I_{OUT}\| \leq 6.0mA$	3.98	3.84	3.70	
		6.0V	$V_{IN} = V_{IH}$ $\|I_{OUT}\| \leq 7.8mA$	5.48	5.34	5.20	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	$V_{IN} = V_{IL}$ $\|I_{OUT}\| \leq 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IL}$ $\|I_{OUT}\| \leq 6.0mA$	0.26	0.33	0.40	
		6.0V	$V_{IN} = V_{IL}$ $\|I_{OUT}\| \leq 7.8mA$	0.26	0.33	0.40	
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum 3-State Leakage Current	I_{OZ}	6.0V	High-Impedance State, $V_{IN} = V_{IL}$ or V_{IH}, $V_{OUT} = V_{CC}$ or GND	±0.5	±5.0	±10.0	µA
Maximum Quiescent Supply Leakage Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	4	40	160	µA

4. $-55^{\circ}C \leq T_J \leq +125^{\circ}C$

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AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Input A to Output Y (Figure 1)	t_{PLH}, t_{PHL}	2.0V	C_L = 50pF, Input $t_r = t_f$ = 6ns	90	115	135	ns
		4.5V		18	23	27	
		6.0V		15	20	23	
Maximum Propagation Delay, $\overline{OE}$ & OE to Output Y (Figure 2, 3)	t_{PLZ}, t_{PHZ}	2.0V	C_L = 50pF, Input $t_r = t_f$ = 6ns	110	140	165	ns
		4.5V		22	28	33	
		6.0V		19	24	28	
Maximum Propagation Delay, OE to Output Y (Figure 2, 3)	t_{PZL}, t_{PZH}	2.0V	C_L = 50pF, Input $t_r = t_f$ = 6ns	110	140	165	ns
		4.5V		22	28	33	
		6.0V		19	24	28	
Maximum Output Rise and Fall Time, Any Output (Figure 1)	t_{TLH}, t_{THL}	2.0V	C_L = 50pF, Input $t_r = t_f$ = 6ns	60	75	90	ns
		4.5V		12	15	18	
		6.0V		10	13	15	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Maximum 3-State Ouput Input (High-Z)	C_{OUT}	-	-	15	15	15	pF
Power Dissipation Capacitance[6]	C_{PD}	-	T_J = 25°C, V_{CC} = 5.0V	TYPICAL			pF
				34			

5. Not production tested in die form, characterized by chip design.
6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveforms

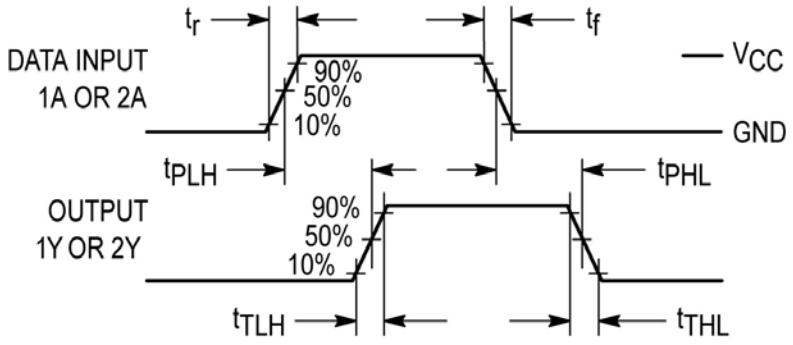


Figure 1 – Propagation Delay - Input 1A or 2A to Output 1Y or 2Y

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Switching Waveforms continued

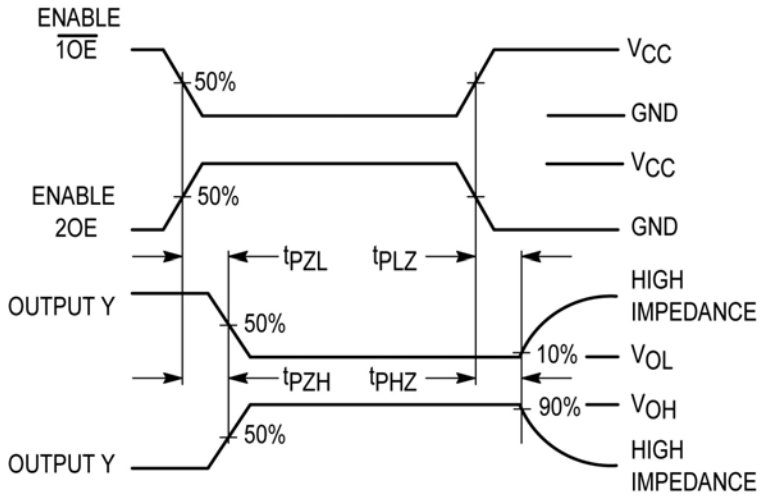
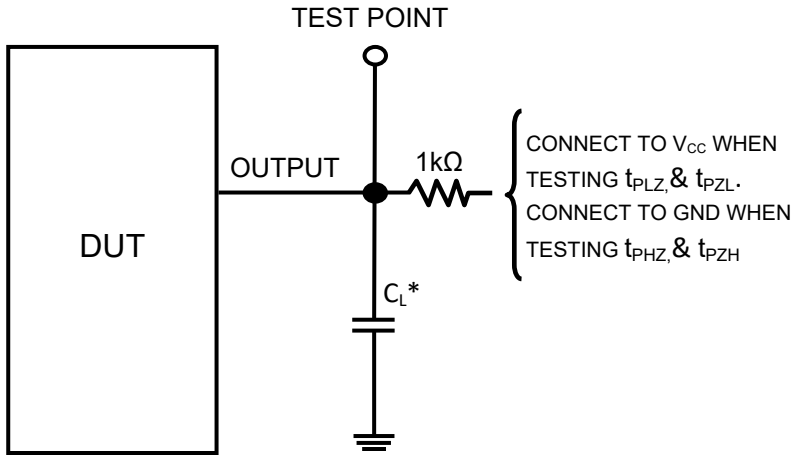


Figure 2 – Propagation Delay - Output Enable to Output 1Y or 2Y

Test Circuit



* Includes all probe and jig capacitance

Figure 3

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